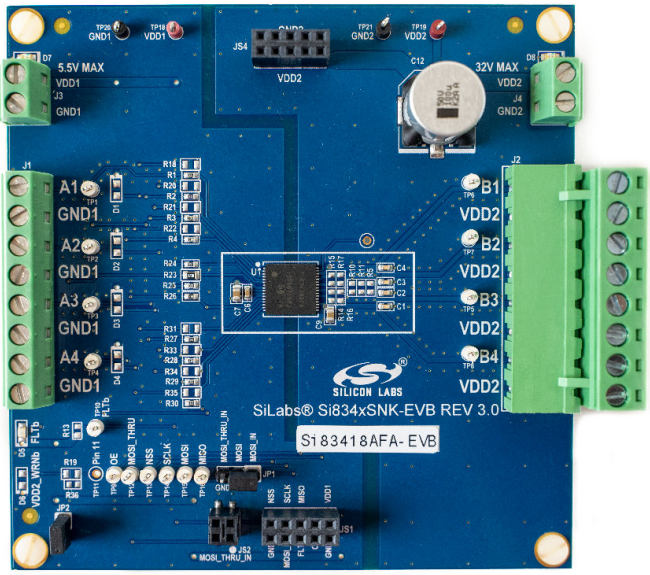
UG390: Si834x-EVB User's Guide

The Si834x-IF provides up to four isolated high-side (sourcing) or low-side (sinking) switches with low R_{ON}. These switches are ideal for driving resistive and inductive loads such as solenoids, relays, and lamps commonly found in industrial control systems like PLCs. Each switch is galvanically isolated for safety using Silicon Laboratories' ground-breaking CMOS-based isolation technology which enables easy interfacing with low voltage 2.25 V MCUs and high CMTI (100 kV/µs).

The Si834x evaluation board allows designers to evaluate Silicon Labs' Si834x family of Isolated Smart Switches. Each board comes populated with one Si834x device, LED status indicators, pluggable load terminals for evaluation of the device's key parameters, and test points for monitoring device pins. SPI-enabled product options contain headers and sockets that enable SPI interfacing and a CP2130 evaluation kit for SPI control. Additional information on the Si834x products can be found at https://www.silabs.com/products/isolation/industrial-io/si834x-isolated-smart-switches.html. The product data sheet and application notes can be referenced to help facilitate designs.

KEY FEATURES

- Si834x-based evaluation board populated with one of the following parts:
  - Si83404AAA
  - Si83414AAA
  - Si83408ADA
  - Si83418ADA
  - Si83408AFA
  - Si83418AFA
- Si834x8xxx products also contain:
  - CP2130 USB to SPI bridge
  - Micro-USB cable
  - 10-pin F-F ribbon cable
  - 10-pin M-M header



Si834x EVB

1. Test Procedure

If you have a SPI-enabled device and received a CP2130 with your evaluation kit, you will need to install the CP2130EK driver: https://www.silabs.com/documents/public/software/CP2130_Windows.exe. The CP2130 data sheet and user guide can be found at https://www.silabs.com/products/development-tools/interface/cp2130ek-evaluation-kit for additional information.

The procedure below assumes you are familiar with the Si834x device. If not, see Section 2: Using the Evaluation Board for key background information. Throughout this document, “sourcing” (or SRC) refers to Si8340x part numbers and their corresponding sourcing PCBs and “sinking” (or SNK) refers to Si8341x part numbers and their corresponding sinking EVBs.

In sections 1.2 Input Configuration, 1.5 Activate Channels, and 1.6 Repeat for Remaining Channels, instructions are separated for Parallel Input Interface and SPI Input Interface. If you are using the Si834x4AAA (sourcing or sinking) or the Si834x8AFA (sourcing or sinking), then follow the Parallel Input Interface instructions for these subsections. If you are using the Si834x8ADA (sourcing or sinking), then follow the SPI Input Interface instructions. Although the Si834x8AFA devices have SPI capabilities, the channel inputs are still controlled through the parallel input interface. See Section 2: Using the Evaluation Board for more details.

The following equipment is required to demonstrate the evaluation board features:

- Function generator for parallel input interface (optional)
- One dual-channel DC power supply or two single supplies: 0-5 V and 0-24 V
- One oscilloscope with at least 2 channels
- Four 10 kΩ through-hole resistors (1 minimum)
- Si834x-EVB kit (includes CP2130 for SPI-enabled devices)
- Si834x-EVB User’s Guide (this document)
- PC with USB connection (for SPI-enabled devices)
- Assorted cables, leads, and probes as necessary to connect equipment to EVB

1.1 DC Supply Configuration

VDD1 supply configuration:

1. Set one supply to output 5 VDC.
2. Turn OFF the supply and connect the positive lead to VDD1 (J3 pin1 or TP18).
3. Connect the negative lead to GND1 (J3 or TP20).
4. Turn ON the supply.
5. Ensure that LED D7 turns on and that LED D5 is blinking (this indicates there is no VDD2 supply).
6. Ensure that the current draw is less than 25 mA. If it is larger, this indicates that either the board or Si834x has been damaged or that the supply is connected backwards.

VDD2 supply configuration:

1. Set the second supply to output 24 VDC.
2. Turn OFF the supply and connect the positive lead to VDD2 (J4 pin1 or TP19).
3. Connect the negative lead to GND2 (J4 or TP21).
4. Turn ON the supply.
5. Ensure that LED D8 turns on and that LED D5 turns off.
6. Ensure that the current draw is less than 25 mA. If it is larger, this indicates that either the board or the Si834x has been damaged or that the supply is connected backwards.

1.2 Input Configuration

There are two primary input interface types for the Si834x product family: parallel and SPI. For all devices that have parallel or parallel/SPI input interfaces, the inputs are controlled manually using the input channels A1-A4. For devices that are SPI only, the inputs are controlled by sending SPI commands via the CP2130 USB to SPI bridge.

Devices with parallel input interface:

1. Turn ON the function generator with the output disabled.*
2. Adjust the output to provide a 100 Hz, 0 to 5 V peak square wave with 50% duty cycle.
3. Connect the positive lead of the generator to A1 (J1 pin1 or TP1) and ground the connection to GND1 (J1, J3, or TP20).
4. If possible, configure the function generator for a High-Z (high impedance) load.

Note: If you do not have a waveform generator, or prefer not to use one, you may simply apply 5 V to the input channels on the Si834x to observe the output channel coming on. The proper configuration is shown in the figures below.

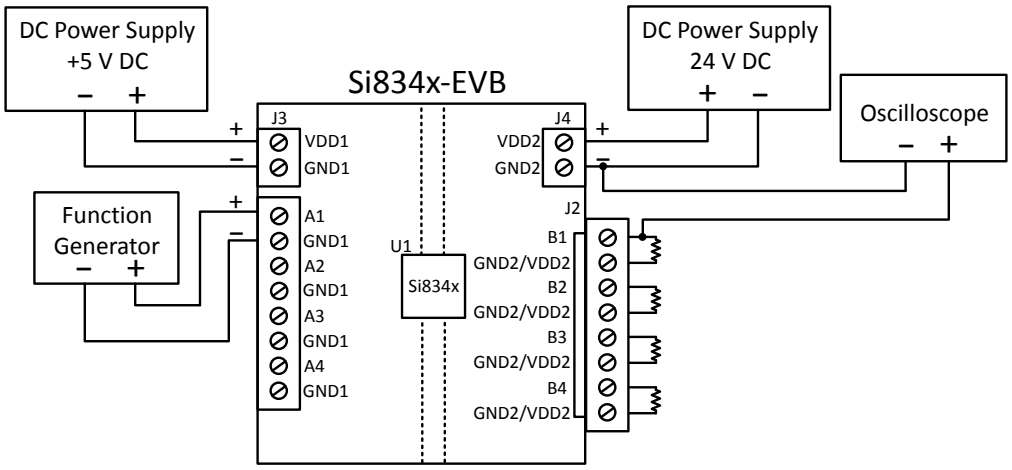


Figure 1.1. Configuration for Parallel Input Interface

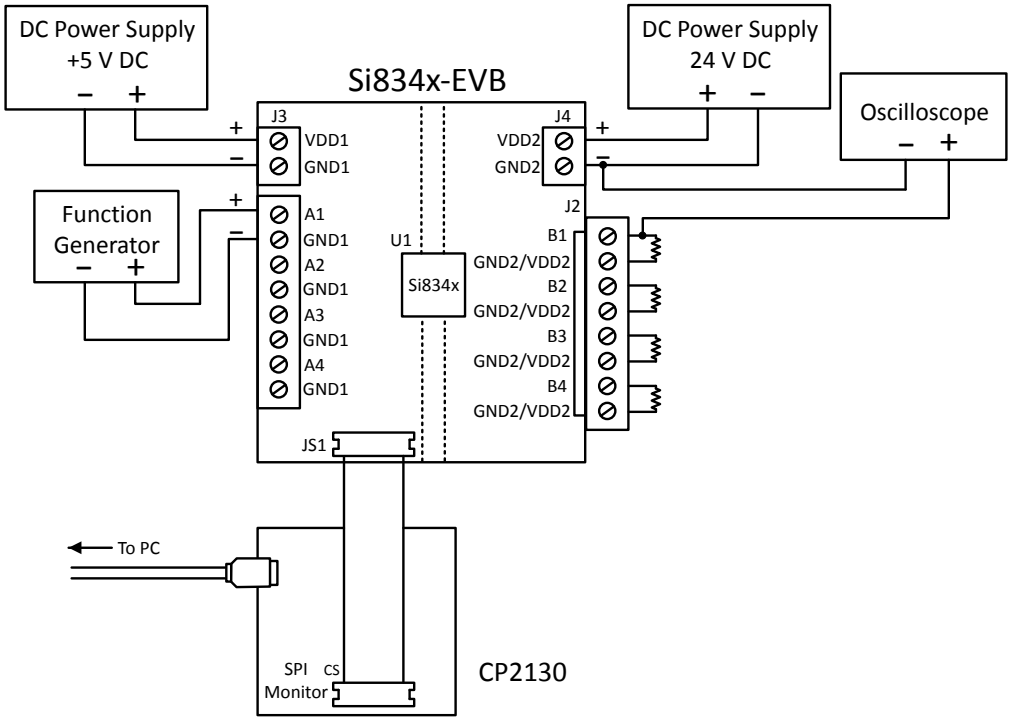


Figure 1.2. Configuration for Parallel Input Interface with SPI Capabililties

Devices with SPI input interface:

1. Connect the CP2130 to your PC using the micro-USB cable included with the kit.
2. Connect the CP2130 to the Si834x-EVB using the ribbon cable provided.
   a. Place the 10-pin M2M header included in the kit into one end of the ribbon cable.
   b. Connect this end of the cable to JS1 on the Si834x-EVB.
   c. Connect the other end of the cable to the 10-pin header on the CP2130 labeled SPI MONITOR.
   d. Ensure that the pin labeled CS on the SPI MONITOR header is aligned with the pin labeled NSS on JS1 of the EVB. This can be done by ensuring that the red wire on the cable is located on the same side of the headers as the CS and NSS pins.

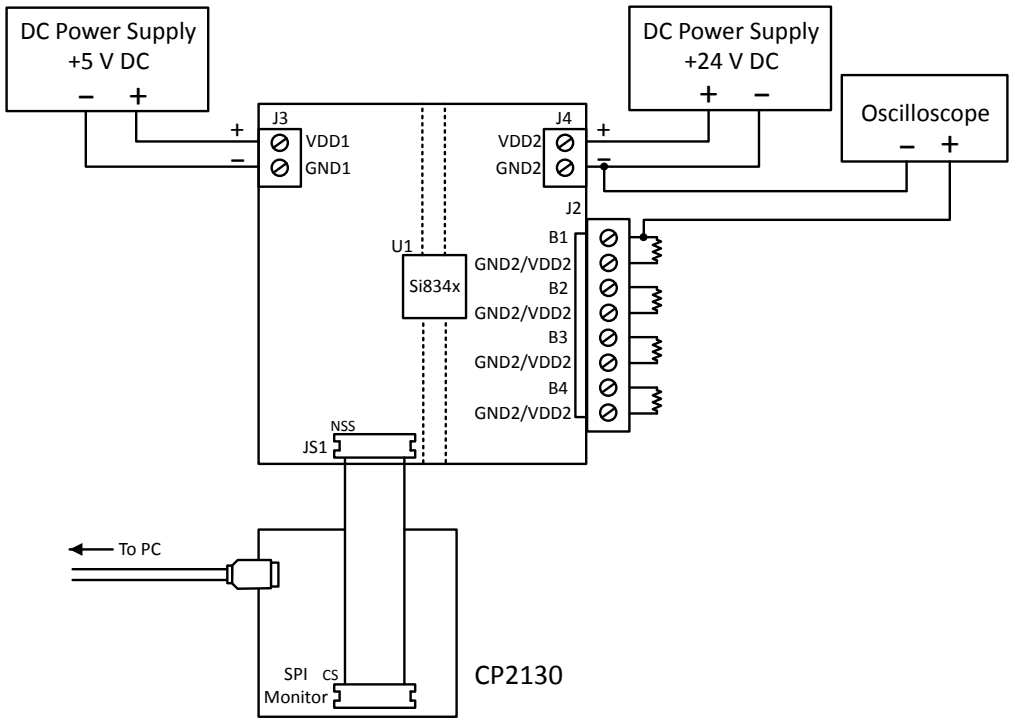


Figure 1.3. Configuration for SPI Input Interface

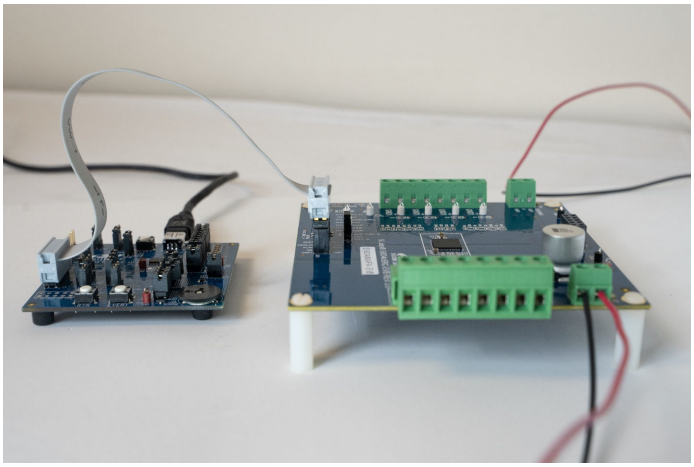


Figure 1.4. Connection between CP2130 and Si834x EVB

3. Load the CP2130 Evaluation Tool installed with the driver above.
4. In the “Connection” box, the “Choose device:” dropdown should already be populated with the address of the CP2130 plugged into the PC. If it is not, disconnect the CP2130 and reconnect it.
5. Select “Connect”. Ensure that D10 of the CP2130 flashes green to indicate a good connection.

6. Configure the CP2130 as follows:
   a. Set the SPI Transfer Type to WriteRead
   b. In Test Configuration, set the Total Bytes to 3 and the Timeout to 1000 ms.
   c. In SPI Parameters, set the Phase to Trailing Edge, Polarity to Active Low, Chip Select Mode to Push-Pull, and Clock Frequency to 375 kHz. Change Chip Select to 0, check the Toggle CS box, check the Inter-Byte Delay box and enter 1 in the adjacent box.
   d. Finally, set Data Transfer to Text Box and ensure that the Display box is checked next to Receive Data.
   e. Your settings should look like Figure 1.5 CP2130 Configuration Window on page 5 when complete:

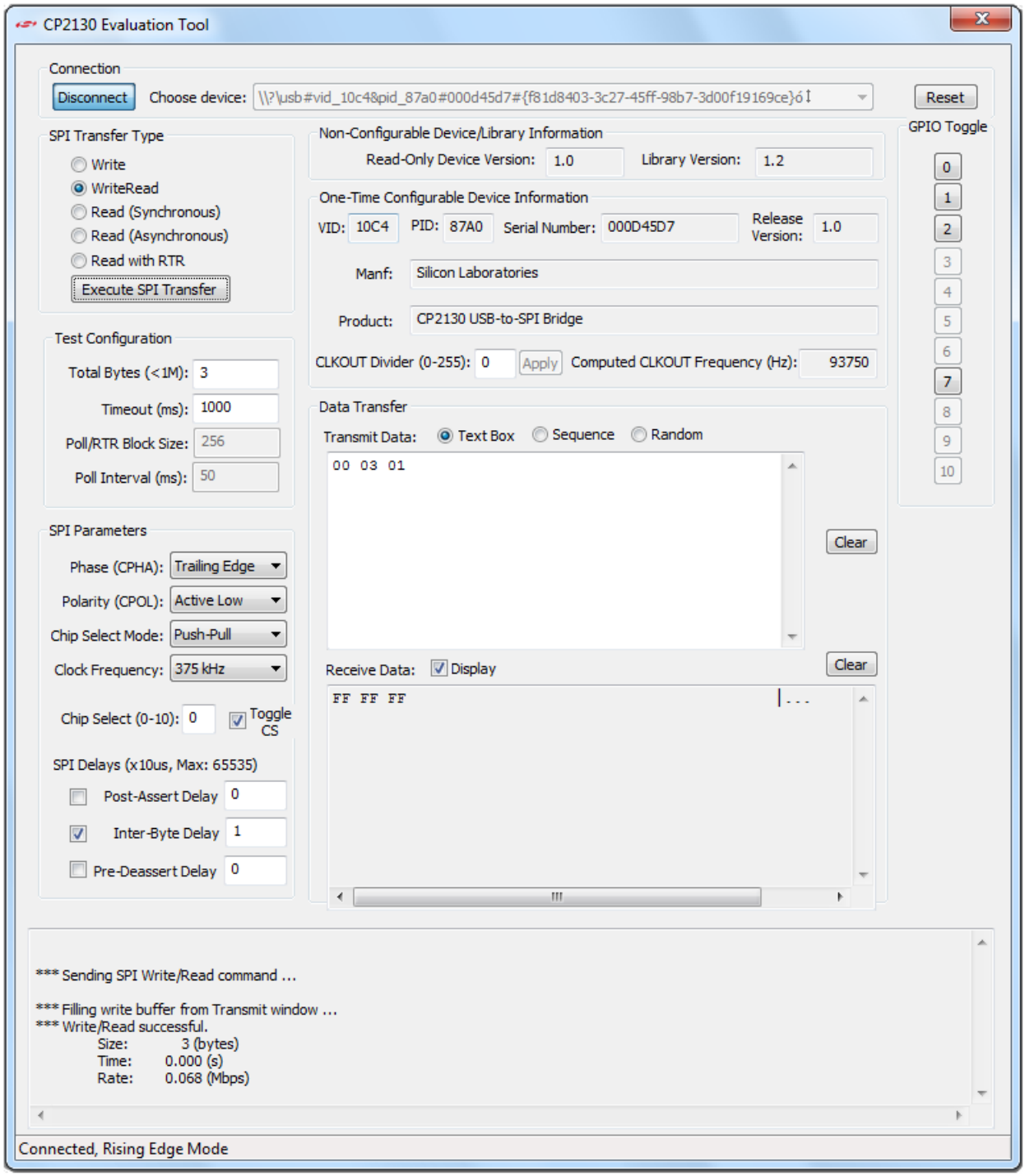


Figure 1.5. CP2130 Configuration Window

1.3 Load Configuration

1. Turn OFF the 24 VDC power supply.
2. Connect a 10 kΩ resistor to channel B1 by placing one lead in the first slot of the terminal block (J2) and screwing it down. Place the other lead in the second slot (J2) and screw it down. This connection is the same for both SRC and SNK EVBs.
3. Populate channels B2, B3, and B4 with the remaining resistors.
4. Turn ON the 24 V supply.

1.4 Oscilloscope Setup

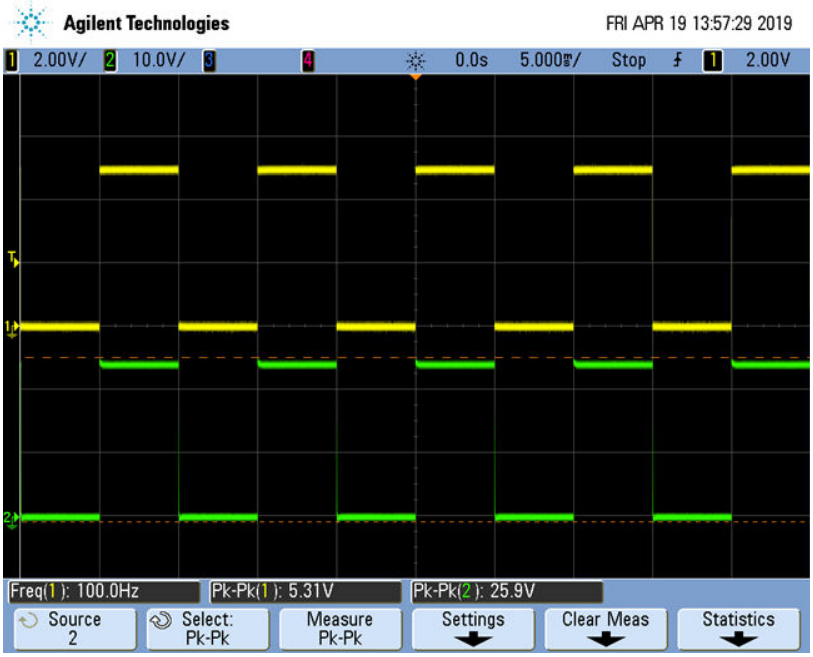
1. Parallel input only: connect the CH1 probe to A1 (TP1) and ground the probe to GND1 (TP20).
2. Connect the CH2 probe to B1 (TP6) and ground the probe to GND2 (TP21).
3. Set the scope to Trigger on a rising edge on CH1 and adjust the trigger level to approximately 2 V.
4. Set CH1 to 2 V per division and CH2 to 10 V per division.
5. Adjust the horizontal zoom to 500 µs per division.

1.5 Activate Channels

Devices with parallel input interface:

1. Enable the function generator output on channel A1, or apply 5 V directly.
2. Ensure that D1 turns on (Si834x4AAA-EVBs only).
3. Adjust the vertical and horizontal divisions to properly view the waveform as seen in the image below.

   For parallel input devices, a 100 Hz square wave with 50% duty cycle should appear on Channel 1, and a similar waveform with peak voltage of 24 V should appear on Channel 2. Note that the output waveform in the figure below is for a sourcing device, and the polarity will be opposite for sinking devices.



Devices with SPI input interface:

1. In the CP2130 Evaluation Tool, enter the command **00 03 01** in the textbox.
2. Press Execute SPI Transfer.
3. Ensure that D1 turns on. On the oscilloscope, B1 should appear as a line of magnitude 24 V (SRC) or 0 V (SNK).

1.6 Repeat for Remaining Channels

Devices with parallel input interface:

1. Disable the function generator output.
2. Connect the CH1 probe to A2 (TP2).
3. Connect the CH2 probe to B2 (TP7).
4. Connect the positive lead of the function generator to A2 (TP2).
5. Enable the function generator.
6. Ensure that LED D2 turns on (Si834x4AAA-EVBs only).
7. Repeat steps 1-5 with channels A3 and A4 using test point TP3 for A3, TP5 for B3, TP4 for A4, and TP8 for B4.

Devices with SPI input interface:

1. In the Evaluation Tool, enter the command **00 01 00** and Execute SPI Transaction to disable channel A1.
2. Connect the CH2 probe to B2 (TP7).
3. Enter the command **00 01 02** and Execute SPI Transaction to enable channel A2.
4. Ensure that D2 turns on.
5. Connect the CH2 probe to B3 (TP5).
6. Enter the command **00 01 04** and Execute SPI Transaction to enable channel A3.
7. Ensure that D3 turns on.
8. Connect the CH2 probe to B4 (TP8).
9. Enter the command **00 01 08** and Execute SPI Transaction to enable channel A4.
10. Ensure that D4 turns on.

2. Using the Evaluation Board

The Si834x-EVB comes populated with one of four different Si834x devices that require different input types and load configurations. This section will explain those differences and how to configure your setup to properly utilize the evaluation board.

Table 2.1. Si834x Input and Output Configurations

Part Number	Input Interface	Switch Type	Load Terminals	PCB
Si83404AAA	Parallel	High-Side (SRC)	Bn and GND2	Si834xSRC-EVB Rev 2.0
Si83414AAA	Parallel	Low-Side (SNK)	Bn and VDD2	Si834xSNK-EVB Rev 2.0
Si83408ADA	SPI	High-Side (SRC)	Bn and GND2	Si834xSRC-EVB Rev 3.0
Si83418ADA	SPI	Low-Side (SNK)	Bn and VDD2	Si834xSNK-EVB Rev 3.0
Si83408AFA	Parallel/SPI	High-Side (SRC)	Bn and GND2	Si834xSRC-EVB Rev 3.0
S83418AFA	Parallel/SPI	Low Side (SNK)	Bn and VDD2	Si834xSNK-EVB Rev 3.0

2.1 Load Termination

Sourcing parts utilize high side switches that require the load to be connected from the channel output (Bn) to GND2. Sinking parts contain a low side switch that require the load to instead be connected from output (Bn) to VDD2. The output-side screw terminals (J2) on the sourcing EVBs contain connections to GND2, while the sinking EVBs contain connections to VDD2. This allows J2 pins 2, 4, 6, and 8 to be used for load termination on both the sourcing and sinking evaluation boards.

2.2 Inputs to the Device

Depending on the part number of your product, the channel inputs will be supplied either through a parallel digital interface or by a SPI controller.

Parallel Input: The Si834x4AAA and Si834x8AFA products require the user to directly apply an input voltage to enable and disable the channels. The input-side screw terminals (J1) contain connections to the channel inputs and GND1, allowing the user to apply an input by connecting the input source to adjacent pins in the terminal.

SPI Input: The Si834x8ADA products are SPI-enabled devices that require a master device to send commands that enable or disable the channels. The female header JS1 serves as the SPI port for the onboard device and contains connections to the device's SPI pins such as OE, CLR, MOSI, and MISO. A detailed pinout can be found in the schematics in Section 3.

Parallel Input with SPI Capabilities: The Si834x8AFA products have parallel input interface but also have SPI capabilities that allow the user to read and write to registers that contain diagnostic information and provide configurability. To utilize these SPI capabilities in conjunction with the parallel input, the user should configure the EVB setup as shown in Figure 1.2 Configuration for Parallel Input Interface with SPI Capabililties on page 3. The example commands in Section 2.4: Basic SPI Commands that enable or disable the channels will simply read back the status of the channels instead of enabling or disabling.

2.3 Daisy Chaining SPI Devices

The SPI-enabled devices can be daisy chained to allow a single master to send commands to multiple slaves. Outlined below are the steps necessary to properly configure the EVBs to enable the daisy chain functionality of the devices.

MOSI Jumper Configuration:

There are two MOSI inputs for each SPI-enabled device: MOSI_IN and MOSI_THRU_IN. The user can select from these inputs by moving a jumper across the appropriate pins on JP1. The jumper is placed across MOSI_IN by default and should remain there if the device is being used as the 0^{th} device (first slave) in the chain. Each device in the chain passes the master command to the next device after decrementing the chip address by 1. Therefore, all EVBs behind the 0th device (top board) in the chain should have JP1 configured to pass the MOSI_THRU_IN signal to the device. In general, follow these rules:

1. For the 0^{th} device, ensure that JP1 is placed on MOSI and MOSI_IN, and that JP2 is populated.
2. For subsequent devices, move JP1 to connect MOSI_THRU_IN and remove JP2.

Fault LED Jumper Configuration:

The fault (FLT\) LED indicator is connected to the Si834x device through JP2 on the EVB. The jumper is populated by default and removing it will disable the LED. In a daisy chain configuration, the FLT\ pin of all devices are tied together to drive the fault LED indicator on the top board. Therefore, the LED indicators must be disabled on all boards but the top one. In general, JP2 should be removed to disable this indicator on all boards beneath the top board.

Stacking the EVBs:

The Si834x-EVB has been designed to allow the user to stack multiple evaluation boards on top of one another to form a compact chain. The boards will be daisy chained in ascending order from top to bottom, with the 0^{th} device on the top. Follow these steps to stack multiple evaluation boards:

1. Remove the four nylon standoffs from the board that will be placed underneath the stack as the next device in the daisy chain.
2. Align headers from top to bottom as such: JS1 to JS1, JS3 to JS2, and JS4 to JS4. Note that JS3 is the male header located directly beneath JS2.
3. Press the top board down until all three headers are firmly in place. Guide the male end of the standoffs on the top board into the mounting holes of the bottom board.
4. Return the four standoffs to the bottom board, using the screws extending from the standoffs above to secure them into place.

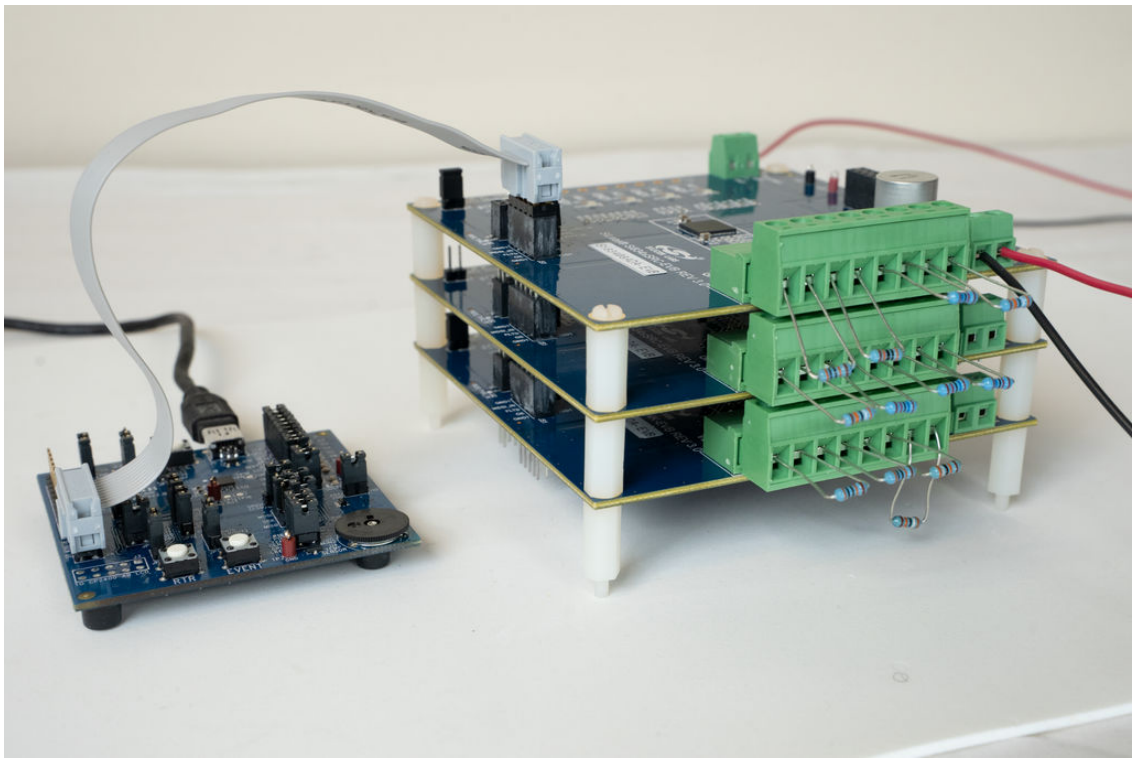


Figure 2.1. Si834x-EVB Stack Diagram

2.4 Basic SPI Commands

This section provides basic SPI commands that can be used to interface with the SPI-enabled devices. For a detailed overview of the SPI capabilities of the Si834x, refer to the Si834x data sheet.

Table 2.2. Basic SPI Commands

Command Description	Command	Read/Write	Register
Enable channels A1-A4[1]	**00 03 0F**	W	SWITCH_EN
Disable channels A1-A4[1]	**00 03 00**	W	SWITCH_EN
Read channel status	**40 03 00**	R	CHAN_STATUS
Read master diagnostics	**40 00 00**	R	MASTER_DIAG
Read diagnostics for channels B1/B2	**40 01 00**	R	DIAG_B21
Read diagnostics for channels B3/B4	**40 02 00**	R	DIAG_B43
Read diagnostics on second device in daisy chain	**50 00 00**	R	DIAG_B21
Clear all faults on third device in daisy chain	**08 05 0F**	W	CLR_DIAG

Note:
1. Si834x8ADA devices only.

3. Evaluation Board Schematics

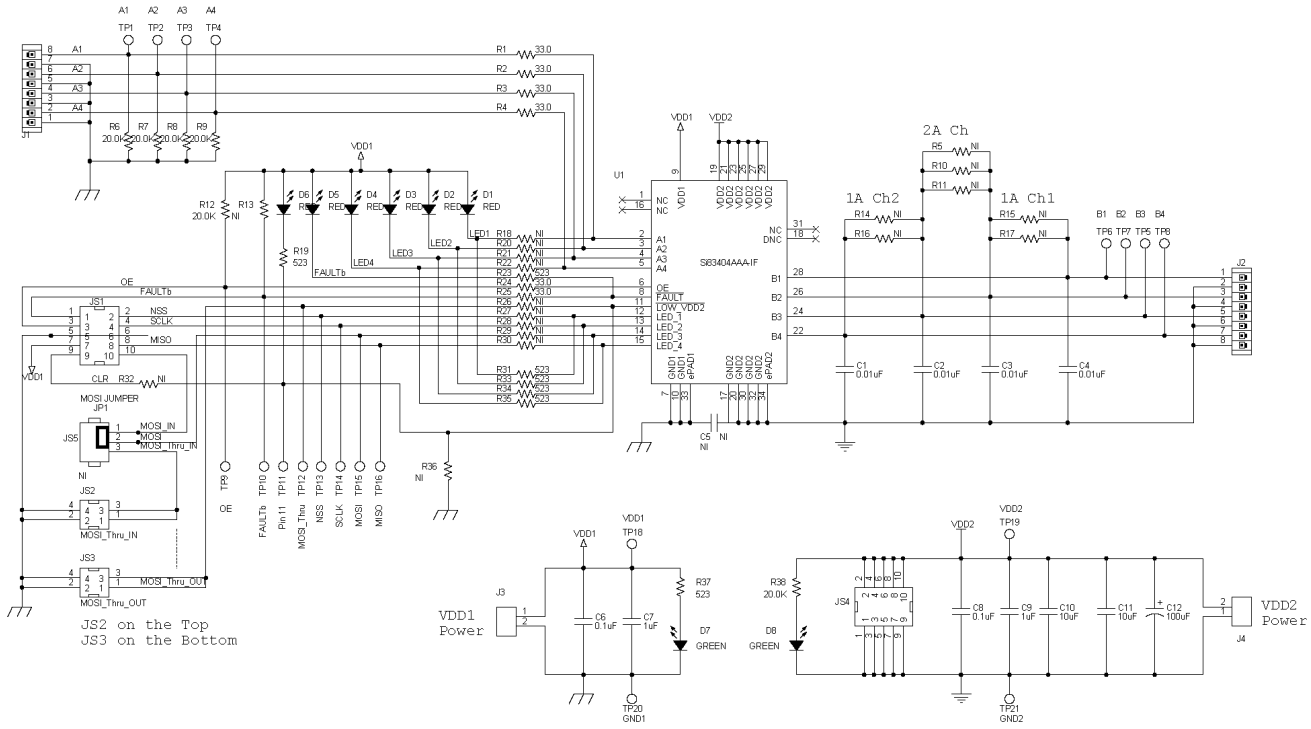


Figure 3.1. Si83404AAA Schematic Diagram

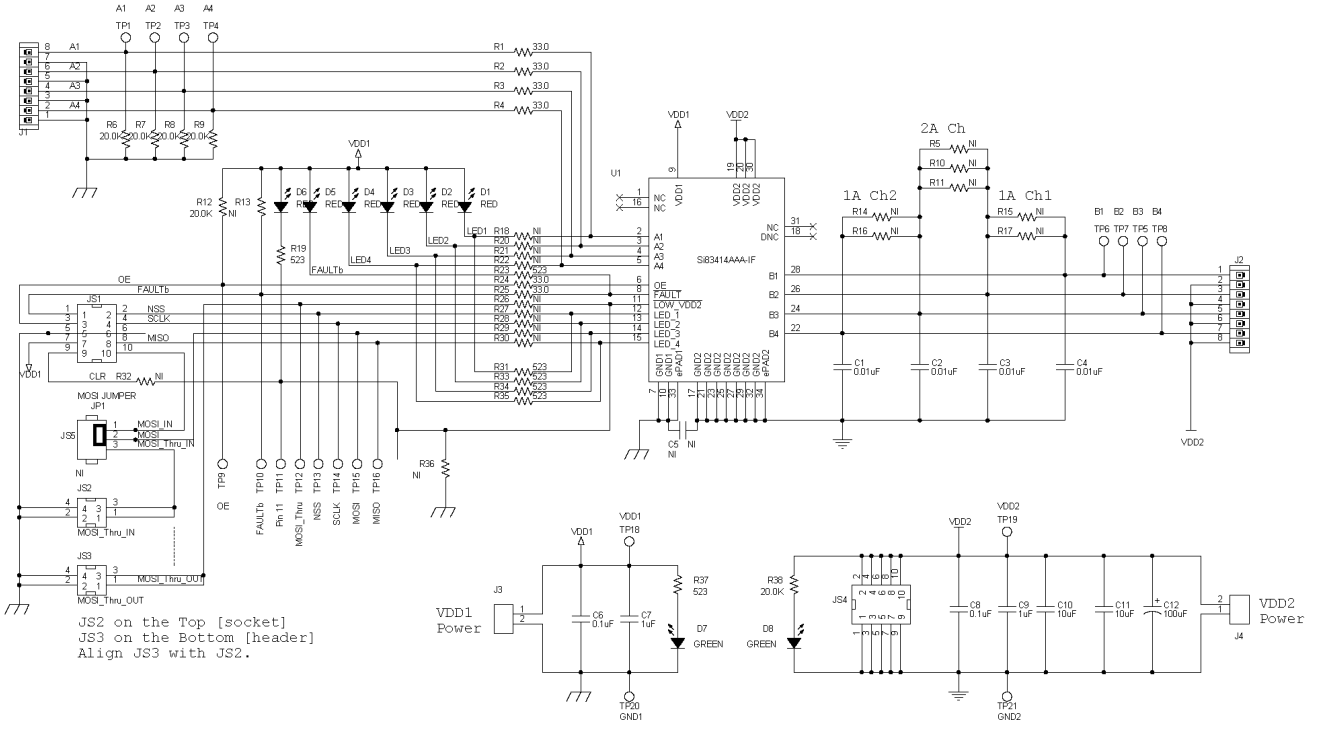


Figure 3.2. Si83414AAA Schematic Diagram

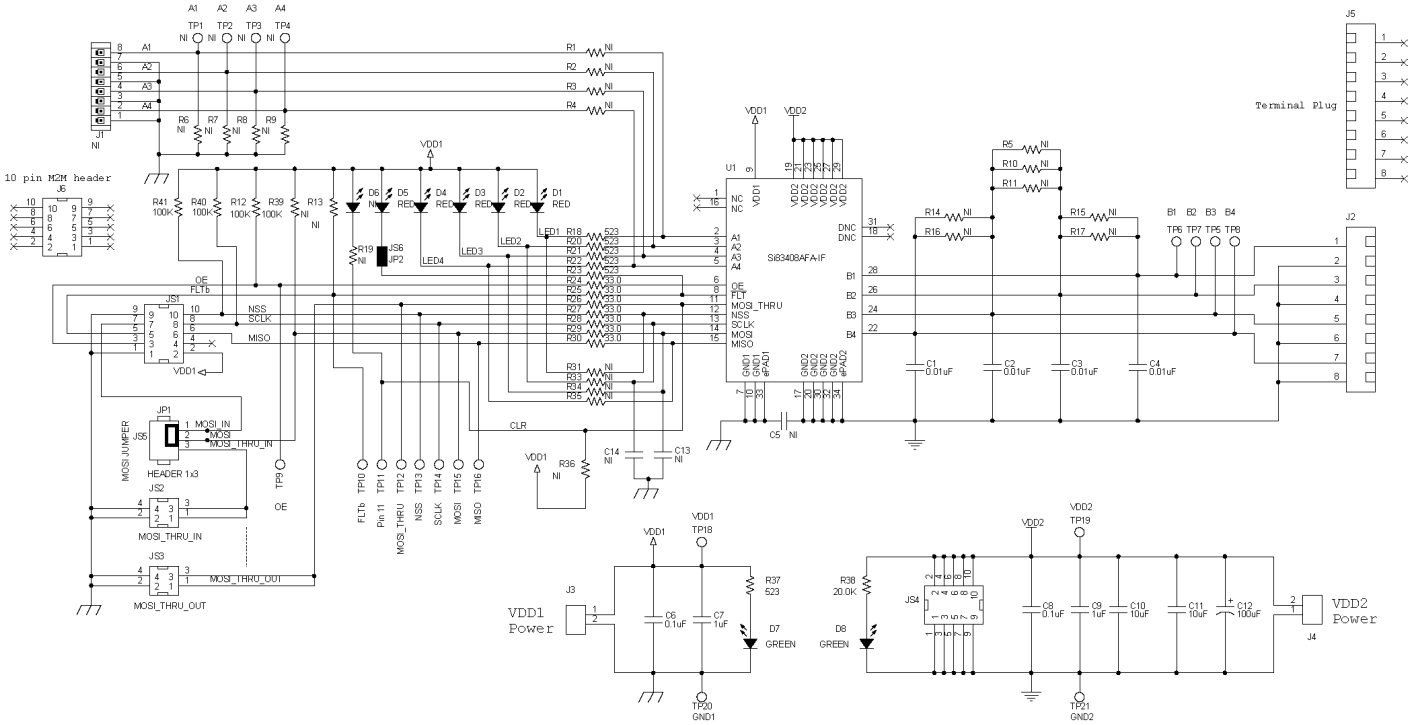


Figure 3.3. Si83408ADA Schematic Diagram

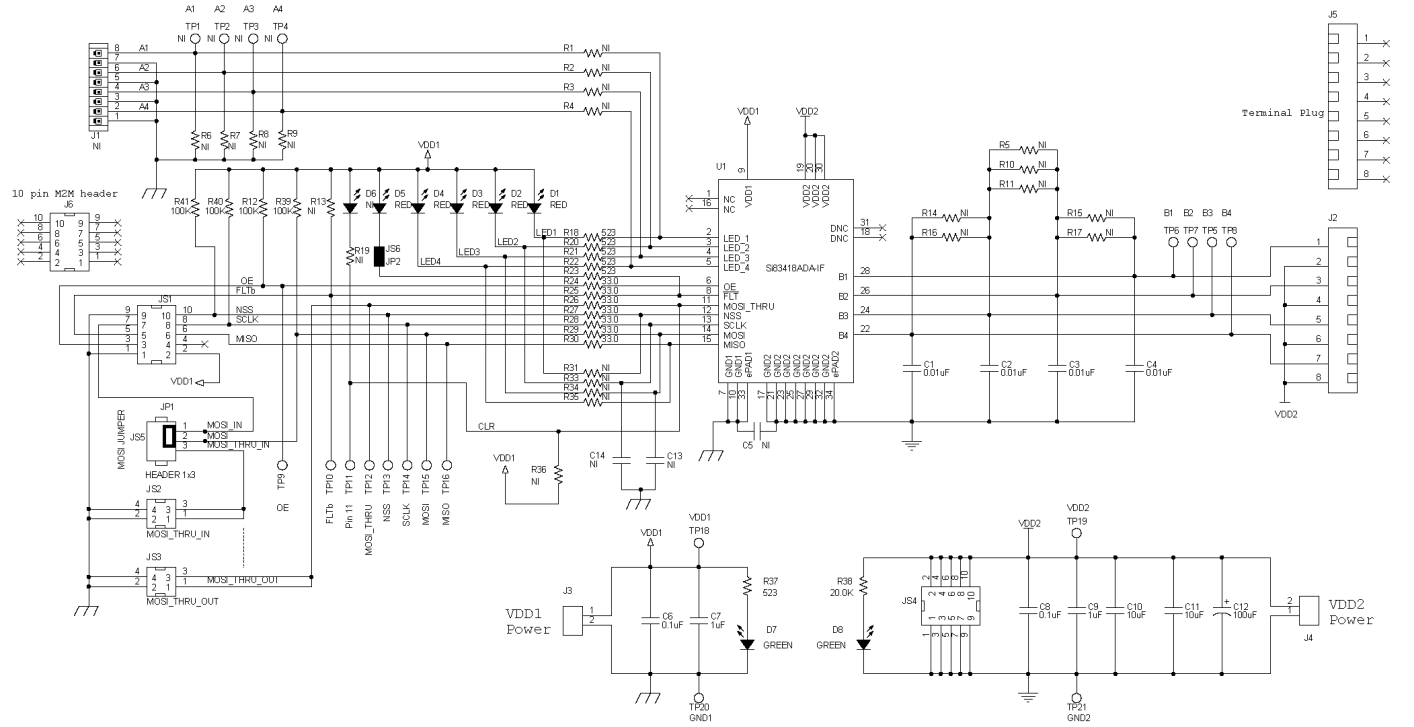


Figure 3.4. Si83418ADA Schematic Diagram

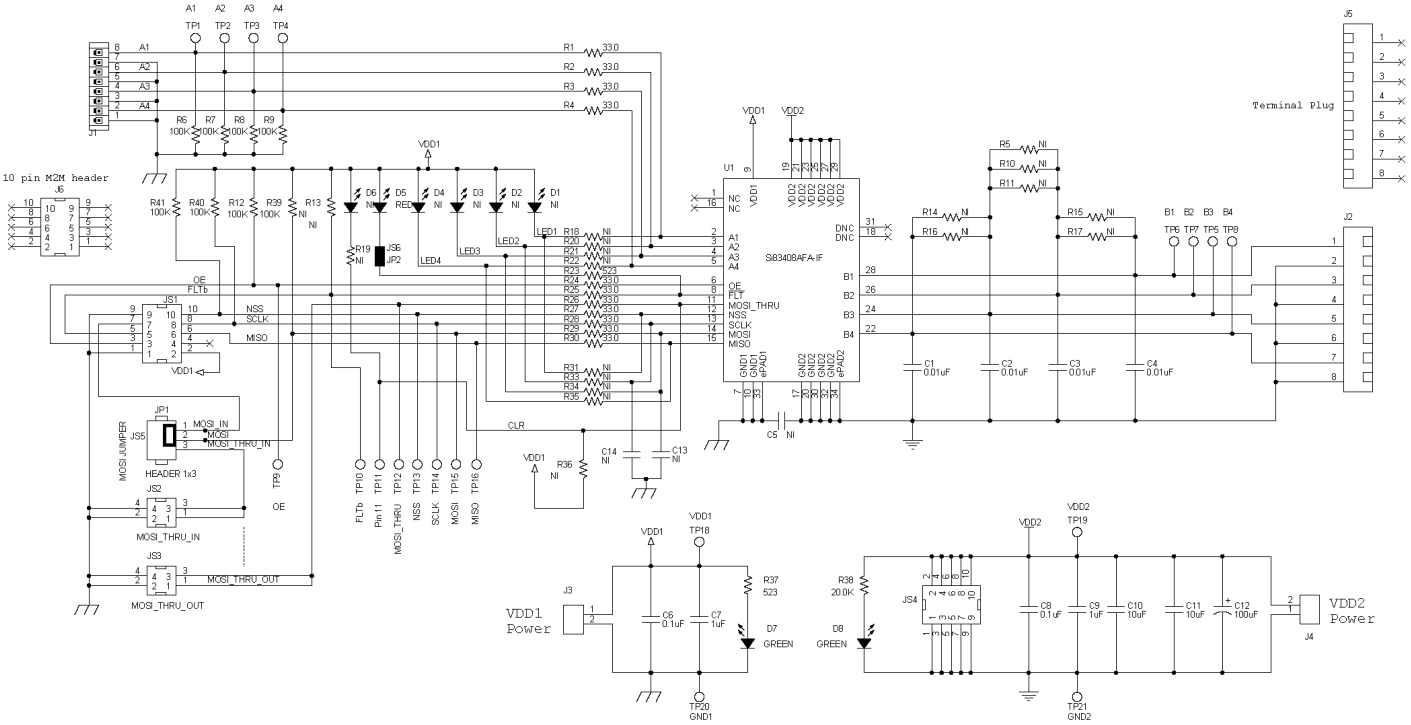


Figure 3.5. Si83408AFA Schematic Diagram

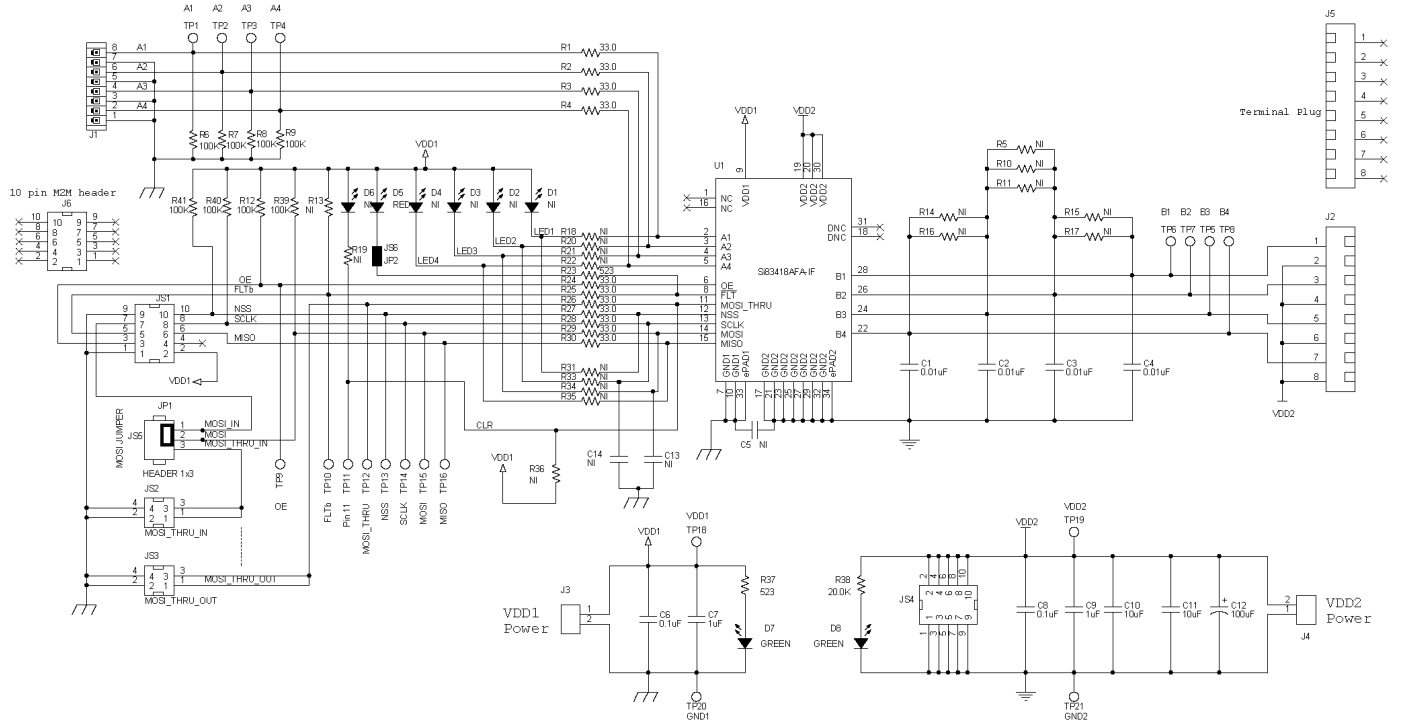


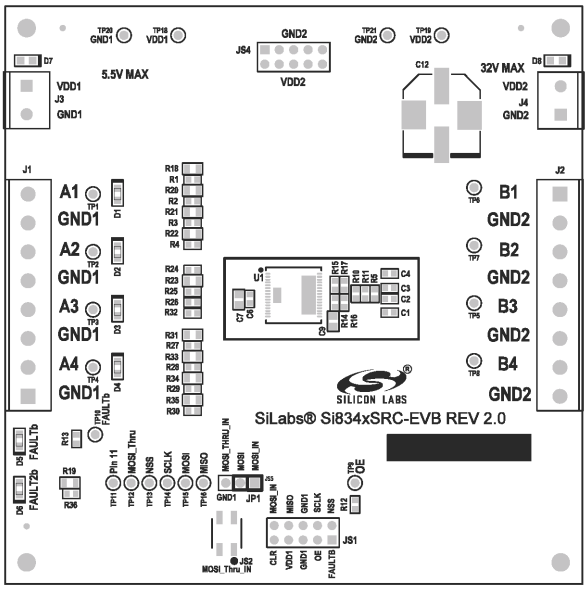
Figure 3.6. Si83418AFA Schematic Diagram

4. Evaluation Board Layouts

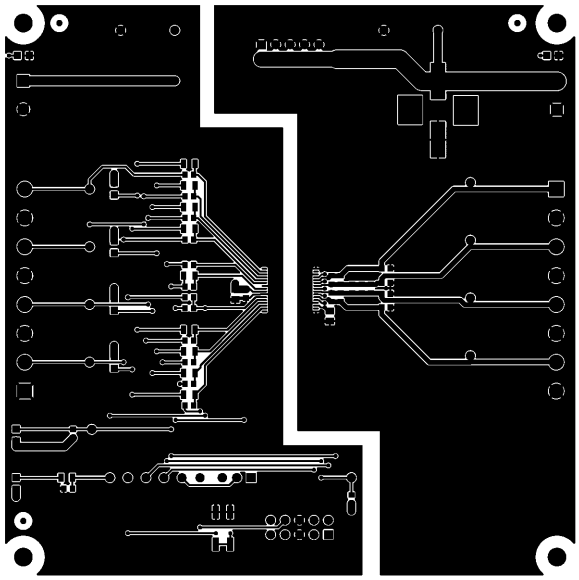
4.1 Si834xSRC-EVB Rev 2.0 Layouts

The Si834xSRC-EVB Rev 2.0 PCBs are used for the Si83414AAA-EVB only.

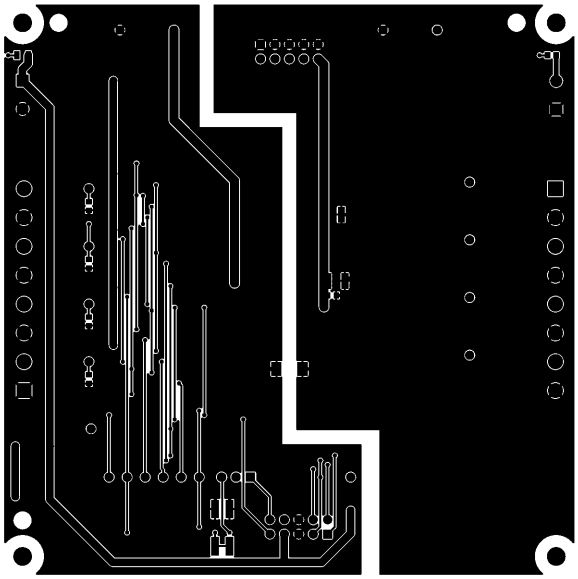
PRIMARY SILKSCREEN



PRIMARY SIDE



SECONDARY SIDE



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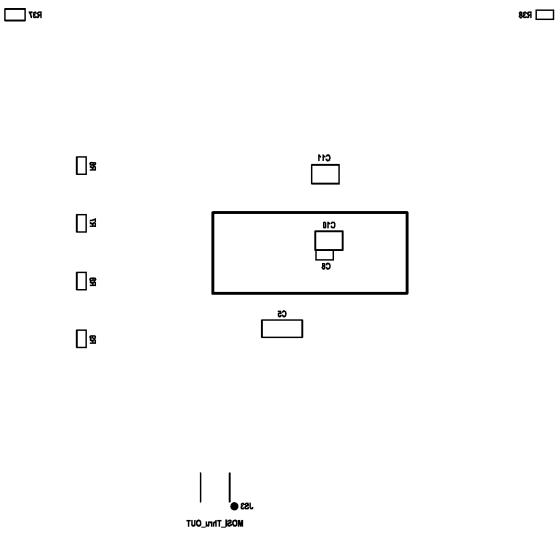
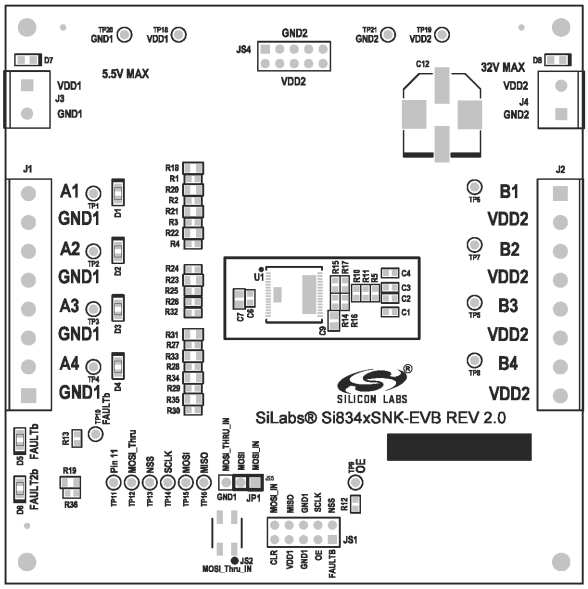


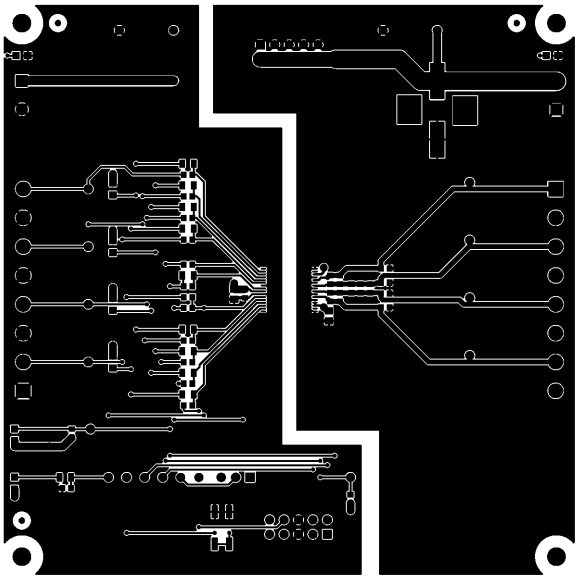
4.2 Si834xSNK-EVB Rev 2.0 Layouts

The Si834xSNK-EVB Rev 2.0 PCBs are used for the Si83404AAA-EVB only.

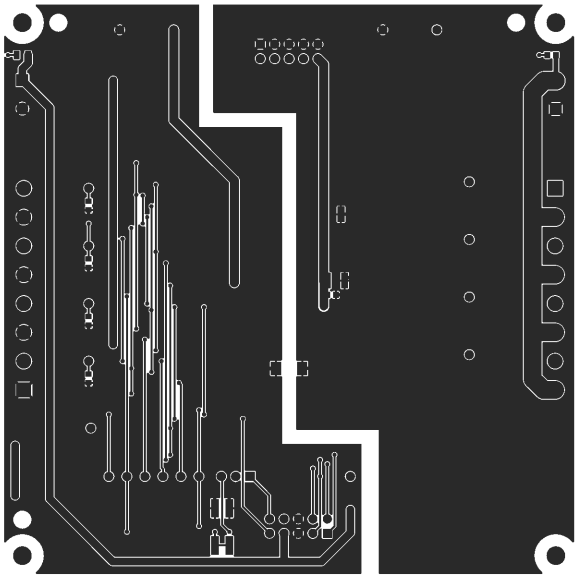
PRIMARY SILKSCREEN



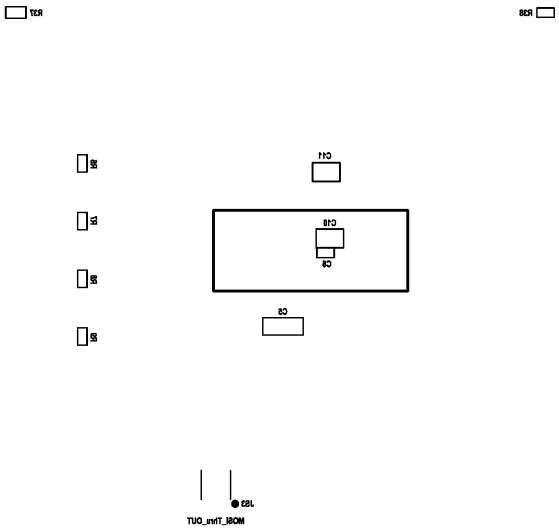
PRIMARY SIDE



SECONDARY SIDE



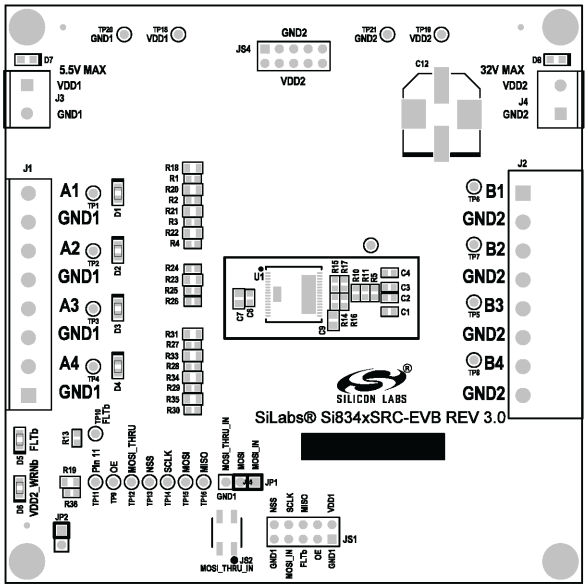
SECONDARY SILKSCREEN



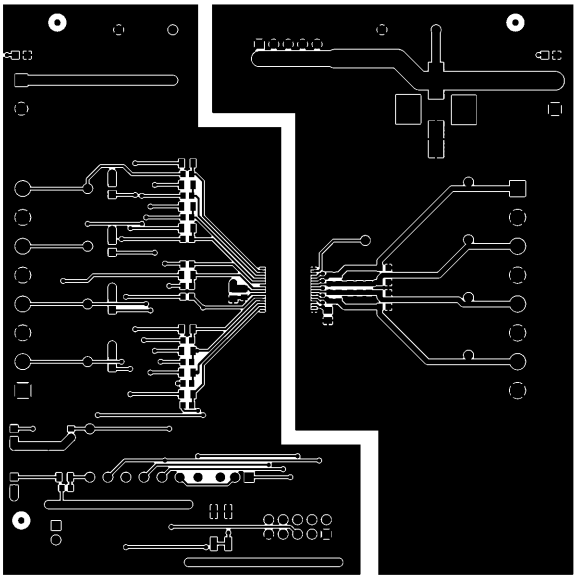
4.3 Si834xSRC-EVB Rev 3.0 Layouts

The Si834xSRC-EVB Rev 3.0 PCBs are used for the Si83408ADA-EVB and Si83418AFA-EVB.

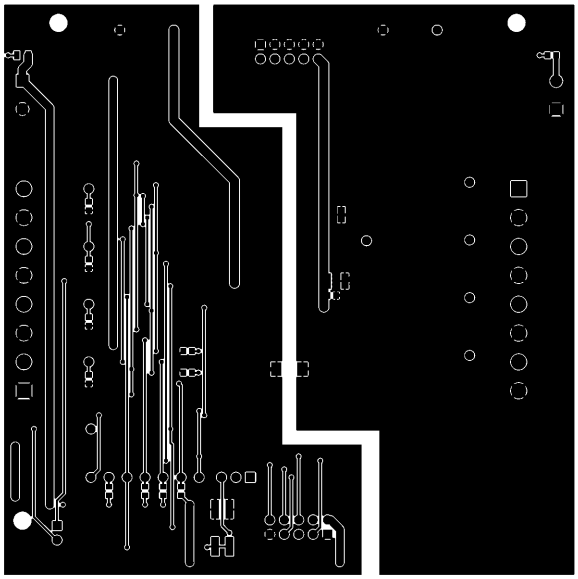
PRIMARY SILKSCREEN



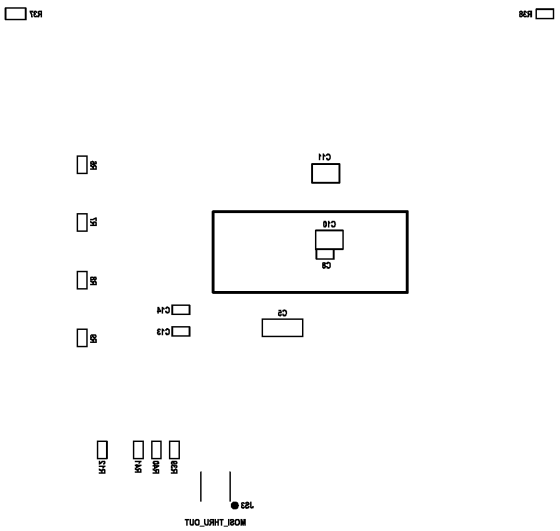
PRIMARY SIDE



SECONDARY SIDE



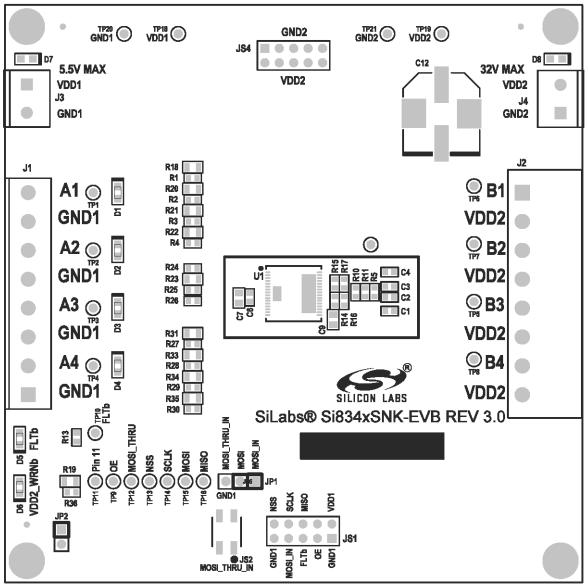
SECONDARY SILKSCREEN



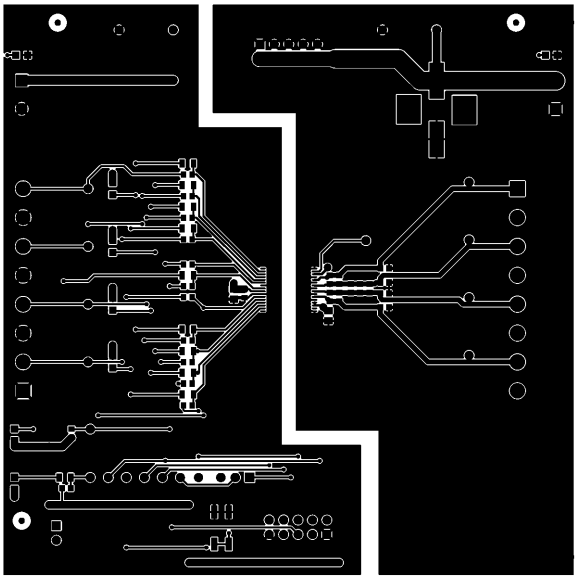
4.4 Si834xSNK-EVB Rev 3.0 Layouts

The Si834xSNK-EVB Rev 3.0 PCBs are used for the Si83418ADA-EVB and Si83418AFA-EVB.

PRIMARY SILKSCREEN



PRIMARY SIDE



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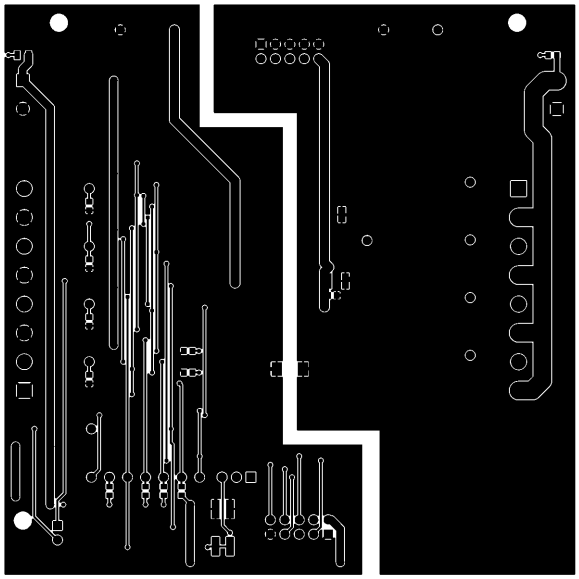
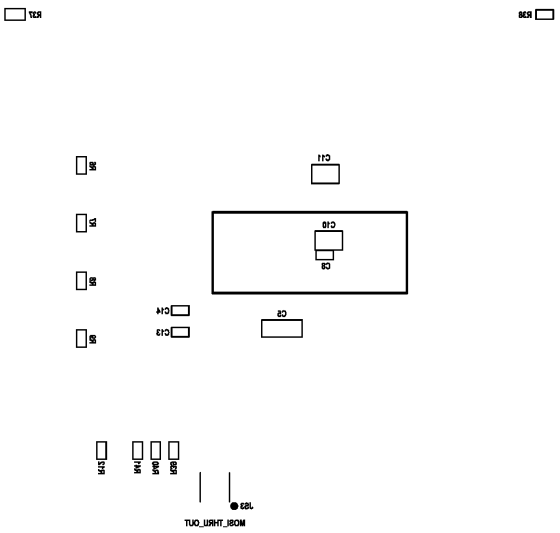


SECONDARY SILKSCREEN



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