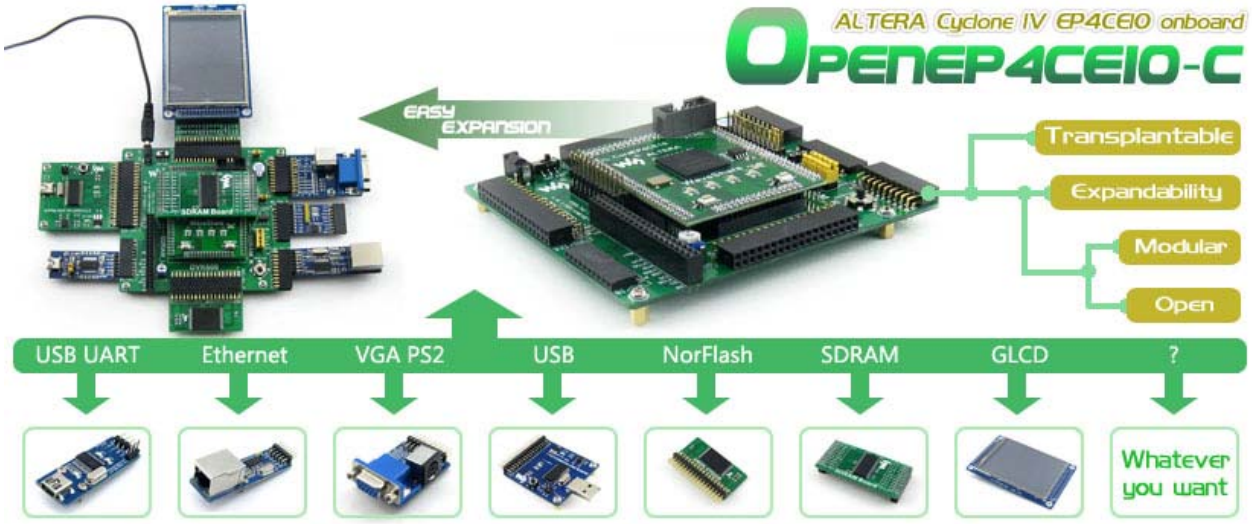
OpenEP4CE10-C Package B

DVD с ПО и примерами можно скачать по ссылке:
https://mega.co.nz/#!wFsRWTjD!oI6XYfkh7BaErq6681Zb9dn79tHa_S3HPIeCuDmm9L0

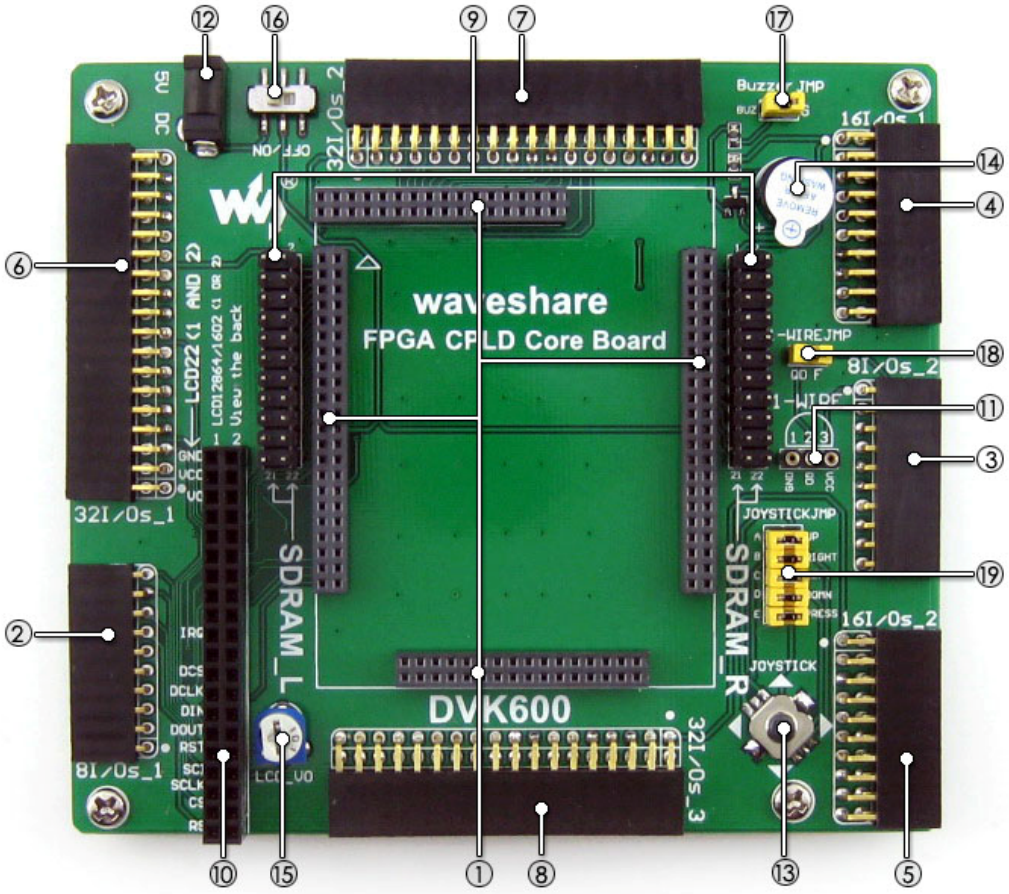


Overview

OpenEP4CE10-C is an FPGA development board that consists of the mother board **DVK600** and the FPGA core board **CoreEP4CE10**.

OpenEP4CE10-C supports further expansion with various optional accessory boards for specific application. The modular and open design makes it the ideal for starting application development with ALTERA Cyclone IV series FPGA devices. OpenEP4CE10-C enables you to start your design with the Nios II processor easily and quickly.

What's on the mother board



1. FPGA CPLD core board connector: for easily connecting core boards which integrate an FPGA CPLD chip onboard
2. 8I/Os_1 interface, for connecting accessory boards/modules
3. 8I/Os_2 interface, for connecting accessory boards/modules
4. 16I/Os_1 interface, for connecting accessory boards/modules
5. 16I/Os_2 interface, for connecting accessory boards/modules
6. 32I/Os_1 interface, for connecting accessory boards/modules
7. 32I/Os_2 interface, for connecting accessory boards/modules
8. 32I/Os_3 interface, for connecting accessory boards/modules

All the I/O interfaces above:

- capable of being simulated as USART, I2C, SPI, PS/2, etc.
- capable of driving devices such as FRAM, FLASH, USB, Ethernet, etc.

9. SDRAM interface
    - for connecting SDRAM accessory board
    - also works as FPGA CPLD pins expansion connectors
10. LCD interface, for connecting LCD22, LCD12864, LCD1602
11. ONE-WIRE interface: easily connects to ONE-WIRE devices (TO-92 package), such as temperature sensor (DS18B20), electronic registration number (DS2401), etc.
12. 5V DC jack
13. Joystick: five positions
14. Buzzer
15. Potentiometer: for LCD22 backlight adjustment, or LCD12864, LCD1602 contrast adjustment
16. Power switch

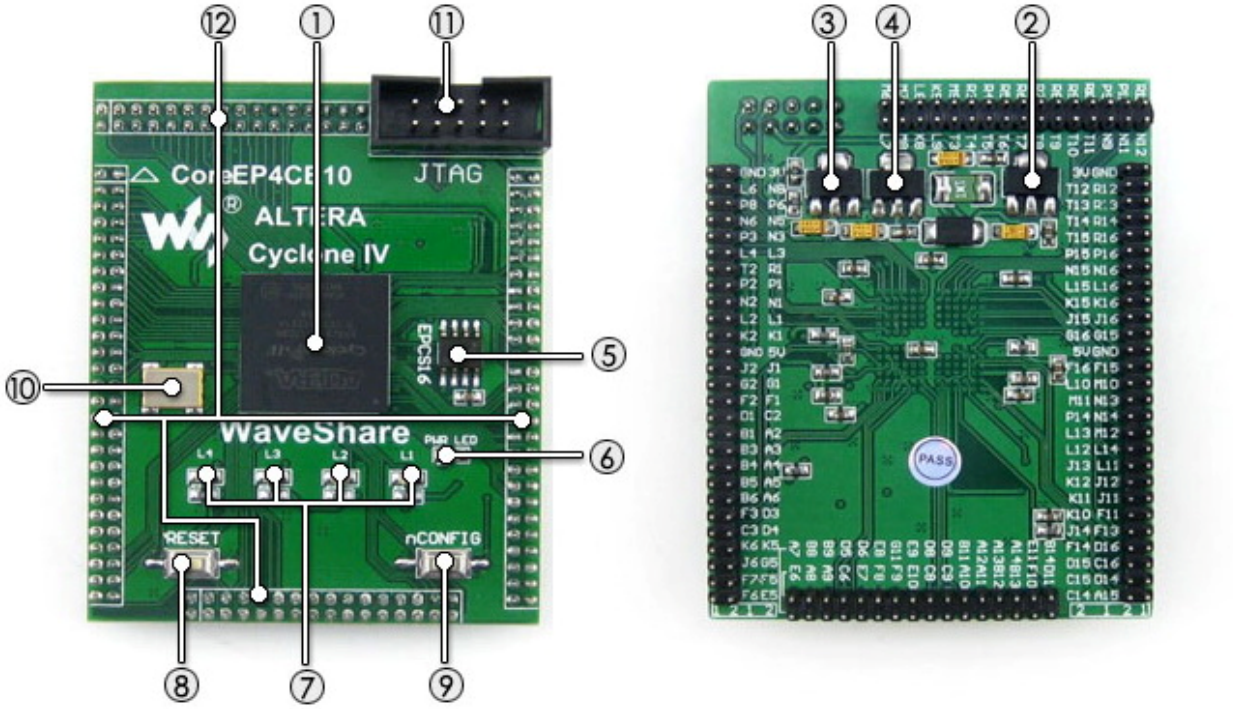
17. Buzzer jumper
18. ONE-WIRE jumper
19. Joystick jumper

For jumpers 17-19:

- short the jumper to connect to I/Os used in example code
- open the jumper to connect to other custom pins via jumper wires

The DVK600 supports a wide range of different core boards, therefore, some of the interfaces may be Not-Connected and useless while connecting to certain core board. For instance, while connecting to Core3S500E/CoreEP2C8, the '⑧ 32I/Os_3' is Not-Connected.

What's on the CoreEP4CE10



1. EP4CE10F17C8N: the ALTERA Cyclone IV FPGA device which features:
    - **Operating Frequency:** 50MHz
    - **Operating Voltage:** 1.15V～3.465V
    - **Package:** BGA256
    - **I/Os:** 164
    - **LEs:** 10K
    - **RAM:** 414kb
    - **PLLs:** 2
    - **Debugging/Programming:** supports JTAG
2. AMS1117-3.3 (on bottom side), 3.3V voltage regulator
3. AMS1117-2.5 (on bottom side), 2.5V voltage regulator
4. AMS1117-1.2 (on bottom side), 1.2V voltage regulator
5. EPCS16, onboard serial FLASH memory, for storing code
6. Power indicator
7. LEDs
8. Reset button
9. nCONFIG button: for re-configuring the FPGA chip, the equivalent of power reseting

10. 50M active crystal
11. JTAG interface: for debugging/programming
12. FPGA pins expander, VCC, GND and all the I/O ports are accessible on expansion connectors for further expansion

Examples

The OpenEP4CE10-C FPGA development board comes with various examples codes for the supported peripherals, which give you a quick start to develop your own application.

Peripheral	Description	Interface	Verilog	VHDL	NIOS II C
S29GL128P	NorFLASH	32I/Os			√
AT24CXX	EEPROM	I2C	√	√	√
FM24CXX	FRAM	I2C	√	√	√
AT45DBXX	DATAFLASH	SPI			√
SD card	FLASH	SPI			√
H57V1262GTR	SDRAM	parallel			√
PCF8563	RTC	I2C			√
DS18B20	Temperature sensor	1-WIRE	√	√	√
SP3232	Serial communication	UART	√	√	√
SP3485	Serial communication	UART	√	√	√
PL2303	USB TO UART	UART	√	√	√
FT245	USB TO FIFO	parallel			√
CY7C68013A	USB DEVICE	I/Os		√	
ENC28J60	Ethernet controller	SPI			√
Buzzer	Sound device	1I/O (PWM)	√	√	√
PS/2 keyboard	Input device	PS/2	√		√
Single buttons	Input device	----	√	√	√

4x4 keypad	Input device	8I/Os	√	√	√
Joystick	Input device	5I/Os	√	√	√
LED	Display device	----	√	√	√
8 SEG LED	Display device	13I/Os	√	√	√
VGA monitor	Display device	VGA	√	√	
Character LCD	Display device	11I/Os	√	√	
Graphic LCD	Display device	11I/Os	√		
3.2 inch multi-color LCD + touch screen	Display device + Input device	32I/Os			√

Debugging/Programming Interface

The OpenEP4CE10-C FPGA development board integrates JTAG interface for programming/debugging.

JTAG Signal Names & Description

Pin	Signal Name	Description
1	TCK	Clock signal
2	GND	Signal ground
3	TDO	Data from device
4	VCC(TRGT)	Target power supply
5	TMS	JTAG state machine control
6	NC	No connect
7	NC	No connect
8	NC	No connect
9	TDI	Data to device
10	GND	Signal ground

JTAG Header Pinout