DUAL PROCESSOR SUPERVISORS

FEATURES

- **Dual Supervisory Circuits for DSP- and Processor-Based Systems**
- **Power-On Reset Generator with Fixed Delay Time of 200ms; no External Capacitor Needed**
- **Watchdog Timer Retriggers the $\overline{\text{RESET}}$ Output at SENSEn ≥ V_{IT+}**
- **Temperature-Compensated Voltage Reference**
- **Maximum Supply Current of 40μA**
- **Supply Voltage Range: 2.7V to 6V**
- **Defined $\overline{\text{RESET}}$ Output From V_{DD} ≥ 1.1V**
- **MSOP-8 and SO-8 Packages**
- **Temperature Range: –40°C to +85°C**

APPLICATIONS

- **Processor Supply Monitoring**
- **Industrial Equipment**
- **Automotive Systems**
- **Portable/Battery-Powered Equipment**
- **Wireless Communication Systems**
- **Notebook/Desktop Computers**

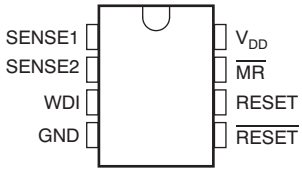
DESCRIPTION

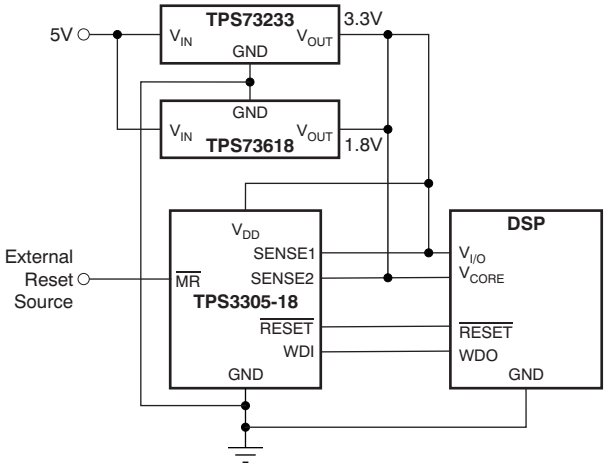
The TPS3305 family is a series of micropower supply voltage supervisors designed for circuit initialization. Its dual monitor topology is well-suited to use in DSP and processor-based systems, which often require two supply voltages, core and I/O.

$\overline{\text{RESET}}$ is asserted when the voltage at either SENSEn pin falls below its threshold voltage, V_{IT}. When both SENSEn pins are again above their respective threshold voltages, $\overline{\text{RESET}}$ is held low for the factory-programmed delay time (200ms typ). $\overline{\text{RESET}}$ is also asserted if the watchdog input (WDI) is not toggled for more than 1.6s typ.

The TPS3305-xx devices are available in either 8-pin MSOP or SO packages, and are specified for operation over a temperature range of –40°C to +85°C.

D OR DGN PACKAGE
(TOP VIEW)





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (TYP)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3305-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3305-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3305-33	5.0 V	3.3 V	4.55 V	2.93 V

(1) For the most current specifications and package information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating junction temperature range (unless otherwise noted).

	UNIT
Supply voltage range, V_{DD}	–0.3V to +7V
$V_{\overline{MR}}$, V_{WDI}	–0.3V to V_{DD} + 0.3V
Input voltage at SENSE1 and SENSE2, V_I	(V_{DD} + 0.3)V_{IT} / 1.25V
V_{RESET}, $V_{\overline{RESET}}$	–0.3V to +7V
Maximum low output current, I_{OL}	5mA
Maximum high output current, I_{OH}	–5mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	±20mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±20mA
Continuous total power dissipation	See Dissipation Ratings Table
Operating junction temperature range, T_J	–40°C to +85°C
Storage temperature range, T_{stg}	–65°C to +150°C
Soldering temperature	+260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

DISSIPATION RATINGS TABLE

PACKAGE	T_A ≤ +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DGN	2.14W	17.1mW/°C	1.37W	1.11W
D	725mW	5.8mW/°C	464mW	377mW

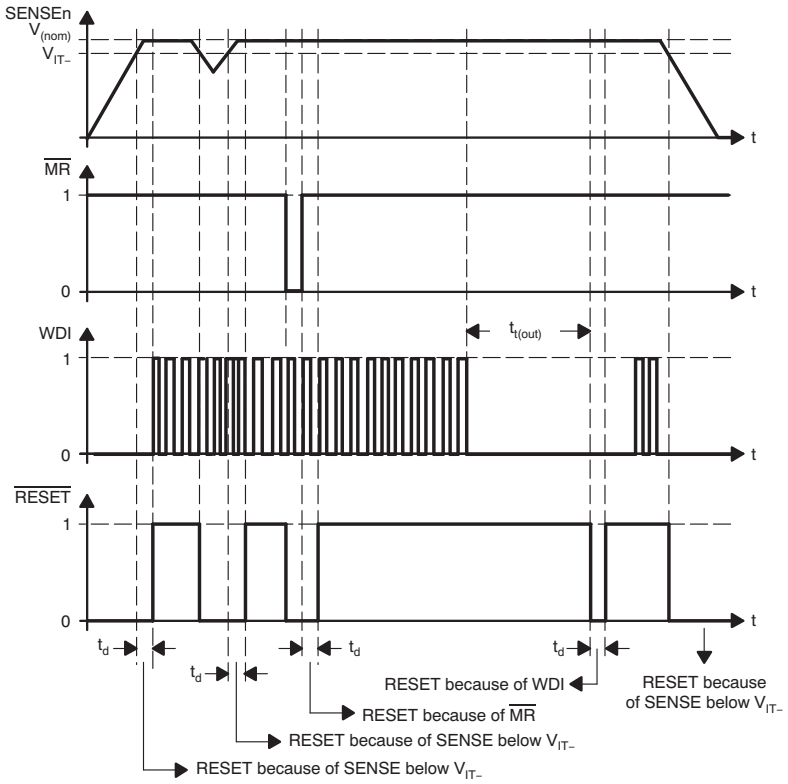
ELECTRICAL CHARACTERISTICS

Over operating junction temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	TPS3305-xx MIN	TPS3305-xx TYP	TPS3305-xx MAX	UNIT
V_{DD}	Input supply range			2.7		6.0	V
T_J	Operating junction temperature range			–40		+85	°C
V_{OH}	High-level output voltage		V_{DD} = 2.7V to 6V, I_{OH} = –20µA	V_{DD} – 0.2V			V
			V_{DD} = 3.3V, I_{OH} = –2mA	V_{DD} – 0.4V			V
			V_{DD} = 6V, I_{OH} = –3mA	V_{DD} – 0.4V			V
V_{OL}	Low-level output voltage		V_{DD} = 2.7V to 6V, I_{OL} = 20µA			0.2	V
			V_{DD} = 3.3V, I_{OL} = 2mA			0.4	V
			V_{DD} = 6V, I_{OL} = 3mA			0.4	V
	Power-up reset voltage(1)		V_{DD} ≥ 1.1V, I_{OL} = 20µA			0.4	V
$V_{IT–}$	Negative-going input threshold voltage(2)	VSENSE1, VSENSE2	V_{DD} = 2.7V to 6V, T_A = 0°C to +85°C	1.64	1.68	1.72	V
				2.20	2.25	2.30	V
				2.86	2.93	3.0	V
				4.46	4.55	4.64	V
		VSENSE1, VSENSE2	V_{DD} = 2.7V to 6V, T_A = –40°C to +85°C	1.64	1.68	1.73	V
				2.20	2.25	2.32	V
				2.86	2.93	3.02	V
				4.46	4.55	4.67	V
V_{hys}	Hysteresis at VSENSEn input		$V_{IT–}$= 1.68V		15		mV
			$V_{IT–}$ = 2.25V		20		mV
			$V_{IT–}$ = 2.93V		30		mV
			$V_{IT–}$ = 4.55V		40		mV
$I_{H(AV)}$	Average high-level input current	WDI	WDI = V_{DD} = 6V Time average (dc = 88%)		100	150	µA
$I_{L(AV)}$	Average low-level input current	WDI	WDI = 0V, V_{DD} = 6V Time average (dc = 12%)		–15	–20	µA
V_{IH}	High-level input voltage at $\overline{MR}$ and WDI			0.7 x V_{DD}			V
V_{IL}	Low-level input voltage at $\overline{MR}$ and WDI					0.3 x V_{DD}	V
Δt / ΔV	Input transition rise and fall rate at $\overline{MR}$					50	ns/V
I_H	High-level input current	WDI	WDI = V_{DD} = 6V		120	170	µA
		$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6V		–130	–180	µA
		SENSE1	VSENSE1 = V_{DD} = 6V		5	8	µA
		SENSE2	VSENSE2 = V_{DD} = 6V		6	9	µA
I_L	Low-level input current	WDI	WDI = 0V, V_{DD} = 6V		–120	–170	µA
		$\overline{MR}$	$\overline{MR}$ = 0V, V_{DD} = 6V		–430	–600	µA
		SENSEn	VSENSE1,2 = 0V	–1		1	µA
I_{DD}	Supply current					40	µA
C_I	Input capacitance		V_I = 0V to V_{DD}		10	pF	

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1 µF ceramic) should be placed close to the supply terminals.

TIMING DIAGRAM



TIMING REQUIREMENTS

At V_{DD} = 2.7V to 6V, R_L = 1MΩ, C_L = 50pF, and T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2V$, $V_{SENSEnH} = V_{IT+} + 0.2V$	6			µs
		$\overline{MR}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns
		WDI		100			ns

SWITCHING CHARACTERISTICS

At V_{DD} = 2.7V to 6V, R_L = 1MΩ, C_L = 50pF, and T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time-out		$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$ See Timing Diagram	1.1	1.6	2.3	s
t_d	Delay time		$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$ See Timing Diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESET}$, $\overline{MR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$, $\overline{MR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$, SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	µs
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{RESET}$, SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	µs

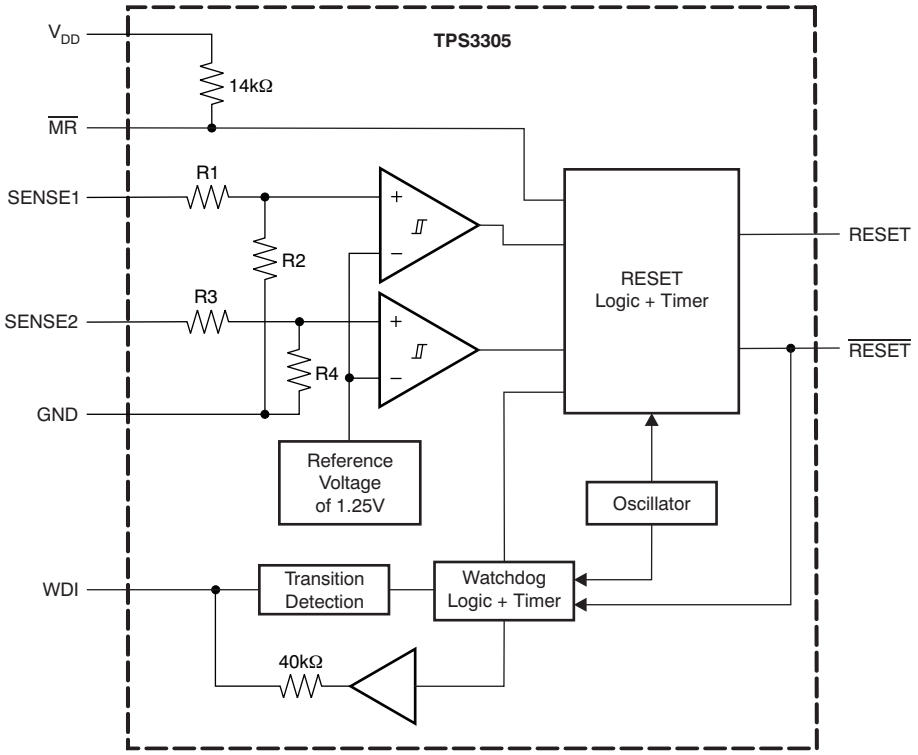
DEVICE INFORMATION

FUNCTION/TRUTH TABLE(1)

$\overline{MR}$	SENSE1 > V_{IT1}	SENSE2 > V_{IT2}	$\overline{RESET}$	RESET
L	X	X	L	H
H	0	0	L	H
H	0	1	L	H
H	1	0	L	H
H	1	1	H	L

(1) **X** = Don't care

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
GND	4	Ground
$\overline{MR}$	7	Manual reset
$\overline{RESET}$	5	Active-low reset output
RESET	6	Active-high reset output
SENSE1	1	Sense voltage input 1
SENSE2	2	Sense voltage input 2
WDI	3	Watchdog timer input
V_{DD}	8	Supply voltage

TYPICAL CHARACTERISTICS

NORMALIZED SENSE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE AT V_{DD}

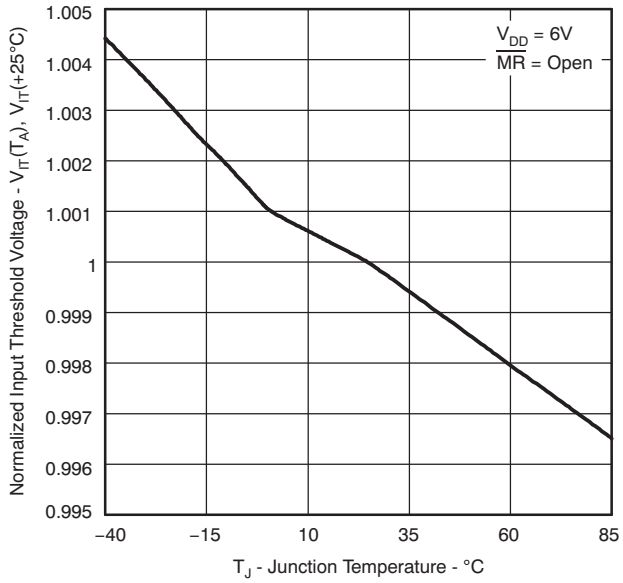


Figure 1.

SUPPLY CURRENT vs SUPPLY VOLTAGE

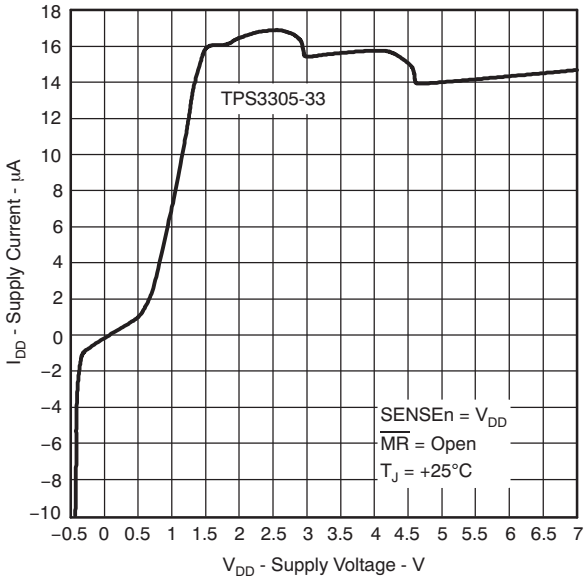


Figure 2.

INPUT CURRENT vs INPUT VOLTAGE AT $\overline{MR}$

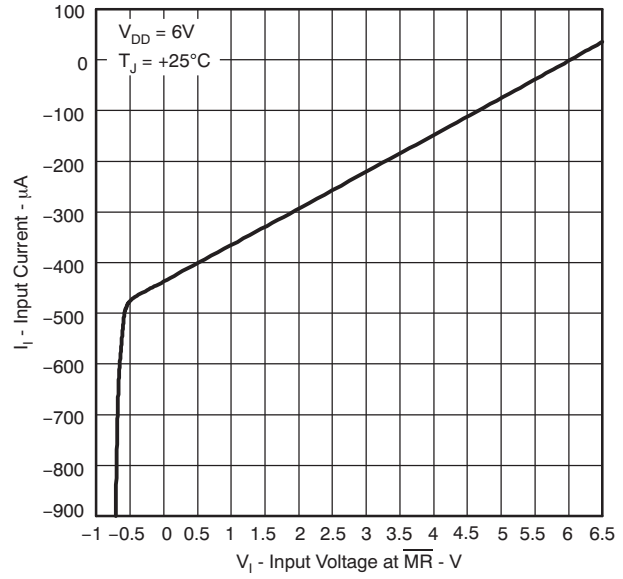


Figure 3.

MINIMUM PULSE DURATION AT SENSE vs THRESHOLD OVERDRIVE

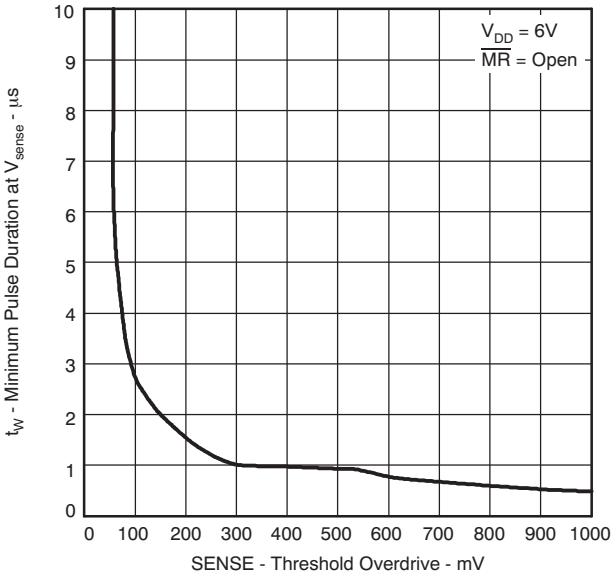


Figure 4.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

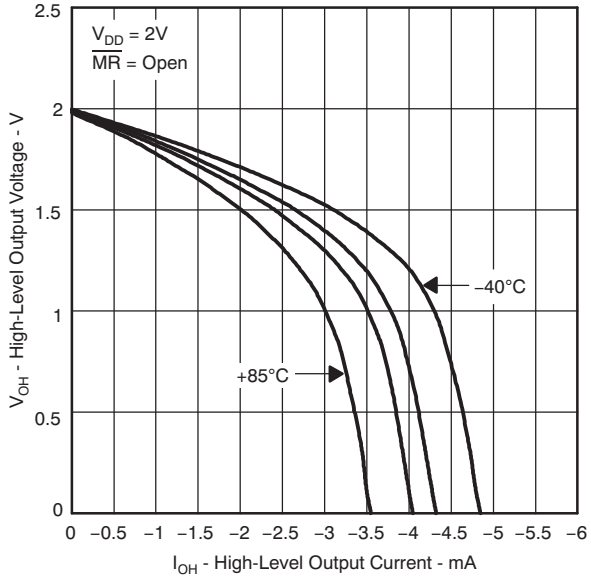


Figure 5.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

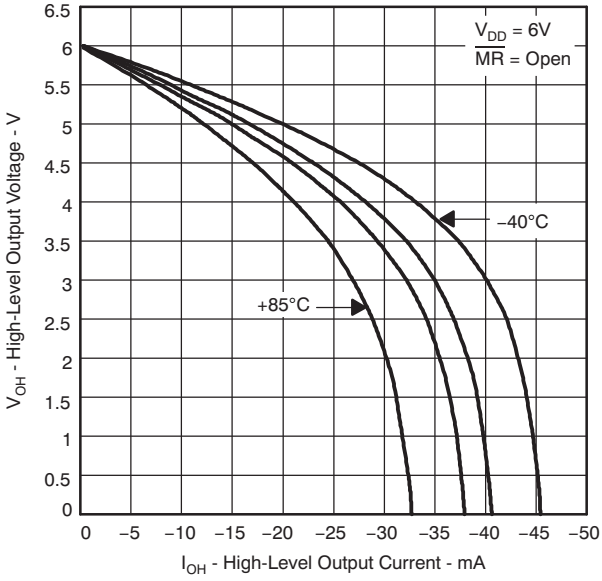


Figure 6.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

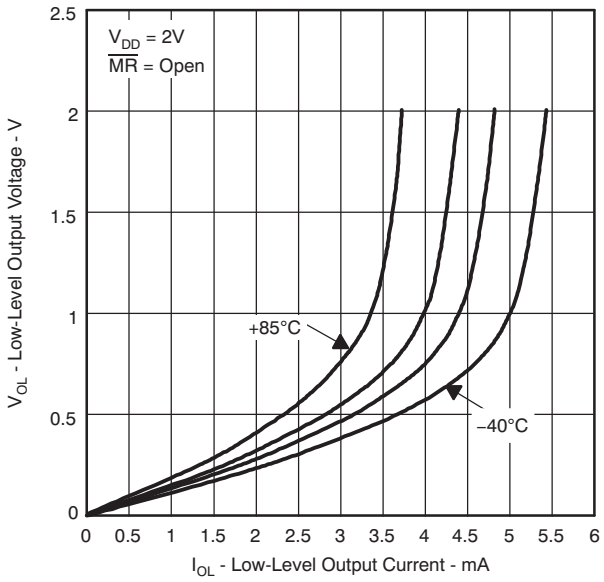


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

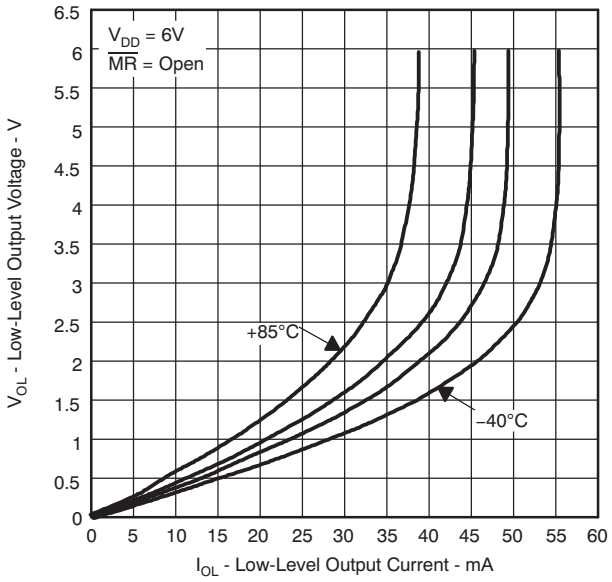


Figure 8.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3305-18D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518	Samples
TPS3305-18DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518	Samples
TPS3305-18DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM	Samples
TPS3305-18DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM	Samples
TPS3305-18DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM	Samples
TPS3305-18DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAM	Samples
TPS3305-18DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518	Samples
TPS3305-18DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30518	Samples
TPS3305-25D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30525	Samples
TPS3305-25DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAN	Samples
TPS3305-25DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAN	Samples
TPS3305-25DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30525	Samples
TPS3305-33D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533	Samples
TPS3305-33DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533	Samples
TPS3305-33DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO	Samples
TPS3305-33DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO	Samples
TPS3305-33DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO	Samples
TPS3305-33DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAO	Samples
TPS3305-33DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	30533	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

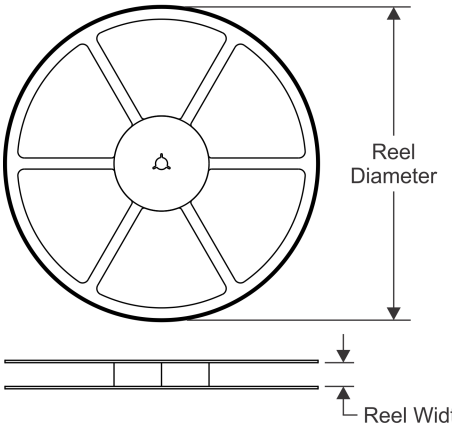
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

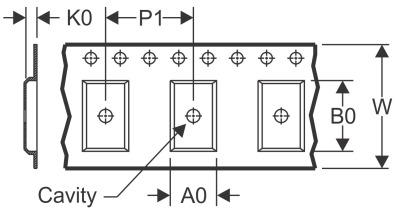
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

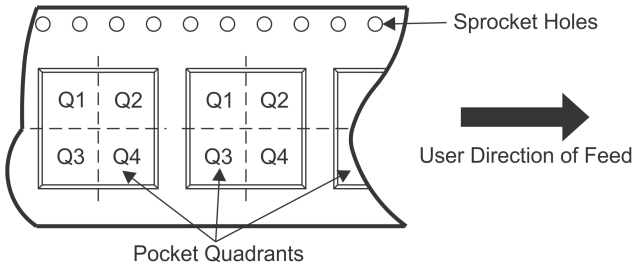


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

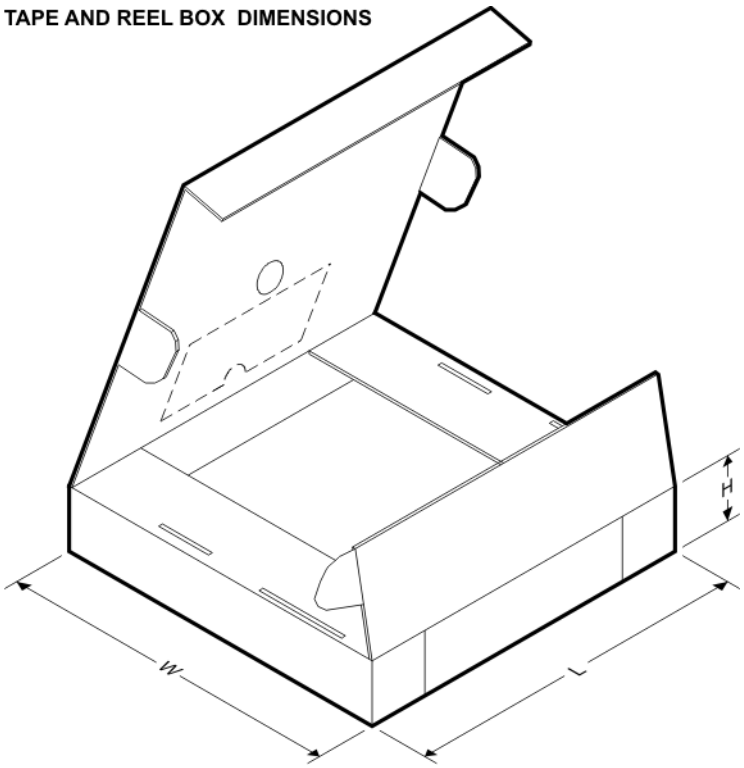
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3305-18DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-18DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3305-25DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3305-33DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3305-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3305-18DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3305-18DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3305-25DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3305-25DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS3305-33DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPS3305-33DR	SOIC	D	8	2500	350.0	350.0	43.0

GENERIC PACKAGE VIEW

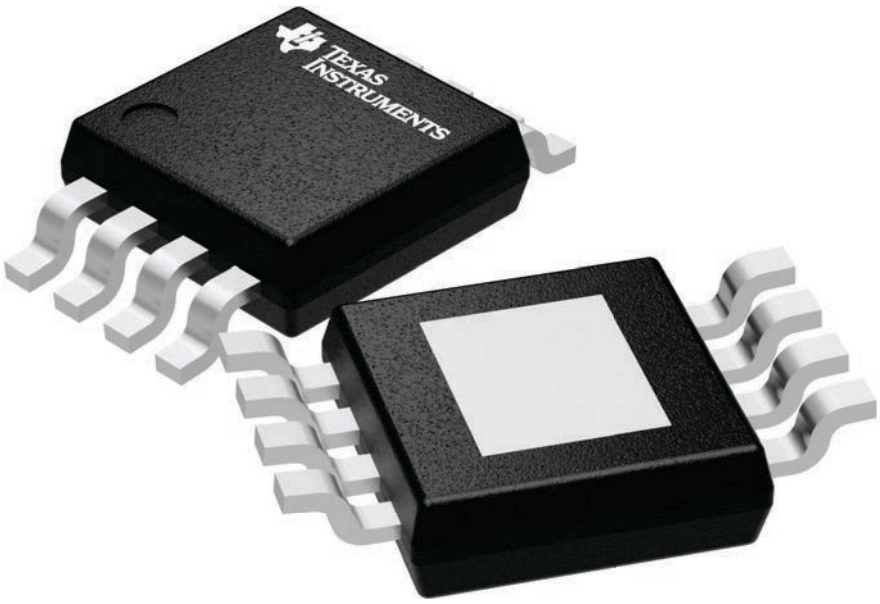
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

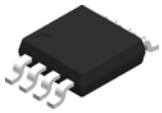
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

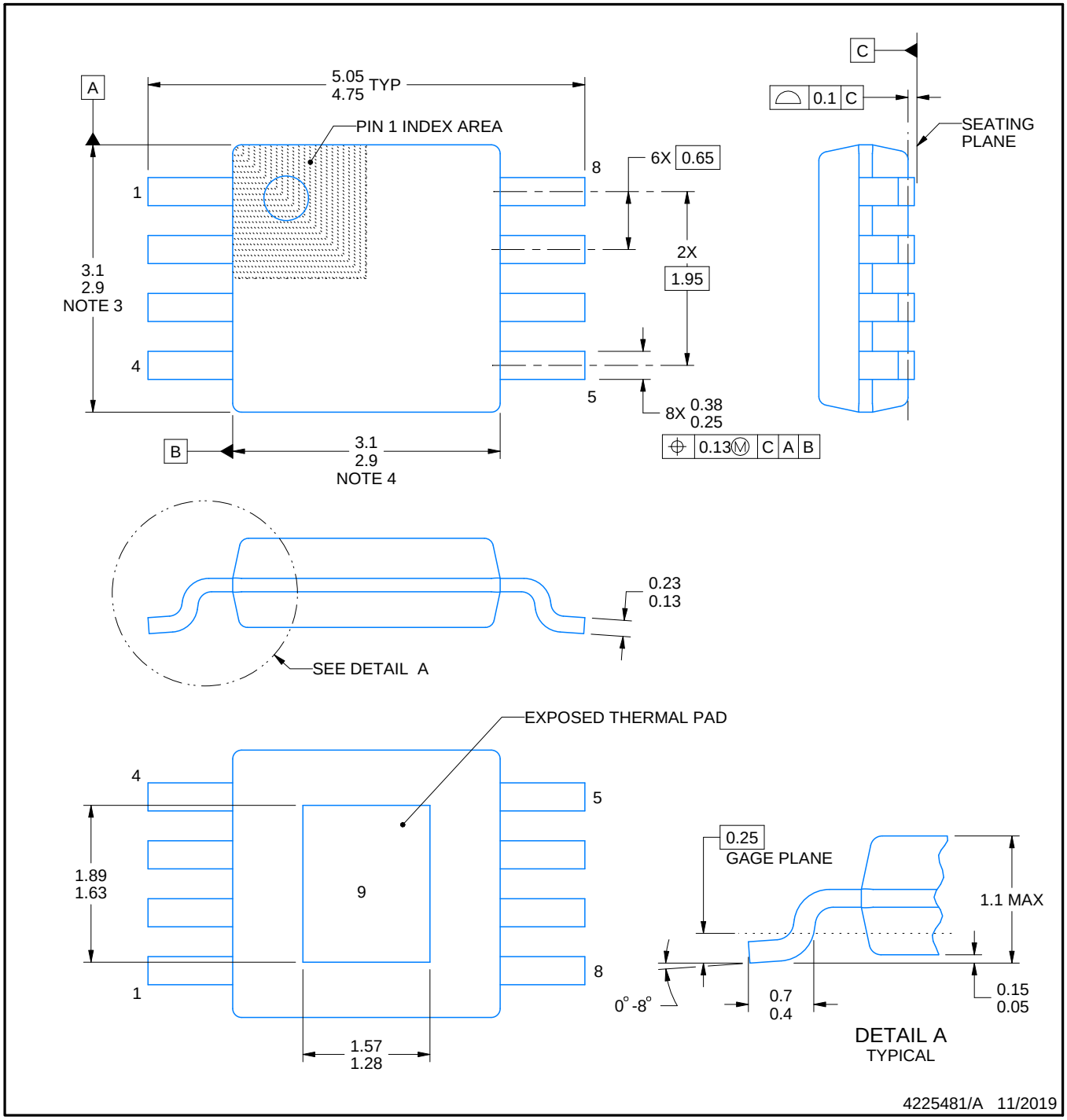
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

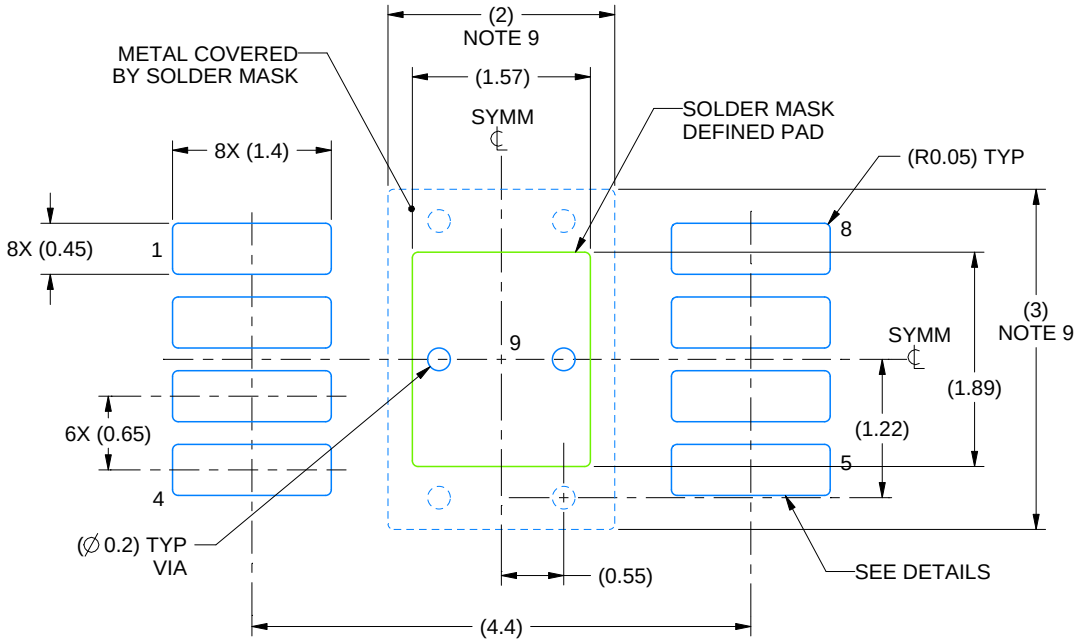
SMALL OUTLINE PACKAGE



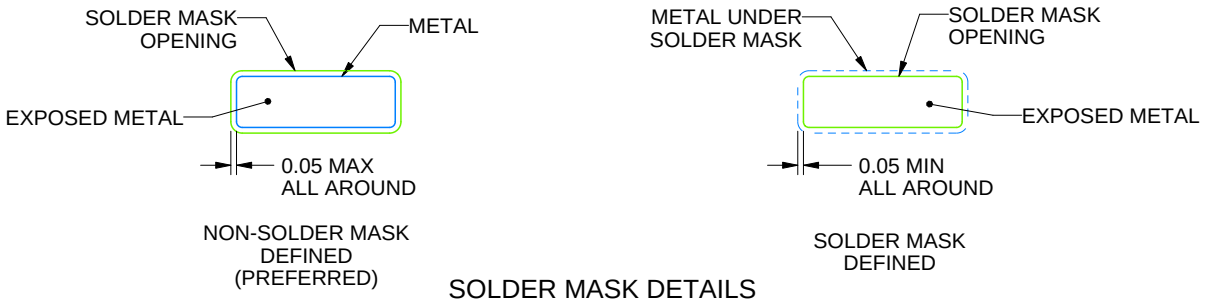
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

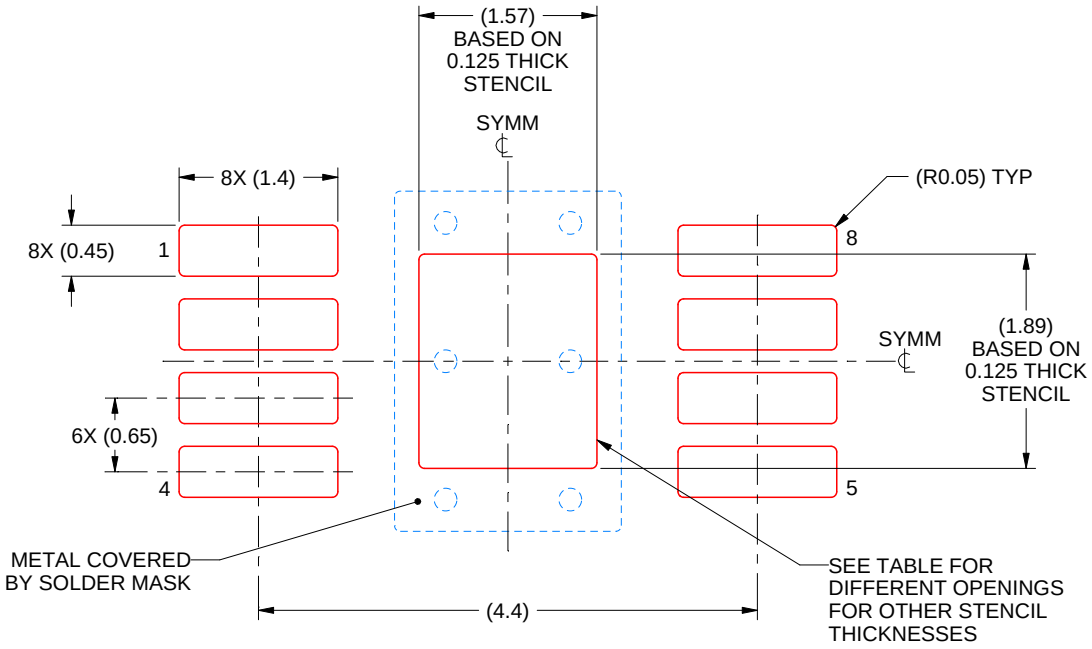


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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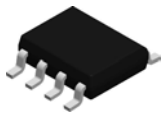
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

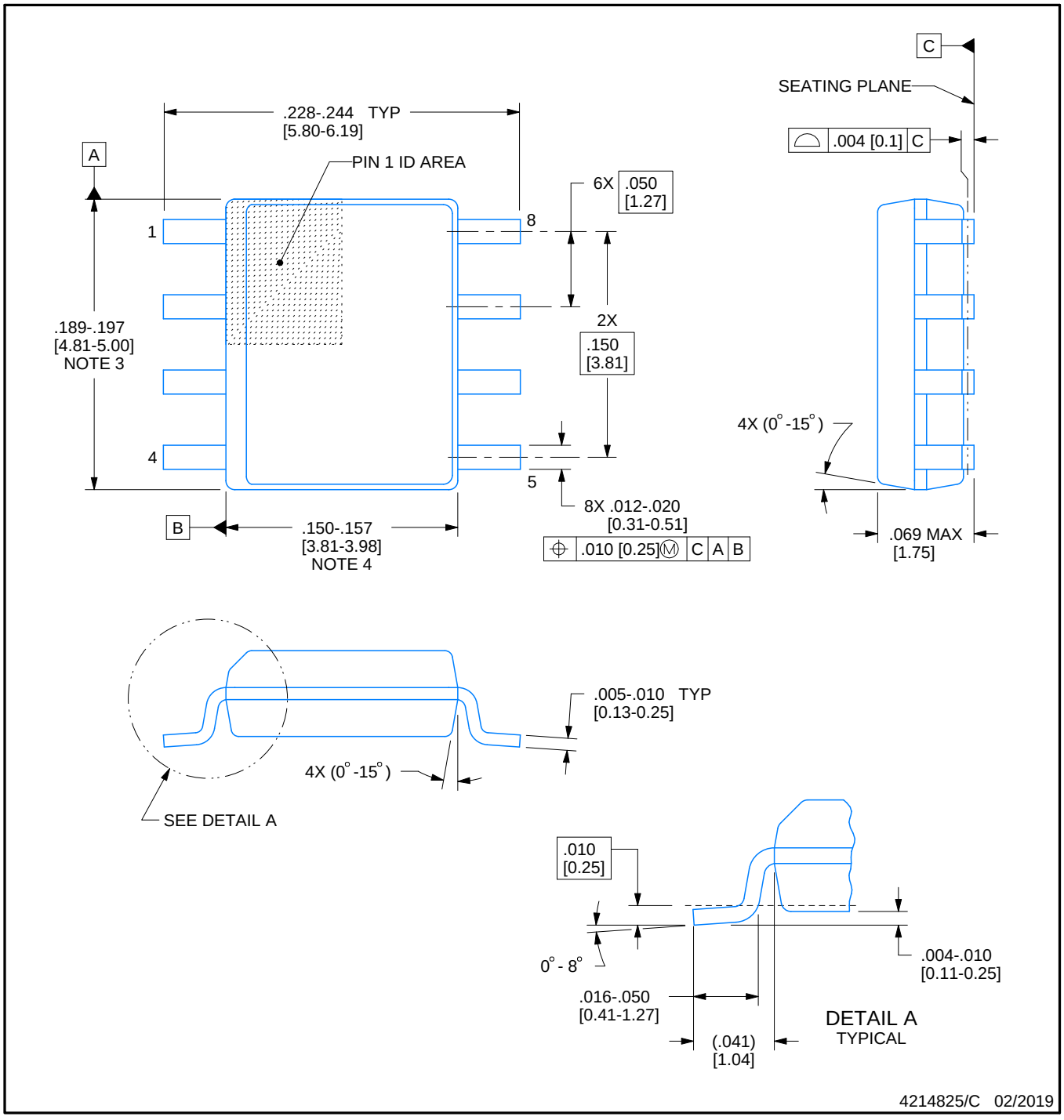


PACKAGE OUTLINE

D0008A

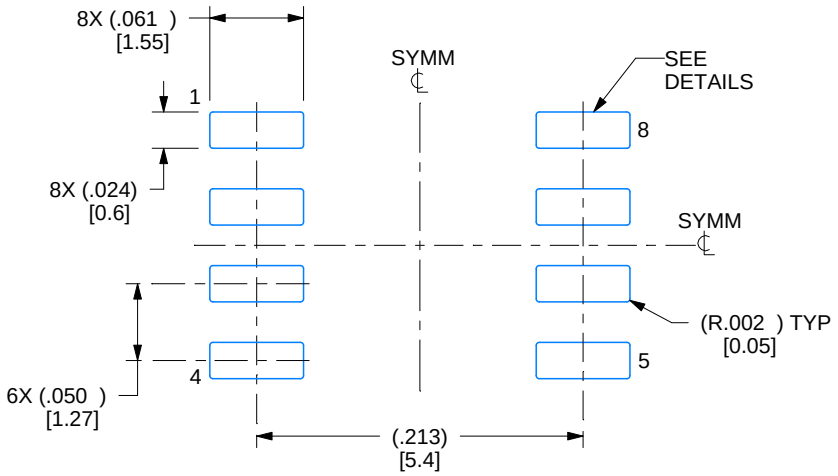
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

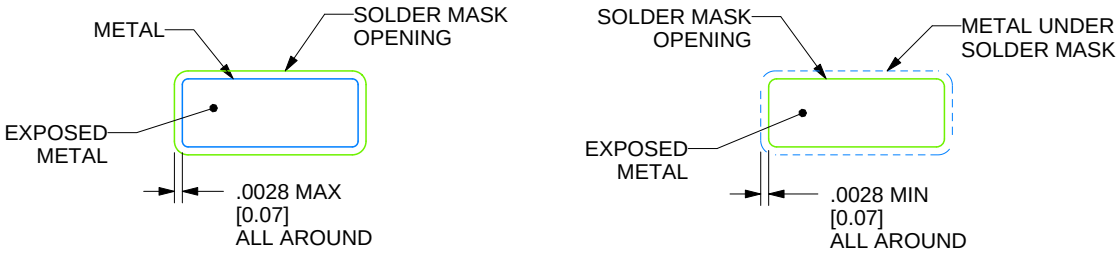


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

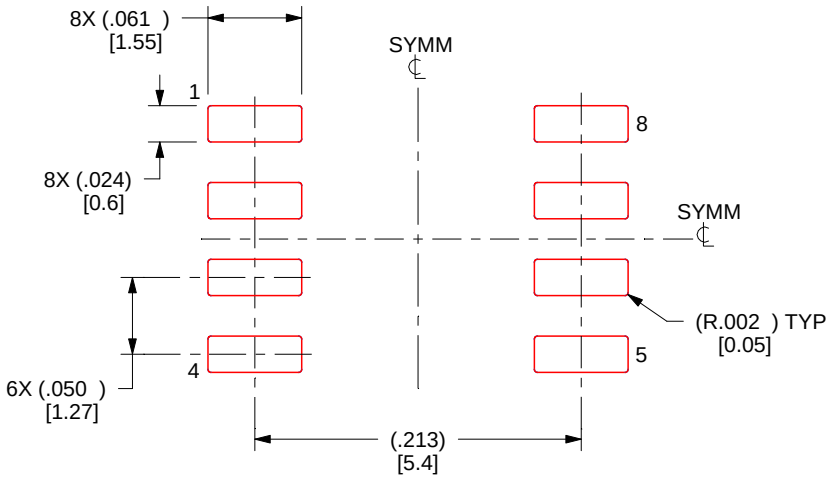
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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