TEXAS INSTRUMENTS

TPS62200, TPS62201, TPS62202, TPS62203
TPS62204, TPS62205, TPS62207, TPS62208

SLVS417F – MARCH 2002 – REVISED JUNE 2015

TPS6220x High-Efficiency, SOT23 Step-Down, DC-DC Converter

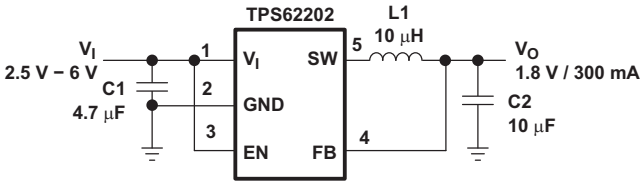
1 Features

- High-Efficiency Synchronous Step-Down Converter With up to 95% Efficiency
- 2.5-V to 6-V Input Voltage Range
- Adjustable Output Voltage Range From 0.7 V to V_I
- Fixed Output Voltage Options Available
- Up to 300-mA Output Current
- 1-MHz Fixed-Frequency PWM Operation
- Highest Efficiency Over Wide Load Current Range Due to Power Save Mode
- 15-µA Typical Quiescent Current
- Soft Start
- 100% Duty Cycle Low-Dropout Operation
- Dynamic Output-Voltage Positioning
- Available in a 5-Pin SOT23 Package

2 Applications

- PDAs and Pocket PCs
- Cellular Phones and Smart Phones
- Low Power DSP Supplies
- Digital Cameras
- Portable Media Players
- Portable Equipment

Typical Application Schematic



(Fixed Output Voltage Version)

3 Description

The TPS6220x devices are a family of high-efficiency synchronous step-down converters ideally suited for portable systems powered by 1-cell Li-Ion or 3-cell NiMH/NiCd batteries. The devices are also suitable to operate from a standard 3.3-V or 5-V voltage rail.

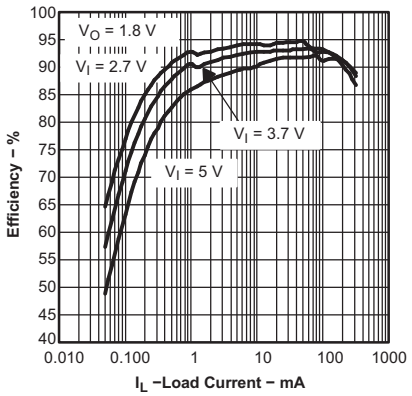
With an output voltage range of 6 V down to 0.7 V and up to 300 mA output current, the devices are ideal to power low voltage DSPs and processors used in PDAs, pocket PCs, and smart phones. Under nominal load current, the devices operate with a fixed switching frequency of typically 1 MHz. At light load currents, the part enters the power save mode operation; the switching frequency is reduced and the quiescent current is typically only 15 µA; therefore, it achieves the highest efficiency over the entire load current range. The TPS6220x needs only three small external components. Together with the SOT23 package, a minimum system solution size is achieved. An advanced fast response voltage mode control scheme achieves superior line and load regulation with small ceramic input and output capacitors.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6220x	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2006) to Revision F	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed the format of this data sheet to the new SDA format. No markup for changes.	1

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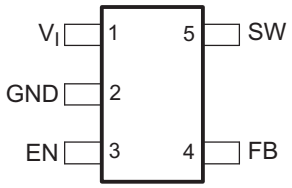
5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	This is the enable pin of the device. Pulling this pin to ground forces the device into shutdown mode. Pulling this pin to Vin enables the device. This pin must not be left floating and must be terminated.
FB	4	I	This is the feedback pin of the device. Connect this pin directly to the output if the fixed output voltage version is used. For the adjustable version an external resistor divider is connected to this pin. The internal voltage divider is disabled for the adjustable version.
GND	2	—	Ground
SW	5	I/O	Connect the inductor to this pin. This pin is the switch pin and is connected to the internal MOSFET switches.
V_I	1	I	Supply voltage pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Supply voltages (2)	–0.3	7.0	V
	Voltages on pins SW, EN, FB (2)	–0.3	V_{CC} +0.3	V
P_D	Continuous power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Supply voltage	2.5		6.0	V
V_O	Output voltage for adjustable output voltage version	0.7		V_I	V
I_O	Output current			300	mA
L	Inductor(1)	4.7	10		µH
C_I	Input capacitor(1)		4.7		µF
C_O	Output capacitor(1)		10		µF
T_A	Operating ambient temperature	40		85	°C
T_J	Operating junction temperature	40		125	°C

(1) See *Application and Implementation* for further information.

6.4 Thermal Information

THERMAL METRIC(1)		TPS6220x DBV [SOT-23] 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	125	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

V_I = 3.6 V, V_O = 1.8 V, I_O = 200 mA, EN = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage			2.5		6	V
I_Q	Operating quiescent current		I_O = 0 mA, Device is not switching		15	30	µA
	Shutdown supply current		EN = GND		0.1	1	µA
	Undervoltage lockout threshold			1.5		2	V
ENABLE							
$V_{(EN)}$	EN high level input voltage			1.3			V
	EN low level input voltage					0.4	V
$I_{(EN)}$	EN input bias current		EN = GND or VIN		0.01	0.1	µA
POWER SWITCH							
r_{ds}(ON)	P-channel MOSFET on-resistance		V_{IN} = V_{GS} = 3.6 V		530	690	mΩ
			V_{IN} = V_{GS} = 2.5 V		670	850	
	N-channel MOSFET on-resistance		V_{IN} = V_{GS} = 3.6 V		430	540	mΩ
			V_{IN} = V_{GS} = 2.5 V		530	660	
$I_{lkg_(P)}$	P-channel leakage current		V_{DS} = 6.0 V		0.1	1	µA
$I_{lkg_(N)}$	N-channel leakage current		V_{DS} = 6.0 V		0.1	1	µA
$I_{(LIM)}$	P-channel current limit		2.5 V < Vin < 6.0 V	380	480	670	mA
OSCILLATOR							
f_S	Switching frequency			650	1000	1500	kHz
OUTPUT							
V_O	Adjustable output voltage	TPS62200		0.7		V_{IN}	V
V_{ref}	Reference voltage				0.5		V
	Feedback voltage (1)	TPS62200	V_I = 3.6 V to 6 V, I_O = 0 mA	0%		3%	
		Adjustable	V_I = 3.6 V to 6 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
V_O	Fixed output voltage(1)	TPS62207	V_I = 2.5 V to 6 V, I_O = 0 mA	0%		3%	
		1.2 V	V_I = 2.5 V to 6 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62201	V_I = 2.5 V to 6 V, I_O = 0 mA	0%		3%	
		1.5 V	V_I = 2.5 V to 6 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62204	V_I = 2.5 V to 6 V, I_O = 0 mA	0%		3%	
		1.6 V	V_I = 2.5 V to 6 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62202	V_I = 2.5 V to 6 V, I_O = 0 mA	0%		3%	
		1.8 V	V_I = 2.5 V to 6 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62208	V_I = 2.5 V to 6 V, I_O = 0 mA	0%		3%	
		1.875 V	V_I = 2.5 V to 6 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62205	V_I = 2.7 V to 6 V, I_O = 0 mA	0%		3%	
		2.5 V	V_I = 2.7 V to 6 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62203	V_I = 3.6 V to 6 V, I_O = 0 mA	0%		3%	
		3.3 V	V_I = 3.6 V to 6 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
	Line regulation		V_I = 2.5 V to 6 V, I_O = 10 mA		0.26		%/V
	Load regulation		I_O = 100 mA to 300 mA		0.0014		%/mA
I_{lkg}	Leakage current into SW pin		Vin > Vout, 0 V ≤ Vsw ≤ Vin		0.1	1	µA
I_{lkg}(Rev)	Reverse leakage current into pin SW		Vin = open, EN = GND, V_{SW} = 6 V		0.1	1	µA

(1) For output voltages ≤ 1.2 V, a 22-µF output capacitor value is required to achieve a maximum output voltage accuracy of 3% while operating in power save mode (PFM mode).

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6.6 Typical Characteristics

Table 1. Table of Graphs

			FIGURES
η	Efficiency	vs Load current	Figure 6, Figure 7, Figure 8
		vs Input voltage	Figure 9
I_Q	No load quiescent current	vs Input voltage	Figure 1
f_s	Switching frequency	vs Temperature	Figure 10
V_o	Output voltage	vs Output current	Figure 11
r_{ds}(on)	r_{ds}(on) - P-channel switch,	vs Input voltage	Figure 2
	r_{ds}(on) - N-channel rectifier switch	vs Input voltage	Figure 3
	Line transient response		Figure 12
	Load transient response		Figure 13
	Power save mode operation		Figure 14
	Start-up		Figure 15

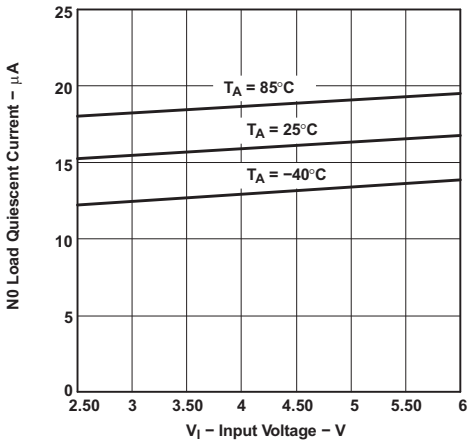

Figure 1. No Load Quiescent Current vs Input Voltage

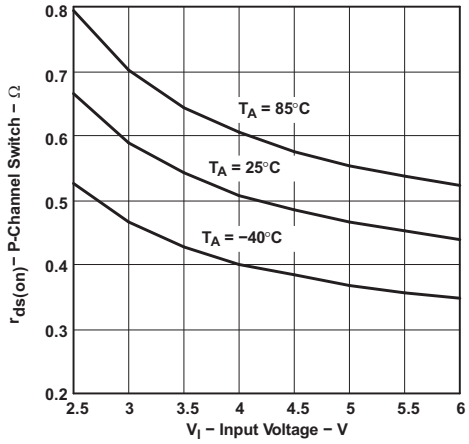

Figure 2. r_{ds}(on) P-Channel Switch vs Input Voltage

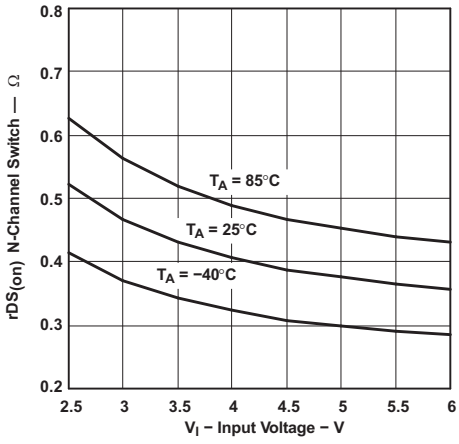

Figure 3. r_{ds}(on) N-Channel Switch vs Input Voltage

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7 Detailed Description

7.1 Overview

The TPS6220x device is a synchronous step-down converter operating with typically 1-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents and in power save mode operating with pulse frequency modulation (PFM) at light load currents.

During PWM operation the converter uses a unique fast response, voltage mode, controller scheme with input voltage feed forward. This achieves good line and load regulation and allows the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. Then the N-channel rectifier switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The GM amplifier and input voltage determines the rise time of the Sawtooth generator; therefore any change in input voltage or output voltage directly controls the duty cycle of the converter. This gives a very good line and load transient regulation.

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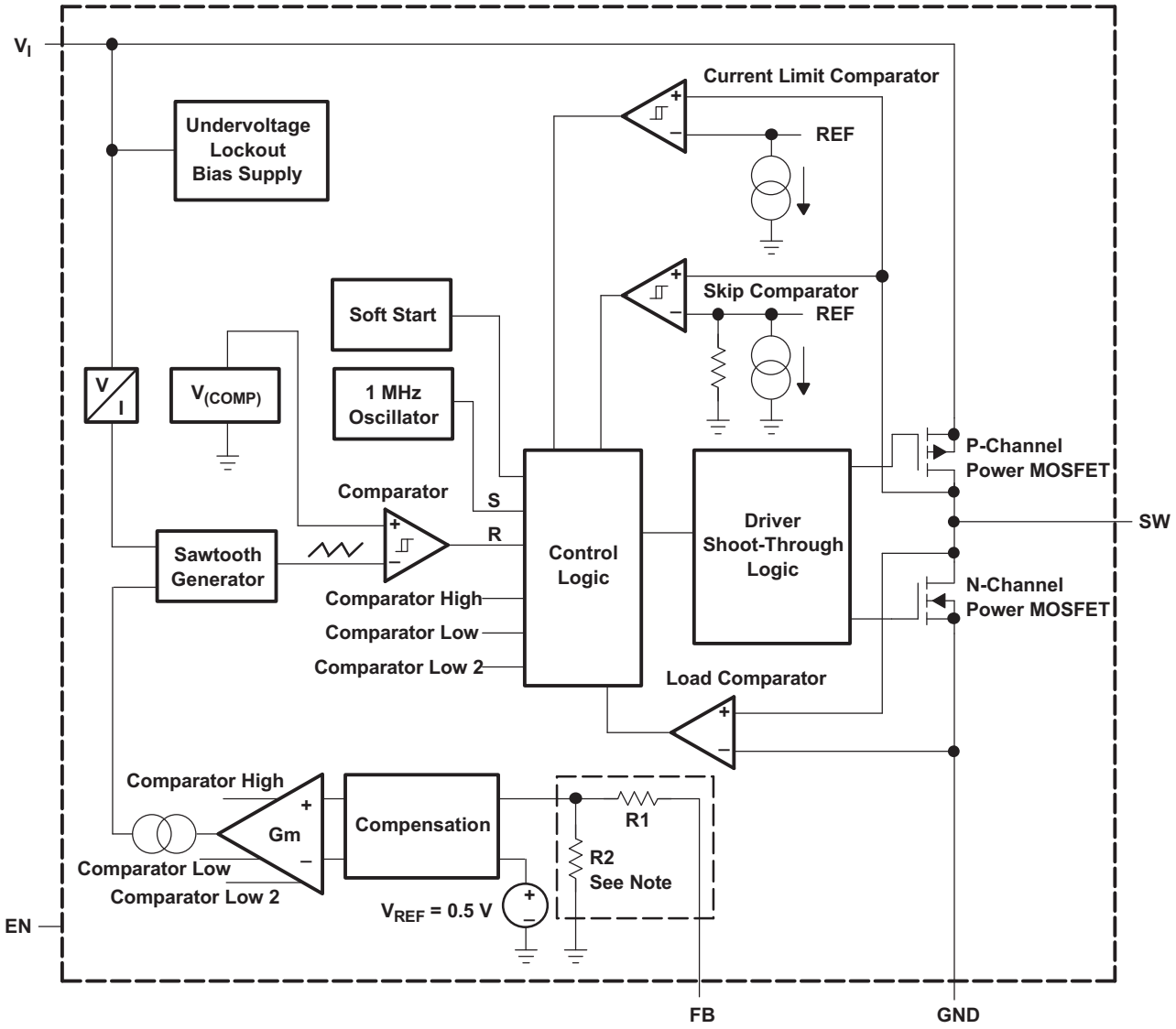
7.2 Functional Block Diagram



For the adjustable version (TPS62200), the internal feedback divider is disabled and the FB pin is directly connected to the internal GM amplifier.

7.3 Feature Description

7.3.1 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

7.3.2 Dynamic Voltage Positioning

As described in the power save mode operation sections and as detailed in Figure 4, the output voltage is typically 0.8% above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. During a load transient from full load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel rectifier switch.

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Feature Description (continued)

7.3.3 Soft Start

The TPS6220x has an internal soft start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage in case a battery or a high-impedance power source is connected to the input of the TPS6220x.

The soft start is implemented as a digital circuit increasing the switch current in steps of typically 60 mA, 120 mA, 240 mA, and then the typical switch current limit of 480 mA. Therefore the start-up time mainly depends on the output capacitor and load current. Typical start-up time with a 10-µF output capacitor and 200-mA load current is 800 µs.

7.3.4 Low Dropout Operation 100% Duty Cycle

The TPS6220x offers a low input to output voltage difference, while still maintaining operation with the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation, depending on the load current and output voltage, can be calculated as:

$$Vin_{min} = Vout_{max} + Iout_{max} \times \left(r_{ds}(ON)_{max} + R_L\right)$$

where

- $Iout_{max}$ = maximum output current plus inductor ripple current.
- $r_{ds}(ON)_{max}$ = maximum P-channel switch $r_{ds}(ON)$.
- R_L = DC resistance of the inductor.
- $Vout_{max}$ = nominal output voltage plus maximum output voltage tolerance. (1)

7.3.5 Enable

Pulling the enable low forces the part into shutdown, with a shutdown quiescent current of typically 0.1 µA. In this mode, the P-channel switch and N-channel rectifier are turned off, the internal resistor feedback divider is disconnected, and the whole device is in shutdown mode. If an output voltage, which could be an external voltage source or super capacitor, is present during shutdown, the reverse leakage current is specified under *Electrical Characteristics*. For proper operation the enable pin must be terminated and must not be left floating.

Pulling the enable high starts up the TPS6220x with the soft start as previously described.

7.4 Device Functional Modes

7.4.1 Power Save Mode Operation

As the load current decreases, the converter enters the power save mode operation. During power save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

Two conditions allow the converter to enter the power save mode operation. One is when the converter detects the discontinuous conduction mode. The other is when the peak switch current in the P-channel switch goes below the skip current limit. The typical skip current limit can be calculated as

$$I_{skip} \le 66\ mA + \frac{Vin}{160\ \Omega} \quad (2)$$

During the power save mode, the output voltage is monitored with the comparator by the thresholds comparator low and comparator high. As the output voltage falls below the comparator low threshold set to typically 0.8% above Vout nominal, the P-channel switch turns on. The P-channel switch is turned off as the peak switch current is reached. The typical peak switch current can be calculated:

$$I_{peak} = 66\ mA + \frac{Vin}{80\ \Omega} \quad (3)$$

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Device Functional Modes (continued)

The N-channel rectifier is turned on and the inductor current ramps down. As the inductor current approaches zero, the N-channel rectifier is turned off and the P-channel switch is turned on again, starting the next pulse. The converter continues these pulses until the comparator high threshold (set to typically 1.6% above Vout nominal) is reached. The converter enters a sleep mode, reducing the quiescent current to a minimum. The converter wakes up again as the output voltage falls below the comparator low threshold again. This control method reduces the quiescent current typically to 15 µA and reduces the switching frequency to a minimum, thereby achieving the high converter efficiency. Setting the skip current thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic output voltage achieving lower absolute voltage drops during heavy load transient changes. This allows the converter to operate with a small output capacitor of just 10 µF and still have a low absolute voltage drop during heavy load transient changes. See Figure 4 for detailed operation of the power save mode.

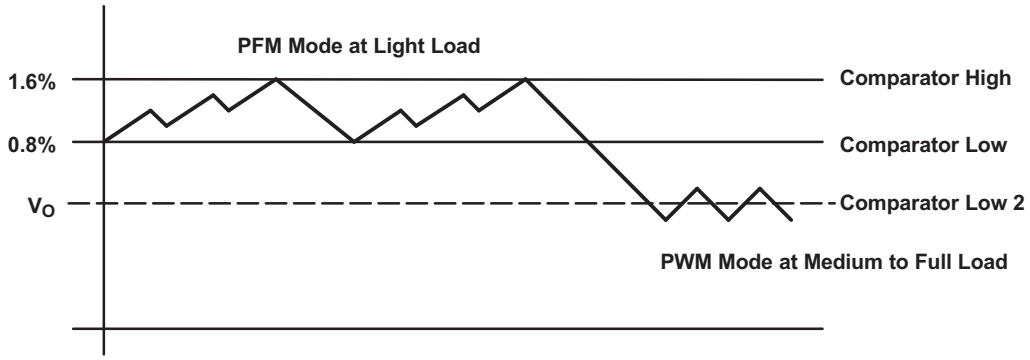

Figure 4. Power Save Mode Thresholds and Dynamic Voltage Positioning

The converter enters the fixed frequency PWM mode again as soon as the output voltage falls below the comparator low 2 threshold.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS6220x devices are a family of high-efficiency synchronous step-down converters ideally suited for portable systems powered by 1-cell Li-Ion or 3-cell NiMH/NiCd batteries. The devices are also suitable to operate from a standard 3.3-V or 5-V voltage rail.

8.2 Typical Application

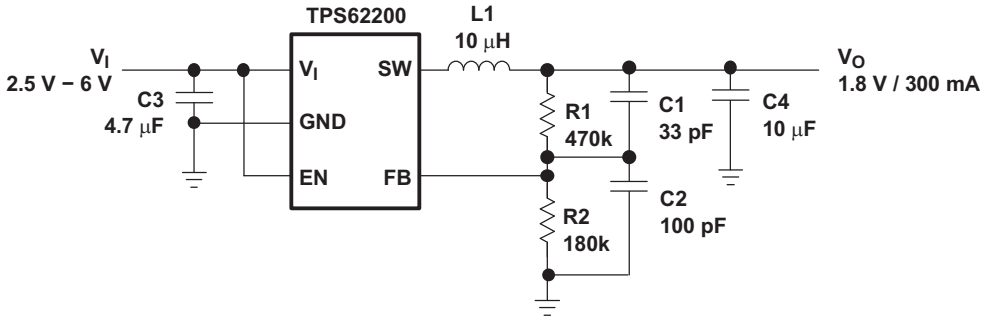

Figure 5. Typical Application Circuit for the Adjustable Output Voltage

8.2.1 Design Requirements

The *Detailed Design Procedure* provides a component selection to operate the device within the *Recommended Operating Conditions*.

8.2.2 Detailed Design Procedure

8.2.2.1 Adjustable Output Voltage Version

When the adjustable output voltage version TPS62200 is used, the output voltage is set by the external resistor-divider. See Figure 5.

The output voltage is calculated as:

$$V_{out} = 0.5\ V \times \left(1 + \frac{R1}{R2}\right)$$

where

- R1 + R2 ≤ 1 MΩ and internal reference voltage V(ref)typ = 0.5 V. (4)

R1 + R2 should not be greater than 1 MΩ for reasons of stability. To keep the operating quiescent current to a minimum, the feedback resistor-divider should have high impedance with R1+R2 ≤ 1 MΩ. Because of the high impedance and the low reference voltage of V_{ref} = 0.5 V, the noise on the feedback pin (FB) needs to be minimized. Using a capacitive divider C1 and C2 across the feedback resistors minimizes the noise at the feedback without degrading the line or load transient performance.

C1 and C2 should be selected as:

$$C1 = \frac{1}{2 \times \pi \times 10\ kHz \times R1}$$

where

- R1 = upper resistor of voltage divider.

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Typical Application (continued)

- C1 = upper capacitor of voltage divider. (5)

For C1 a value should be chosen that comes closest to the calculated result.

$$C2 = \frac{R1}{R2} \times C1$$

where

- R2 = lower resistor of voltage divider.
- C2 = lower capacitor of voltage divider. (6)

For C2 the selected capacitor value should always be selected larger than the calculated result. For example, in Figure 5 for C2, 100 pF are selected for a calculated result of C2 = 86.17 pF.

If quiescent current is not a key design parameter, C1 and C2 can be omitted, and a low-impedance feedback divider must be used with R1+R2 <100 kΩ. This design reduces the noise available on the feedback pin (FB) as well, but increases the overall quiescent current during operation.

8.2.2.2 Inductor Selection

The TPS6220x device is optimized to operate with a typical inductor value of 10 µH.

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Although the inductor core material has less effect on efficiency than its DC resistance, an appropriate inductor core material must be used.

The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current, and the lower the conduction losses of the converter. On the other hand, larger inductor values cause a slower load transient response. Usually the inductor ripple current, as calculated below, is around 20% of the average output current.

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current that is calculated as:

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- f = switching frequency (1 MHz typical, 650 kHz minimal).
- L = inductor value.
- ΔI_L = peak-to-peak inductor ripple current.
- I_{Lmax} = maximum inductor current. (7)

The highest inductor current occurs at maximum Vin.

A more conservative approach is to select the inductor current rating just for the maximum switch current of 670 mA. Refer to Table 2 for inductor recommendations.

Table 2. Recommended Inductors

INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
10 µH 10 µH 10 µH 10 µH	Sumida CDRH5D28-100 Sumida CDRH5D18-100 Sumida CDRH4D28-100 Coilcraft DO1608-103	High efficiency
6.8 µH 10 µH 10 µH 10 µH 10 µH	Sumida CDRH3D16-6R8 Sumida CDRH4D18-100 Sumida CR32-100 Sumida CR43-100 Murata LQH4C100K04	Smallest solution

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8.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Also the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 4.7-µF input capacitor is sufficient. The capacitor can be increased without any limit for better input-voltage filtering. If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements.

Ceramic capacitors show a good performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the device for best performance (refer to Table 3 for recommended components).

8.2.2.4 Output Capacitor Selection

The advanced fast response voltage mode control scheme of the TPS6220x allows the use of tiny ceramic capacitors with a value of 10 µF without having large output voltage under and overshoots during heavy load transients.

Ceramic capacitors with low ESR values have the lowest output voltage ripple and are therefore recommended. If required, tantalum capacitors may be used as well (refer to Table 3 for recommended components).

At nominal load current the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (8)$$

where

- the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the device operates in power save mode, and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the output voltage Vo.

Table 3. Recommended Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
4.7 µF	0805	Taiyo Yuden JMK212BY475MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106MG TDK C12012X5ROJ106K	Ceramic Ceramic
10 µF	1206	Taiyo Yuden JMK316BJ106KL TDK C3216X5ROJ106M	Ceramic
22 µF	1210	Taiyo Yuden JMK325BJ226MM	Ceramic

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8.2.3 Application Curves

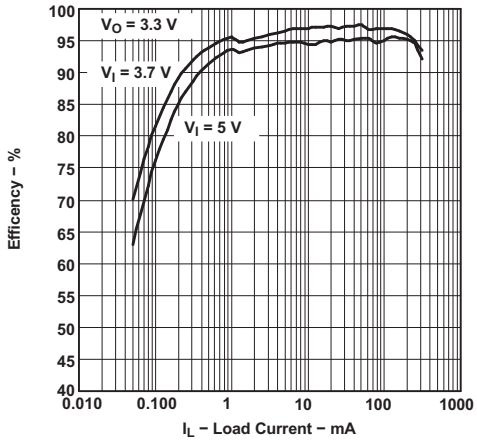

Figure 6. Efficiency vs Load Current

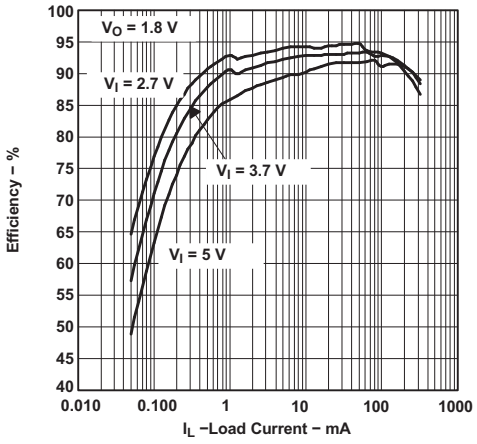

Figure 7. Efficiency vs Load Current

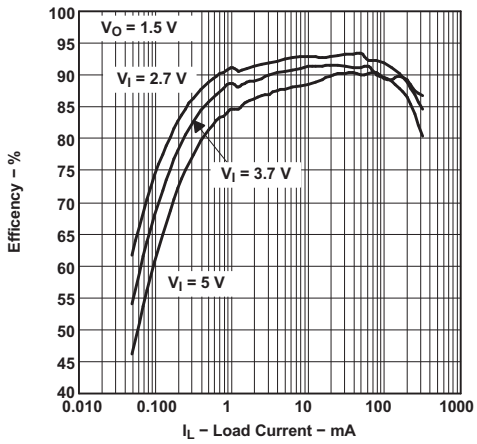

Figure 8. Efficiency vs Load Current

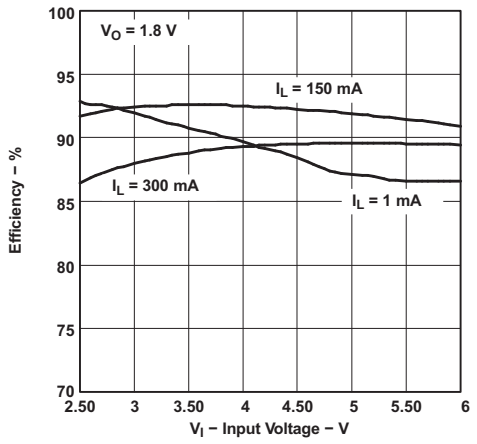

Figure 9. Efficiency vs Input Voltage

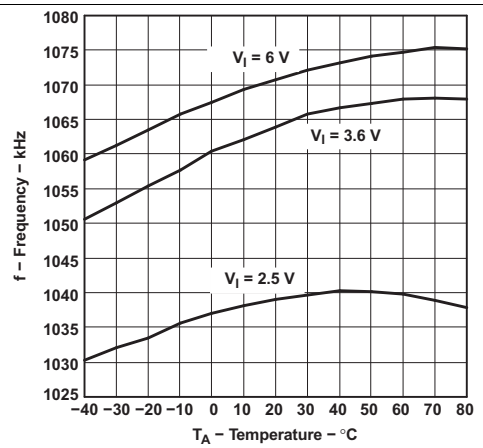

Figure 10. Frequency vs Temperature

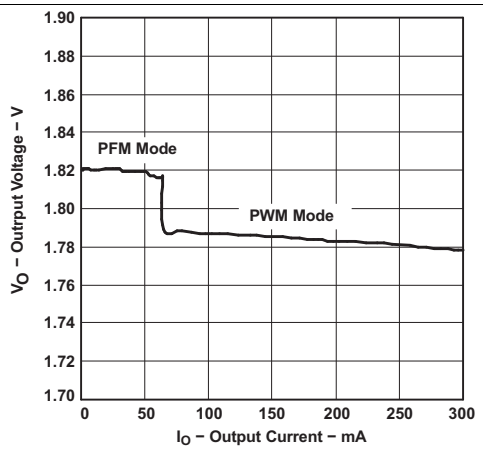

Figure 11. Output Voltage vs Output Current

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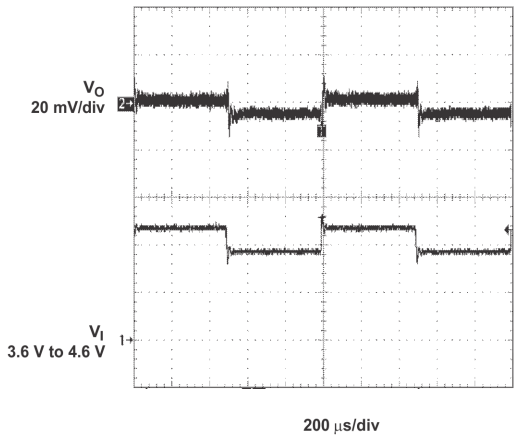

Figure 12. Line Transient Response

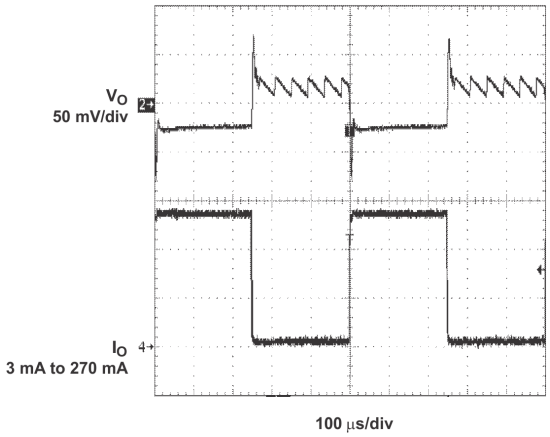

Figure 13. Load Transient Response

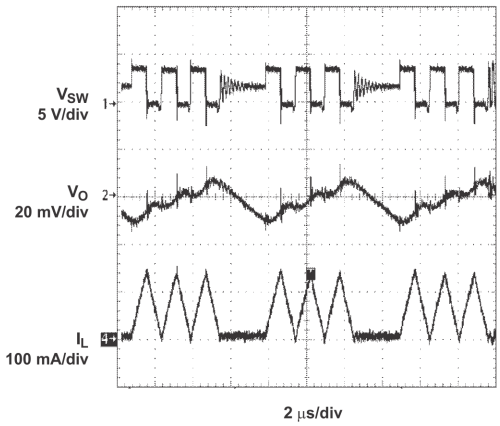

Figure 14. Power Save Mode Operation

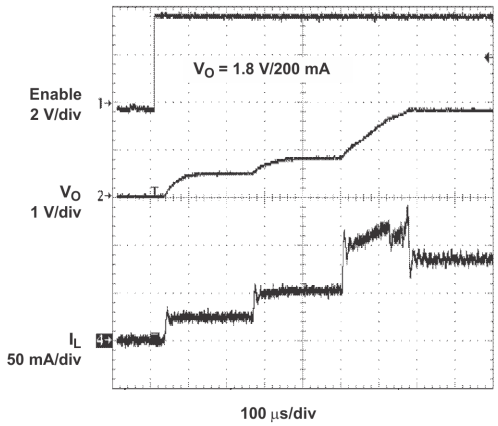

Figure 15. Start-Up

8.3 System Examples

8.3.1 Various Output Voltages

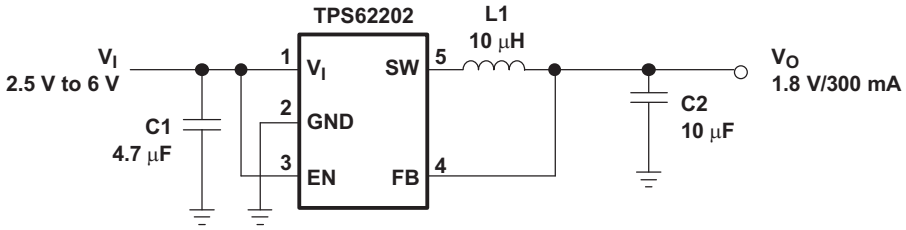

Figure 16. Li-Ion to 1.8-V Fixed Output Voltage Version

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System Examples (continued)

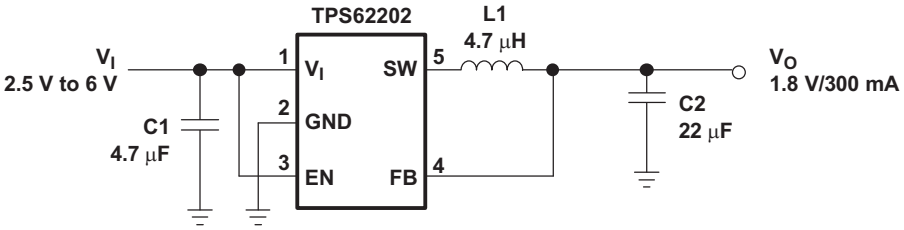

Figure 17. 1.8 V Fixed Output Voltage Version Using 4.7-µH Inductor

8.3.2 Adjustable Output Voltage Version Set to 1.5 V

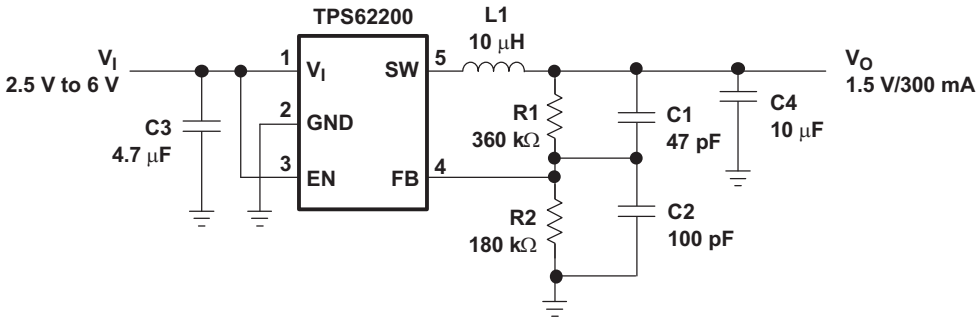

Figure 18. Adjustable Output Voltage Version Set to 1.5 V

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9 Power Supply Recommendations

The TPS6220x device family has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage, and output current of the TPS6220x.

10 Layout

10.1 Layout Guidelines

- For all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator shows stability problems as well as EMI problems.
- Therefore use wide and short traces for the main current paths, as indicated in bold in Figure 19. The input capacitor should be placed as close as possible to the IC pins.
- The feedback resistor network must be routed away from the inductor and switch node to minimize noise and magnetic interference. To further minimize noise from coupling into the feedback network and feedback pin, the ground plane or ground traces must be used for shielding. This becomes very important especially at high switching frequencies of 1 MHz.

10.2 Layout Example

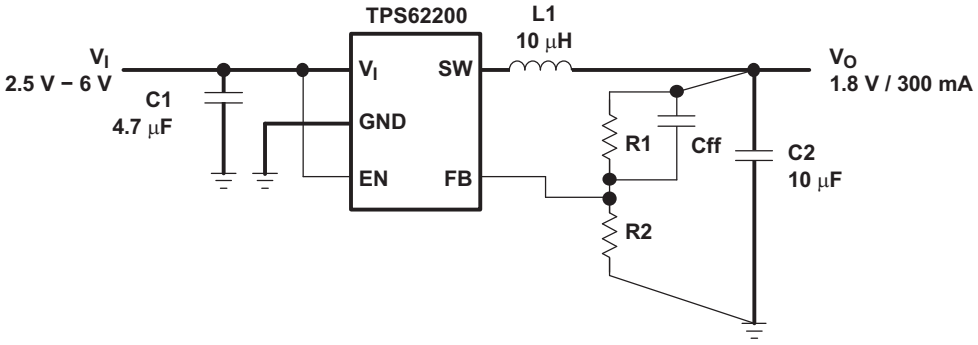

Figure 19. Layout Diagram

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62200	Click here	Click here	Click here	Click here	Click here
TPS62201	Click here	Click here	Click here	Click here	Click here
TPS62202	Click here	Click here	Click here	Click here	Click here
TPS62203	Click here	Click here	Click here	Click here	Click here
TPS62204	Click here	Click here	Click here	Click here	Click here
TPS62205	Click here	Click here	Click here	Click here	Click here
TPS62207	Click here	Click here	Click here	Click here	Click here
TPS62208	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62200DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHKI	Samples
TPS62200DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHKI	Samples
TPS62200DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHKI	Samples
TPS62201DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHLI	Samples
TPS62201DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHLI	Samples
TPS62201DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHLI	Samples
TPS62202DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHMI	Samples
TPS62202DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHMI	Samples
TPS62202DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHMI	Samples
TPS62203DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHNI	Samples
TPS62203DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHNI	Samples
TPS62203DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHNI	Samples
TPS62203DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHNI	Samples
TPS62204DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHSI	Samples
TPS62204DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHSI	Samples
TPS62205DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHTI	Samples
TPS62205DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHTI	Samples
TPS62205DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHTI	Samples
TPS62205DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHTI	Samples
TPS62207DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJGI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62207DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJGI	Samples
TPS62207DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJGI	Samples
TPS62208DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALW	Samples
TPS62208DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALW	Samples
TPS62208DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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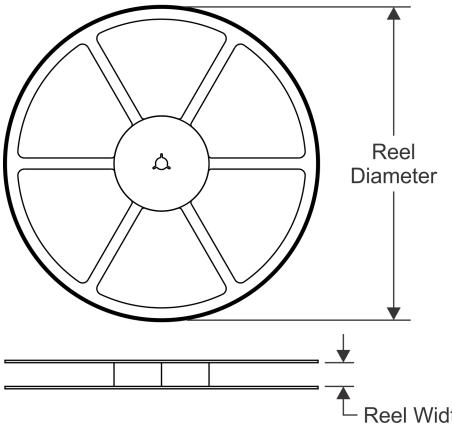
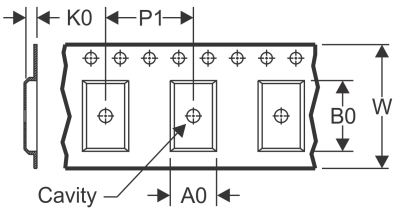
TAPE AND REEL INFORMATION

REEL DIMENSIONS

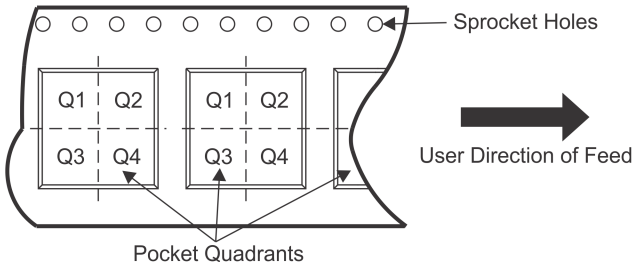


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

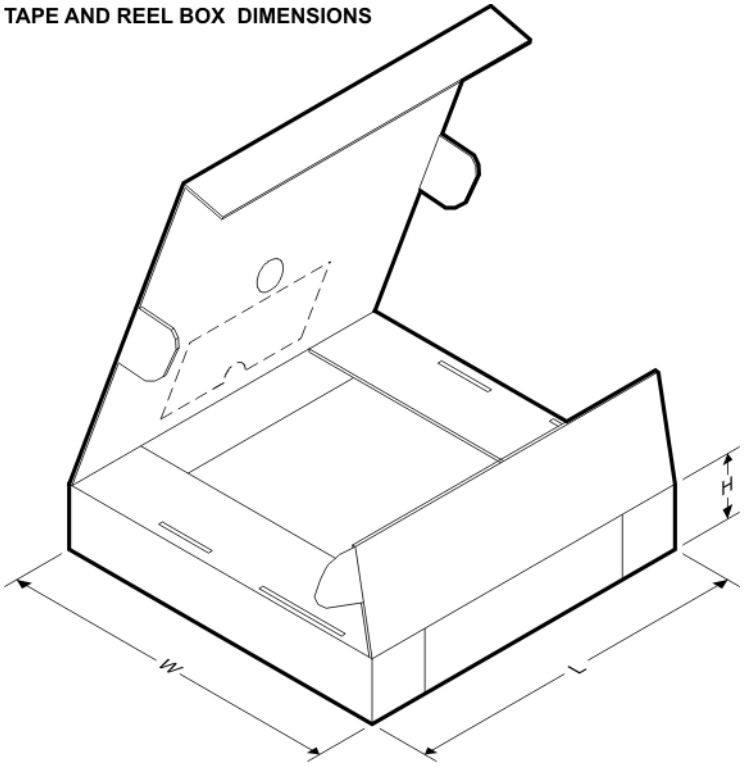


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62200DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62200DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62200DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62200DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62201DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62201DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62201DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62201DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62202DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62202DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62202DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS62202DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62203DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62203DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62203DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62203DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62204DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62204DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62204DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62204DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62205DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62205DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62205DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62205DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62207DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62207DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62207DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62207DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62208DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS62208DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62208DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS62208DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62200DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS62200DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS62200DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0

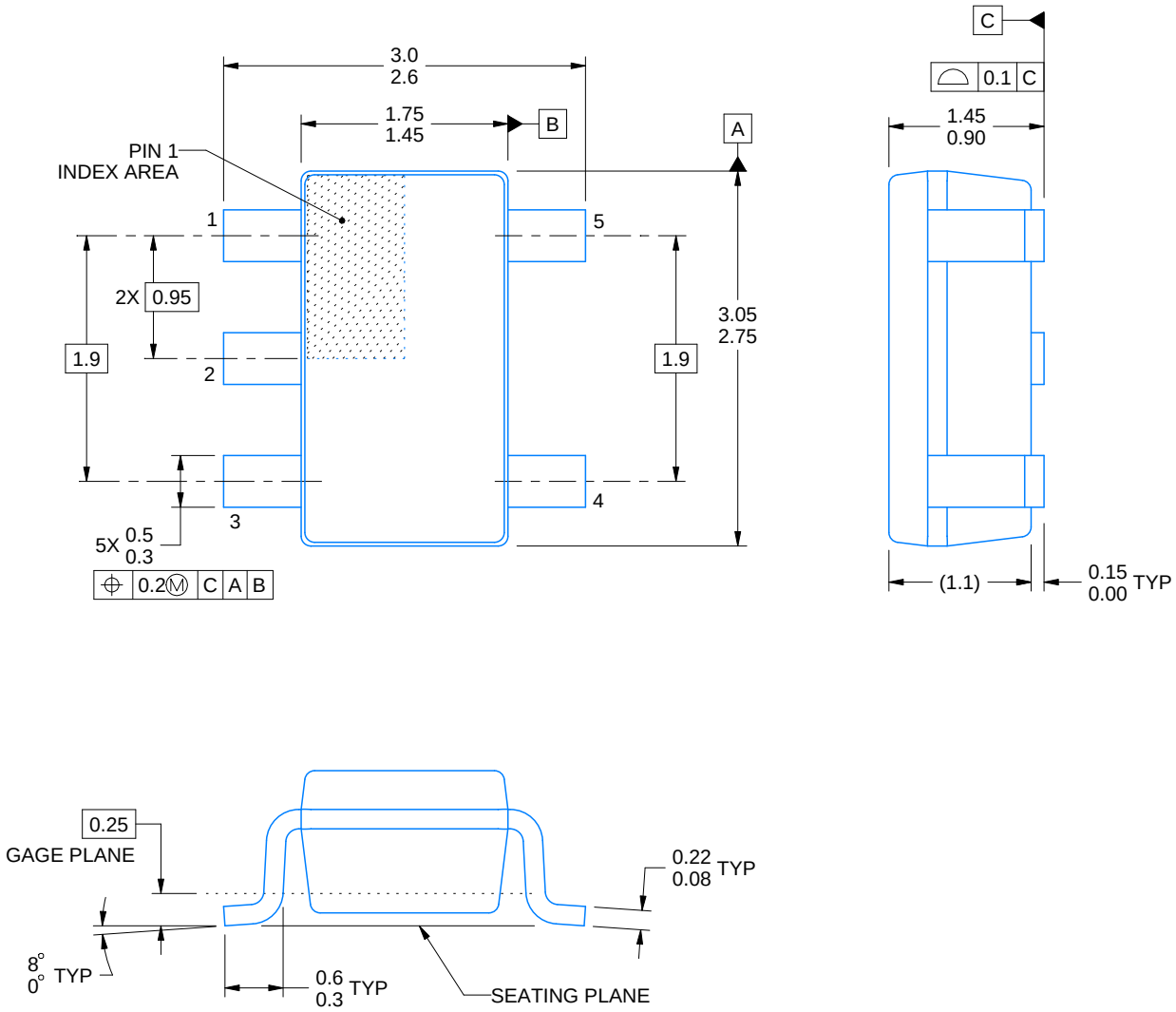
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62200DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS62201DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS62201DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS62201DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS62201DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS62202DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS62202DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS62202DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS62202DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS62203DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS62203DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS62203DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS62203DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS62204DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS62204DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS62204DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS62204DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS62205DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS62205DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS62205DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS62205DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS62207DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS62207DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS62207DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS62207DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS62208DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS62208DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS62208DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS62208DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

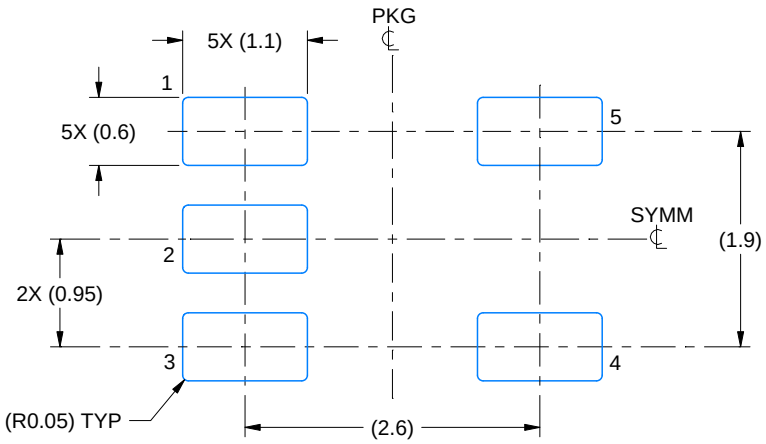
SMALL OUTLINE TRANSISTOR



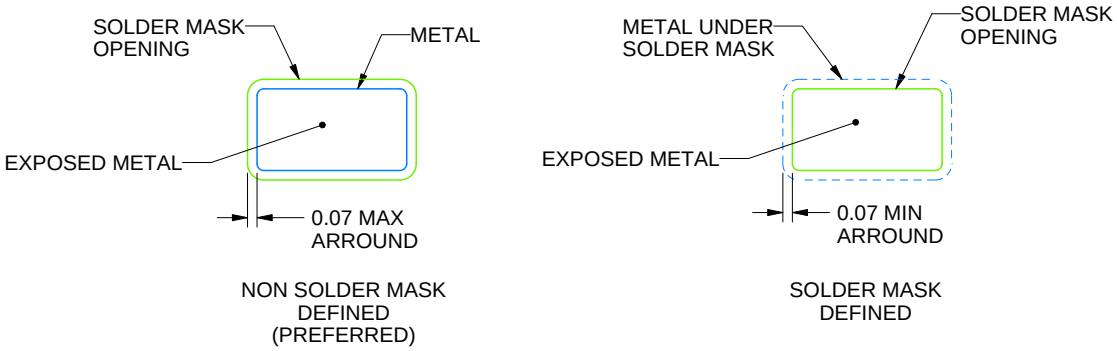
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

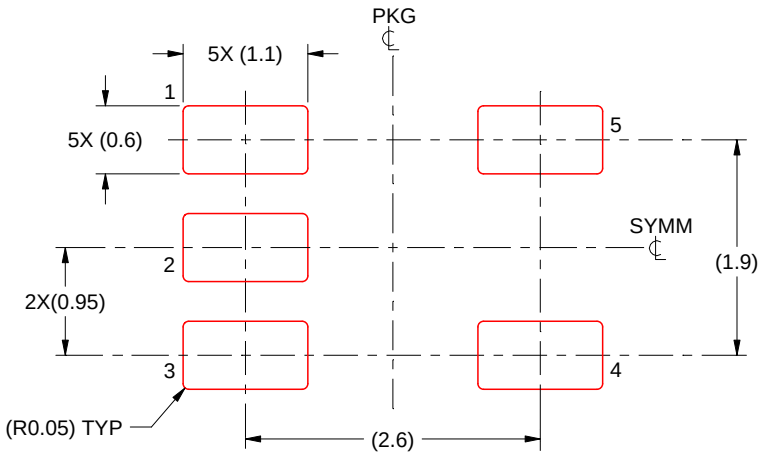


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

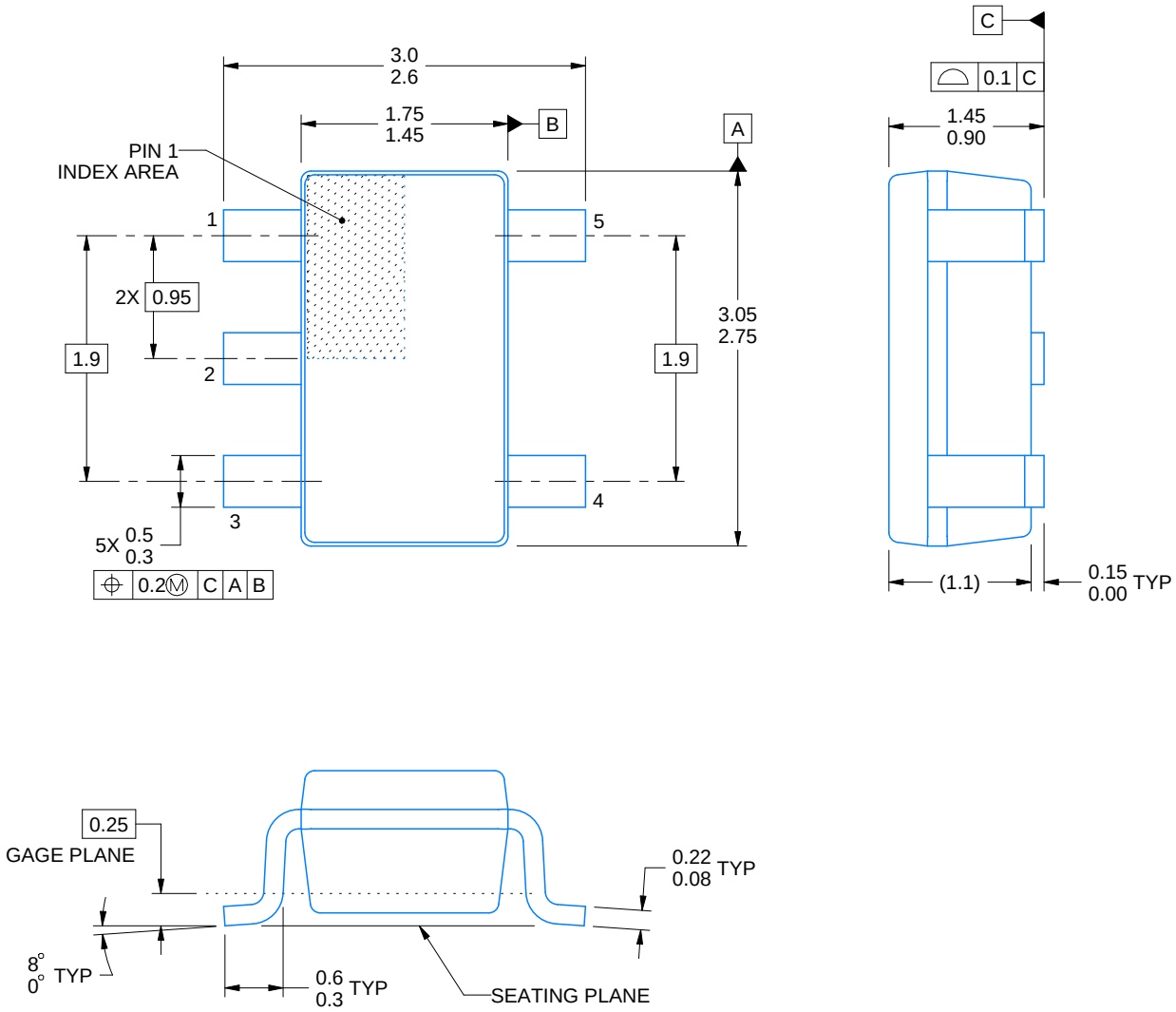
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

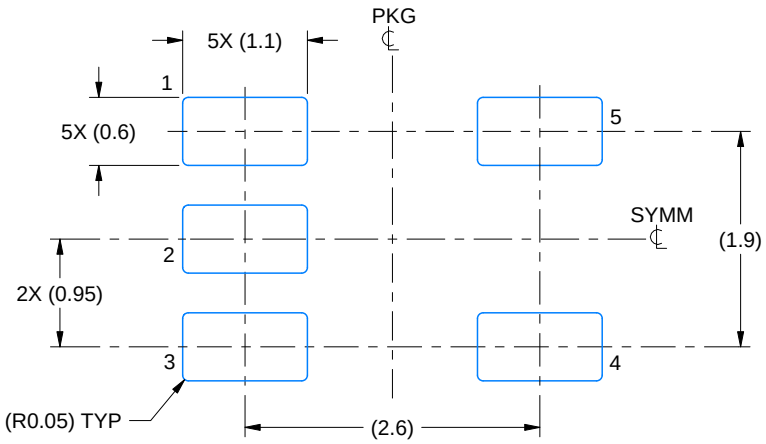
SMALL OUTLINE TRANSISTOR



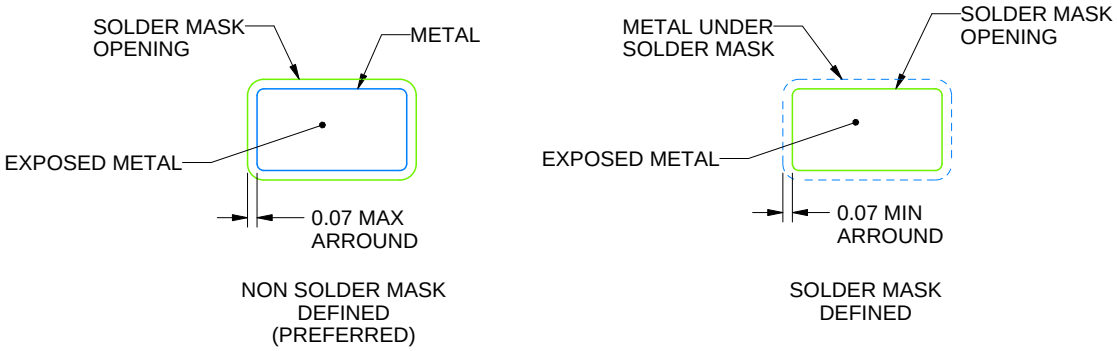
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

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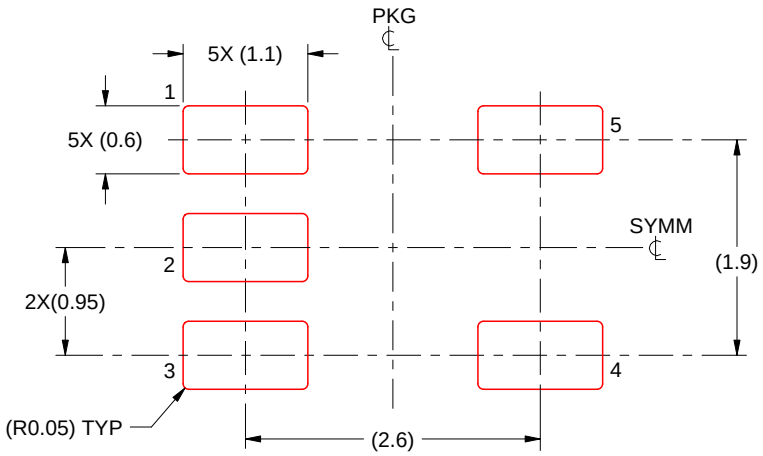
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

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8. Board assembly site may have different recommendations for stencil design.

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