Vishay Siliconix

N-Channel 8 V (D-S) MOSFET

DESCRIPTION

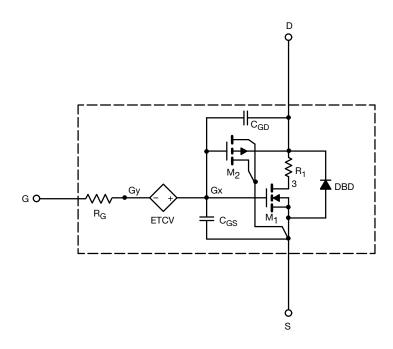
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- · Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.50	-	V
Drain-Source On-State Resistance a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 7.2 \text{ A}$	0.014	0.014	Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 6.7 \text{ A}$	0.016	0.016	
Forward Transconductance a	9 _{fs}	$V_{DS} = 4 \text{ V}, I_{D} = 7.2 \text{ A}$	61	75	S
Body Diode Voltage	V _{SD}	I _S = 5.8 A	0.70	0.82	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 4 V, V _{GS} = 0 V, f = 1 MHz	1080	1070	pF
Output Capacitance	C _{oss}		386	385	
Reverse Transfer Capacitance	C _{rss}		201	200	
Total Gate Charge	Qg	$V_{DS} = 4 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 7.2 \text{ A}$	10	10.5	nC
		V _{DS} = 4 V, V _{GS} = 2.5 V, I _D = 7.2 A	6	6	
Gate-Source Charge	Q_{gs}		1.6	1.6	
Gate-Drain Charge	Q_{gd}		1.1	1	

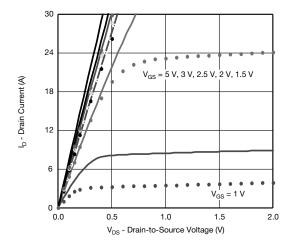
Notes

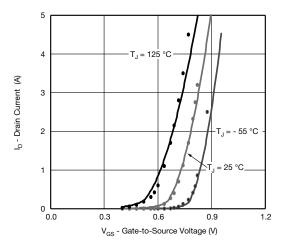
- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

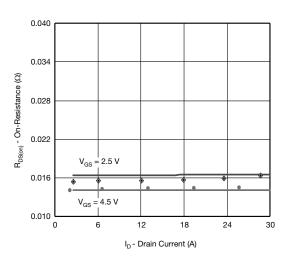
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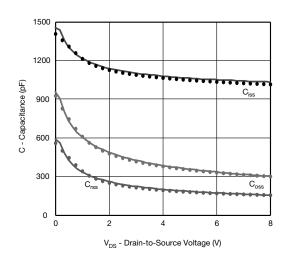
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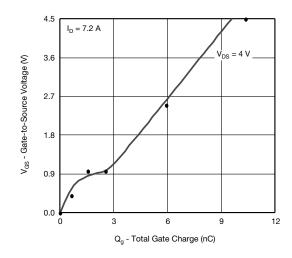
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25~^{\circ}C$, unless otherwise noted)

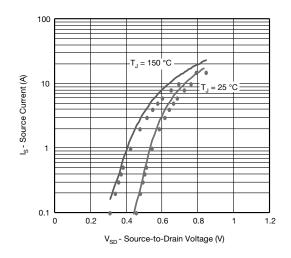












Note

Dots and squares represent measured data.
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