

FEATURES

Throughput

- 3 MSPS (wideband warp and warp mode)
- 2 MSPS (normal mode)
- 1.25 MSPS (impulse mode)

2.048 V internal reference

Differential input range: $\pm V_{REF}$ (V_{REF} up to 2.5 V)

INL: ± 2 LSB maximum, ± 1 LSB typical

16-bit resolution with no missing codes

SINAD: 89 dB typical @ 100 kHz

THD: -101 dB typical @ 100 kHz

No pipeline delay (SAR architecture)

Parallel (16- or 8-bit bus) and serial 5 V/3.3 V/2.5 V interface

SPI[®]-/QSPI[™]-/MICROWIRE[™]-/DSP-compatible

2.5 V single-supply operation

Power dissipation: 65 mW typical @ 3 MSPS

48-lead LQFP and 48-lead LFCSP packages

Speed upgrade of the [AD7677](#)

APPLICATIONS

- Medical instruments
- High speed data acquisition
- Digital signal processing
- Communications
- Instrumentation
- Spectrum analysis
- ATE

GENERAL DESCRIPTION

The AD7621 is a 16-bit, 3 MSPS, charge redistribution SAR, fully differential analog-to-digital converter (ADC) that operates from a single 2.5 V power supply. It contains a high speed 16-bit sampling ADC, an internal conversion clock, an internal reference (and buffer), error correction circuits, and both serial and parallel system interface ports. It features two very high sampling rate modes (wideband warp and warp), a fast mode (normal) for asynchronous rate applications, and a reduced power mode (impulse) for low power applications where the power is scaled with the throughput. Operation is specified from -40°C to $+85^{\circ}\text{C}$.

Rev. A

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FUNCTIONAL BLOCK DIAGRAM

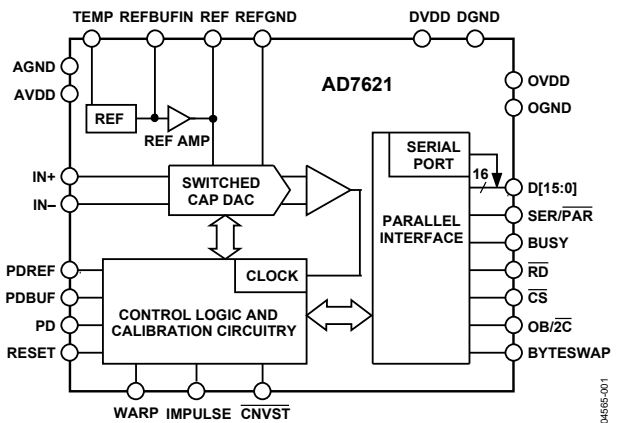


Figure 1.

Table 1. PuISAR Selection

| Type/kSPS | 100 to 250 | 500 to 570 | 800 to 1000 | >1000 |
|-------------------------------|---|--|--|------------------------|
| Pseudo Differential | AD7651 AD7660/61 | AD7650/52 AD7664/66 | AD7653 AD7667 | |
| True Bipolar | AD7663 | AD7665 | AD7671 | |
| True Differential | AD7675 | AD7676 | AD7677 | AD7621 |
| 18-Bit | AD7678 | AD7679 | AD7674 | AD7641 |
| Multichannel/ Simultaneous | | AD7654 | AD7655 | |

PRODUCT HIGHLIGHTS

1. Fast Throughput.
The AD7621 is a 3 MSPS, charge redistribution, 16-bit SAR ADC.
2. Superior Linearity.
The AD7621 has no missing 16-bit code.
3. Internal Reference.
The AD7621 has a 2.048 V internal reference with a typical drift of ± 7 ppm/ $^{\circ}\text{C}$.
4. Single-Supply Operation.
The AD7621 operates from a 2.5 V single supply and typically dissipates 65 mW. In impulse mode, its power dissipation decreases with the throughput.
5. Serial or Parallel Interface.
Versatile parallel (16- or 8-bit bus) or 2-wire serial interface arrangement compatible with 2.5 V, 3.3 V, or 5 V logic.

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REVISION HISTORY

8/2020—Rev. 0 to Rev. A

| | |
|---|------------|
| Changed CP-48-1 to CP-48-4..... | Throughout |
| Added Figure 4; Renumbered Sequentially | 8 |
| Updated Outline Dimensions..... | 28 |
| Changes to Ordering Guide..... | 29 |

5/2005—Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 2.5 V; OVDD = 2.3 V to 3.6 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|-------------------|-------|-------------------|------------------|
| RESOLUTION | | 16 | | | Bits |
| ANALOG INPUT | | | | | |
| Voltage Range | V _{IN+} – V _{IN-} | –V _{REF} | | V _{REF} | V |
| Operating Input Voltage | V _{IN+} , V _{IN-} to AGND | –0.1 | | AVDD ¹ | V |
| Analog Input CMRR | f _{IN} = 100 kHz | | 55 | | dB |
| Input Current | 3 MSPS throughput | | 25 | | μA |
| Input Impedance ² | | | | | |
| THROUGHPUT SPEED | | | | | |
| Complete Cycle | Wideband warp, warp modes | | | 333 | ns |
| Throughput Rate | Wideband warp, warp modes | 0.001 | | 3 | MSPS |
| Time Between Conversions | Wideband warp, warp modes | | | 1 | ms |
| Complete Cycle | Normal mode | | | 500 | ns |
| Throughput Rate | Normal mode | 0 | | 2 | MSPS |
| Complete Cycle | Impulse mode | | | 800 | ns |
| Throughput Rate | Impulse mode | 0 | | 1.25 | MSPS |
| DC ACCURACY | | | | | |
| All modes | | | | | |
| Integral Linearity Error ³ | V _{REF} = 2.048 V, PDREF = high | –2 | ±1 | +2 | LSB ⁴ |
| No Missing Codes | V _{REF} = 2.048 V, PDREF = high | 16 | | | Bits |
| Differential Linearity Error | V _{REF} = 2.048 V, PDREF = high | –1 | | +2 | LSB |
| Transition Noise | V _{REF} = 2.5 V | | 0.69 | | LSB |
| Transition Noise | V _{REF} = 2.048 V | | 0.82 | | LSB |
| Zero Error, T _{MIN} to T _{MAX} ⁵ | | –30 | | +30 | LSB |
| Zero Error Temperature Drift | | | ±1 | | ppm/°C |
| Gain Error, T _{MIN} to T _{MAX} ⁵ | | –0.38 | | +0.38 | % of FSR |
| Gain Error Temperature Drift | | | ±2 | | ppm/°C |
| Power Supply Sensitivity | AVDD = 2.5 V ± 5% | | ±3 | | LSB |
| AC ACCURACY | | | | | |
| Dynamic Range | f _{IN} = 20 kHz, V _{REF} = 2.5 V | | 90.5 | | dB ⁶ |
| Signal-to-Noise | f _{IN} = 20 kHz, V _{REF} = 2.5 V | 88 | 90 | | dB |
| | f _{IN} = 20 kHz, V _{REF} = 2.048 V | 86 | 88 | | dB |
| | f _{IN} = 100 kHz, V _{REF} = 2.5 V | | 89.2 | | dB |
| Spurious-Free Dynamic Range | f _{IN} = 20 kHz | | 103 | | dB |
| | f _{IN} = 100 kHz | | 101 | | dB |
| Total Harmonic Distortion | f _{IN} = 20 kHz | | –102 | | dB |
| | f _{IN} = 100 kHz | | –100 | | dB |
| Signal-to-(Noise + Distortion) | f _{IN} = 20 kHz, V _{REF} = 2.5 V | 87.5 | 89.8 | | dB |
| | f _{IN} = 20 kHz, V _{REF} = 2.048 V | | 87.5 | | dB |
| | f _{IN} = 100 kHz, V _{REF} = 2.5 V | | 89 | | dB |
| –3 dB Input Bandwidth | | | 50 | | MHz |
| SAMPLING DYNAMICS | | | | | |
| Aperture Delay | | | 1 | | ns |
| Aperture Jitter | | | 5 | | ps rms |
| Transient Response | Full-scale step | | | 50 | ns |
| INTERNAL REFERENCE | | | | | |
| Output Voltage | PDREF = PDBUF = low REF @ 25°C | 2.038 | 2.048 | 2.058 | V |
| Temperature Drift | –40°C to +85°C | | ±7 | | ppm/°C |
| Line Regulation | AVDD = 2.5 V ± 5% | | ±15 | | ppm/V |

AD7621

| Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|-------------------|-------|------|------------|
| Turn-On Settling Time | $C_{REF} = 10 \mu F$ | | 5 | | ms |
| REFBUFIN Output Voltage | REFBUFIN @ 25°C | | 1.2 | | V |
| REFBUFIN Output Resistance | | | 6.33 | | k Ω |
| EXTERNAL REFERENCE | PDREF = PDBUF = high | | | | |
| Voltage Range | REF | 1.8 | 2.048 | AVDD | V |
| Current Drain | 3 MSPS throughput | | 250 | | μA |
| REFERENCE BUFFER | PDREF = high, PDBUF = low | | | | |
| REFBUFIN Input Voltage Range | | 1.05 | 1.2 | 1.30 | V |
| TEMPERATURE PIN | | | | | |
| Voltage Output | @ 25°C | | 273 | | mV |
| Temperature Sensitivity | | | 0.85 | | mV/°C |
| Output Resistance | | | 4.7 | | k Ω |
| DIGITAL INPUTS | | | | | |
| Logic Levels | | | | | |
| V_{IL} | | -0.3 | | +0.6 | V |
| V_{IH} | | 1.7 | | 5.25 | V |
| I_{IL} | | -1 | | +1 | μA |
| I_{IH} | | -1 | | +1 | μA |
| DIGITAL OUTPUTS | | | | | |
| Data Format ⁷ | | | | | |
| Pipeline Delay ⁸ | | | | | |
| V_{OL} | $I_{SINK} = 500 \mu A$ | | | 0.4 | V |
| V_{OH} | $I_{SOURCE} = -500 \mu A$ | OVDD - 0.3 | | | V |
| POWER SUPPLIES | | | | | |
| Specified Performance | | | | | |
| AVDD | | 2.37 | 2.5 | 2.63 | V |
| DVDD | | 2.37 | 2.5 | 2.63 | V |
| OVDD | | 2.30 ⁹ | | 3.6 | V |
| Operating Current ¹⁰ | 3 MSPS throughput | | | | |
| AVDD ¹¹ | With internal reference | | 25.2 | | mA |
| DVDD | | | 3.6 | | mA |
| OVDD | | | 1 | | mA |
| Power Dissipation ¹¹ | | | | | |
| With Internal Reference ¹⁰ | 3 MSPS throughput | | 70 | 86 | mW |
| Without Internal Reference ¹⁰ | 3 MSPS throughput | | 65 | 80 | mW |
| With Internal Reference ¹² | 1.25 MSPS throughput | | 42 | 55 | mW |
| Without Internal Reference ¹² | 1.25 MSPS throughput | | 37 | 50 | mW |
| In Power-Down Mode ¹³ | PD = high | | 600 | | μW |
| TEMPERATURE RANGE ¹⁴ | | | | | |
| Specified Performance | T_{MIN} to T_{MAX} | -40 | | +85 | °C |

¹ When using an external reference. With the internal reference, the input range is -0.1 V to V_{REF} .

² See the Analog Inputs section.

³ Linearity is tested using endpoints, not best fit. Tested with an external reference at 2.048 V.

⁴ LSB means least significant bit. With the ± 2.048 V input range, 1 LSB is 62.5 μV .

⁵ See the Voltage Reference Input section. These specifications do not include the error contribution from the external reference.

⁶ All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.

⁷ Parallel or serial 16-bit.

⁸ Conversion results are available immediately after completed conversion.

⁹ See the Absolute Maximum Ratings section.

¹⁰ In warp mode. Tested in parallel reading mode.

¹¹ With internal reference, PDREF and PDBUF are low; without internal reference, PDREF and PDBUF are high.

¹² In impulse mode. Tested in parallel reading mode.

¹³ With all digital inputs forced to OVDD.

¹⁴ Consult factory for extended temperature range.

TIMING SPECIFICATIONS

AVDD = DVDD = 2.5 V; OVDD = 2.3 V to 3.6 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------------|-------------|-------------|-----------------|------|
| CONVERSION AND RESET (Refer to Figure 31 and Figure 32) | | | | | |
| Convert Pulse Width | t ₁ | 15 | | 70 ¹ | ns |
| Time Between Conversions (Warp ² Mode/Normal Mode/Impulse Mode) ³ | t ₂ | 333/500/800 | | | ns |
| $\overline{\text{CNVST}}$ Low to BUSY High Delay | t ₃ | | | 23 | ns |
| BUSY High All Modes (Except Master Serial Read After Convert) | t ₄ | | | 283/430/560 | ns |
| Aperture Delay | t ₅ | | 1 | | ns |
| End of Conversion to BUSY Low Delay | t ₆ | 10 | | | ns |
| Conversion Time (Warp Mode/Normal Mode/Impulse Mode) | t ₇ | | | 283/430/560 | ns |
| Acquisition Time (Warp Mode/Normal Mode/Impulse Mode) | t ₈ | 50/70/50 | | | ns |
| RESET Pulse Width | t ₉ | 15 | | | ns |
| RESET Low to BUSY High Delay ⁴ | t ₃₈ | | 10 | | ns |
| BUSY High Time from RESET Low ⁴ | t ₃₉ | | 600 | | ns |
| PARALLEL INTERFACE MODES (Refer to Figure 34 and Figure 36) | | | | | |
| $\overline{\text{CNVST}}$ Low to DATA Valid Delay (Warp Mode/Normal Mode/Impulse Mode) | t ₁₀ | | | 283/430/560 | ns |
| DATA Valid to BUSY Low Delay | t ₁₁ | 2 | | | ns |
| Bus Access Request to DATA Valid | t ₁₂ | | | 20 | ns |
| Bus Relinquish Time | t ₁₃ | 2 | | 15 | ns |
| MASTER SERIAL INTERFACE MODES⁵ (Refer to Figure 38 and Figure 39) | | | | | |
| $\overline{\text{CS}}$ Low to SYNC Valid Delay | t ₁₄ | | | 10 | ns |
| $\overline{\text{CS}}$ Low to Internal SCLK Valid Delay ⁵ | t ₁₅ | | | 10 | ns |
| $\overline{\text{CS}}$ Low to SDOUT Delay | t ₁₆ | | | 10 | ns |
| $\overline{\text{CNVST}}$ Low to SYNC Delay (Warp Mode/Normal Mode/Impulse Mode) | t ₁₇ | | 12/137/263 | | ns |
| SYNC Asserted to SCLK First Edge Delay | t ₁₈ | 0.5 | | | ns |
| Internal SCLK Period ⁶ | t ₁₉ | 8 | | 12 | ns |
| Internal SCLK High ⁶ | t ₂₀ | 2 | | | ns |
| Internal SCLK Low ⁶ | t ₂₁ | 3 | | | ns |
| SDOUT Valid Setup Time ⁶ | t ₂₂ | 1 | | | ns |
| SDOUT Valid Hold Time ⁶ | t ₂₃ | 0 | | | ns |
| SCLK Last Edge to SYNC Delay ⁶ | t ₂₄ | 0 | | | ns |
| $\overline{\text{CS}}$ High to SYNC HI-Z | t ₂₅ | | | 10 | ns |
| $\overline{\text{CS}}$ High to Internal SCLK HI-Z | t ₂₆ | | | 10 | ns |
| $\overline{\text{CS}}$ High to SDOUT HI-Z | t ₂₇ | | | 10 | ns |
| BUSY High in Master Serial Read after Convert ⁶ | t ₂₈ | | See Table 4 | | |
| $\overline{\text{CNVST}}$ Low to SYNC Asserted Delay (All Modes) | t ₂₉ | | 275/400/500 | | ns |
| SYNC Deasserted to BUSY Low Delay | t ₃₀ | | 13 | | ns |

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-----------------|------|-----|-----|------|
| SLAVE SERIAL INTERFACE MODES ⁵ (Refer to Figure 41 and Figure 42) | | | | | |
| External SCLK Setup Time | t ₃₁ | 5 | | | ns |
| External SCLK Active Edge to SDOOUT Delay | t ₃₂ | 1 | | 8 | ns |
| SDIN Setup Time | t ₃₃ | 5 | | | ns |
| SDIN Hold Time | t ₃₄ | 5 | | | ns |
| External SCLK Period | t ₃₅ | 12.5 | | | ns |
| External SCLK High | t ₃₆ | 5 | | | ns |
| External SCLK Low | t ₃₇ | 5 | | | ns |

¹ See the Conversion Control section.

² All timings for wideband warp mode are the same as warp mode.

³ In warp mode only, the time between conversions is 1 ms; otherwise, there is no required maximum time.

⁴ See the Digital Interface, and RESET sections.

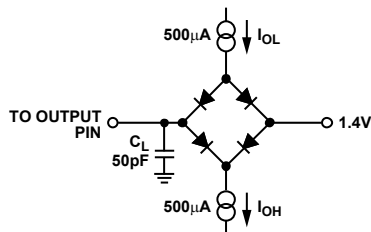
⁵ In serial interface modes, the SYNC, SCLK, and SDOOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.

⁶ In serial master read during convert mode. See Table 4 for serial master read after convert mode timing specifications.

SERIAL CLOCK TIMING SPECIFICATIONS

Table 4. Serial Clock Timings in Master Read After Convert Mode

| DIVSCLK[1] DIVSCLK[0] | Symbol | 0 0 | 0 1 | 1 0 | 1 1 | Unit |
|---|-----------------|--------|--------|--------|--------|------|
| SYNC to SCLK First Edge Delay Minimum | t ₁₈ | 0.5 | 3 | 3 | 3 | ns |
| Internal SCLK Period Minimum | t ₁₉ | 8 | 16 | 32 | 64 | ns |
| Internal SCLK Period Maximum | t ₁₉ | 12 | 25 | 50 | 100 | ns |
| Internal SCLK High Minimum | t ₂₀ | 2 | 6 | 15 | 31 | ns |
| Internal SCLK Low Minimum | t ₂₁ | 3 | 7 | 16 | 32 | ns |
| SDOOUT Valid Setup Time Minimum | t ₂₂ | 1 | 5 | 5 | 5 | ns |
| SDOOUT Valid Hold Time Minimum | t ₂₃ | 0 | 0.5 | 10 | 28 | ns |
| SCLK Last Edge to SYNC Delay Minimum | t ₂₄ | 0 | 0.5 | 9 | 26 | ns |
| BUSY High Width Maximum (Wideband and Warp Modes) | t ₂₈ | 0.500 | 0.720 | 1.160 | 2.040 | μs |
| BUSY High Width Maximum (Normal Mode) | t ₂₈ | 0.650 | 0.870 | 1.310 | 2.190 | μs |
| BUSY High Width Maximum (Impulse Mode) | t ₂₈ | 0.780 | 1.000 | 1.440 | 2.320 | μs |



NOTE
IN SERIAL INTERFACE MODES, THE SYNC, SCLK AND SDOOUT ARE DEFINED WITH A MAXIMUM LOAD. C_L OF 10 pF; OTHERWISE, THE LOAD IS 60 pF MAXIMUM.

Figure 2. Load Circuit for Digital Interface Timing, SDOOUT, SYNC, and SCLK Outputs, C_L = 10 pF

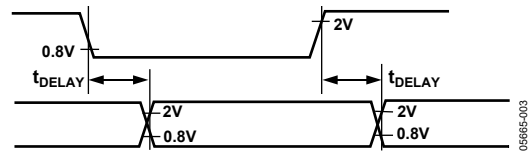


Figure 3. Voltage Reference Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|--|---------------------------------|
| Analog Inputs/Outputs IN+ ¹ , IN–, REF, REFBUFIN, TEMP, INGND, REFGND to AGND | AVDD + 0.3 V to AGND – 0.3 V |
| Ground Voltage Differences AGND, DGND, OGND | ±0.3 V |
| Supply Voltages | |
| AVDD, DVDD | –0.3 V to +2.7 V |
| OVDD | –0.3 V to +3.8 V |
| AVDD to DVDD | ±2.8 V |
| AVDD to OVDD | +2.8 V to –3.8 V |
| OVDD to DVDD ² | ≤ +0.3 V if DVDD < 2.3 V |
| Digital Inputs | –0.3 V to +5.5 V |
| PDREF, PDBUF ³ | ±20 mA |
| Internal Power Dissipation ⁴ | 700 mW |
| Internal Power Dissipation ⁵ | 2.5 W |
| Junction Temperature | 125°C |
| Storage Temperature Range | –65°C to +125°C |

¹ See the Analog Inputs section.² See the Power Supply section.³ See the Voltage Reference Input section.⁴ Specification is for the device in free air: 48-Lead LQFP; $\theta_{JA} = 91^\circ\text{C}/\text{W}$,
 $\theta_{JC} = 30^\circ\text{C}/\text{W}$.⁵ Specification is for the device in free air: 48-Lead LFCSP; $\theta_{JA} = 26^\circ\text{C}/\text{W}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

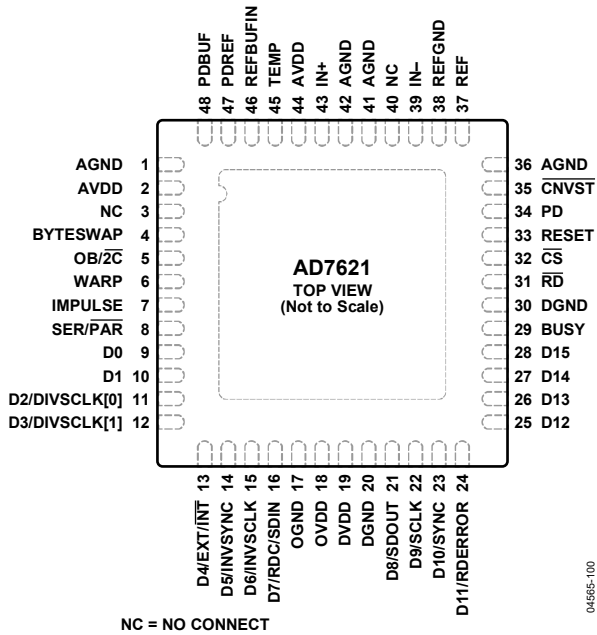


ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

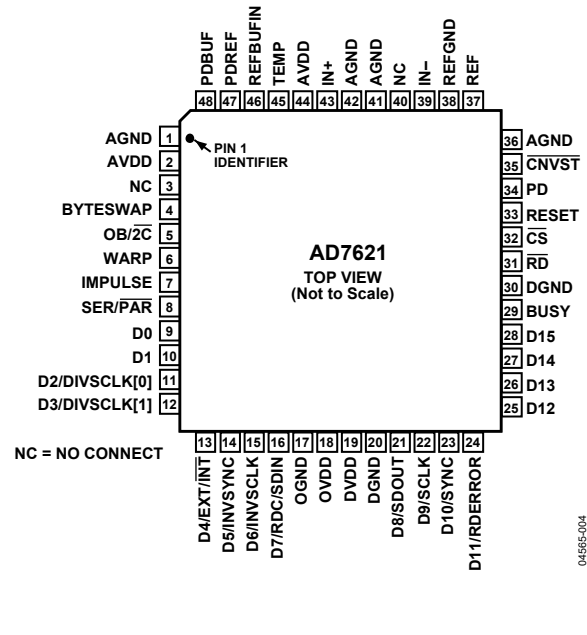
AD7621

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NC = NO CONNECT

Figure 4. 48-Lead LFCSP Pin Configuration



NC = NO CONNECT

Figure 5. 48-Lead LQFP Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|-----------|------------------------------|-------------------|--|
| 1, 41, 42 | AGND | P | Analog Power Ground Pin. |
| 2, 44 | AVDD | P | Input Analog Power Pins. Nominally 2.5 V. |
| 3, 40 | NC | | No Connect. |
| 4 | BYTESWAP | DI | Parallel Mode Selection (8-Bit/16-Bit). When high, the LSB is output on D[15:8] and the MSB is output on D[7:0]; when low, the LSB is output on D[7:0] and the MSB is output on D[15:8]. |
| 5 | OB/2C | DI | Straight Binary/Binary Twos Complement Output. When high, the digital output is straight binary; when low, the MSB is inverted resulting in a twos complement output from its internal shift register. |
| 6 | WARP | DI | Conversion Mode Selection. When WARP = high and IMPULSE = high, this selects wideband mode with slightly improved linearity and THD. When WARP = high and IMPULSE = low, this selects warp mode. In either mode, these are the fastest modes; maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When WARP = low and IMPULSE = low, this input selects normal mode where full accuracy is maintained independent of the minimum conversion rate. |
| 7 | IMPULSE | DI | Conversion Mode Selection. When IMPULSE = high and WARP = low, this input selects impulse mode, a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate. |
| 8 | SER/PAR | DI | Serial/Parallel Selection Input. When high, the serial interface is selected and some bits of the data bus are used as a serial port; the remaining data bits are high impedance outputs. When SER/PAR = low, the parallel port is selected. |
| 9, 10 | D[0:1] | DO | Bit 0 and Bit 1 of the Parallel Port Data Output Bus. |
| 11, 12 | D[2:3] or DIVSCLK[0:1] | DI/O | When SER/PAR = low, these outputs are used as Bit 2 and Bit 3 of the parallel port data output bus. When SER/PAR = high, serial clock division selection. When using serial master read after convert mode (EXT/INT = low, RDC/SDIN = low) these inputs can be used to slow down the internally generated serial clock that clocks the data output. In other serial modes, these pins are high impedance outputs. |

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|---------------------------------------|-------------------|---|
| 13 | D4 or EXT/ $\overline{\text{INT}}$ | DI/O | When SER/ $\overline{\text{PAR}}$ = low, this output is used as Bit 4 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ = high, serial clock source select. This input is used to select the internally generated (master) or external (slave) serial data clock. When EXT/ $\overline{\text{INT}}$ = low: master mode. The internal serial clock is selected on SCLK output. When EXT/ $\overline{\text{INT}}$ = high: slave mode. The output data is synchronized to an external clock signal, gated by $\overline{\text{CS}}$, connected to the SCLK input. |
| 14 | D5 or INVSYNC | DI/O | When SER/ $\overline{\text{PAR}}$ = low this output is used as Bit 5 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ = high, invert sync select. In serial master mode (EXT/ $\overline{\text{INT}}$ = low), this input is used to select the active state of the SYNC signal. When INVSYNC = low, SYNC is active high. When INVSYNC = high, SYNC is active low. |
| 15 | D6 or INVSCCLK | DI/O | When SER/ $\overline{\text{PAR}}$ = low this output is used as Bit 6 of the parallel port data output bus. Invert SCLK Select. In all serial modes, this input is used to invert the SCLK signal. |
| 16 | D7 or RDC or SDIN | DI/O | Bit 7 of the Parallel Port Data Output Bus. When SER/ $\overline{\text{PAR}}$ = high, read during convert. When using Serial Master mode (EXT/ $\overline{\text{INT}}$ = low), RDC is used to select the read mode. When RDC = high, the previous conversion result is read during current conversion and the period of SCLK changes (see the Master Serial Interface section). When RDC = low (read after convert), the current result is read after conversion. Serial Data In. When using serial slave mode, (EXT/ $\overline{\text{INT}}$ = high), SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 16 SCLK periods after the initiation of the read sequence. |
| 17 | OGND | P | Input/Output Interface Digital Power Ground. |
| 18 | OVDD | P | Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (2.5 V or 3 V). |
| 19 | DVDD | P | Digital Power. Nominally at 2.5 V. |
| 20 | DGND | P | Digital Power Ground. |
| 21 | D8 or SDOUT | DO | When SER/ $\overline{\text{PAR}}$ = low this output is used as Bit 8 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ = high, serial data output. In serial mode, this pin is used as the serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7621 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/ $\overline{2C}$. In master mode (EXT/ $\overline{\text{INT}}$ = low), SDOUT is valid on both edges of SCLK. In slave mode (EXT/ $\overline{\text{INT}}$ = high): When INVSCCLK = low, SDOUT is updated on SCLK rising edge and valid on the next falling edge. When INVSCCLK = high, SDOUT is updated on SCLK falling edge and valid on the next rising edge. |
| 22 | D9 or SCLK | DI/O | Parallel Port Data Output Bus Bit 9. When SER/ $\overline{\text{PAR}}$ = low, this output is used as Bit 9 of the parallel port data output bus. Serial Clock. When SER/ $\overline{\text{PAR}}$ = high, serial clock. In all serial modes, this pin is used as the serial data clock input or output, dependent upon the logic state of the EXT/ $\overline{\text{INT}}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCCLK pin. |
| 23 | D10 or SYNC | DO | When SER/ $\overline{\text{PAR}}$ = low, this output is used as Bit 10 of the parallel port data output bus. When SER/ $\overline{\text{PAR}}$ = high, frame synchronization. In serial master mode (EXT/ $\overline{\text{INT}}$ = low), this output is used as a digital output frame synchronization for use with the internal data clock. When a read sequence is initiated and INVSYNC = low, SYNC is driven high and remains high while SDOUT output is valid. When a read sequence is initiated and INVSYNC = high, SYNC is driven low and remains low while SDOUT output is valid. |
| 24 | D11 or RDERROR | DO | Parallel Port Data Output Bus Bit 11. When SER/ $\overline{\text{PAR}}$ = low, this output is used as Bit 11 of the parallel port data output bus. Read Error. When SER/ $\overline{\text{PAR}}$ = high, read error. In serial slave mode (EXT/ $\overline{\text{INT}}$ = high), this output is used as an incomplete read error flag. If a data read is started and not completed when the current conversion is complete, the current data is lost and RDERROR is pulsed high. |

AD7621

| Pin No. | Mnemonic | Type ¹ | Description |
|----------|--------------------|-------------------|--|
| 25 to 28 | D[12:15] | DO | Bit 12 to Bit 15 of the Parallel Port Data Output Bus. |
| 29 | BUSY | DO | Busy Output. Transitions high when a conversion is started, and remains high until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data ready clock signal. |
| 30 | DGND | P | Digital Power Ground. |
| 31 | \overline{RD} | DI | Read Data. When \overline{CS} and \overline{RD} are both low, the interface parallel or serial output bus is enabled. |
| 32 | \overline{CS} | DI | Chip Select. When \overline{CS} and \overline{RD} are both low, the interface parallel or serial output bus is enabled. \overline{CS} is also used to gate the external clock in slave serial mode. |
| 33 | RESET | DI | Reset Input. When high, reset the AD7621. Current conversion if any is aborted. Falling edge of RESET enables the calibration mode indicated by pulsing BUSY high. Refer to the Digital Interface section. If not used, this pin can be tied to DGND. |
| 34 | PD | DI | Power-Down Input. When high, power down the ADC. Power consumption is reduced and conversions are inhibited after the current one is completed. |
| 35 | \overline{CNVST} | DI | Conversion Start. A falling edge on \overline{CNVST} puts the internal sample-and-hold into the hold state and initiates a conversion. |
| 36 | AGND | P | Analog Power Ground Pin. |
| 37 | REF | AI/O | Reference Output/Input. When PDREF/PDBUF = low, the internal reference and buffer are enabled producing 2.048 V on this pin. When PDREF/PDBUF = high, the internal reference and buffer are disabled allowing an externally supplied voltage reference up to AVDD volts. Decoupling is required with or without the internal reference and buffer. Refer to the Voltage Reference Input section. |
| 38 | REFGND | AI | Reference Input Analog Ground. |
| 39 | IN- | AI | Differential Negative Analog Input. |
| 43 | IN+ | AI | Differential Positive Analog Input. |
| 45 | TEMP | AO | Temperature Sensor Analog Output. |
| 46 | REFBUFIN | AI/O | Internal Reference Output/Reference Buffer Input. When PDREF/PDBUF = low, the internal reference and buffer are enabled producing the 1.2 V (typical) bandgap output on this pin, which needs external decoupling. The internal fixed gain reference buffer uses this to produce 2.048V on the REF pin. When using an external reference with the internal reference buffer (PDBUF = low, PDREF = high), applying 1.2 V on this pin produces 2.048 V on the REF pin. Refer to the Voltage Reference Input section. |
| 47 | PDREF | DI | Internal Reference Power-Down Input. When low, the internal reference is enabled. When high, the internal reference is powered down and an external reference must be used. |
| 48 | PDBUF | DI | Internal Reference Buffer Power-Down Input. When low, the buffer is enabled (must be low when using internal reference). When high, the buffer is powered-down. |

¹ AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DI/O = bidirectional digital; DO = digital output; P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from negative full-scale through positive full-scale. The point used as negative full-scale occurs ½ LSB before the first code transition. Positive full-scale is defined as a level 1½ LSBs beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Gain Error

The first transition (from 000...00 to 000...01) should occur for an analog voltage ½ LSB above the nominal negative full-scale (–2.0479688 V for the ±2.048 V range). The last transition (from 111...10 to 111...11) should occur for an analog voltage 1½ LSBs below the nominal full-scale (2.0479531 V for the ±2.048 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Zero Error

The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Dynamic Range

Dynamic range is the ratio of the rms value of the full-scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

Aperture Delay

Aperture delay is a measure of the acquisition performance measured from the falling edge of the CNVST input to when the input signal is held for a conversion.

Transient Response

The time required for the AD7621 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN} , $T(25^\circ\text{C})$, and T_{MAX} . It is expressed in ppm/°C as

$$TCV_{REF}(\text{ppm}/^\circ\text{C}) = \frac{V_{REF}(\text{Max}) - V_{REF}(\text{Min})}{V_{REF}(25^\circ\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

$V_{REF}(\text{Max})$ = maximum V_{REF} at T_{MIN} , $T(25^\circ\text{C})$, or T_{MAX}

$V_{REF}(\text{Min})$ = minimum V_{REF} at T_{MIN} , $T(25^\circ\text{C})$, or T_{MAX}

$V_{REF}(25^\circ\text{C})$ = V_{REF} at 25°C

T_{MAX} = +85°C

T_{MIN} = –40°C

TYPICAL PERFORMANCE CHARACTERISTICS

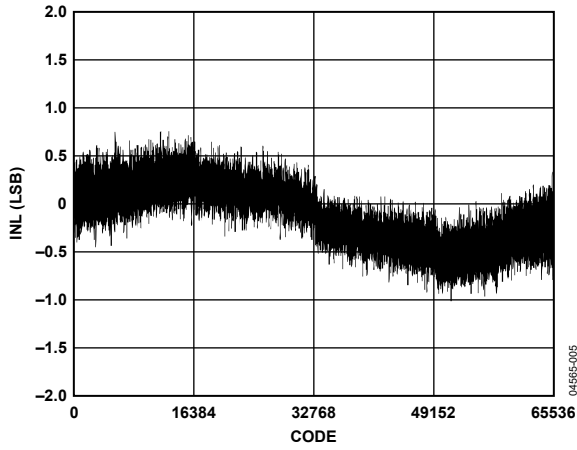


Figure 6. Integral Nonlinearity vs. Code

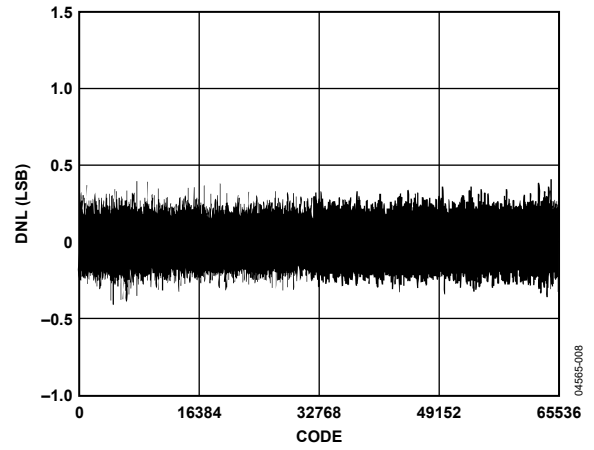


Figure 9. Differential Nonlinearity vs. Code

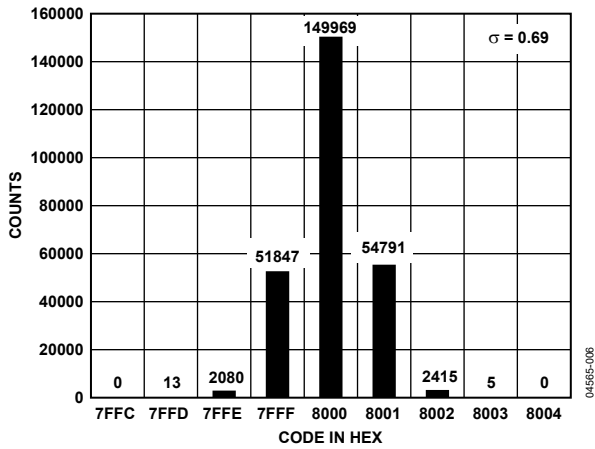


Figure 7. Histogram of 261,120 Conversions of a DC Input at the Code Center (External Reference)

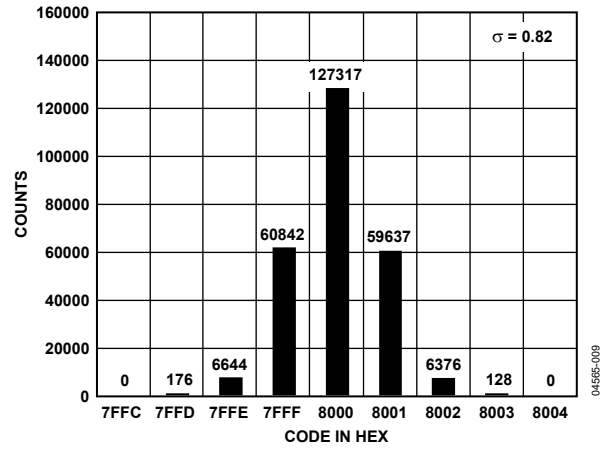


Figure 10. Histogram of 261,120 Conversions of a DC Input at the Code Center (Internal Reference)

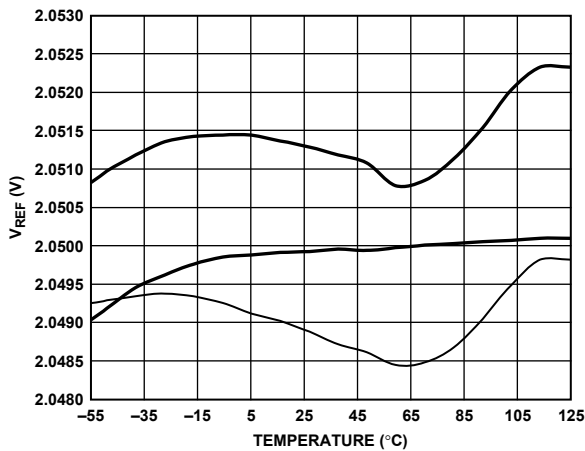


Figure 8. Typical Reference Voltage Output vs. Temperature (3 Units)

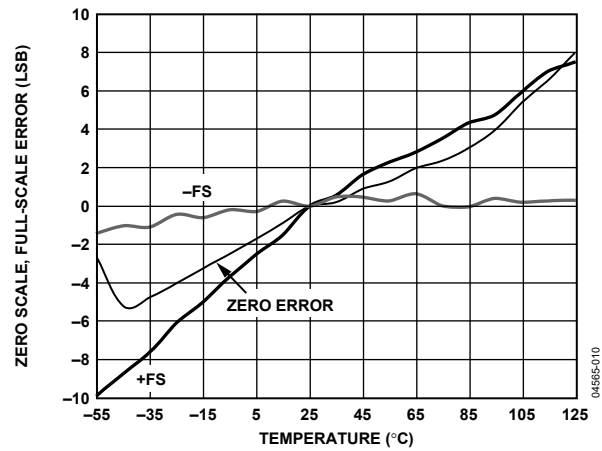


Figure 11. Zero Error, Positive and Negative Full Scale vs. Temperature

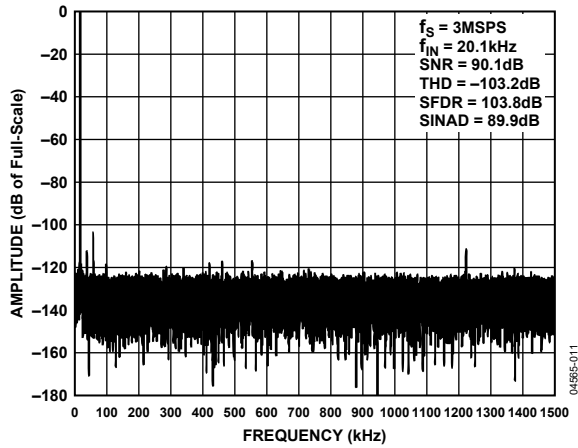


Figure 12. FFT 20 kHz

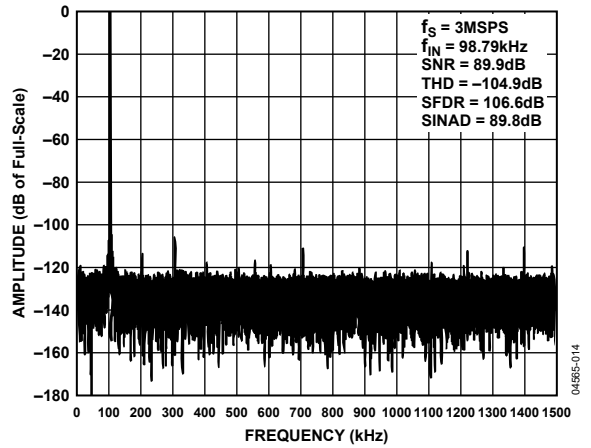


Figure 15. FFT 100 kHz

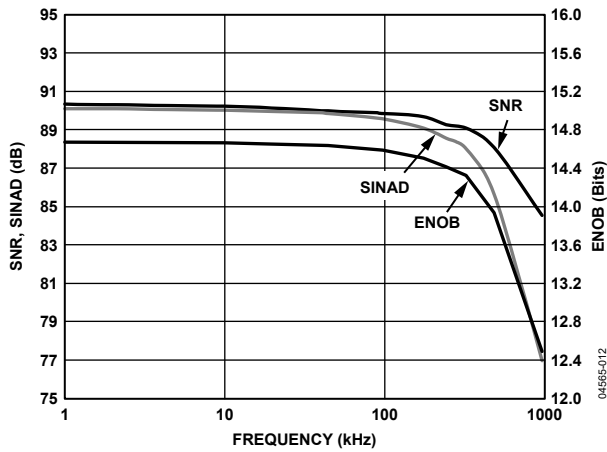


Figure 13. SNR, SINAD and ENOB vs. Frequency

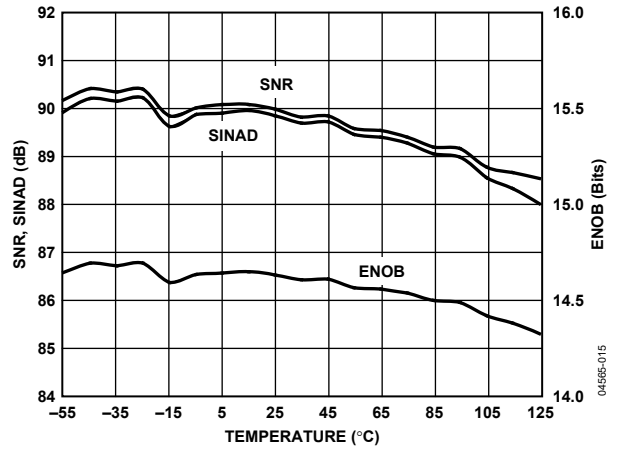


Figure 16. SNR, SINAD, and ENOB vs. Temperature

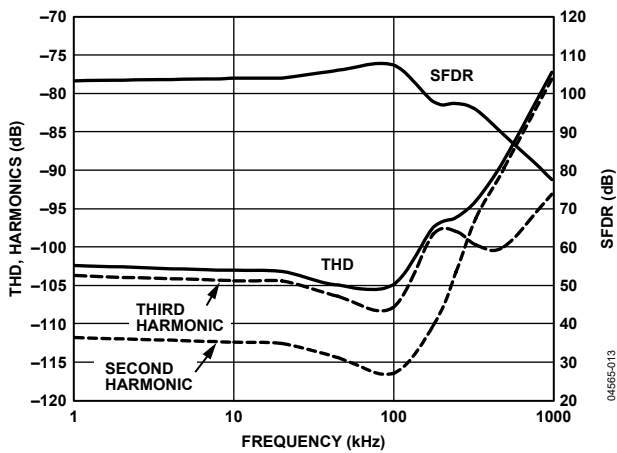


Figure 14. THD, Harmonics, and SFDR vs. Frequency

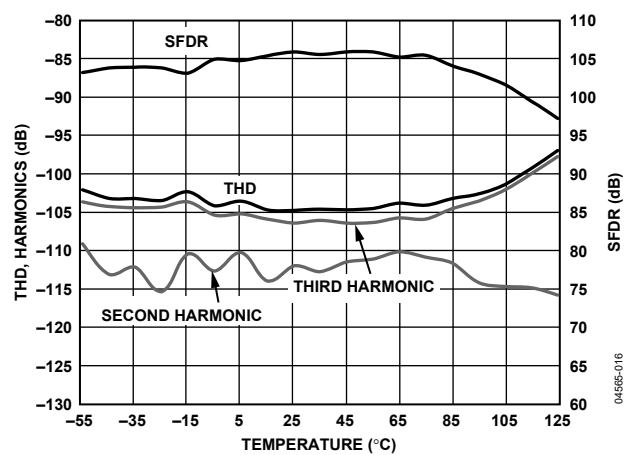


Figure 17. THD, Harmonics, and SFDR vs. Temperature

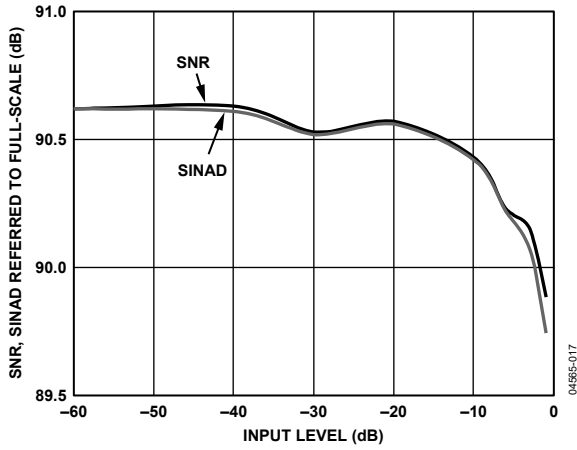


Figure 18. SNR and SINAD vs. Input Level (Referred to Full Scale)

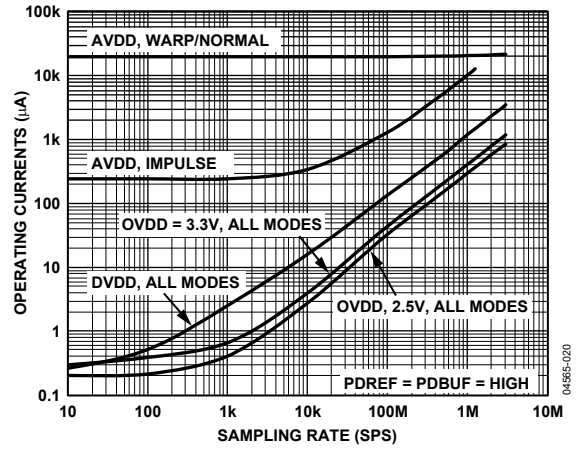


Figure 20. Operating Current vs. Sample Rate

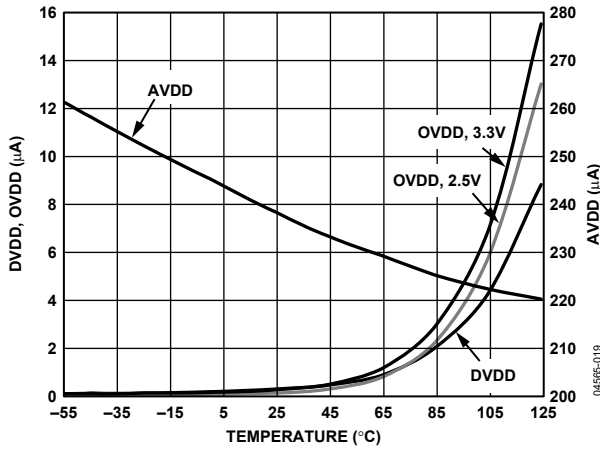


Figure 19. Power-Down Operating Currents vs. Temperature

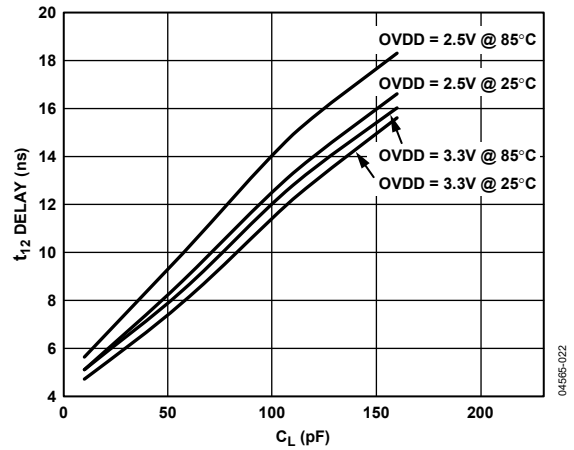


Figure 21. Typical Delay vs. Load Capacitance C_L

THEORY OF OPERATION

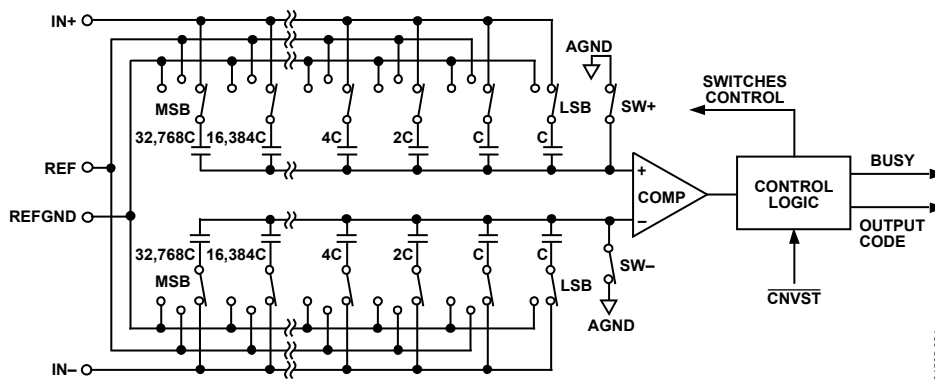


Figure 22. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7621 is a very fast, low power, single-supply, precise, 16-bit analog-to-digital converter (ADC) using successive approximation architecture. The AD7621 features different modes to optimize performances according to the applications. In warp mode, the AD7621 is capable of converting 3,000,000 samples per second (3 MSPS).

The AD7621 provides the user with an on-chip track-and-hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7621 can be operated from a single 2.5 V supply and be interfaced to either 5 V, 3.3 V, or 2.5 V digital logic. It is housed in 48-lead LQFP or tiny LFCSP packages that combine space savings with flexibility, allowing the AD7621 to be configured as either a serial or parallel interface. The AD7621 is pin-to-pin-compatible with, and a speed upgrade of, the [AD7677](#).

CONVERTER OPERATION

The AD7621 is a successive approximation analog-to-digital converter (ADC) based on a charge redistribution DAC. Figure 22 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW-. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN- inputs. A conversion phase is initiated once the acquisition phase is complete and the CNVST input goes low. When the conversion phase begins, SW+ and SW- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFVND input. Therefore, the differential voltage between the inputs (IN+ and IN-) captured at the end of the acquisition

phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFVND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ through $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

MODES OF OPERATION

The AD7621 features four modes of operation: wideband warp, warp, normal, and impulse. Each of these modes is more suitable to specific applications.

Wideband warp (WARP = high, IMPULSE = high) and warp (WARP = high, IMPULSE = low) modes allow the fastest conversion rate up to 3 MSPS. However, in these modes, the full specified accuracy is guaranteed only when the time between conversions does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms (after power up), the first conversion result should be ignored. These modes make the AD7621 ideal for applications where both high accuracy and fast sample rate are required. Wideband warp mode offers slightly improved linearity and THD over warp mode.

Normal mode (WARP = low, IMPULSE = low) is the fastest mode (2 MSPS) without any limitation on time between conversions. This mode makes the AD7621 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

Impulse mode (WARP = low, IMPULSE = high), the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 1.25 MSPS. In this mode, the ADC powers down circuits after conversion making the AD7621 ideal for battery-powered applications.

TRANSFER FUNCTIONS

Using the $\overline{OB/2C}$ digital input, the AD7621 offers two output codings: straight binary and twos complement. The LSB size with $V_{REF} = 2.048\text{ V}$ is $2 \times V_{REF}/65536$, which is $62.5\ \mu\text{V}$. Refer to Figure 23 and Table 7 for the ideal transfer characteristic.

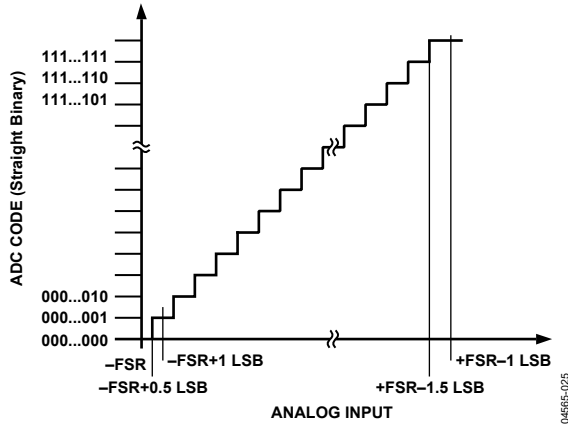


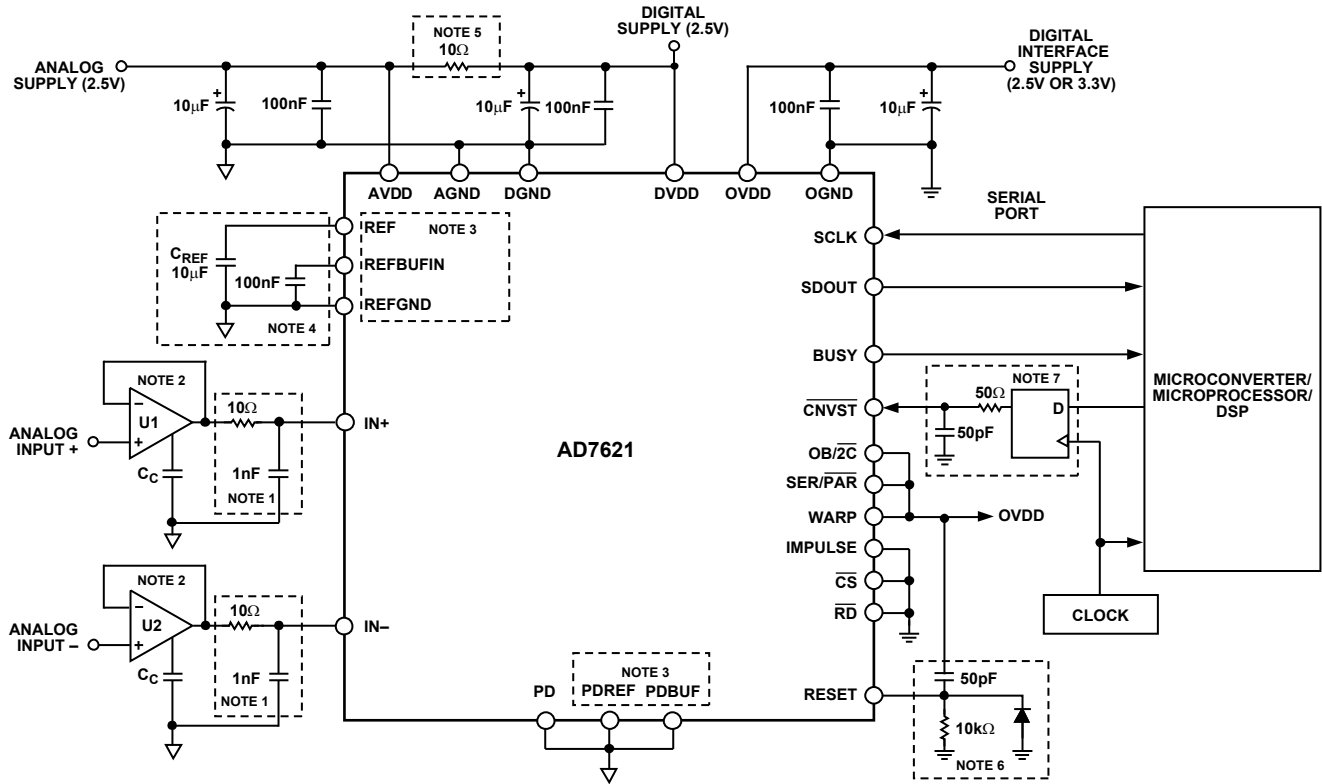
Figure 23. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

| Description | Analog Input $V_{REF} = 2.048\text{ V}$ | Digital Output Code | |
|------------------|--|---------------------|---------------------|
| | | Straight Binary | Twos Complement |
| FSR - 1 LSB | +2.047938 V | 0xFFFF ¹ | 0x7FFF ⁶ |
| FSR - 2 LSB | +2.047875 V | 0xFFFE | 0x7FFE |
| Midscale + 1 LSB | +62.5 μV | 0x8001 | 0x0001 |
| Midscale | 0 V | 0x8000 | 0x0000 |
| Midscale - 1 LSB | -62.5 μV | 0x7FFF | 0xFFFF |
| -FSR + 1 LSB | -2.047938 V | 0x0001 | 0x8001 |
| -FSR | -2.048 V | 0x0000 ² | 0x8000 ⁷ |

¹ This is also the code for overrange analog input ($V_{IN+} - V_{IN-}$ above $V_{REF} - V_{REFGND}$).

² This is also the code for underrange analog input ($V_{IN+} - V_{IN-}$ below $-V_{REF} + V_{REFGND}$).



1. SEE ANALOG INPUT SECTION.
2. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
3. THE CONFIGURATION SHOWN IS USING THE INTERNAL REFERENCE. SEE VOLTAGE REFERENCE INPUT SECTION.
4. A $10\ \mu\text{F}$ CERAMIC CAPACITOR (X5R, 1206 SIZE) IS RECOMMENDED (e.g., PANASONIC ECJ3YB0J106M).
SEE VOLTAGE REFERENCE INPUT SECTION.
5. OPTION, SEE POWER SUPPLY SECTION.
6. OPTION, SEE POWER UP SECTION.
7. OPTIONAL LOW JITTER CNVST, SEE CONVERSION CONTROL SECTION.

Figure 24. Typical Connection Diagram

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TYPICAL CONNECTION DIAGRAM

Figure 24 shows a typical connection diagram for the AD7621. Different circuitry from that shown in this diagram are optional and are discussed below.

ANALOG INPUTS

Figure 25 shows an equivalent circuit of the input structure of the AD7621.

The two diodes, D_1 and D_2 , provide ESD protection for the analog inputs, $IN+$ and $IN-$. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V as this causes the diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 100 mA maximum. For instance, these conditions could eventually occur when the input buffer's $U1$ or $U2$ supplies are different from $AVDD$. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

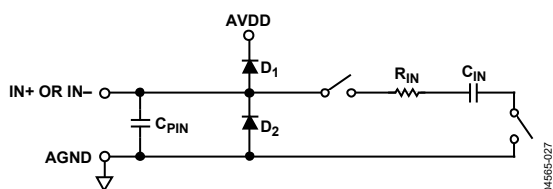


Figure 25. AD7621 Simplified Analog Input.

The analog input of AD7621 is a true differential structure. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 26, representing the typical CMRR over frequency with internal and external references.

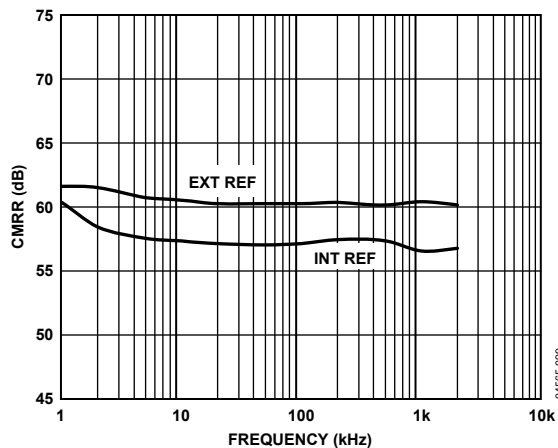


Figure 26. Analog Input CMRR vs. Frequency

During the acquisition phase for ac signals, the impedance of the analog inputs, $IN+$ and $IN-$, can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN} . C_{PIN} is primarily the pin capacitance. R_{IN} is typically 350 Ω and is a lumped component

comprised of some serial resistors and the on resistance of the switches. C_{IN} is typically 12 pF and is mainly the ADC sampling capacitor. During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN} , R_{IN} and C_{IN} make a one-pole, low-pass filter that has a typical -3 dB cutoff frequency of 50 MHz, thereby reducing an undesirable aliasing effect while limiting noise from the inputs.

Since the input impedance of the AD7621 is very high, the AD7621 can be directly driven by a low impedance source without gain error. To further improve the noise filtering achieved by the AD7621 analog input circuit, an external, one-pole RC filter between the amplifier's outputs and the ADC analog inputs can be used, as shown in Figure 24. However, large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 27.

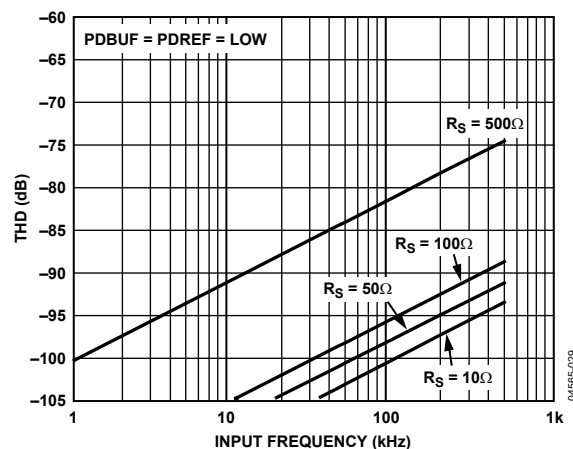


Figure 27. THD vs. Analog Input Frequency and Source Resistance

DRIVER AMPLIFIER CHOICE

Although the AD7621 is easy to drive, the driver amplifier needs to meet the following requirements:

- Together, the driver amplifier and the AD7621 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection. The AD8021 op amp, which combines ultralow noise and high gain bandwidth, meets this settling time requirement even when used with gains up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7621. The noise

AD7621

coming from the driver is filtered by the AD7621 analog input circuit one-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{53}{\sqrt{2809 + \pi^2 f_{-3dB}^2 (Ne_N)^2}} \right)$$

where:

f_{-3dB} is the input bandwidth of the AD7621 (50 MHz) or the cutoff frequency of the input filter (16 MHz), if one is used.

N is the noise factor of the amplifier (+1 in buffer configuration).

e_N is the equivalent input voltage noise density of the op amp, in nV/\sqrt{Hz} .

For instance, a driver with an equivalent input noise density of $2.1 nV/\sqrt{Hz}$, like the AD8021 with a noise gain of +1 when configured as a buffer, degrades the SNR by only 0.33 dB when using the RC filter in Figure 24, and by 1 dB without.

- The driver needs to have a THD performance suitable to that of the AD7621. Figure 14 gives the THD vs. frequency that the driver should exceed.

The AD8021 meets these requirements and is appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type. Moreover, the use of a noninverting +1 gain arrangement is recommended and helps to obtain the best signal-to-noise ratio.

The AD8022 can also be used when a dual version is needed and a gain of 1 is present. The AD829 is an alternative in applications where high frequency (above 100 kHz) performance is not required. In applications with a gain of 1, an 82 pF compensation capacitor is required. The AD8610 is an option when low bias current is needed in low frequency applications.

Single-to-Differential Driver

For applications using unipolar analog signals, a single-ended-to-differential driver, as shown in Figure 28, allows for a differential input into the part. This configuration, when provided an input signal of 0 to V_{REF} , will produce a differential $\pm V_{REF}$ with midscale at $V_{REF}/2$. The one-pole filter using $R = 10 \Omega$ and $C = 1 nF$ provides a corner frequency of 16 MHz.

If the application can tolerate more noise, the AD8139 differential driver can be used.

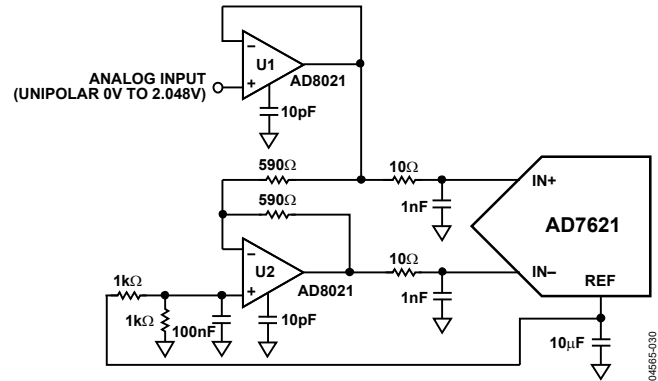


Figure 28. Single-Ended-to-Differential Driver Circuit (Internal Reference Buffer Used)

VOLTAGE REFERENCE INPUT

The AD7621 allows the choice of either a very low temperature drift internal voltage reference or an external reference.

Unlike many ADCs with internal references, the internal reference of the AD7621 provides excellent performance and can be used in almost all applications.

Internal Reference (PDBUF = Low, PDREF = Low)

To use the internal reference, the PDREF and PDBUF inputs must be low. This produces a 1.2 V band gap output on REFBUFIN which, amplified by the internal buffer, results in a 2.048 V reference on the REF pin.

The internal reference is temperature-compensated to $2.048 V \pm 10 mV$. The reference is trimmed to provide a typical drift of $7 ppm/^\circ C$. This typical drift characteristic is shown in Figure 8.

The output resistance of the REFBUFIN is $6.33 k\Omega$ (minimum) when the internal reference is enabled. It is necessary to decouple this with a ceramic capacitor greater than 100 nF. Thus, the capacitor provides an RC filter for noise reduction.

Since the output impedance of REFBUFIN is typically $6.33 k\Omega$, relative humidity (among other industrial contaminants) can directly affect the drift characteristics of the reference. Typically, a guard ring is used to reduce the effects of drift under such circumstances. However, since the AD7621 has a fine lead pitch, guarding this node is not practical. Therefore, in these industrial and other types of applications, it is recommended to use a conformal coating such as Dow Corning 1-2577 or Humiseal 1B73.

External 1.2 V Reference and Internal Buffer (PDREF = High, PDBUF = Low)

To use an external reference with the internal buffer, PDREF should be high and PDBUF should be low. This powers down the internal reference and allows the 1.2 V reference to be applied to REFBUFIN.

External Reference (PDBUF = High, PRBUF = High)

To use an external reference directly on the REF pin, PDREF and PDBUF should both be high.

For improved drift performance, an external reference, such as the [AD780](#) or [ADR431](#), can be used. The advantages of directly using the external voltage reference are:

- SNR and dynamic range improvement (about 1.7 dB) resulting from the use of a reference voltage very close to the supply (2.5 V) instead of a typical 2.048 V reference when the internal reference is used. This is calculated by

$$SNR = 20 \log \left(\frac{2.048}{2.50} \right)$$

- Power savings when the internal reference is powered down (PBREF = PDBUF = high).

PDREF and PDBUF power down the internal reference and the internal reference buffer, respectively.

Reference Decoupling

Whether using an internal or external reference, the AD7621 voltage reference input (REF) has a dynamic input impedance; therefore, it should be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference, but usually consists of a low ESR capacitor connected to REF and REFGND with minimum parasitic inductance. A 10 μ F (X5R, 1206 size) ceramic chip capacitor (or 47 μ F tantalum capacitor) is appropriate when using either the internal reference or one of these recommended reference voltages:

- The low noise, low temperature drift [ADR431](#) and [AD780](#)
- The low power [ADR291](#)
- The low cost [AD1582](#)

The placement of the reference decoupling is also important to the performance of the AD7621. The decoupling capacitor should be mounted on the same side as the ADC right at the REF pin with a thick PCB trace. The REFGND should also connect to the reference decoupling capacitor with the shortest distance.

For applications that use multiple AD7621 devices, it is more effective to use the internal reference buffer in order to buffer the reference voltage.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a ± 15 ppm/ $^{\circ}$ C TC of the reference changes full-scale by ± 1 LSB/ $^{\circ}$ C.

Temperature Sensor

The TEMP pin measures the temperature of the AD7621. To improve the calibration accuracy over the temperature range, the output of the TEMP pin is applied to one of the inputs of the analog switch (such as, [ADG779](#)), and the ADC itself is used to measure its own temperature. This configuration is shown in Figure 29.

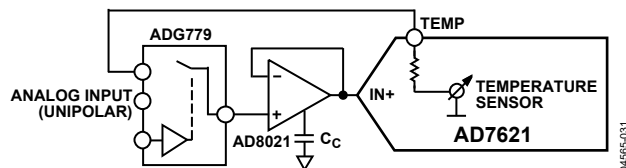


Figure 29. Use of the Temperature Sensor

POWER SUPPLY

The AD7621 uses three sets of power supply pins: an analog 2.5 V supply AVDD, a digital 2.5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.3 V and 5.25 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 24.

Power Sequencing

The AD7621 is independent of power supply sequencing once OVDD does not exceed DVDD by more than 0.3 V until DVDD = 2.3 V during any time; for instance, at power-up or power-down (see the Absolute Maximum Ratings section). Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 30.

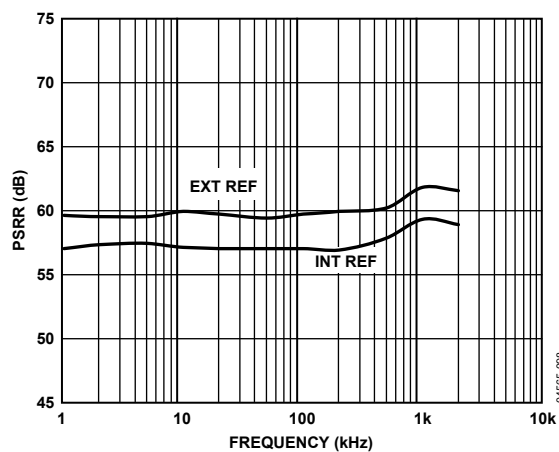


Figure 30. PSRR vs. Frequency

Power-Up

At power-up, or returning to operational mode from the power-down mode ($PD = \text{high}$), the AD7621 engages an initialization process. During this time, the first 128 conversions should be ignored or the RESET input could be pulsed to engage a faster initialization process. Refer to the Digital Interface section for RESET and timing details.

A simple power-on reset circuit, as shown in Figure 24, can be used to minimize the digital interface. As OVDD powers up, the capacitor is shorted and brings RESET high; it is then charged returning RESET to low. However, this circuit only works when powering up the AD7621 because the power down mode ($PD = \text{high}$) does not power down any of the supplies. As a result, RESET is low.

POWER DISSIPATION VS. THROUGHPUT

In impulse mode, the AD7621 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low which allows a significant power saving when the conversion rate is reduced (see Figure 31). This feature makes the AD7621 ideal for very low power, battery-operated applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, drive the digital inputs close to the power rails (that is, OVDD and OGND).

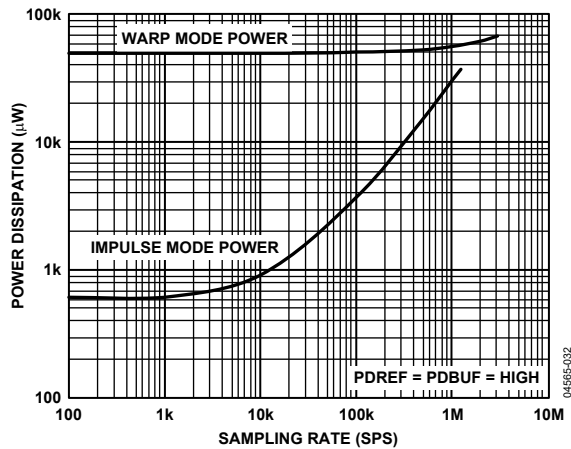


Figure 31. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

The AD7621 is controlled by the \overline{CNVST} input. A falling edge on \overline{CNVST} is all that is necessary to initiate a conversion. Detailed timing diagrams of the conversion process are shown in Figure 32. Once initiated, it cannot be restarted or aborted, even by the power-down input, PD, until the conversion is complete. The \overline{CNVST} signal operates independently of \overline{CS} and \overline{RD} signals.

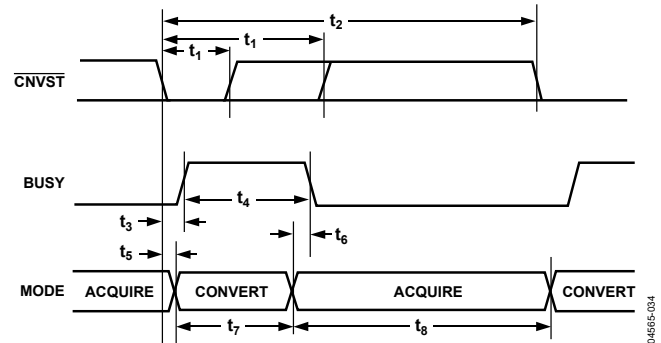


Figure 32. Basic Conversion Timing

For optimal performance, the rising edge of \overline{CNVST} should not occur after the maximum \overline{CNVST} low time, t_1 , or until the end of conversion.

Although \overline{CNVST} is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot, undershoot, or ringing.

The \overline{CNVST} trace should be shielded with ground and a low value (such as 50 Ω) serial resistor termination should be added close to the output of the component that drives this line. Also, a 60 pF capacitor is recommended to further reduce the effects of overshoot and undershoot as shown in Figure 24.

For applications where SNR is critical, the \overline{CNVST} signal should have very low jitter. This can be achieved by using a dedicated oscillator for \overline{CNVST} generation, or by clocking \overline{CNVST} with a high frequency, low jitter clock, as shown in Figure 24.

INTERFACES

DIGITAL INTERFACE

The AD7621 has a versatile digital interface that can be set up as either a serial or parallel interface with the host system. The serial interface is multiplexed on the parallel data bus. The AD7621 digital interface also accommodates 2.5 V, 3.3 V, or 5 V logic with either OVDD at 2.5 V or 3.3 V. OVDD defines the logic high output voltage. In most applications, the OVDD supply pin of the AD7621 is connected to the host system interface 2.5 V or 3.3 V digital supply. Finally, by using the $\overline{\text{OB}}/\overline{2\text{C}}$ input pin, both twos complement or straight binary coding can be used.

The two signals, $\overline{\text{CS}}$ and $\overline{\text{RD}}$, control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{\text{CS}}$ allows the selection of each AD7621 in multicircuit applications and is held low in a single AD7621 design. $\overline{\text{RD}}$ is generally used to enable the conversion result on the data bus.

RESET

The RESET input is used to reset the AD7621 and generate a fast initialization. A rising edge on RESET aborts the current conversion (if any) and tristates the data bus. The falling edge of RESET clears the data bus and engages the initialization process indicated by pulsing BUSY high. Conversions can take place after the falling edge of BUSY. Refer to Figure 33 for the RESET timing details.

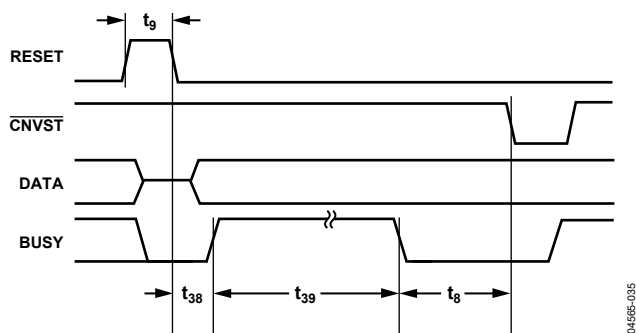


Figure 33. RESET Timing

04565-035

PARALLEL INTERFACE

The AD7621 is configured to use the parallel interface when SER/PAR is held low.

Master Parallel Interface

Data can be continuously read by tying $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low thus requiring minimal microprocessor connections. However, in this mode the data bus is always driven and cannot be used in shared bus applications (unless the device is held in RESET). Figure 34 details the timing for this mode.

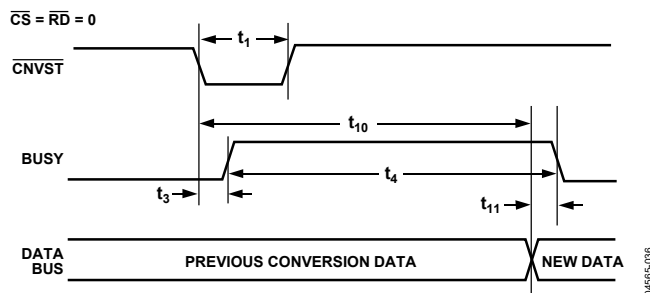


Figure 34. Master Parallel Data Timing for Reading (Continuous Read)

04565-036

Slave Parallel Interface

In slave parallel reading mode, the data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 35 and Figure 36, respectively. When the data is read during the conversion, it is recommended that it is read-only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

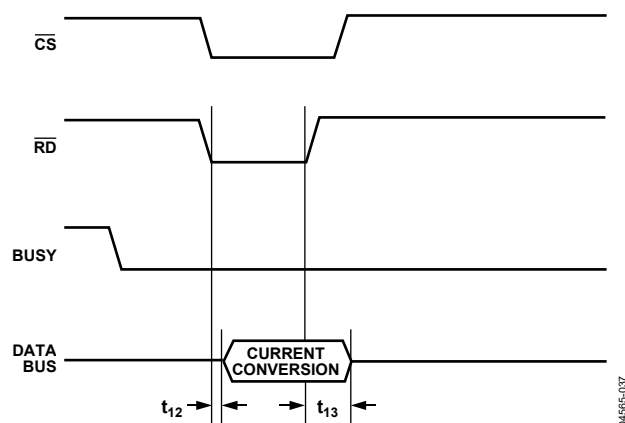


Figure 35. Slave Parallel Data Timing for Reading (Read After Convert)

04565-037

AD7621

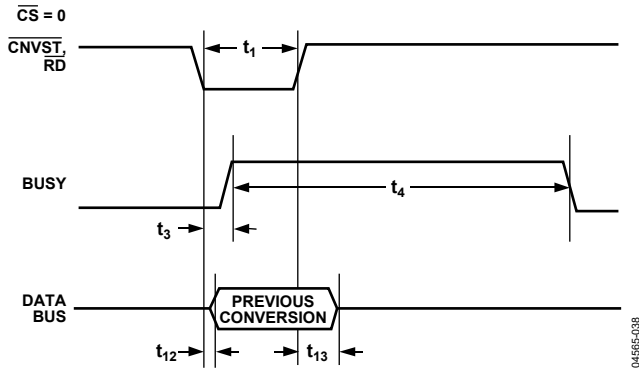


Figure 36. Slave Parallel Data Timing for Reading (Read During Convert)

8-Bit Interface (Master or Slave)

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 37, when BYTESWAP is low, the LSB byte is output on D[7:0] and the MSB is output on D[15:8]. When BYTESWAP is high, the LSB and MSB bytes are swapped, and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16-bit data can be read in two bytes on either D[15:8] or D[7:0]. This interface can be used in both master and slave parallel reading modes.

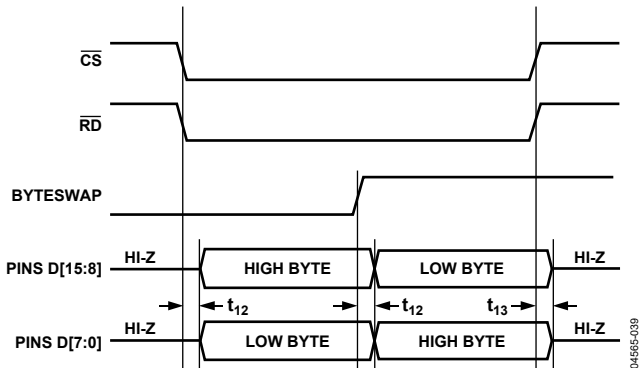


Figure 37. 8-Bit and 16-Bit Parallel Interface

SERIAL INTERFACE

The AD7621 is configured to use the serial interface when SER/PAR is held high. The AD7621 outputs 16 bits of data, MSB first, on the $SDOUT$ pin. This data is synchronized with the 16 clock pulses provided on the $SCLK$ pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The AD7621 is configured to generate and provide the serial data clock $SCLK$ when the EXT/INT pin is held low. The AD7621 also generates a $SYNC$ signal to indicate to the host when the serial data is valid. The serial clock $SCLK$ and the $SYNC$ signal can be inverted, if desired. Depending on the read during convert input, $RDC/SDIN$, the data can be read after each conversion or during the following conversion. Figure 38 and Figure 39 show detailed timing diagrams of these two modes.

Usually, because the AD7621 is used with a fast throughput, the master read during conversion mode is the most recommended serial mode. In this mode, the serial clock and data toggle at appropriate instants, minimizing potential feedthrough between digital activity and critical conversion decisions. In this mode, the $SCLK$ period changes since the LSBs require more time to settle and the $SCLK$ is derived from the SAR conversion cycle.

In read after conversion mode, unlike other modes, the $BUSY$ signal returns low after the 16 data bits are pulsed out and not at the end of the conversion phase resulting in a longer $BUSY$ width. As a result, the maximum throughput cannot be achieved in this mode.

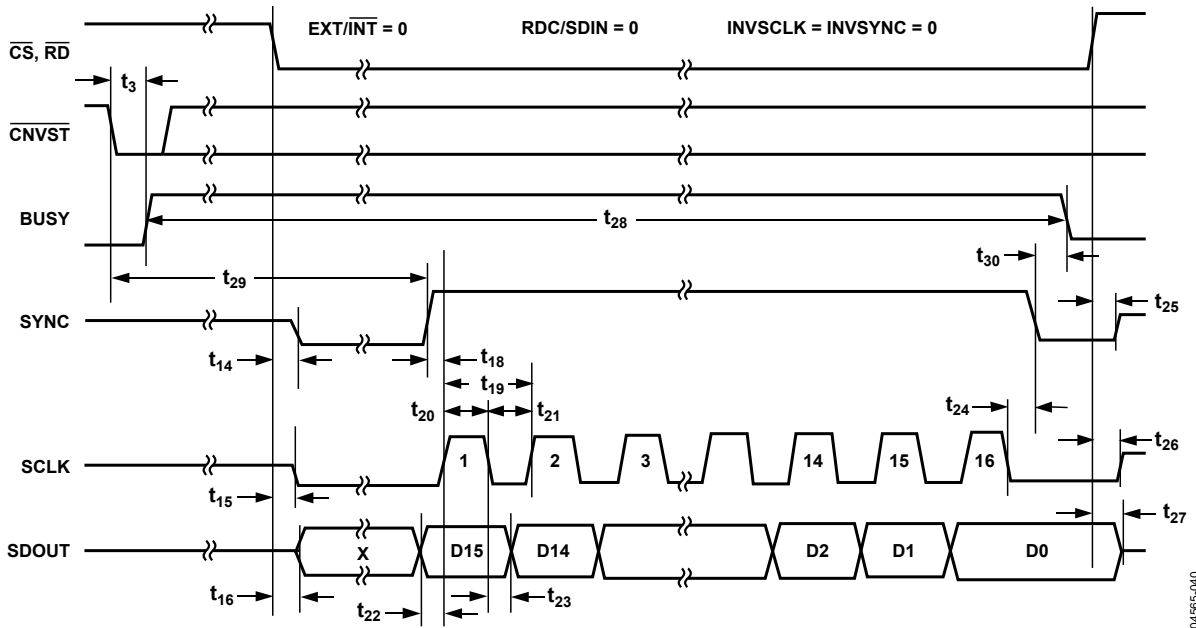


Figure 38. Master Serial Data Timing for Reading (Read After Convert)

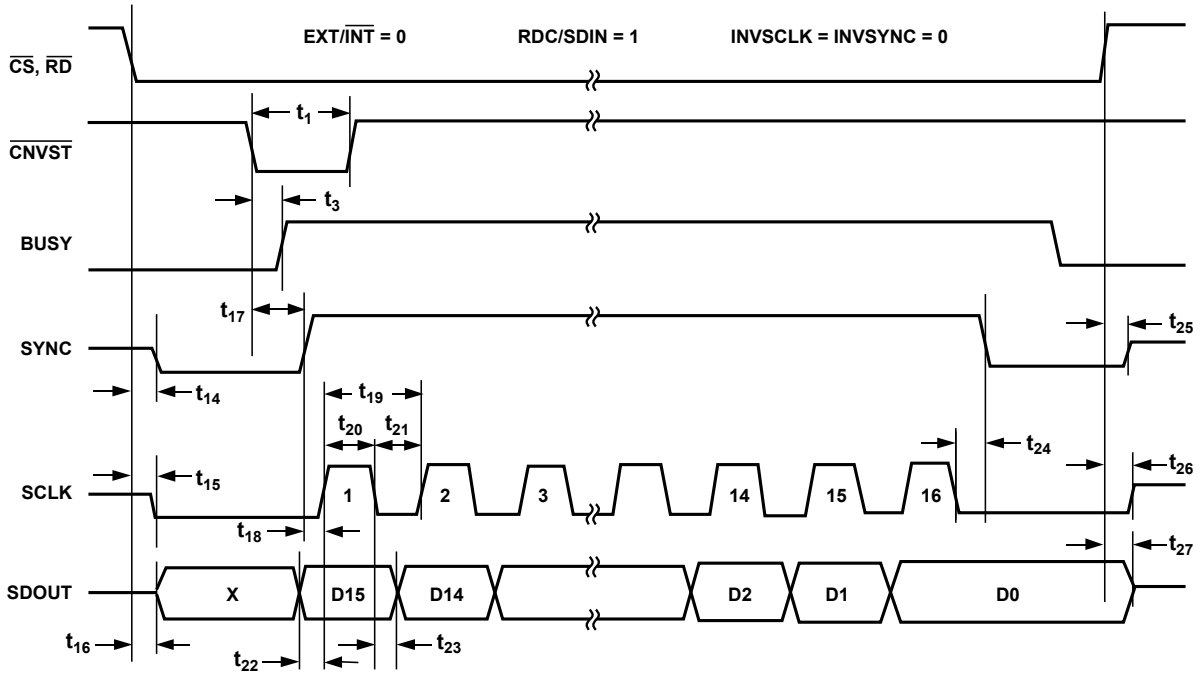


Figure 39. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

SLAVE SERIAL INTERFACE

External Clock

The AD7621 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/INT pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by \overline{CS} . When \overline{CS} and \overline{RD} are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or a discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 41 and Figure 42 show the detailed timing diagrams of these methods.

While the AD7621 is performing a bit decision, it is important that voltage transients be avoided on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7621 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when \overline{BUSY} is low or, more importantly, that it does not transition during the latter half of \overline{BUSY} high.

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 41 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by \overline{BUSY} returning low, the conversion result can be read while both \overline{CS} and \overline{RD} are low. Data is shifted out MSB first with 16 clock pulses and is valid on the rising and falling edges of the clock.

Among the advantages of this method is the fact that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 80 MHz, which accommodates both the slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7621 provides a daisy-chain feature using the RDC/SDIN pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired, as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 40. Simultaneous sampling is possible by using a

common \overline{CNVST} signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOUT. Hence, the MSB of the upstream converter just follows the LSB of the downstream converter on the next SCLK cycle.

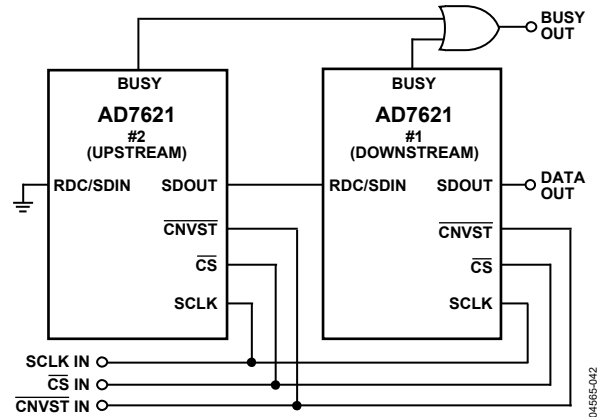


Figure 40. Two AD7621 Devices in a Daisy-Chain Configuration

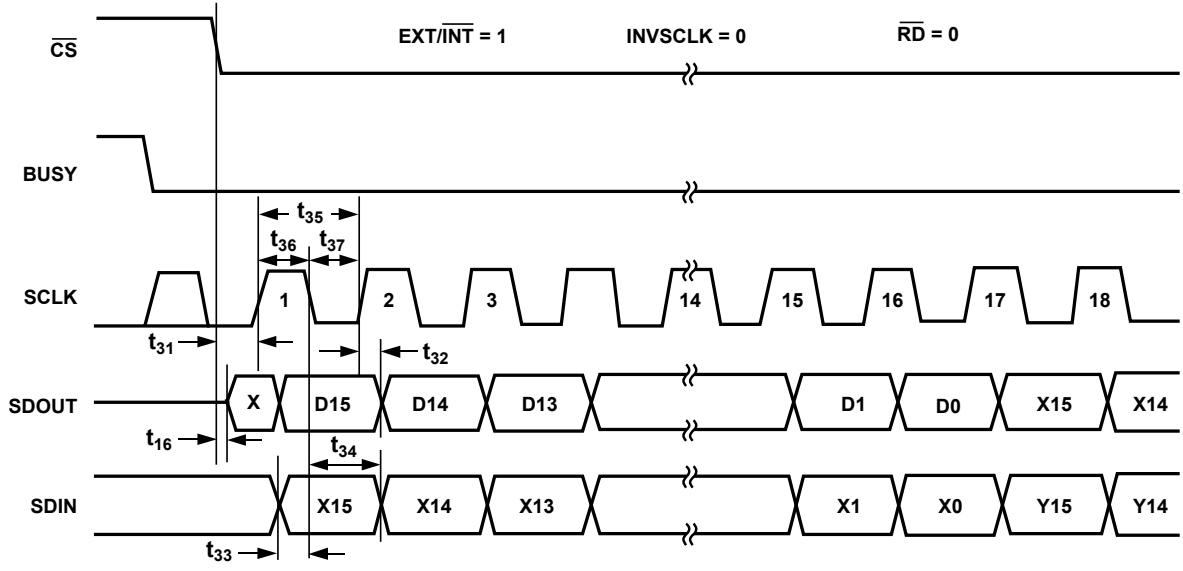
External Clock Data Read During Previous Conversion

Figure 42 shows the detailed timing diagrams of this method. During a conversion, while both \overline{CS} and \overline{RD} are low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and falling edge of the clock. The 16 bits have to be read before the current conversion is complete, otherwise, $\overline{RDERROR}$ is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock (at least 30 MHz when impulse mode is used, 60 MHz when normal mode is used, or 80 MHz when warp mode is used) is recommended to ensure that all the bits are read during the first half of the SAR conversion phase.

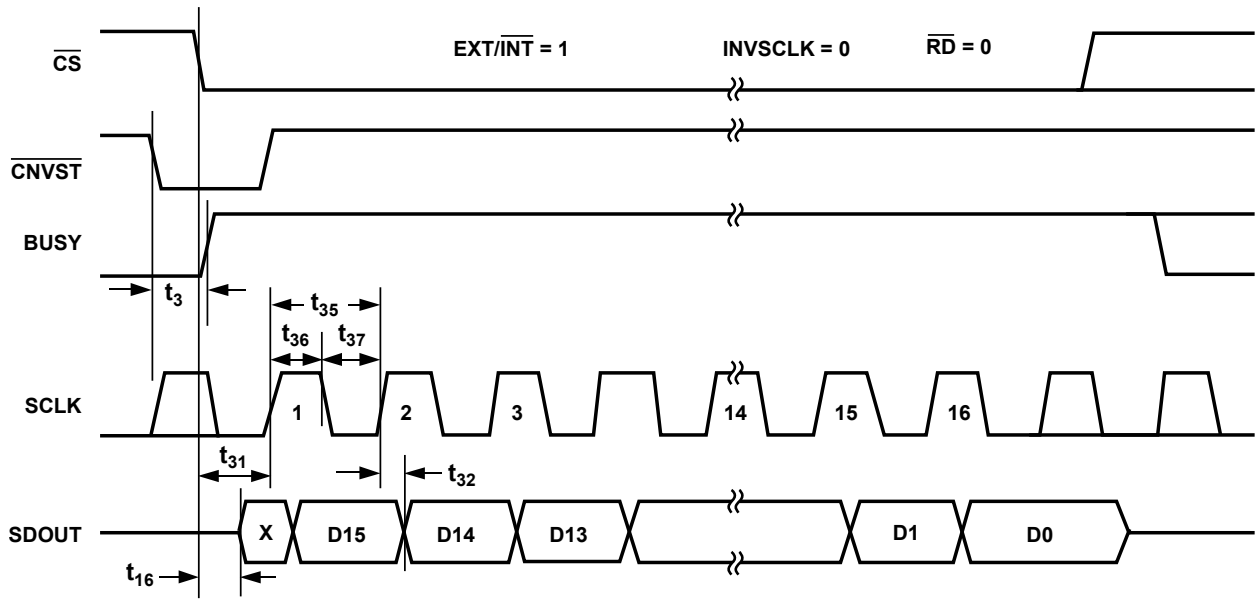
It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion has been initiated. However, this is not recommended when using the fastest throughput of any mode since the acquisition times are only 70 ns, 100 ns, and 50 ns for warp, normal, and impulse modes.

If the maximum throughput is not used, thus allowing more acquisition time, then the use of a slower clock speed can be used to read the data.



04565-043

Figure 41. Slave Serial Data Timing for Reading (Read After Convert)



04565-044

Figure 42. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

AD7621

MICROPROCESSOR INTERFACING

The AD7621 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7621 is designed to interface with a parallel 8-bit or 16-bit wide interface, or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7621 to prevent digital noise from coupling into the ADC. The following section illustrates the use of the AD7621 with an ADSP-219x SPI-equipped DSP.

SPI Interface (ADSP-219x)

Figure 43 shows an interface diagram between the AD7621 and an SPI-equipped DSP, ADSP-219x. To accommodate the slower speed of the DSP, the AD7621 acts as a slave device and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command could be initiated in response to an internal timer interrupt. The reading process can be initiated in response to the end-of-conversion signal (BUSY

going low) using an interrupt line of the DSP. The serial peripheral interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, clock phase bit (CPHA) = 1, and SPI interrupt enable (TIMOD) = 00 by writing to the SPI control register (SPICLTx). It should be noted that to meet all timing requirements, the SPI clock should be limited to 17 Mb/s allowing it to read an ADC result in less than 1 μ s. When a higher sampling rate is desired, use one of the parallel interface modes.

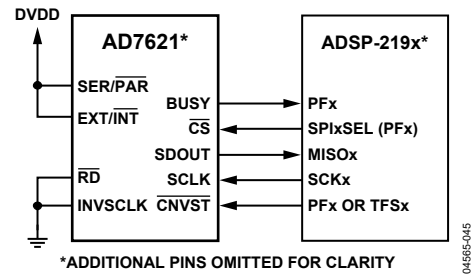


Figure 43. Interfacing the AD7621 to SPI Interface

APPLICATION

LAYOUT

While the AD7621 has very good immunity to noise on the power supplies, exercise care with the grounding layout. To facilitate the use of ground planes that can be easily separated, design the printed circuit board that houses the AD7621 so that the analog and digital sections are separated and confined to certain areas of the board. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7621, or as close as possible to the AD7621. If the AD7621 is in a system where multiple devices require analog-to-digital ground connections, the connections should still be made at one point only, a star ground point, established as close as possible to the AD7621.

To prevent coupling noise onto the die, avoid radiating noise, and to reduce feedthrough:

- Do not run digital lines under the device.
- Do run the analog ground plane under the AD7621.
- Do shield fast switching signals, like $\overline{\text{CNVST}}$ or clocks, with digital ground to avoid radiating noise to other sections of the board, and never run them near analog signal paths.
- Avoid crossover of digital and analog signals.
- Run traces on different but close layers of the board, at right angles to each other, to reduce the effect of feedthrough through the board.

The power supply lines to the AD7621 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the impedance of the supplies presented to the AD7621, and to reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each of the power supplies pins, AVDD, DVDD, and OVDD. The capacitors should be placed close to, and ideally right up against, these pins and their corresponding ground pins. Additionally, low ESR 10 μF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7621 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, and no separate supply is available, it is recommended to connect the DVDD digital supply to the analog supply AVDD through an RC filter, and to connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. Refer to Figure 24 for an example of this configuration. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

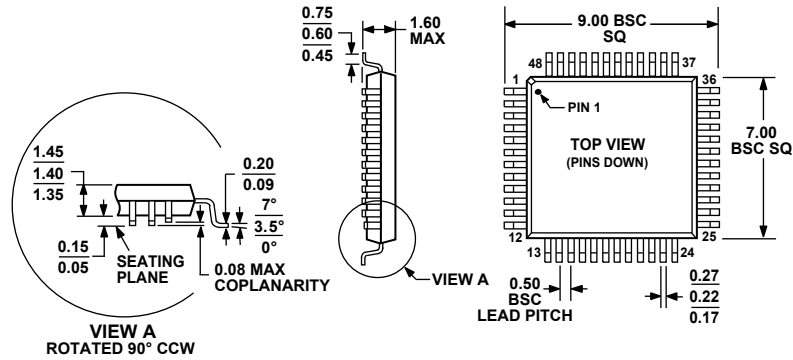
The AD7621 has four different ground pins: REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and, because it carries pulsed currents, should be a low impedance return to the reference. AGND is the ground to which most internal ADC analog signals are referenced; it must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. To minimize parasitic inductances, place the decoupling capacitor close to the ADC and connect it with short, thick traces.

EVALUATING THE AD7621 PERFORMANCE

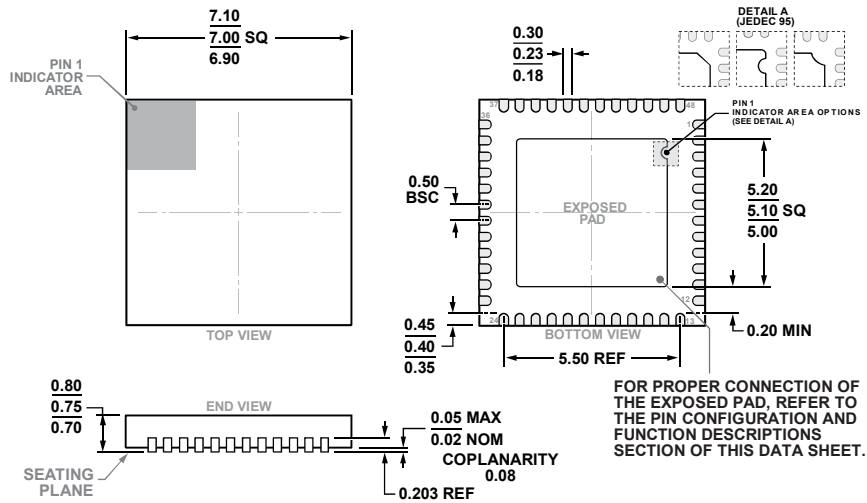
A recommended layout for the AD7621 is outlined in the documentation of the [EVAL-AD7621CB](#) evaluation board for the AD7621. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the [EVAL-CONTROLBRD3](#).

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026BBC

Figure 44. 48-Lead Low Profile Quad Flatpack (LQFP)
[ST-48]
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WKGD-4

Figure 45. 48-Lead Lead Frame Chip Scale Package (LFCSP)
7 mm × 7 mm Body and 0.75 mm Package Height
[CP-48-4]
Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-------------------------------|--------------------------|--|-----------------------|
| AD7621ACP | −40°C to +85°C | 48-Lead Lead Frame Chip Scale (LFCSP) | CP-48-4 |
| AD7621ACPRL | −40°C to +85°C | 48-Lead Lead Frame Chip Scale (LFCSP) | CP-48-4 |
| AD7621ACPZ ¹ | −40°C to +85°C | 48-Lead Lead Frame Chip Scale (LFCSP) | CP-48-4 |
| AD7621ACPZRL ¹ | −40°C to +85°C | 48-Lead Lead Frame Chip Scale (LFCSP) | CP-48-4 |
| AD7621AST | −40°C to +85°C | 48-Lead Low Profile Quad Flatpack (LQFP) | ST-48 |
| AD7621ASTRL | −40°C to +85°C | 48-Lead Low Profile Quad Flatpack (LQFP) | ST-48 |
| AD7621ASTZ ¹ | −40°C to +85°C | 48-Lead Low Profile Quad Flatpack (LQFP) | ST-48 |
| AD7621ASTZRL ¹ | −40°C to +85°C | 48-Lead Low Profile Quad Flatpack (LQFP) | ST-48 |
| EVAL-AD7621CB ² | | Evaluation Board | |
| EVAL-CONTROLBRD3 ³ | | Controller Board | |

¹ Z = Pb-free part.

² This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD3 for evaluation/demonstration purposes.

³ This board allows a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the CB designators.

AD7621

NOTES

NOTES

AD7621

NOTES

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