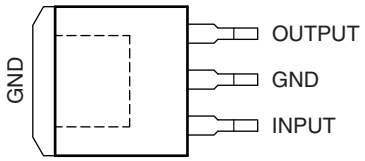
LOW-DROPOUT FIXED-VOLTAGE REGULATORS

Check for Samples: TL760M33-Q1

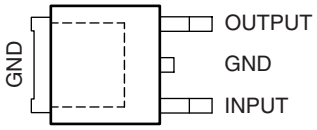
FEATURES

- **Qualified for Automotive Applications**
- **±3% Output Voltage Variation Across Load and Temperature**
- **Load-Dump Protection**
- **500-mV Maximum Dropout Voltage at 500 mA**
- **Fixed 3.3-V Output**
- **Internal Thermal-Overload Protection**
- **Internal Overvoltage Protection**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**

KTT (TO-263) PACKAGE
(TOP VIEW)



KVU (TO-252) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TL760M33-Q1 low-dropout regulator offers a variety of fixed-voltage options that offer a maximum continuous input voltage of 26 V. Utilizing a pnp pass element, this regulator is capable of sourcing 500 mA of current, with a specified maximum dropout of 500 mV, making the TL760M33-Q1 ideal for low-voltage applications. Additionally, the TL760M33-Q1 regulator offers very tight output accuracy of ±3% across operating load and temperature ranges. Other convenient features the regulators provide are internal overcurrent limiting, thermal-overload protection, and overvoltage protection. The TL760M33-Q1 is load-dump protected to its maximum operating condition of 45 V. Stability has been optimized for typical automotive applications and low-cost capacitors.

ORDERING INFORMATION(1)

T_A	V_O (TYP)	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	3.3 V	TO-263 – KTT	Reel of 500	TL760M33QKTTRQ1	TL760M33Q1
		TO-252 – KVU	Reel of 2500	TL760M33QKVURQ1	760M33Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating virtual junction temperature range (unless otherwise noted)

V_I	Maximum input voltage	45 V
T_J	Operating virtual junction temperature	150°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE THERMAL DATA(1)

PACKAGE	BOARD	θ_{JA}
TO-252 (KVU)	High K, JESD 51-5	30.3°C/W
TO-263 (KTT)	High K, JESD 51-5	26.9°C/W

(1) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.

THERMAL RESISTANCE

1-oz copper, one-layer PCB

THERMAL RESISTANCE	VALUE
R_{JA}	55°C/W (area = 240 mm^2)
R_{JC}	5.5°C/W from FET to tab
R_{JC}	0.1°C/W from die center to tab

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_I	Input voltage	3.8	26	V
I_O	Output current	0	500	mA
T_J	Operating virtual-junction temperature	–40	150	°C

ELECTRICAL CHARACTERISTICS

V_I = 6 V, I_O = 500 mA, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_O	Output voltage	I_O = 5 mA to 500 mA, V_I = 3.8 V to 26 V, T_J = 125°C		3.2	3.3	3.4	V
		T_J = 150°C, I_O = 5 mA to 300 mA, V_I = 3.8 V to 26 V		3.2	3.3	3.4	
I_Q	Current consumption, $I_Q = I_I – I_O$	V_I = 6 V	I_O = 250 mA		8	15	mA
			I_O = 500 mA		20	30	
	Line regulation	V_I = 3.8 V to 28 V			10	25	mV
PSRR	Power-supply ripple rejection	f = 100 Hz, V_{ripple} = 0.5 V_{PP}, V_I = 6 V			62		dB
	Load regulation	I_O = 5 mA to 500 mA			5	30	mV
V_{DO}	Dropout voltage(2)	I_O = 250 mA				400	mV
		I_O = 500 mA				500	

(1) Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω on the output.
(2) Measured when the output voltage, V_O, has dropped 100 mV from the nominal value obtained when V_I = 6 V

COMPENSATION-CAPACITOR SELECTION INFORMATION

The TL760M is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range. Figure 1 can be used to establish the capacitance value and ESR range for the best regulator performance.

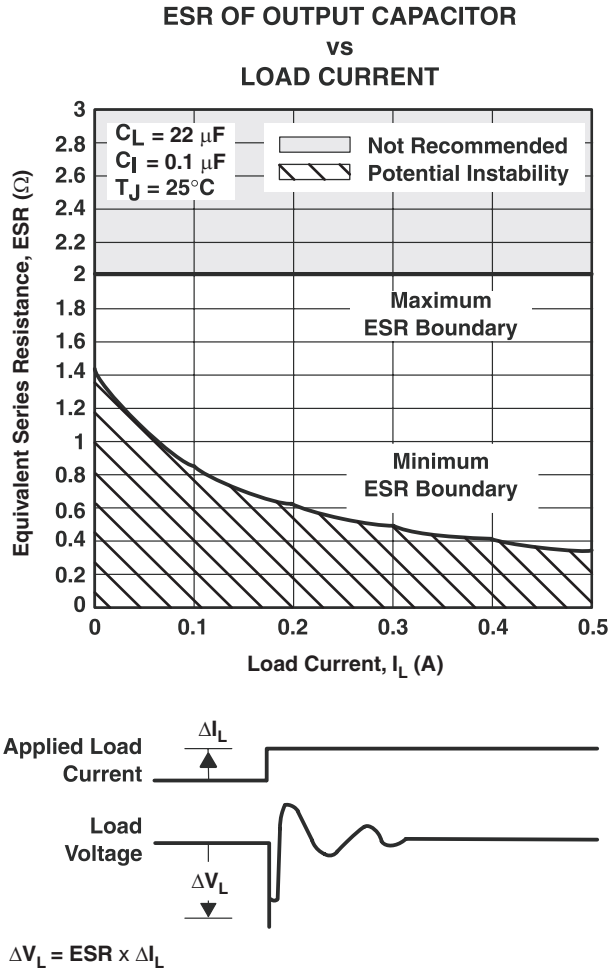


Figure 1.

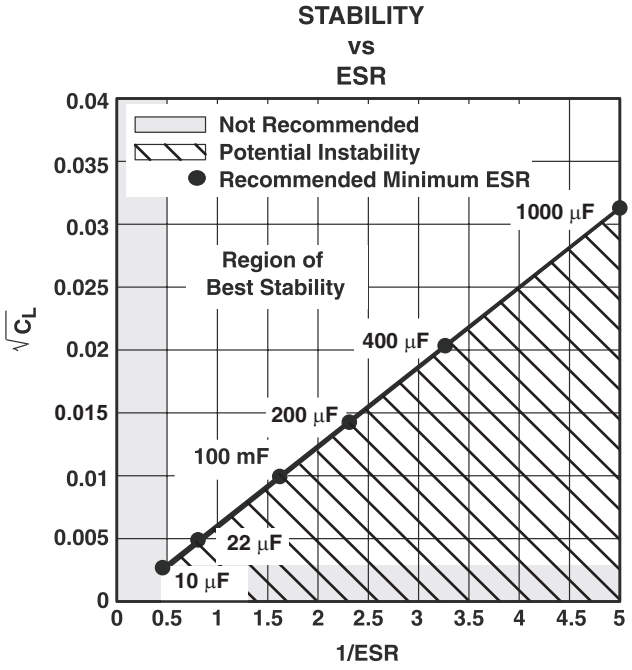


Figure 2.

TYPICAL APPLICATION SCHEMATIC

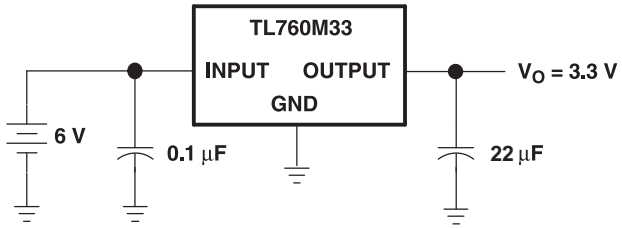


Figure 3.

TYPICAL CHARACTERISTICS

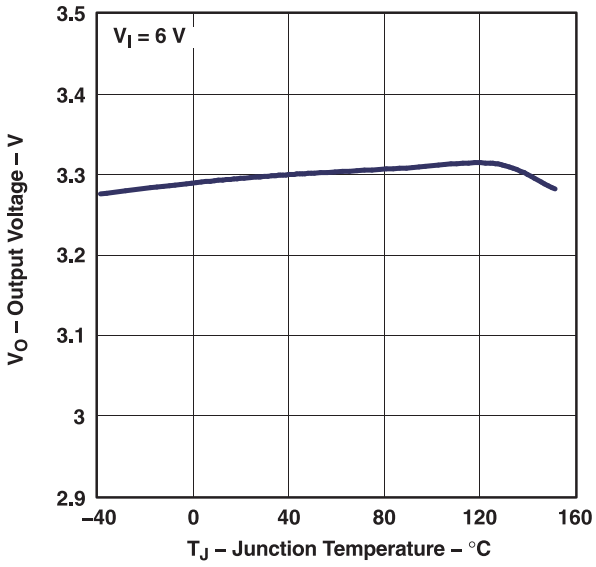


Figure 4.

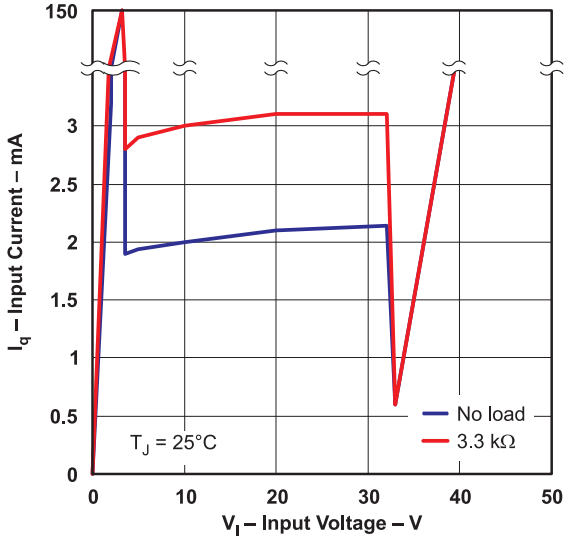


Figure 5.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL760M33QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL760M33Q1	Samples
TL760M33QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	760M33Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

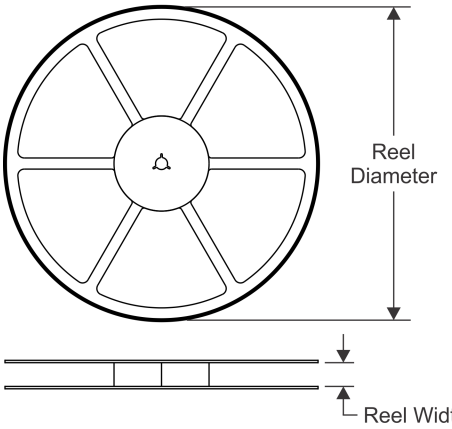
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

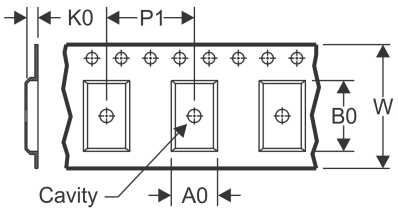
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

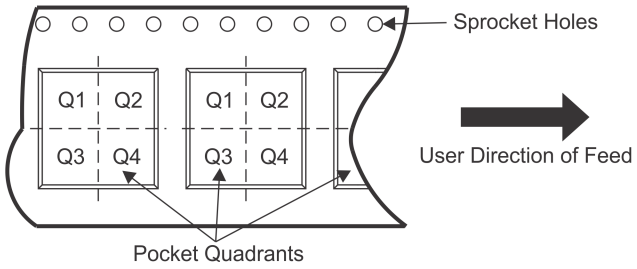


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

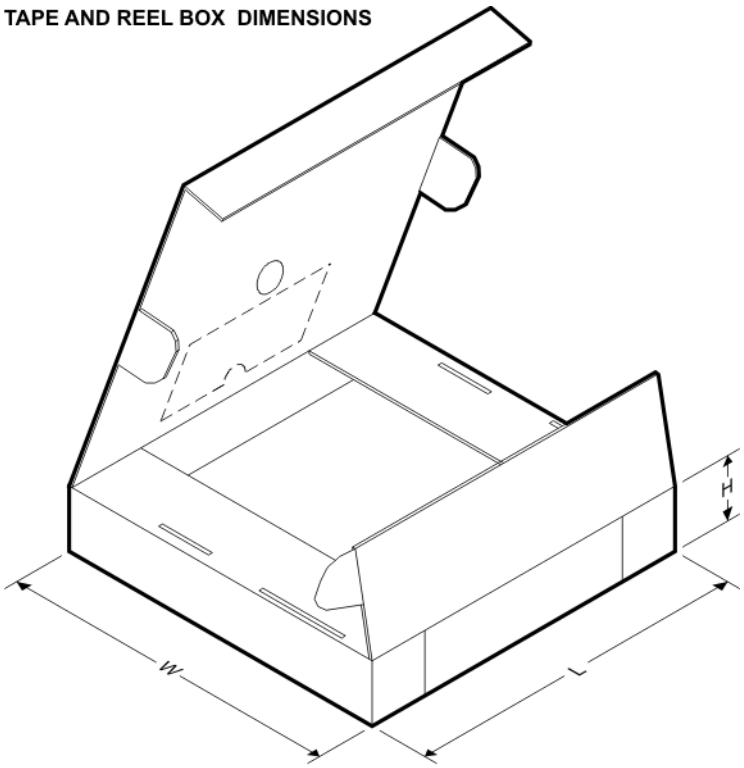
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL760M33QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



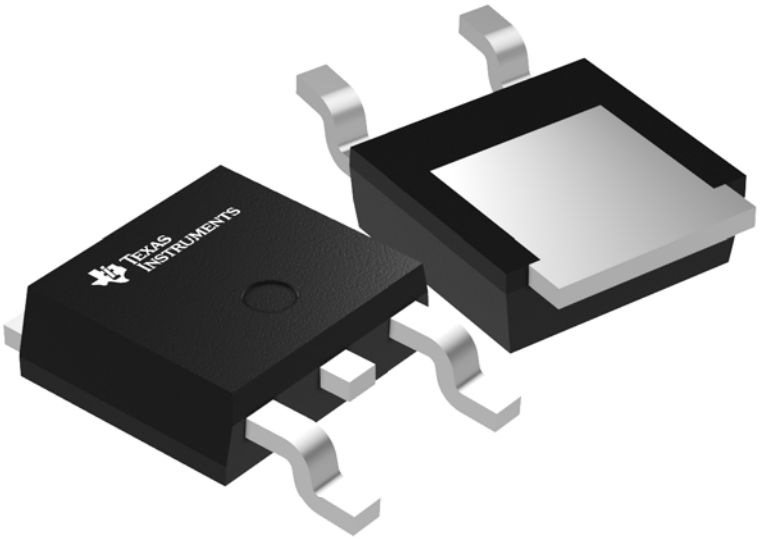
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL760M33QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



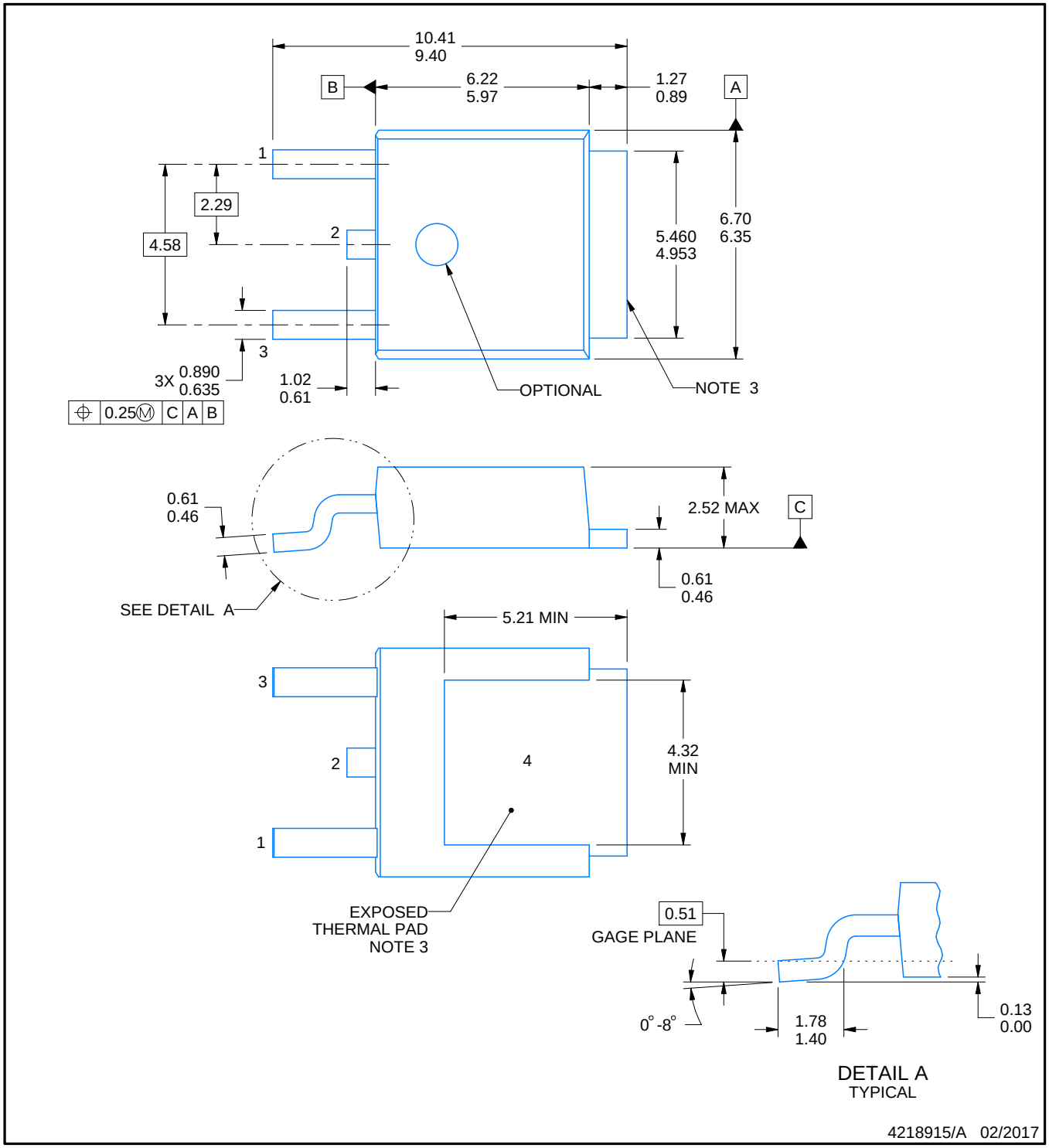
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

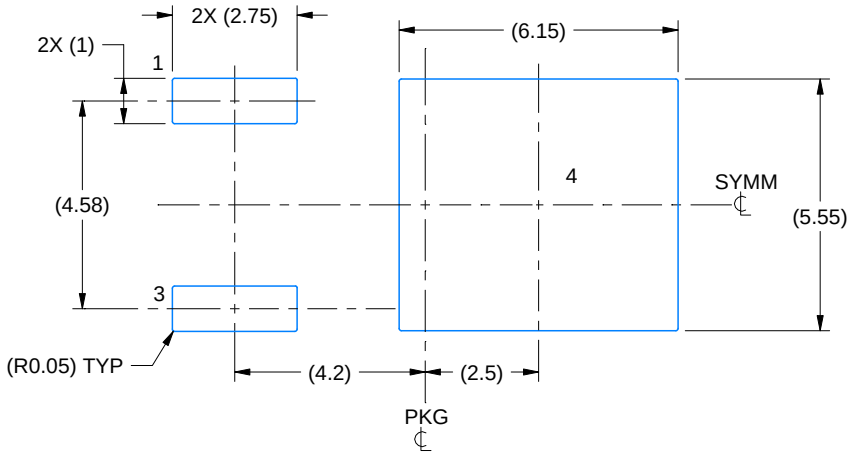
TO-252 - 2.52 mm max height

TO-252

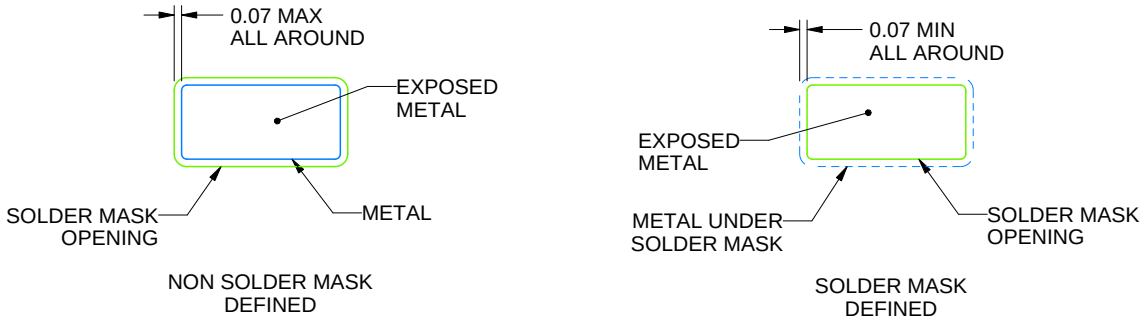


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

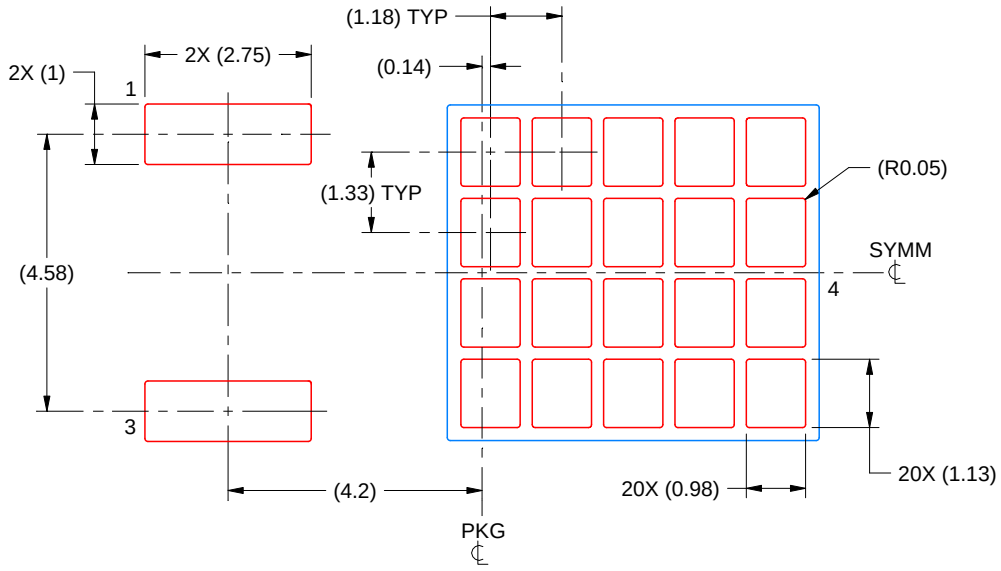
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

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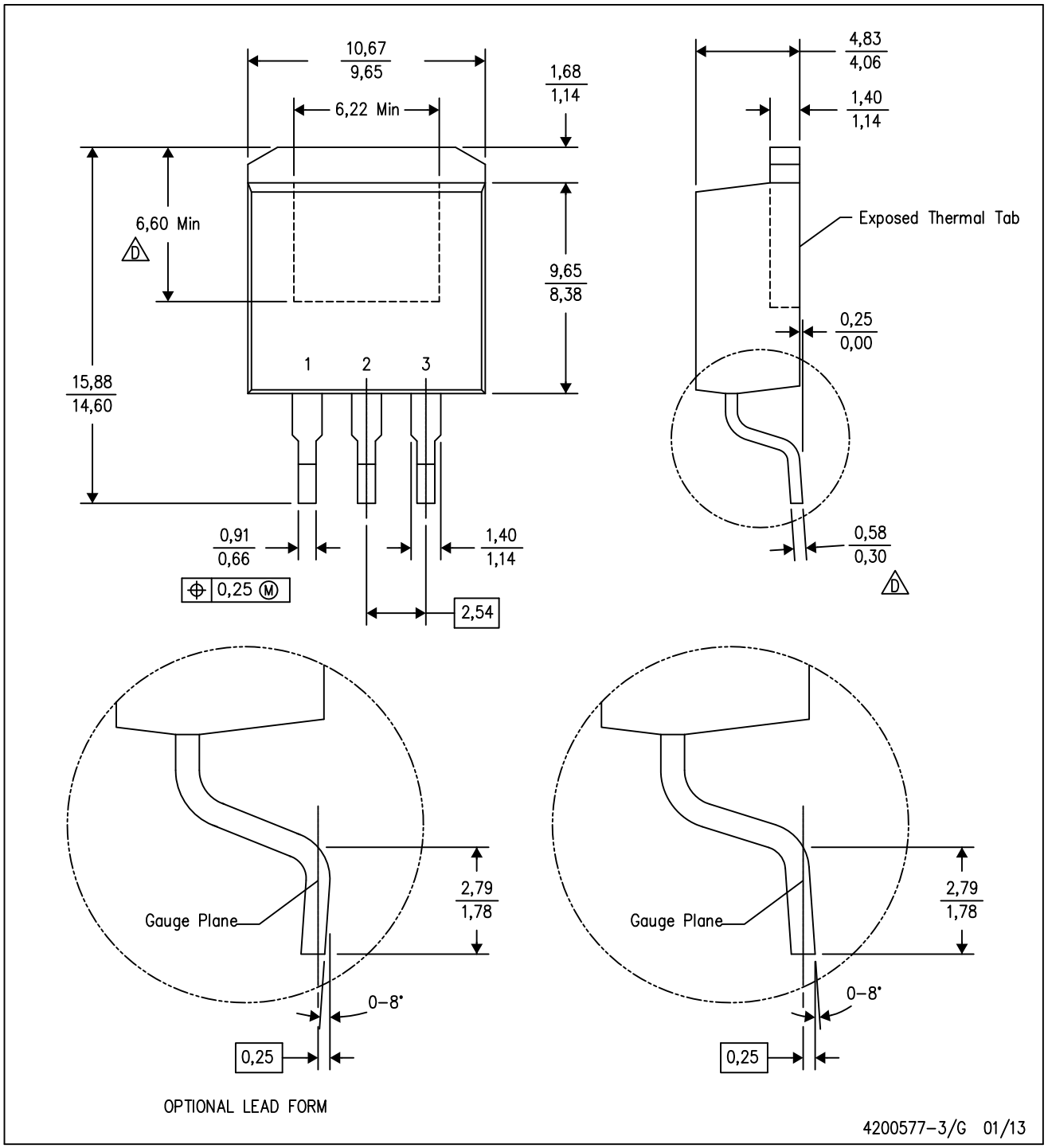
NOTES: (continued)

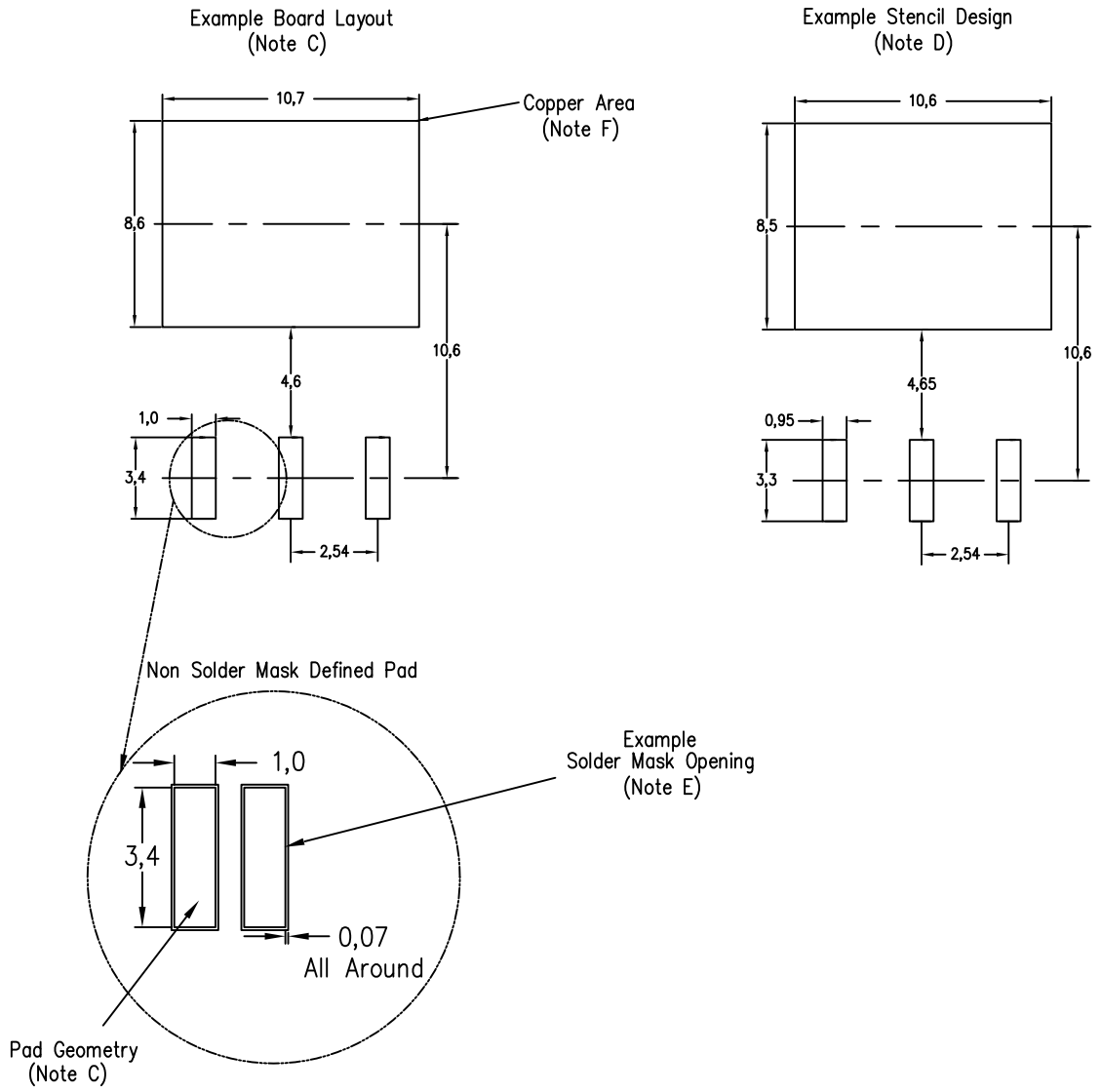
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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