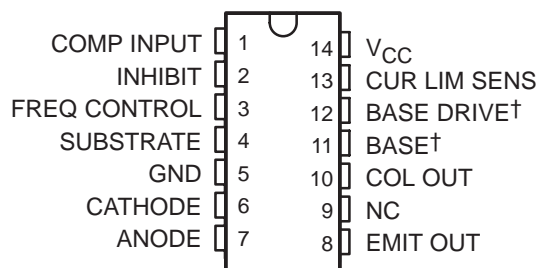


500-mA PEAK STEP-UP, STEP-DOWN, INVERTING SWITCHING VOLTAGE REGULATOR

SLVS009F – JUNE 1976 – REVISED FEBRUARY 2005

- High Efficiency . . . 60% or Greater
- Peak Switch Current . . . 500 mA
- Input Current Limit Protection
- TTL-Compatible Inhibit
- Adjustable Output Voltage
- Input Regulation . . . 0.2% Typ
- Output Regulation . . . 0.4% Typ
- Soft Start-Up Capability
- Can be Used in Buck, Boost, and Inverting Configurations

D, N, OR PW PACKAGE
(TOP VIEW)

NC – No internal connection

†BASE (11) and BASE DRIVE (12) are used for device testing only. They normally are not used in circuit applications of the device.

description/ordering information

The TL497A incorporates all the active functions required in the construction of switching voltage regulators. It also can be used as the control element to drive external components for high-power-output applications. The TL497A was designed for ease of use in step-up, step-down, or voltage-inversion applications requiring high efficiency.

The TL497A is a fixed-on-time variable-frequency switching-voltage-regulator control circuit. The switch-on time is programmed by a single external capacitor connected between FREQ CONTROL and GND. This capacitor, C_T , is charged by an internal constant-current generator to a predetermined threshold. The charging current and the threshold vary proportionally with V_{CC} . Thus, the switch-on time remains constant over the specified range of input voltage (4.5 V to 12 V). Typical on times for various values of C_T are as follows:

| TIMING CAPACITOR, C_T (pF) | 200 | 250 | 350 | 400 | 500 | 750 | 1000 | 1500 | 2000 |
|------------------------------|-----|-----|-----|-----|-----|-----|------|------|------|
| ON TIME (μ s) | 19 | 22 | 26 | 32 | 44 | 56 | 80 | 120 | 180 |

The output voltage is controlled by an external resistor ladder network (R_1 and R_2 in Figures 1, 2, and 3) that provides a feedback voltage to the comparator input. This feedback voltage is compared to the reference voltage of 1.2 V (relative to SUBSTRATE) by the high-gain comparator. When the output voltage decays below the value required to maintain 1.2 V at the comparator input, the comparator enables the oscillator circuit, which charges and discharges C_T as described above. The internal pass transistor is driven on during the charging of C_T . The internal transistor can be used directly for switching currents up to 500 mA. Its collector and emitter are uncommitted, and it is current driven to allow operation from the positive supply voltage or ground. An internal Schottky diode matched to the current characteristics of the internal transistor also is available for blocking or commutating purposes. The TL497A also has on-chip current-limit circuitry that senses the peak currents in the switching regulator and protects the inductor against saturation and the pass transistor against overstress. The current limit is adjustable and is programmed by a single sense resistor, R_{CL} , connected between V_{CC} and CUR LIM SENS. The current-limit circuitry is activated when 0.7 V is developed across R_{CL} . External gating is provided by the INHIBIT input. When the INHIBIT input is high, the output is turned off.

Simplicity of design is a primary feature of the TL497A. With only six external components (three resistors, two capacitors, and one inductor), the TL497A operates in numerous voltage-conversion applications (step-up, step-down, invert) with as much as 85% of the source power delivered to the load. The TL497A replaces the TL497 in all applications.

The TL497AC is characterized for operation from 0°C to 70°C. The TL497AI is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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TL497A

500-mA PEAK STEP-UP, STEP-DOWN, INVERTING SWITCHING VOLTAGE REGULATOR

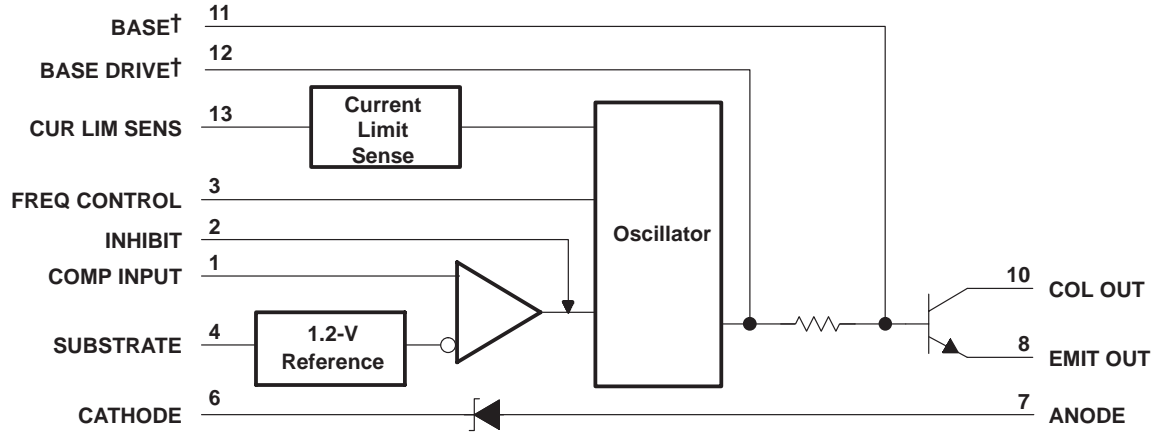
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AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | | | CHIP FORM (Y) |
|----------------|-------------------|-----------------|---------------------------|---------------|
| | SMALL-OUTLINE (D) | PLASTIC DIP (N) | SHRINK SMALL-OUTLINE (PW) | |
| 0°C to 70°C | TL497ACD | TL497ACN | TL497ACPW | TL497AY |
| -40°C to 85°C | TL497AID | TL497AIN | — | — |

The D and PW packages are only taped and reeled. Add the suffix R to the device type (e.g., TL497ACPWR). Chip forms are tested at 25°C.

functional block diagram



† BASE and BASE DRIVE are used for device testing only. They normally are not used in circuit applications of the device.

500-mA PEAK STEP-UP, STEP-DOWN, INVERTING SWITCHING VOLTAGE REGULATOR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 15 V |
| Output voltage, V_O | 35 V |
| Input voltage, V_I (COMP INPUT) | 5 V |
| Input voltage, V_I (INHIBIT) | 5 V |
| Diode reverse voltage | 35 V |
| Power switch current | 750 mA |
| Diode forward current | 750 mA |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package | 86°C/W |
| N package | 101°C/W |
| PW package | 113°C/W |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | 260°C |
| Storage temperature range, T_{Stg} | -65°C to 150°C |

†Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values, except diode voltages, are with respect to network ground terminal.
 - Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 - The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

| | | MIN | MAX | UNIT | |
|---|--|------------|-----------|------|----|
| Supply voltage, V_{CC} | | 4.5 | 12 | V | |
| High-level input voltage, V_{IH} | INHIBIT pin | 2.5 | | V | |
| Low-level input voltage, V_{IL} | INHIBIT pin | | 0.8 | V | |
| Output voltage | Step-up configuration (see Figure 1) | $V_I + 2$ | 30 | V | |
| | Step-down configuration (see Figure 2) | V_{ref} | $V_I - 1$ | | |
| | Inverting regulator (see Figure 3) | $-V_{ref}$ | -25 | | |
| Power switch current | | | 500 | mA | |
| Diode forward current | | | 500 | mA | |
| Operating free-air temperature range, T_A | | TL497AC | 0 | 70 | °C |
| | | TL497AI | -40 | 85 | |

TL497A

500-mA PEAK STEP-UP, STEP-DOWN, INVERTING SWITCHING VOLTAGE REGULATOR

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electrical characteristics over recommended operating conditions, $V_{CC} = 6\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A † | TL497AC | | | TL497AI | | | UNIT |
|-----------------------------------|---|--------------------------------|------------|------|------|---------|------|---------------|------|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| High-level input current, INHIBIT | $V_{I(I)} = 5\text{ V}$ | Full range | 0.8 | 1.5 | | 0.8 | 1.5 | mA | |
| Low-level input current, INHIBIT | $V_{I(I)} = 0\text{ V}$ | Full range | 5 | 10 | | 5 | 20 | μA | |
| Comparator reference voltage | $V_I = 4.5\text{ V to }6\text{ V}$ | Full range | 1.08 | 1.2 | 1.32 | 1.14 | 1.2 | 1.26 | V |
| Comparator input bias current | $V_I = 6\text{ V}$ | Full range | 40 | 100 | | 40 | 100 | μA | |
| Switch on-state voltage | $V_I = 4.5\text{ V}$ | $I_O = 100\text{ mA}$ | 25°C | 0.13 | 0.2 | 0.13 | 0.2 | V | |
| | | $I_O = 500\text{ mA}$ | Full range | 0.85 | | | 1 | | |
| Switch off-state current | $V_I = 4.5\text{ V}, V_O = 30\text{ V}$ | 25°C | 10 | 50 | | 10 | 50 | μA | |
| | | Full range | 200 | | | 500 | | | |
| Sense voltage, CUR LIM SENS | $V_I = 6\text{ V}$ | 25°C | 0.45 | 1 | | 0.45 | 1 | V | |
| Diode forward voltage | | $I_O = 10\text{ mA}$ | Full range | 0.75 | 0.85 | 0.75 | 0.95 | V | |
| | | $I_O = 100\text{ mA}$ | Full range | 0.9 | 1 | 0.9 | 1.1 | | |
| | | $I_O = 500\text{ mA}$ | Full range | 1.33 | 1.55 | 1.33 | 1.75 | | |
| Diode reverse voltage | | $I_O = 500\text{ }\mu\text{A}$ | Full range | 30 | | | V | | |
| | | $I_O = 200\text{ }\mu\text{A}$ | Full range | 30 | | | | | |
| On-state supply current | | 25°C | 11 | 14 | | 11 | 14 | mA | |
| | | Full range | 15 | | | 16 | | | |
| Off-state supply current | | 25°C | 6 | 9 | | 6 | 9 | mA | |
| | | Full range | 10 | | | 11 | | | |

† Full range is 0°C to 70°C for the TL497AC and –40°C to 85°C for the TL497AI.

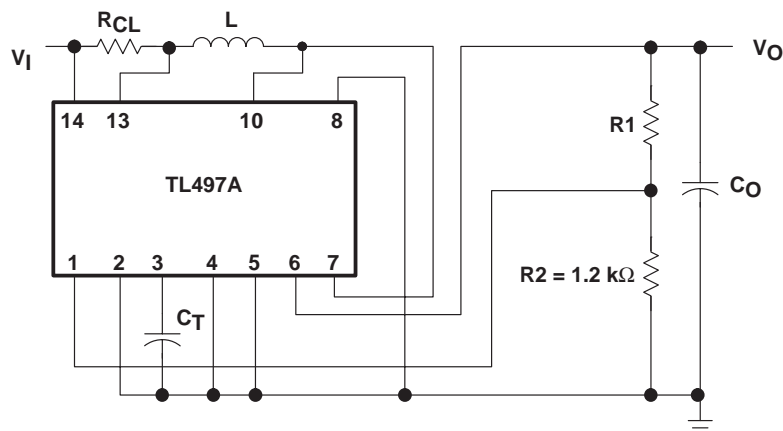
‡ All typical values are at $T_A = 25^\circ\text{C}$.

electrical characteristics over recommended operating conditions, $V_{CC} = 6\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

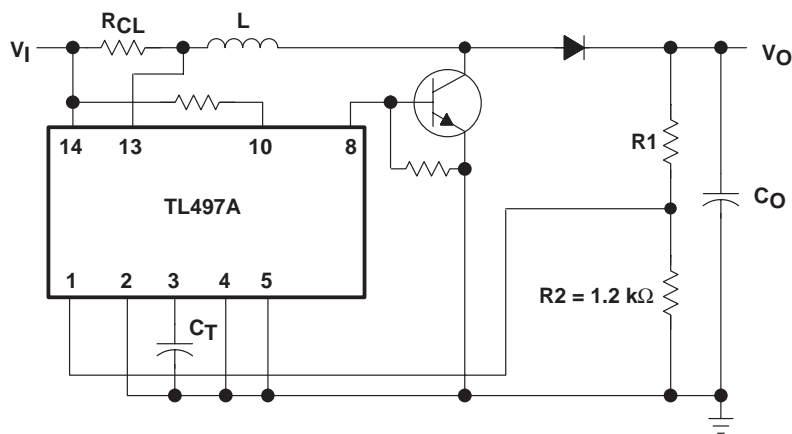
| PARAMETER | TEST CONDITIONS | TL497AY | | | UNIT |
|-----------------------------------|---|---------|-----|-----|---------------|
| | | MIN | TYP | MAX | |
| High-level input current, INHIBIT | $V_{I(I)} = 5\text{ V}$ | 0.8 | | | mA |
| Low-level input current, INHIBIT | $V_{I(I)} = 0\text{ V}$ | 5 | | | μA |
| Comparator reference voltage | $V_I = 4.5\text{ V to }6\text{ V}$ | 1.2 | | | V |
| Comparator input bias current | $V_I = 6\text{ V}$ | 40 | | | μA |
| Switch on-state voltage | $V_I = 4.5\text{ V}, I_O = 100\text{ mA}$ | 0.13 | | | V |
| Switch off-state current | $V_I = 4.5\text{ V}, V_O = 30\text{ V}$ | 10 | | | μA |
| Diode forward voltage | | 0.75 | | | V |
| | | 0.9 | | | |
| | | 1.33 | | | |
| On-state supply current | | 11 | | | mA |
| Off-state supply current | | 6 | | | mA |



APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)} < 500 \text{ mA}$)



EXTENDED POWER CONFIGURATION
(using external transistor)

DESIGN EQUATIONS

- $I_{(PK)} = 2 I_O \max \left[\frac{V_O}{V_I} \right]$

- $L (\mu\text{H}) = \frac{V_I}{I_{(PK)}} t_{on} (\mu\text{s})$

Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T (\text{pF}) \approx 12 t_{on} (\mu\text{s})$

- $R1 = (V_O - 1.2 \text{ V}) \text{ k}\Omega$

- $R_{CL} = \frac{0.5 \text{ V}}{I_{(PK)}}$

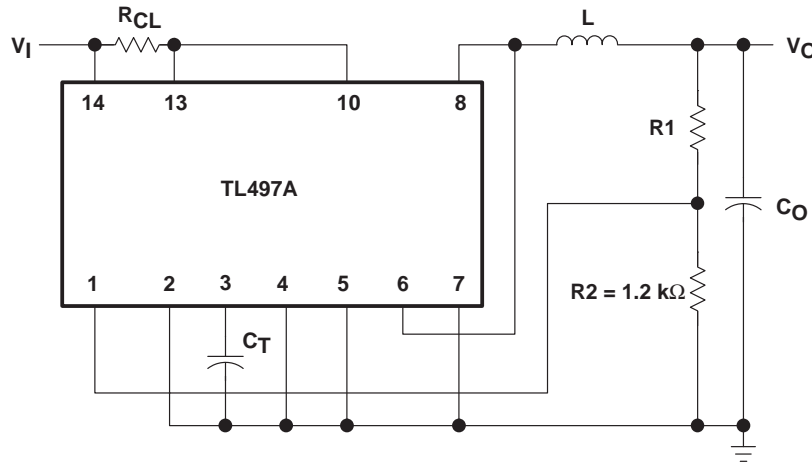
- $C_O (\mu\text{F}) \approx t_{on} (\mu\text{s}) \frac{\left[\frac{V_I}{V_O} I_{(PK)} + I_O \right]}{V_{\text{ripple (PK)}}$

Figure 1. Positive Regulator, Step-Up Configurations

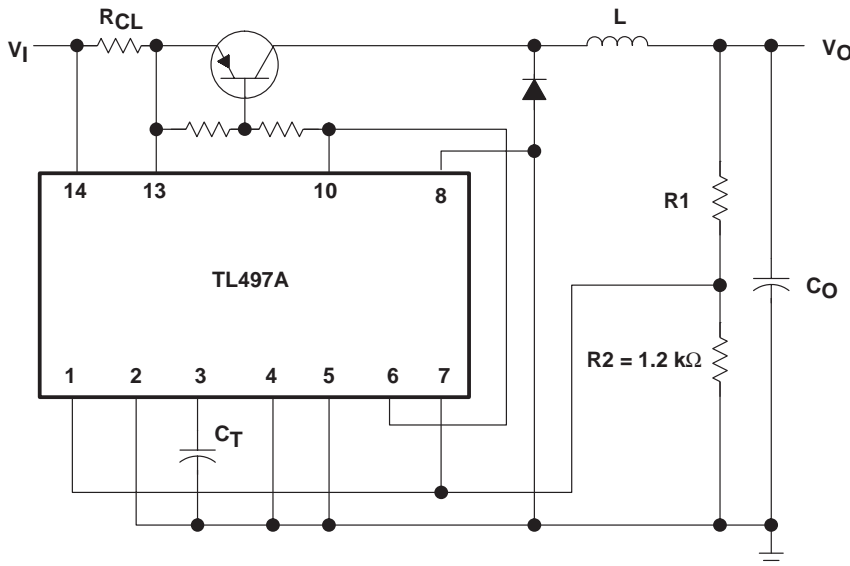
TL497A 500-mA PEAK STEP-UP, STEP-DOWN, INVERTING SWITCHING VOLTAGE REGULATOR

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APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)} < 500$ mA)



EXTENDED POWER CONFIGURATION
(using external transistor)

DESIGN EQUATIONS

- $I_{(PK)} = 2 I_{O \text{ max}}$

- $L (\mu\text{H}) = \frac{V_I - V_O}{I_{(PK)}} t_{on} (\mu\text{s})$

Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

- $C_T (\text{pF}) \approx 12 t_{on} (\mu\text{s})$

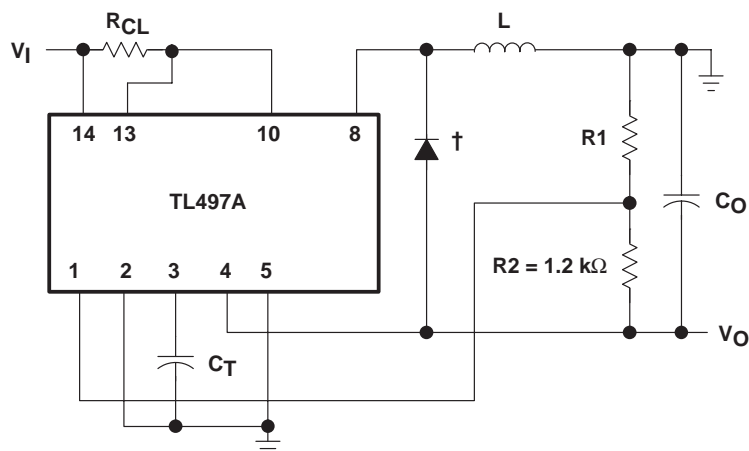
- $R1 = (V_O - 1.2 \text{ V}) \text{ k}\Omega$

- $R_{CL} = \frac{0.5 \text{ V}}{I_{(PK)}}$

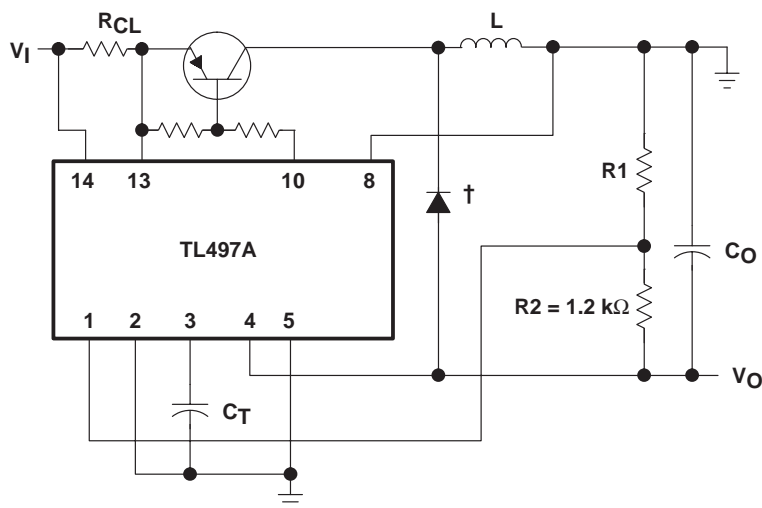
- $C_O (\mu\text{F}) \approx t_{on} (\mu\text{s}) \frac{\left[\frac{V_I - V_O}{V_O} I_{(PK)} + I_O \right]}{V_{\text{ripple (PK)}}$

Figure 2. Positive Regulator, Step-Down Configurations

APPLICATION INFORMATION



BASIC CONFIGURATION
(Peak Switching Current = $I_{(PK)} < 500 \text{ mA}$)



EXTENDED POWER CONFIGURATION
(using external transistor)

DESIGN EQUATIONS

- $I_{(PK)} = 2 I_O \max \left[1 + \frac{|V_O|}{V_I} \right]$

- $L (\mu\text{H}) = \frac{V_I}{I_{(PK)}} t_{on}(\mu\text{s})$

Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

- $C_T(\text{pF}) \approx 12 t_{on}(\mu\text{s})$

- $R_1 = (|V_O| - 1.2 \text{ V}) \text{ k}\Omega$

- $R_{CL} = \frac{0.5 \text{ V}}{I_{(PK)}} \left[\frac{V_I}{|V_O|} I_{(PK)} + I_O \right]$
- $C_O (\mu\text{F}) \approx t_{on}(\mu\text{s}) \frac{V_{ripple}(\text{PK})}{V_{ripple}(\text{PK})}$

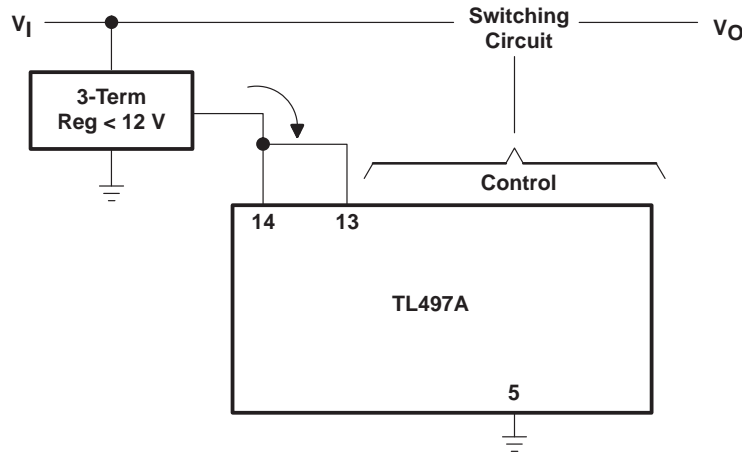
† Use external catch diode, e.g., 1N4001, when building an inverting supply with the TL497A.

Figure 3. Inverting Applications

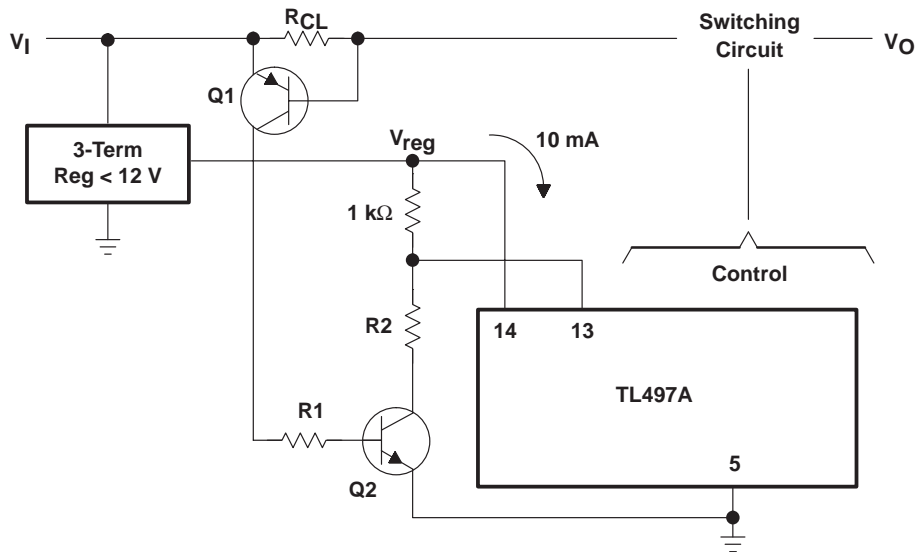
TL497A 500-mA PEAK STEP-UP, STEP-DOWN, INVERTING SWITCHING VOLTAGE REGULATOR

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APPLICATION INFORMATION



EXTENDED INPUT CONFIGURATION WITHOUT CURRENT LIMIT



DESIGN EQUATIONS

- $R_{CL} = \frac{V_{BE(Q1)}}{I_{limit} (PK)}$
- $R1 = \frac{V_1}{I_B(Q2)}$
- $R2 = (V_{reg} - 1) 10 \text{ k}\Omega$

CURRENT LIMIT FOR EXTENDED INPUT CONFIGURATION

Figure 4. Extended Input Voltage Range ($V_1 > 12 \text{ V}$)

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL497ACD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL497AC | Samples |
| TL497ACDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL497AC | Samples |
| TL497ACN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL497ACN | Samples |
| TL497ACNE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL497ACN | Samples |
| TL497ACNSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL497A | Samples |
| TL497ACPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T497A | Samples |
| TL497AID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL497AI | Samples |
| TL497AIDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL497AI | Samples |
| TL497AIN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL497AIN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL497ACDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL497ACNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TL497ACPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL497AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL497ACDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL497ACNSR | SO | NS | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| TL497ACPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| TL497AIDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

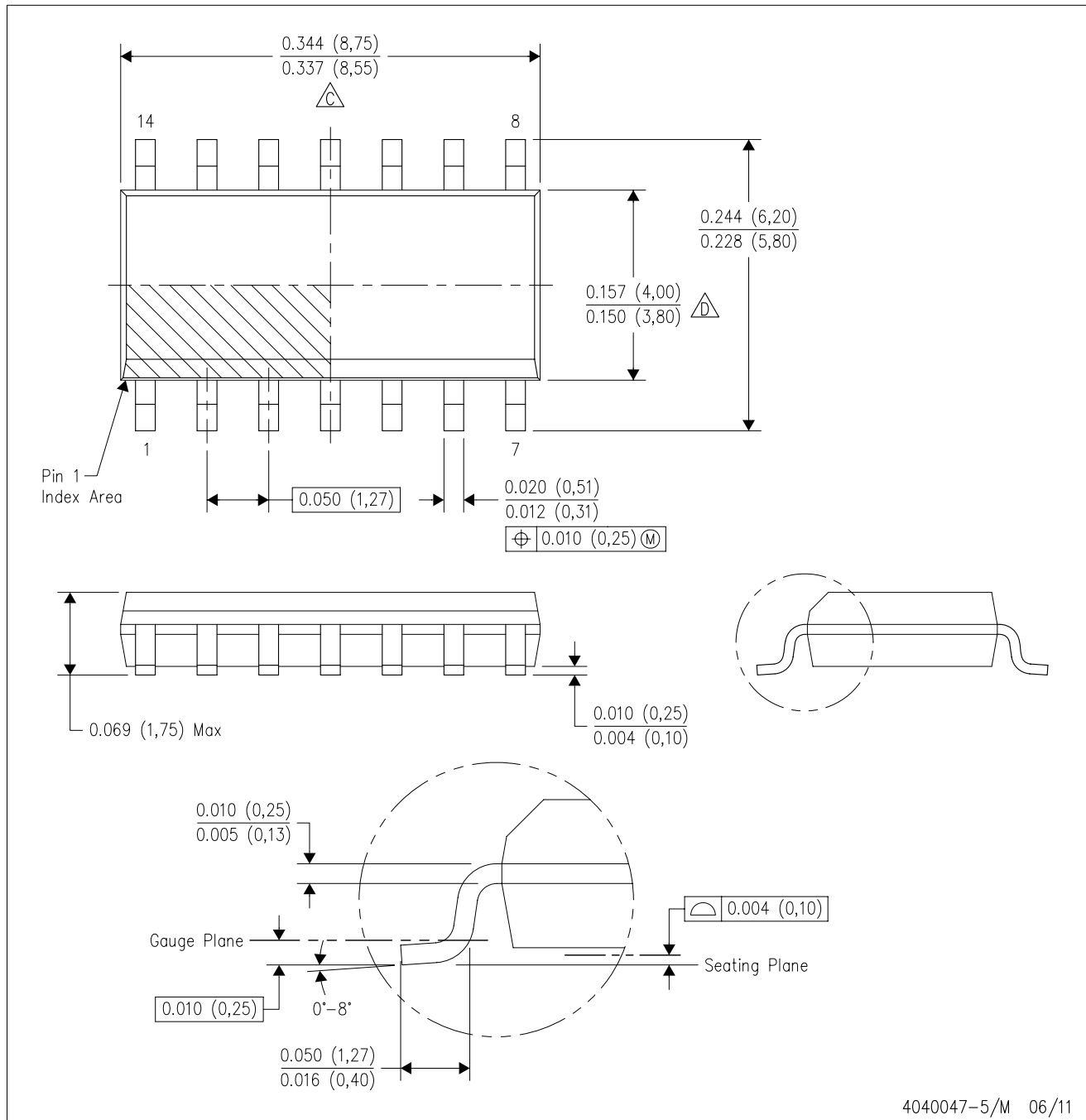
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

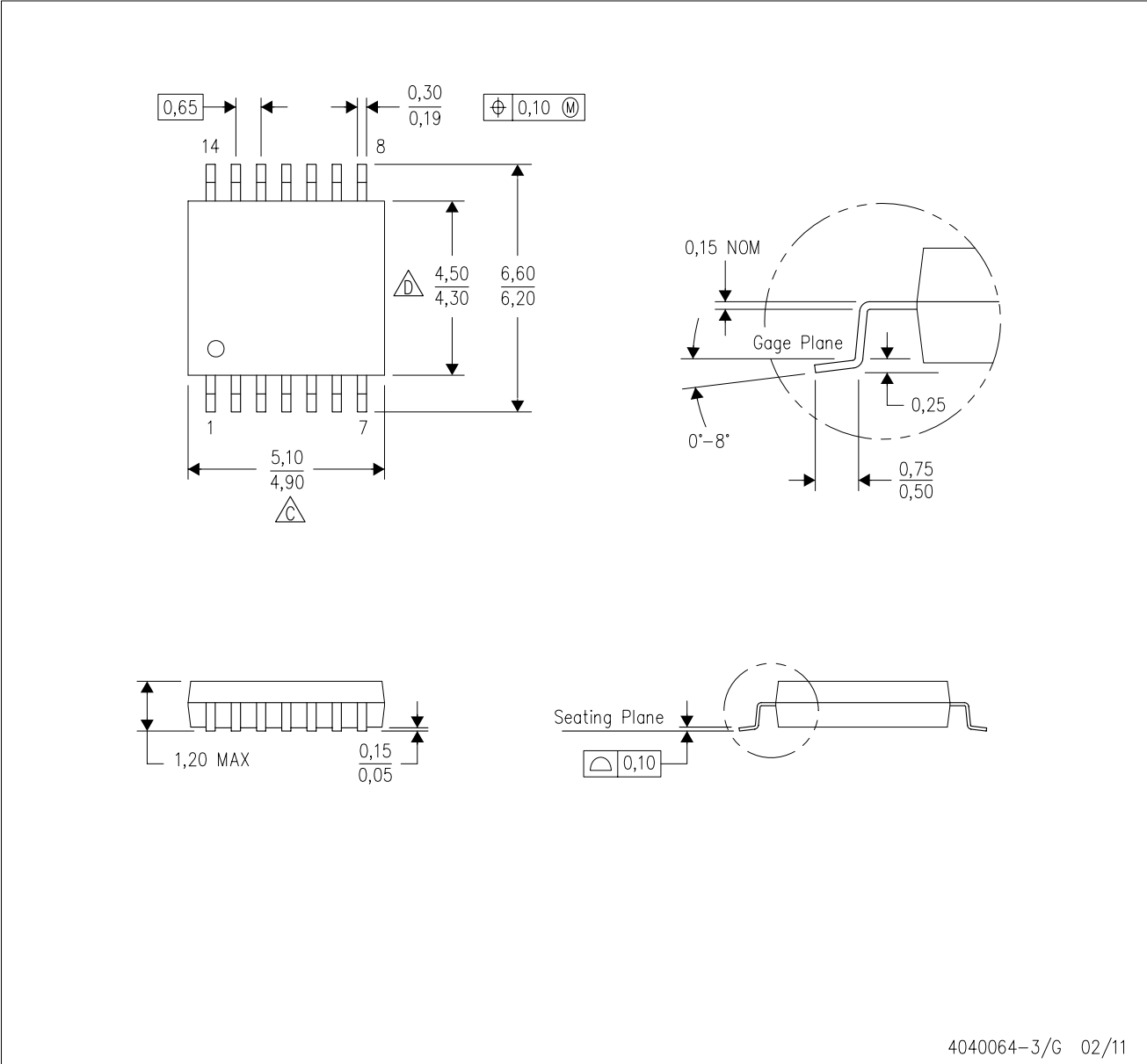
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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