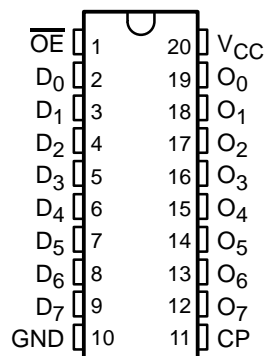


CY54FCT574T, CY74FCT574T 8-BIT REGISTERS WITH 3-STATE OUTPUTS

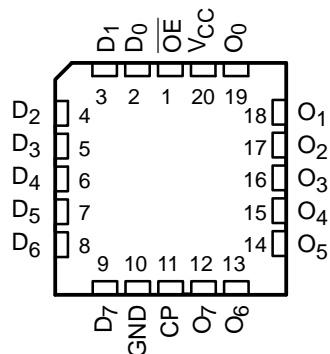
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- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Edge-Triggered D-Type Inputs
- 250-MHz Typical Switching Rate
- CY54FCT574T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT574T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

CY54FCT574T . . . D PACKAGE
CY74FCT574T . . . Q OR SO PACKAGE
(TOP VIEW)



CY54FCT574T . . . L PACKAGE
(TOP VIEW)



description

The 'FCT574T devices are high-speed, low-power, octal D-type flip-flops, featuring separate D-type inputs for each flip-flop. These devices have 3-state outputs for bus-oriented applications. A buffered clock (CP) and output-enable (\overline{OE}) inputs are common to all flip-flops. The 'FCT574T are identical to 'FCT374T, except for a flow-through pinout to simplify board design. The eight flip-flops in the 'FCT574T store the state of their individual D inputs that meet the setup-time and hold-time requirements on the low-to-high CP transition. When \overline{OE} is low, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is high, the outputs are in the high-impedance state. The state of \overline{OE} does not affect the state of the flip-flops.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT574T, CY74FCT574T
8-BIT REGISTERS
WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

| TA | PACKAGE† | | SPEED (ns) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------|-----------------------|------------------|
| -40°C to 85°C | QSOP – Q | Tape and reel | 5.2 | CY74FCT574CTQCT | FCT574C |
| | SOIC – SO | Tube | 5.2 | CY74FCT574CTSOC | FCT574C |
| | | Tape and reel | 5.2 | CY74FCT574CTSOCT | |
| | QSOP – Q | Tape and reel | 6.5 | CY74FCT574ATQCT | FCT574A |
| | SOIC – SO | Tube | 6.5 | CY74FCT574ATSOC | FCT574A |
| | | Tape and reel | 6.5 | CY74FCT574ATSOCT | |
| | QSOP – Q | Tape and reel | 10 | CY74FCT574TQCT | FCT574 |
| | SOIC – SO | Tube | 10 | CY74FCT574TSOC | FCT574 |
| Tape and reel | | 10 | CY74FCT574TSOCT | | |
| -55°C to 125°C | CDIP – D | Tube | 6.2 | CY54FCT574CTDMB | |
| | CDIP – D | Tube | 7.2 | CY54FCT574ATDMB | |
| | LCC – L | Tube | 7.2 | CY54FCT574ATLMB | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|----|-----------------|--------|
| D | CP | \overline{OE} | O |
| H | ↑ | L | H |
| L | ↑ | L | L |
| X | X | H | Z |

H = High logic level, L = Low logic level,
 X = Don't care, Z = High-impedance state,
 ↑ = Low-to-high clock transition

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range to ground potential | –0.5 V to 7 V |
| DC input voltage range | –0.5 V to 7 V |
| DC output voltage range | –0.5 V to 7 V |
| DC output current (maximum sink current/pin) | 120 mA |
| Package thermal impedance, θ_{JA} (see Note 1): Q package | 68°C/W |
| SO package | 58°C/W |
| Ambient temperature range with power applied, T_A | –65°C to 135°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

| | CY54FCT574T | | | CY74FCT574T | | | UNIT |
|--------------------------------------|-------------|-----|-----|-------------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | 0.8 | | | 0.8 | | | V |
| I_{OH} High-level output current | –12 | | | –32 | | | mA |
| I_{OL} Low-level output current | 32 | | | 64 | | | mA |
| T_A Operating free-air temperature | –55 | | 125 | –40 | | 85 | °C |

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

CY54FCT574T, CY74FCT574T
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | CY54FCT574T | | | CY74FCT574T | | | UNIT |
|-------------------|--|--------------------------|------|------|-------------|------|------|------|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _{IN} = -18 mA | | -0.7 | -1.2 | | | | V |
| | V _{CC} = 4.75 V, I _{IN} = -18 mA | | | | | -0.7 | -1.2 | |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -12 mA | 2.4 | 3.3 | | | | | V |
| | V _{CC} = 4.75 V | I _{OH} = -32 mA | | | 2 | | | |
| | | I _{OH} = -15 mA | | | | 2.4 | 3.3 | |
| V _{OL} | V _{CC} = 4.5 V, I _{OL} = 32 mA | | 0.3 | 0.55 | | | | V |
| | V _{CC} = 4.75 V, I _{OL} = 64 mA | | | | | 0.3 | 0.55 | |
| V _{hys} | All inputs | | 0.2 | | | 0.2 | | V |
| I _I | V _{CC} = 5.5 V, V _{IN} = V _{CC} | | | 5 | | | | μA |
| | V _{CC} = 5.25 V, V _{IN} = V _{CC} | | | | | | 5 | |
| I _{IH} | V _{CC} = 5.5 V, V _{IN} = 2.7 V | | | ±1 | | | | μA |
| | V _{CC} = 5.25 V, V _{IN} = 2.7 V | | | | | | ±1 | |
| I _{IL} | V _{CC} = 5.5 V, V _{IN} = 0.5 V | | | ±1 | | | | μA |
| | V _{CC} = 5.25 V, V _{IN} = 0.5 V | | | | | | ±1 | |
| I _{off} | V _{CC} = 0 V, V _{OUT} = 4.5 V | | | ±1 | | | ±1 | μA |
| I _{OS} ‡ | V _{CC} = 5.5 V, V _{OUT} = 0 V | -60 | -120 | -225 | | | | mA |
| | V _{CC} = 5.25 V, V _{OUT} = 0 V | | | | -60 | -120 | -225 | |
| I _{OZH} | V _{CC} = 5.5 V, V _{IN} = 2.7 V | | | 10 | | | | μA |
| | V _{CC} = 5.25 V, V _{IN} = 2.7 V | | | | | | 10 | |
| I _{OZL} | V _{CC} = 5.5 V, V _{IN} = 0.5 V | | | -10 | | | | μA |
| | V _{CC} = 5.25 V, V _{IN} = 0.5 V | | | | | | -10 | |
| I _{CC} | V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V | | 0.1 | 0.2 | | | | mA |
| | V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V | | | | | 0.1 | 0.2 | |
| ΔI _{CC} | V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open | | 0.5 | 2 | | | | mA |
| | V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open | | | | | 0.5 | 2 | |

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | | CY54FCT574T | | CY74FCT574T | | UNIT | |
|----------------------|--|--|--|------|-------------|------|------------|------|
| | | | MIN | TYP† | MAX | MIN | | TYP† |
| I_{CCD}^{\ddagger} | $V_{CC} = 5.5\text{ V}$, Outputs open, One bit switching at 50% duty cycle, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | | 0.06 | 0.12 | | | mA/ MHz | |
| | $V_{CC} = 5.25\text{ V}$, Outputs open, One bit switching at 50% duty cycle, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | | | | 0.06 | 0.12 | | |
| I_C | $V_{CC} = 5.5\text{ V}$, $f_0 = 10\text{ MHz}$, Outputs open, $\overline{OE} = \text{GND}$ | One bit switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle | $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | 0.7 | 1.4 | | mA | |
| | | | $V_{IN} = 3.4\text{ V}$ or GND | 1.2 | 3.4 | | | |
| | | Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle | $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | 1.6 | 3.2 | | | |
| | | | $V_{IN} = 3.4\text{ V}$ or GND | 3.9 | 12.2 | | | |
| | $V_{CC} = 5.25\text{ V}$, $f_0 = 10\text{ MHz}$, Outputs open, $\overline{OE} = \text{GND}$ | One bit switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle | $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | | | 0.7 | | 1.4 |
| | | | $V_{IN} = 3.4\text{ V}$ or GND | | | 1.2 | | 3.4 |
| | | Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle | $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$ | | | 1.6 | | 3.2 |
| | | | $V_{IN} = 3.4\text{ V}$ or GND | | | 3.9 | | 12.2 |
| C_i | | | 5 | 10 | 5 | 10 | pF | |
| C_o | | | 9 | 12 | 9 | 12 | pF | |

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4\text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | CY54FCT574T | | CY54FCT574AT | | CY54FCT574CT | | UNIT |
|-----------------|--------------------------------|-------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, CP high or low | 7 | | 6 | | 6 | | ns |
| t _{su} | Setup time, data before CP↑ | 2 | | 2 | | 2 | | ns |
| t _h | Hold time, data after CP↑ | 1.5 | | 1.5 | | 1.5 | | ns |

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | CY74FCT574T | | CY74FCT574AT | | CY74FCT574CT | | UNIT |
|-----------------|--------------------------------|-------------|-----|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, CP high or low | 7 | | 5 | | 5 | | ns |
| t _{su} | Setup time, data before CP↑ | 2 | | 2 | | 2 | | ns |
| t _h | Hold time, data after CP↑ | 1.5 | | 1.5 | | 1.5 | | ns |

switching characteristics over operating free-air temperature range (see Figure 1)

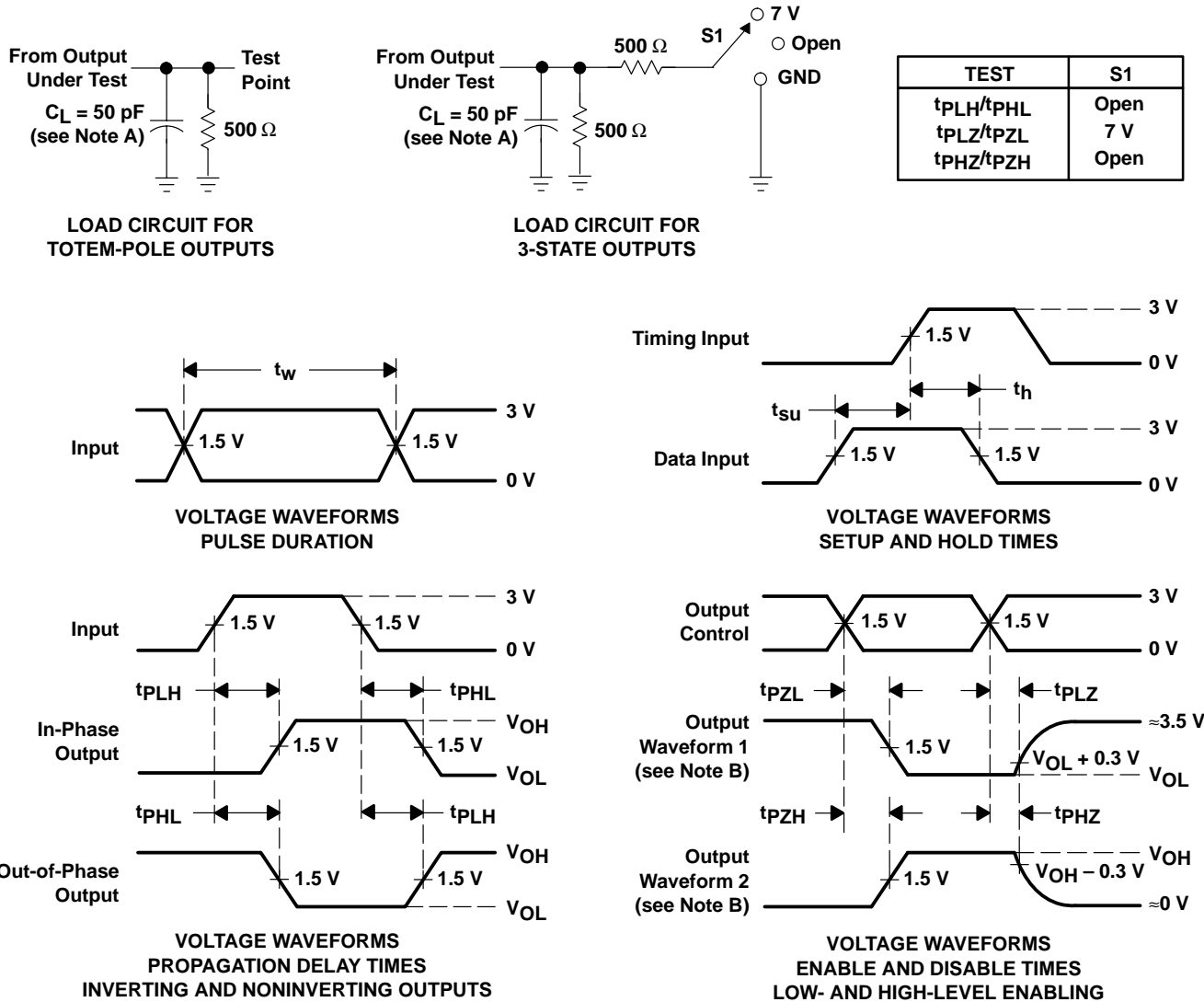
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY54FCT574T | | CY54FCT574AT | | CY54FCT574CT | | UNIT |
|------------------|-----------------|-------------|-------------|-----|--------------|-----|--------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | CP | O | 2 | 11 | 2 | 7.2 | 2 | 6.2 | ns |
| t _{PHL} | | | 2 | 11 | 2 | 7.2 | 2 | 6.2 | |
| t _{PZH} | \overline{OE} | O | 1.5 | 14 | 1.5 | 7.5 | 1.5 | 6.2 | ns |
| t _{PZL} | | | 1.5 | 14 | 1.5 | 7.5 | 1.5 | 6.2 | |
| t _{PHZ} | \overline{OE} | O | 1.5 | 8 | 1.5 | 6.5 | 1.5 | 5.7 | ns |
| t _{PLZ} | | | 1.5 | 8 | 1.5 | 6.5 | 1.5 | 5.7 | |

switching characteristics over operating free-air temperature range (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY74FCT574T | | CY74FCT574AT | | CY74FCT574CT | | UNIT |
|------------------|-----------------|-------------|-------------|------|--------------|-----|--------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | CP | O | 2 | 10 | 2 | 6.5 | 2 | 5.2 | ns |
| t _{PHL} | | | 2 | 10 | 2 | 6.5 | 2 | 5.2 | |
| t _{PZH} | \overline{OE} | O | 1.5 | 12.5 | 1.5 | 6.5 | 1.5 | 5.5 | ns |
| t _{PZL} | | | 1.5 | 12.5 | 1.5 | 6.5 | 1.5 | 5.5 | |
| t _{PHZ} | \overline{OE} | O | 1.5 | 8 | 1.5 | 5.5 | 1.5 | 5 | ns |
| t _{PLZ} | | | 1.5 | 8 | 1.5 | 5.5 | 1.5 | 5 | |



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--|-------------------------|
| 5962-9222203M2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9222203M2A CY54FCT 574ATLMB | Samples |
| 5962-9222203MRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9222203MR A | Samples |
| 5962-9222205MRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9222205MR A | Samples |
| CY54FCT574ATLMB | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9222203M2A CY54FCT 574ATLMB | Samples |
| CY74FCT574ATQCT | ACTIVE | SSOP | DBQ | 20 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT574A | Samples |
| CY74FCT574ATSOC | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT574A | Samples |
| CY74FCT574CTQCT | ACTIVE | SSOP | DBQ | 20 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT574C | Samples |
| CY74FCT574CTSOC | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT574C | Samples |
| CY74FCT574TQCT | ACTIVE | SSOP | DBQ | 20 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT574 | Samples |
| CY74FCT574TSOC | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT574 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CY74FCT574ATQCT | SSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT574CTQCT | SSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT574TQCT | SSOP | DBQ | 20 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CY74FCT574ATQCT | SSOP | DBQ | 20 | 2500 | 356.0 | 356.0 | 35.0 |
| CY74FCT574CTQCT | SSOP | DBQ | 20 | 2500 | 356.0 | 356.0 | 35.0 |
| CY74FCT574TQCT | SSOP | DBQ | 20 | 2500 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9222203M2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| CY54FCT574ATLMB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| CY74FCT574ATSOC | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CY74FCT574CTSOC | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| CY74FCT574TSOC | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |

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