

FEATURES

Ideal for driving high capacitive or low resistive loads
Wide supply range: 10 V to 40 V
High output current drive: 1 A
Wide output voltage swing: 37 V swing with 40 V supply
High slew rate: 2500 V/ μ s
High bandwidth: 52 MHz large signal, 70 MHz small signal
Low noise: 2.1 nV/ $\sqrt{\text{Hz}}$
Quiescent current: 32.5 mA
Power down: 0.75 mA
Short-circuit protection and flag
Current limit: 1.2 A

Thermal protection

APPLICATIONS

Envelope tracking
Power FET driver
Ultrasound
Piezo drivers
PIN diode drivers
Waveform generation
Automated test equipment (ATE)
CCD panel drivers
Composite amplifiers

GENERAL DESCRIPTION

The [ADA4870-KGD](#) is a unity-gain stable, high speed current feedback amplifier capable of delivering 1 A of output current and 2500 V/ μ s slew rate from a 40 V supply. Manufactured using the Analog Devices, Inc., proprietary high voltage extra fast complementary bipolar (XFCB) process, the innovative architecture of the [ADA4870-KGD](#) enables high output power, high speed signal processing solutions in applications that require driving a low impedance load.

The [ADA4870-KGD](#) is ideal for driving high voltage power FETs, piezo transducers, PIN diodes, CCD panels, and a variety of other demanding applications that require high speed from high supply voltage at high output current.

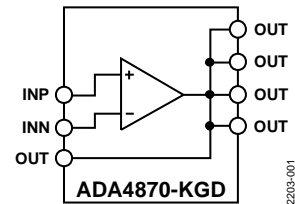
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

The [ADA4870-KGD](#) is available in a 26-pad bare die. The [ADA4870-KGD](#) operates over the industrial temperature range (-40°C to $+85^{\circ}\text{C}$).

Additional application and technical information can be found in the [ADA4870](#) data sheet.

Known Good Die (KGD): these die are fully guaranteed to data sheet specifications.

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REVISION HISTORY

10/14—Revision 0: Initial Version

SPECIFICATIONS

±20 V SUPPLY

$T_{CASE} = 25^{\circ}C$, $A_V = -5$, $R_F = 1.21\text{ k}\Omega$, $R_G = 243\ \Omega$, $C_L = 300\text{ pF}$, $R_S = 5\ \Omega$, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	$V_{OUT} = 2\text{ V p-p}$		60		MHz
	$V_{OUT} = 2\text{ V p-p}, A_V = +2$		70		MHz
	$V_{OUT} = 20\text{ V p-p}$		52		MHz
Slew Rate (Peak)	$V_{OUT} = 30\text{ V step}, A_V = +2$		2500		V/ μ s
Settling Time to 0.1%	$V_{OUT} = 10\text{ V step}$		82		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3	$f = 30\text{ MHz}, V_{OUT} = 20\text{ V p-p}, A_V = -10$		-40/-39		dBc
	$f = 1\text{ MHz}, V_{OUT} = 20\text{ V p-p}, A_V = -10$		-91/-74		dBc
	$f = 0.1\text{ MHz}, V_{OUT} = 20\text{ V p-p}, A_V = -10$		-95/-96		dBc
	$f = 1\text{ MHz}, V_{OUT} = 20\text{ V p-p}, R_L = 25\ \Omega, A_V = -10$		-70/-77		dBc
	$f = 0.1\text{ MHz}, V_{OUT} = 20\text{ V p-p}, R_L = 25\ \Omega, A_V = -10$		-79/-99		dBc
Input Voltage Noise Density	$f = 100\text{ kHz}$		2.1		nV/ $\sqrt{\text{Hz}}$
Input Current Noise Density	$f = 100\text{ kHz}$				
INP			4.2		pA/ $\sqrt{\text{Hz}}$
INN			47		pA/ $\sqrt{\text{Hz}}$
DC PERFORMANCE					
Input Offset Voltage		-15	-1	+10	mV
Input Offset Voltage Drift			4		μ V/ $^{\circ}C$
Input Bias Current					
Noninverting Input			9	23	μ A
Inverting Input			-12	-25	μ A
Input Bias Current Drift, Inverting Input			24		nA/ $^{\circ}C$
Open-Loop Transresistance			2.5		M Ω
INPUT CHARACTERISTICS					
Input Resistance	INP		2		M Ω
Input Capacitance	INP		0.75		pF
Input Common-Mode Voltage Range (V_{ICM})			± 18		V
Common-Mode Rejection Ratio	$V_{ICM} = \pm 2\text{ V}, \pm 18\text{ V}$	58	60		dB
\overline{SD} PIN (SHUTDOWN)					
Input Voltages	High (enabled)	$V_{EE} + 1.1$		$V_{EE} + 5$	V
	Low (power-down)	V_{EE}		$V_{EE} + 0.9$	V
Input Bias Current	Enabled ($\overline{SD} = V_{EE} + 5\text{ V}$)		110		μ A
	Power down ($\overline{SD} = V_{EE}$)		-50		μ A
\overline{ON} PIN (RESET AND SHORT-CIRCUIT PROTECTION)					
Input Voltages	High (power-down)	$V_{EE} + 1.8$		$V_{EE} + 5$	V
	Low (enabled)	V_{EE}		$V_{EE} + 1.3$	V
Input Bias Current	Enabled ($\overline{ON} = V_{EE}$)		-75		μ A
	Power down ($\overline{ON} = V_{EE} + 5\text{ V}$)		100		μ A
OUTPUT CHARACTERISTICS					
Output Voltage Range	$R_G = 1.2\text{ k}\Omega, R_L = \text{open}$		± 18.6		V
	$R_G = 1.2\text{ k}\Omega, R_L = 50\ \Omega$		± 18		V
Output Current Drive			1		A
Short-Circuit Protection Current Limit	$\overline{ON} = \text{floating}$		1.2		A

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		10		40	V
Quiescent Current	$\overline{SD} = V_{EE} + 5\text{ V}, \overline{ON} = V_{EE}$		32.5	33	mA
	$\overline{SD} = V_{EE}, \overline{ON} = \text{not applicable}$		0.75	1	mA
	$\overline{SD} = V_{EE} + 5\text{ V}, \overline{ON} = V_{EE} + 5\text{ V}$		5.1	5.8	mA
Positive Power Supply Rejection Ratio		67	69		dB
Negative Power Supply Rejection Ratio		62	64		dB

±5 V SUPPLY

T_{CASE} = 25°C, A_V = -5, R_F = 1.21 kΩ, R_G = 243 Ω, C_L = 300 pF, R_S = 5 Ω, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
-3 dB Bandwidth	V _{OUT} = 2 V p-p		52		MHz
Settling Time to 0.1%	V _{OUT} = 2 V step		55		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3	f = 30 MHz, V _{OUT} = 2 V p-p, A _V = -10		-42/-38		dBc
	f = 1 MHz, V _{OUT} = 2 V p-p, A _V = -10		-90/-88		dBc
	f = 0.1 MHz, V _{OUT} = 2 V p-p, A _V = -10		-101/-107		dBc
	f = 1 MHz, V _{OUT} = 2 V p-p, R _L = 25 Ω, A _V = -10		-70/-66		dBc
	f = 0.1 MHz, V _{OUT} = 2 V p-p, R _L = 25 Ω, A _V = -10		-85/-86		dBc
Input Voltage Noise Density	f = 100 kHz		2.1		nV/√Hz
Input Current Noise Density	f = 100 kHz		4.2		pA/√Hz
INP			47		pA/√Hz
INN					pA/√Hz
DC PERFORMANCE					
Input Offset Voltage		-15	-4	+5	mV
Input Offset Voltage Drift			14		μV/°C
Input Bias Current					
Noninverting Input			13	23	μA
Inverting Input			-5	-18	μA
Input Bias Current Drift, Inverting Input			10		nA/°C
Open-Loop Transresistance			1.9		MΩ
INPUT CHARACTERISTICS					
Input Resistance	INP		2		MΩ
Input Capacitance	INP		0.75		pF
Input Common-Mode Voltage Range (V _{ICM})			±3.0		V
Common-Mode Rejection Ratio	V _{ICM} = ±0.5 V, ±3.0 V	57	59		dB
SD PIN (SHUTDOWN)					
Input Voltages	High (enabled)	V _{EE} + 1.1		V _{EE} + 5	V
	Low (power-down)	V _{EE}		V _{EE} + 0.9	V
Input Bias Current	Enabled ($\overline{SD} = V_{EE} + 5\text{ V}$)		110		μA
	Power down ($\overline{SD} = V_{EE}$)		-65		μA
ON PIN (RESET AND SHORT-CIRCUIT PROTECTION)					
Input Voltages	High (power-down)	V _{EE} + 1.8		V _{EE} + 5	V
	Low (enabled)	V _{EE}		V _{EE} + 1.3	V
Input Bias Current	Enabled ($\overline{ON} = V_{EE}$)		-75		μA
	Power down ($\overline{ON} = V_{EE} + 5\text{ V}$)		100		μA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Voltage Range	$R_G = 1.2 \text{ k}\Omega$, $R_L = \text{open}$		± 3.7		V
Output Current Drive			1		A
Short-Circuit Protection Current Limit	$\overline{\text{ON}} = \text{floating}$		1.2		A
POWER SUPPLY					
Operating Range		10		40	V
Quiescent Current	$\overline{\text{SD}} = V_{EE} + 5 \text{ V}$, $\overline{\text{ON}} = V_{EE}$		28	30	mA
	$\overline{\text{SD}} = V_{EE}$, $\overline{\text{ON}} = \text{not applicable}$		0.65	1	mA
	$\overline{\text{SD}} = V_{EE} + 5 \text{ V}$, $\overline{\text{ON}} = V_{EE} + 5 \text{ V}$		4.7	5.5	mA
Positive Power Supply Rejection Ratio		66	68		dB
Negative Power Supply Rejection Ratio		61	63		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	42 V
Common-Mode Input Voltage Range	V_{EE} to V_{CC}
Differential Input Voltage Range	± 0.7 V
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+85^{\circ}\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

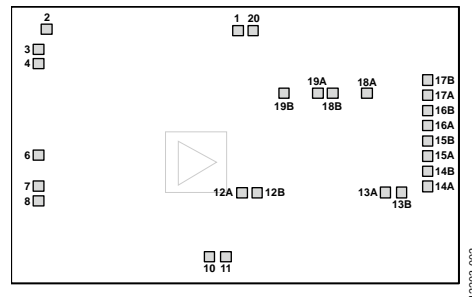


Figure 2. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
1	18.525	747.075	V _{CC}	Positive Power Supply Input
2	-1235.175	+751.875	TFL	Thermal Monitor and Short-Circuit Flag (Referenced to VEE)
3	-1286.125	+624.875	\overline{SD}	Shutdown (Active Low, Referenced to VEE)
4	-1286.525	+532.175	\overline{ON}	Turn On/Enable (Active Low, Referenced to VEE)
5	Not applicable	Not applicable	Not applicable	Not applicable
6	-1288.625	-65.725	INP	Noninverting Input
7	-1290.275	-272.175	INN	Inverting Input
8	-1290.275	-364.875	OUT	Output
9	Not applicable	Not applicable	Not applicable	Not applicable
10	-168.475	-732.375	V _{EE}	Negative Power Supply Input
11	-64.175	-732.325	V _{EE}	Negative Power Supply Input
12A	+46.125	-316.075	V _{EE}	Negative Power Supply Input
12B	+139.025	-316.075	V _{EE}	Negative Power Supply Input
13A	+1037.875	-316.025	V _{EE}	Negative Power Supply Input
13B	+1140.175	-316.025	V _{EE}	Negative Power Supply Input
14A	+1311.275	-272.125	OUT	Output
14B	+1311.275	-177.225	OUT	Output
15A	+1311.275	-82.975	OUT	Output
15B	1311.275	11.225	OUT	Output
16A	1311.275	106.675	OUT	Output
16B	1311.275	210.875	OUT	Output
17A	1311.275	314.225	OUT	Output
17B	1311.275	418.425	OUT	Output
18A	861.925	338.375	V _{CC}	Positive Power Supply Input
18B	636.425	336.725	V _{CC}	Positive Power Supply Input
19A	543.725	336.725	V _{CC}	Positive Power Supply Input
19B	320.675	337.225	V _{CC}	Positive Power Supply Input
20	119.125	747.075	V _{CC}	Positive Power Supply Input

OUTLINE DIMENSIONS

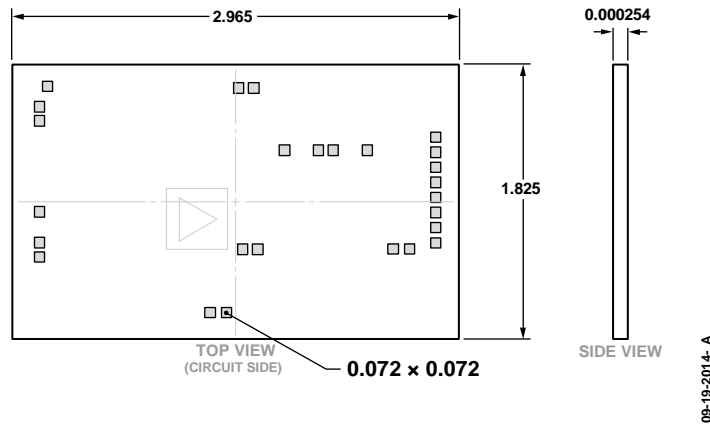


Figure 3. 26-Pad Bare Die [CHIP]
(C-26-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit
Scribe Line Width	75	μm
Die Size	2965 (x) \times 1825 (y)	μm
Thickness	10	mils
Backside	Ti 1000 Å, Ni 3000 Å, Au 1000 Å (Au outermost)	Not applicable
Passivation	5 μm Polyimide on top of 1 μm Oxynitride	Not applicable
Bond Pads (Minimum)	72 \times 72	μm
Bond Pad Composition	AlCu (0.5%)	%
ESD		
Human Body Model (HBM)	4	kV
Field-Induced Charged Device Model (FICDM)	1.25	kV

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Cookson D591-3B sintered Ag conductive
Minimum Bond Line Thickness	1.0 mils minimum
Bonding Sequence	Unspecified

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4870-KGD-DF	-40°C to +85°C	26-Pad Bare Die [CHIP]	C-26-1
ADA4870-KGD-WP	-40°C to +85°C	26-Pad Bare Die [CHIP]	C-26-1