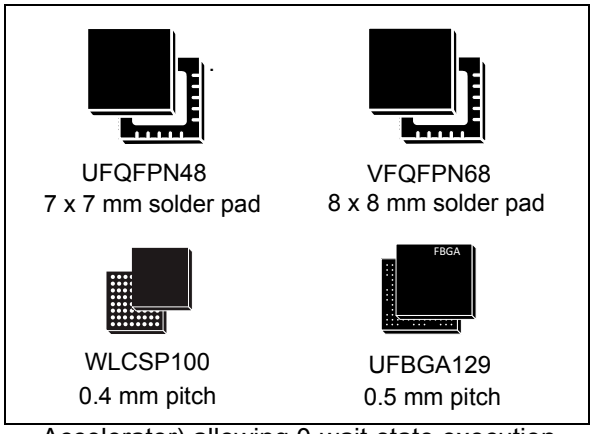
STM32WB55xx

Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M4 with FPU, Bluetooth® 5 and 802.15.4 radio solution

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology
- Radio
  - 2.4 GHz
  - RF transceiver supporting Bluetooth® 5 specification, IEEE 802.15.4-2011 PHY and MAC, supporting Thread and ZigBee® 3.0
  - RX sensitivity: -96 dBm (Bluetooth® Low Energy at 1 Mbps), -100 dBm (802.15.4)
  - Programmable output power up to +6 dBm with 1 dB steps
  - Integrated balun to reduce BOM
  - Support for 2 Mbps
  - Dedicated Arm® 32-bit Cortex® M0 + CPU for real-time Radio layer
  - Accurate RSSI to enable power control
  - Suitable for systems requiring compliance with radio frequency regulations ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66
  - Support for external PA
  - Available integrated passive device (IPD) companion chip for optimized matching solution (MLPF-WB55-01E3 or MLPF-WB55-02E3)
- Ultra-low-power platform
  - 1.71 to 3.6 V power supply
  - – 40 °C to 85 / 105 °C temperature ranges
  - 13 nA shutdown mode
  - 600 nA Standby mode + RTC + 32 KB RAM
  - 2.1 µA Stop mode + RTC + 256 KB RAM
  - Active-mode MCU: < 53 µA / MHz when RF and SMPS on
  - Radio: Rx 4.5 mA / Tx at 0 dBm 5.2 mA
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, adaptive real-time accelerator (ART Accelerator) allowing 0-wait-state execution from Flash memory, frequency up to 64 MHz, MPU, 80 DMIPS and DSP instructions



- Performance benchmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 219.48 CoreMark® (3.43 CoreMark/MHz at 64 MHz)
- Energy benckmark
  - 303 ULPMark™ CP score
- Supply and reset management
  - High efficiency embedded SMPS step-down converter with intelligent bypass mode
  - Ultra-safe, low-power BOR (brownout reset) with five selectable thresholds
  - Ultra-low-power POR/PDR
  - Programmable voltage detector (PVD)
  - V_{BAT} mode with RTC and backup registers
- Clock sources
  - 32 MHz crystal oscillator with integrated trimming capacitors (Radio and CPU clock)
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal low-power 32 kHz (±5%) RC (LSI1)
  - Internal low-power 32 kHz (stability ±500 ppm) RC (LSI2)

  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25% accuracy)
  - High speed internal 16 MHz factory trimmed RC (±1%)
  - 2x PLL for system clock, USB, SAI and ADC
- Memories
  - Up to 1 MB Flash memory with sector protection (PCROP) against R/W operations, enabling authentic Bluetooth® Low Energy and 802.15.4 SW stack
  - Up to 256 KB SRAM, including 64 KB with hardware parity check
  - 20x32-bit backup register
  - Boot loader supporting, USART, SPI, I2C and USB interfaces
  - OTA (over the air) Bluetooth® Low Energy and 802.15.4 update
  - Quad SPI memory interface with XIP
- Rich analog peripherals (down to 1.62 V)
  - 12-bit ADC 4.26 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x ultra-low-power comparator
  - Accurate 2.5 V or 2.048 V reference voltage buffered output
- System peripherals
  - Inter processor communication controller (IPCC) for communication with Bluetooth® Low Energy and 802.15.4
  - HW semaphores for resources sharing between CPUs
  - 2x DMA controllers (7x channels each) supporting ADC, SPI, I2C, USART, QSPI, SAI, AES, timers
  - 1x USART (ISO 7816, IrDA, SPI Master, Modbus and Smartcard mode)
  - 1x LPUART (low power)
  - 2x SPI 32 Mbit/s
  - 2x I2C (SMBus/PMBus)
  - 1x SAI (dual channel high quality audio)
  - 1x USB 2.0 FS device, crystal-less, BCD and LPM
  - Touch sensing controller, up to 18 sensors
  - LCD 8x40 with step-up converter
  - 1x 16-bit, four channels advanced timer
  - 2x 16-bits, two channels timer
  - 1x 32-bits, four channels timer
  - 2x 16-bits ultra-low-power timer
  - 1x independent Systick
  - 1x independent watchdog
  - 1x window watchdog
- Security and ID
  - Secure firmware installation (SFI) for Bluetooth® Low Energy and 802.15.4 SW stack
  - 3x hardware encryption AES maximum 256-bit for the application, the Bluetooth® Low Energy and IEEE802.15.4
  - Customer key storage / key manager services
  - HW public key authority (PKA)
  - Cryptographic algorithms: RSA, Diffie-Helman, ECC over GF(p)
  - True random number generator (RNG)
  - Sector protection against R/W operation (PCROP)
  - CRC calculation unit
  - Die information: 96-bit unique ID
  - IEEE 64-bit unique ID. Possibility to derive 802.15.4 64-bit and Bluetooth® Low Energy 48-bit EUI
- Up to 72 fast I/Os, 70 of them 5 V-tolerant
- Development support
  - Serial wire debug (SWD), JTAG for the Application processor
  - Application cross trigger with input / output
  - Embedded Trace Macrocell™ for application
- All packages are ECOPACK2 compliant

Table 1. Device summary

Reference	Part numbers
STM32WB55xx	STM32WB55CC, STM32WB55RC, STM32WB55VC STM32WB55CE, STM32WB55RE, STM32WB55VE STM32WB55CG, STM32WB55RG, STM32WB55VG

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WB55xx microcontrollers, based on Arm® cores[(a)].

This document must be read in conjunction with the STM32WB55xx reference manual (RM0434), available from the STMicroelectronics website *www.st.com*.

For information on the Arm® Cortex®-M4 and Cortex®-M0+ cores, refer, respectively, to the Cortex®-M4 Technical Reference Manual and to the Cortex®-M0+ Technical Reference Manual, both available on the www.arm.com website.

For information on 802.15.4 refer to the IEEE website (www.ieee.org).

For information on Bluetooth® refer to www.bluetooth.com.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32WB55xx multiprotocol wireless and ultra-low-power devices embed a powerful and ultra-low-power radio compliant with the Bluetooth® Low Energy SIG specification v5.0 and with IEEE 802.15.4-2011. They contain a dedicated Arm® Cortex® -M0+ for performing all the real-time low layer operation.

The STM32WB55xx devices are designed to be extremely low-power and are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 64 MHz. The Cortex®-M4 core features a Floating point unit (FPU) single precision that supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) that enhances application security.

Enhanced inter-processor communication is provided by the IPCC with six bidirectional channels. The HSEM provides hardware semaphores used to share common resources between the two processors.

The STM32WB55xx devices embed high-speed memories (up to 1 Mbyte of Flash memory, up to 256 Kbyte of SRAM), a Quad-SPI Flash memory interface (available on all packages) and an extensive range of enhanced I/Os and peripherals.

Direct data transfer between memory and peripherals and from memory to memory is supported by fourteen DMA channels with a full flexible channel mapping by the DMAMUX peripheral.

The STM32WB55xx devices embed several mechanisms for embedded Flash memory and SRAM: readout protection, write protection and proprietary code readout protection. Portions of the memory can be secured for Cortex® -M0+ exclusive access.

The two AES encryption engines, PKA and RNG enable lower layer MAC and upper layer cryptography. A customer key storage feature may be used to keep the keys hidden.

The devices offer a fast 12-bit ADC and two ultra-low-power comparators associated with a high accuracy reference voltage generator.

These devices embed a low-power RTC, one advanced 16-bit timer, one general-purpose 32-bit timer, two general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 18 capacitive sensing channels are available. The devices also embed an integrated LCD driver up to 8x40 or 4x44, with internal step-up converter.

The STM32WB55xx devices also feature standard and advanced communication interfaces, namely one USART (ISO 7816, IrDA, Modbus and Smartcard mode), one low- power UART (LPUART), two I2Cs (SMBus/PMBus), two SPIs (up to 32 MHz), one serial audio interface (SAI) with two channels and three PDMs, one USB 2.0 FS device with embedded crystal-less oscillator, supporting BCD and LPM and one Quad-SPI with execute-in-place (XIP) capability.

The STM32WB55xx operate in the -40 to +105 °C (+125 °C junction) and -40 to +85 °C (+105 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.

The STM32WB55xx include independent power supplies for analog input for ADC.

The STM32WB55xx integrate a high efficiency SMPS step-down converter with automatic bypass mode capability when the V_{DD} falls below V_{BORx} (x=1, 2, 3, 4) voltage level (default

is 2.0 V). It includes independent power supplies for analog input for ADC and comparators, as well as a 3.3 V dedicated supply input for USB.

A V_{BAT} dedicated supply allows the devices to back up the LSE 32.768KHz oscillator, the RTC and the backup registers, thus enabling the STM32WB55xx to supply these functions even if the main V_{DD} is not present through a CR2032-like battery, a Supercap or a small rechargeable battery.

The STM32WB55xx offers four packages, from 48 to 129 pins.

Table 2. STM32WB55xx devices features and peripheral counts

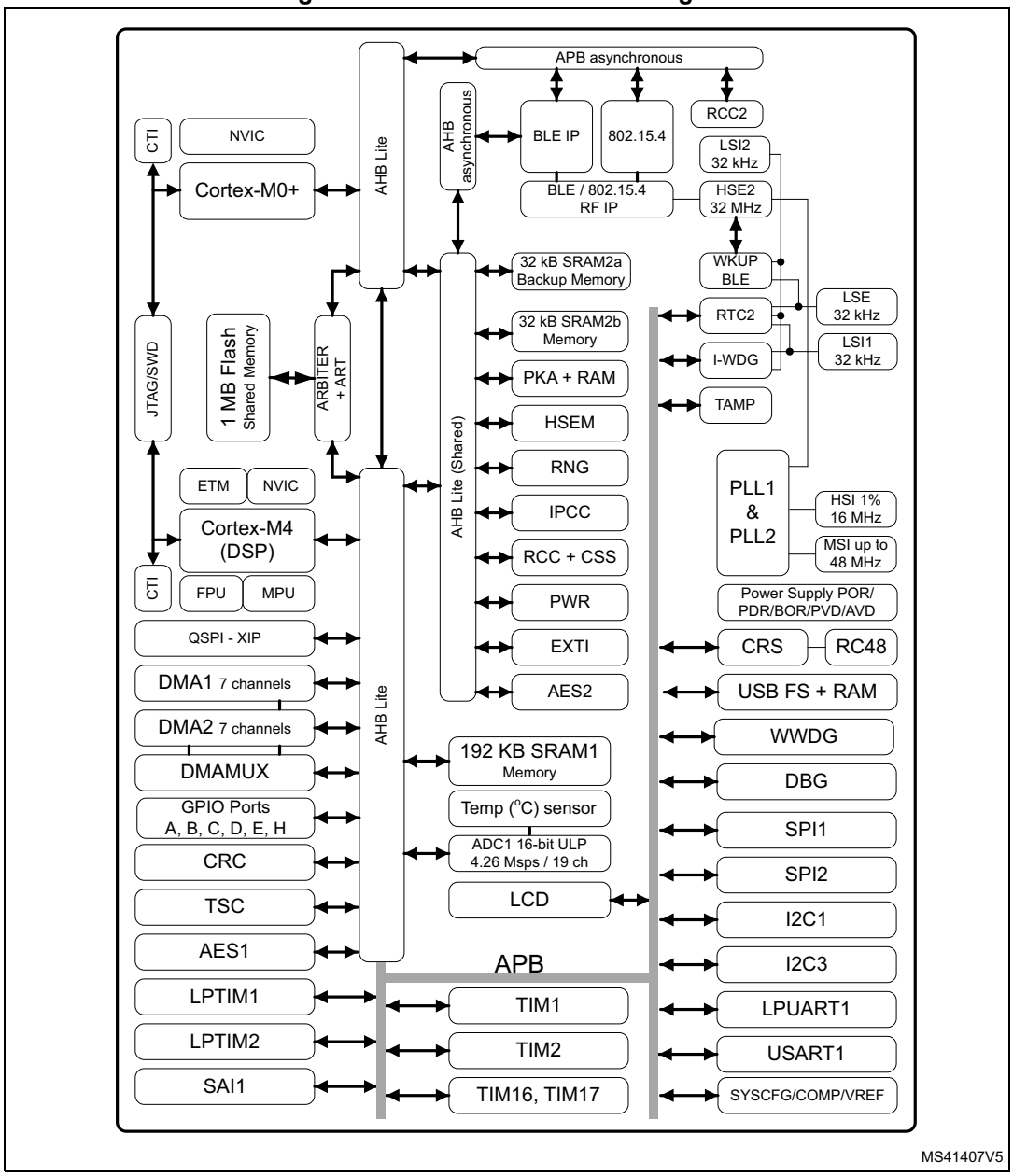
Feature		STM32WB55Cx			STM32WB55Rx			STM32WB55Vx		
Flash memory density		256 KB	512 KB	1 MB	256 KB	512 KB	1 MB	256 KB	512 KB	1 MB
SRAM density		128 KB	256 KB	256 KB	128 KB	256 KB	256 KB	128 KB	256 KB	256 KB
SRAM1		64 KB	192 KB		64 KB	192 KB		64 KB	192 KB	
SRAM2		64 KB								
BLE		V5.0 (2 Mbps)								
802.15.4		Yes								
Timers	Advanced	1 (16 bits)								
	General purpose	2 (16 bits) + 1 (32 bits)								
	Low power	2 (16 bits)								
	SysTick	1								
Comm interface	SPI	1			2					
	I2C	2								
	USART(1)	1								
	LPUART	1								
	SAI	2 channels								
	USB FS	Yes								
	QSPI	1								
RTC		1								
Tamper pin		1			3					
Wakeup pin		2			5					
LCD, COMxSEG		Yes, 4x13			Yes, 4x28			Yes, 8x40 or 4x44		
GPIOs		30			49			72		
Capacitive sensing		No			6			18		
12-bit ADC Number of channels		13 channels (incl. 3 internal)			19 channels (incl. 3 internal)					
Internal V_{ref}		Yes								
Analog comparator		2								
Max CPU frequency		64 MHz								

Table 2. STM32WB55xx devices features and peripheral counts (continued)

Feature	STM32WB55Cx	STM32WB55Rx	STM32WB55Vx
Operating temperature	Ambient :-40 to +85 and -40 to +105 °C Junction: -40 to +105 and -40 to +125 °C		
Operating voltage	1.71 to 3.6 V		
Package	UFQFPN48 7 mm x 7 mm 0.5 mm pitch, solder pad	VFQFPN68 8 mm x 8 mm 0.4 mm pitch, solder pad	WLCSP100 0.4 mm pitch UFBGA129 0.5 mm pitch

1. USART peripheral can be used as SPI.

Figure 1. STM32WB55xx block diagram



3 Functional overview

3.1 Architecture

The STM32WB55xx multiprotocol wireless devices embed a BLE and an 802.15.4 RF subsystem that interfaces with a generic microcontroller subsystem using an Arm® Cortex®-M4 CPU (called CPU1) on which the host application resides.

The RF subsystem is composed of a RF Analog Front end, BLE and 802.15.4 digital MAC blocks as well as of a dedicated Arm® Cortex®-M0+ microcontroller (called CPU2) plus some proprietary peripherals. The RF subsystem performs all of the BLE and 802.15.4 low layer stack, reducing the interaction with the CPU1 to high level exchanges.

Some functions are shared between the RF subsystem CPU (CPU2) and the Host CPU (CPU1):

- Flash memories
- SRAM1, SRAM2a and SRAM2b (SRAM2a can be retained in Standby mode)
- Security peripherals (RNG, AES1, PKA)
- Clock RCC
- Power control (PWR)

The communication and the sharing of peripherals between the RF subsystem and the Cortex®-M4 CPU is performed through a dedicated inter processor communication controller (IPCC) and semaphore mechanism (HSEM).

3.2 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is a processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32WB55xx are compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32WB55xx devices.

3.3 Memories

3.3.1 Adaptive real-time memory accelerator (ART Accelerator)

The ART Accelerator is a memory accelerator optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, that normally require the processor to wait for the Flash memory at higher frequencies.

To release the processor near 80 DMIPS performance at 64 MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 64 MHz.

3.3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU1 accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into eight subareas. The protection area sizes are between 32 bytes and the whole 4 Gbytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location prohibited by the MPU, the RTOS detects it and takes action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3.3 Embedded Flash memory

The STM32WB55xx devices feature up to1 Mbyte of embedded Flash memory available for storing programs and data, as well as some customer keys.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in SRAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex®-M4 and Cortex®-M0+ JTAG and serial wire), boot in SRAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status vs. readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from SRAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No(1)	No(1)	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(2)	No	No	N/A(2)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2a SRAM2b	1	Yes	Yes	Yes(2)	No	No	No(2)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. The option byte can be modified by the RF subsystem.
2. Erased when RDP changes from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 4 Kbyte granularity.
- Proprietary code readout protection (PCROP): two parts of the Flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. Two areas can be selected, with 2 KByte granularity. An additional option bit (PCROP_RDP) makes possible to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

A section of the Flash memory is secured for the RF subsystem CPU2, and cannot be accessed by the host CPU1.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection
- the address of the ECC fail can be read in the ECC register

The embedded Flash memory is shared between CPU1 and CPU2 on a time sharing basis. A dedicated HW mechanism allows both CPUs to perform Write/Erase operations.

3.3.4 Embedded SRAM

The STM32WB55xx devices feature upto 256 KB of embedded SRAM, split in three blocks:

- **SRAM1**: up to 192 KB mapped at address 0x2000 0000
- **SRAM2a**: 32 KB located at address 0x2003 0000 (contiguous to SRAM1) also mirrored at 0x1000 0000, with hardware parity check (this SRAM can be retained in Standby mode)
- **SRAM2b**: 32 KB located at address 0x2003 8000 (contiguous with SRAM2a) and mirrored at 0x1000 8000 with hardware parity check

SRAM2a and SRAM2b can be write-protected, with 1 KB granularity. A section of the SRAM2a and SRAM2b is secured for the RF sub-system and cannot be accessed by the host CPU1.

The SRAMs can be accessed in read/write with 0 wait states for all CPU1 and CPU2 clock speeds.

3.4 Security and safety

The STM32WB55xx contains many security blocks both for the BLE or IEEE 802.14.5 and the Host application.

It includes:

- Customer storage of the BLE and 802.14.5 keys
- Secure Flash memory partition for RF subsystem only access
- Secure SRAM partition, that can be accessed only by the RF subsystem
- True random number generator (RNG)
- Advance encryption standard hardware accelerators (AES-128bit and AES-256bit, supporting chaining modes ECB, CBC, CTR, GCM, GMAC, CCM)
- Private key acceleration (PKA) including:
  - Modular arithmetic including exponentiation with maximum modulo size of 3136 bits
  - Elliptic curves over prime field scalar multiplication, ECDSA signature, ECDSA verification with maximum modulo size of 521 bits
- Cyclic redundancy check calculation unit (CRC)

A specific mechanism is in place to ensure that all the code executed by the RF subsystem CPU2 can be secure, whatever the Host application. For the AES1 a customer key can be managed by the CPU2 and used by the CPU1 to encrypt/decrypt data.

3.5 Boot modes and FW update

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The STM32WB55xx always boot on CPU1 core. The embedded bootloader code makes it possible to boot from various peripherals:

- USB
- UART
- I2C
- SPI

Secure Firmware update (especially BLE and 802.15.4) from system boot and over the air is provided.

3.6 RF subsystem

The STM32WB55xx embed an ultra-low power multi-standard radio Bluetooth® Low Energy (BLE) and 802.15.4 network processor, compliant with Bluetooth® specification v5.0 and IEEE® 802.15.4-2011. The BLE features 1 Mbps and 2 Mbps transfer rates, supports multiple roles simultaneously acting at the same time as Bluetooth® Low Energy sensor and hub device, embeds Elliptic Curve Diffie-Hellman (ECDH) key agreement protocol, thus ensuring a secure connection.

The Bluetooth® Low Energy stack and 802.15.4 Low Level layer run on an embedded Arm® Cortex®-M0+ core (CPU2). The stack is stored on the embedded Flash memory, which is also shared with the Arm® Cortex®-M4 (CPU1) application, making it possible in-field stack update.

3.6.1 RF front-end block diagram

The RF front-end is based on a direct modulation of the carrier in Tx, and uses a low IF architecture in Rx mode.

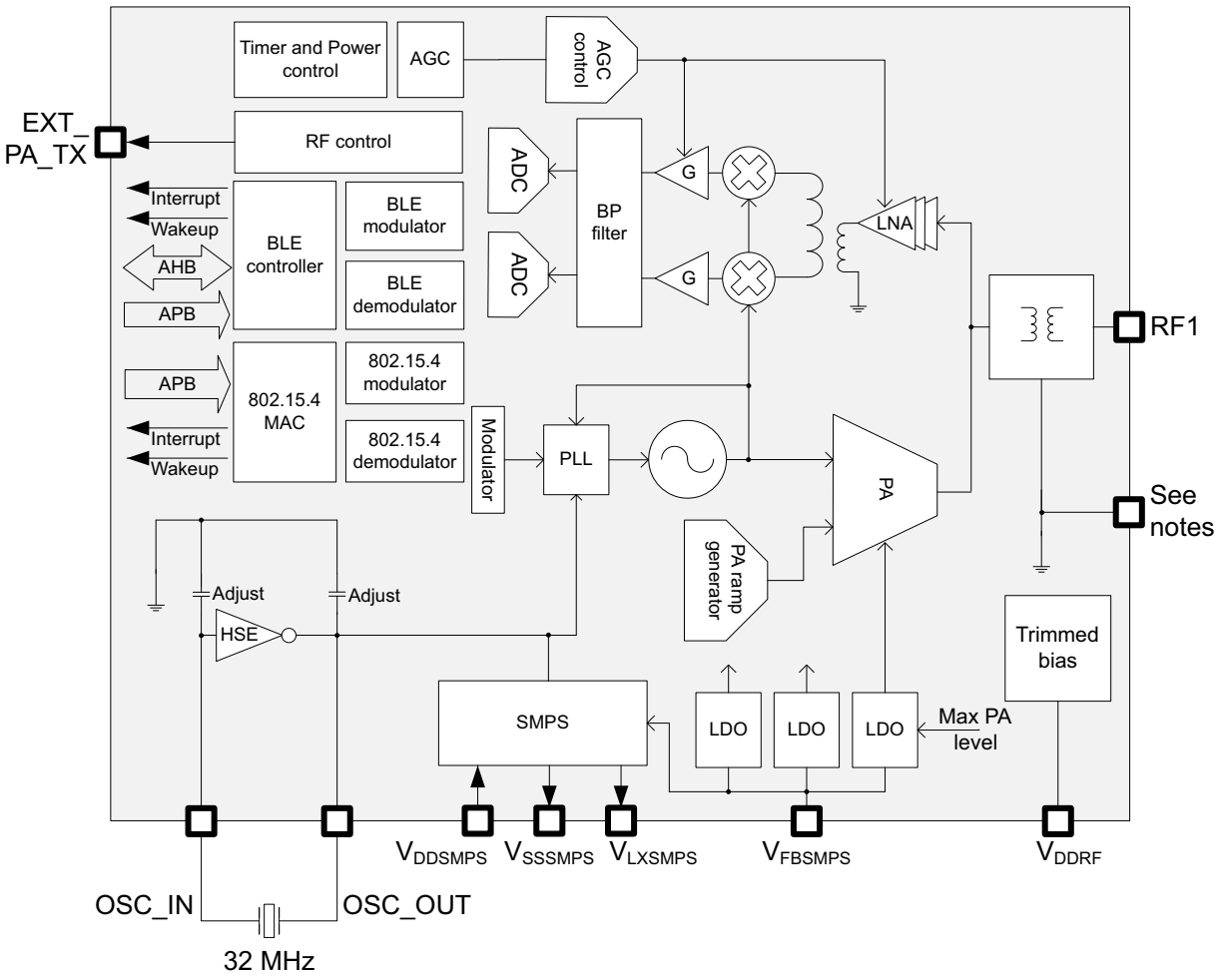
Thanks to an internal transformer at RF pins, the circuit directly interfaces the antenna (single ended connection, impedance close to 50 Ω). The natural bandpass behavior of the internal transformer, simplifies outside circuitry aimed for harmonic filtering and out of band interferer rejection.

In Transmit mode, the maximum output power is user selectable through the programmable LDO voltage of the power amplifier. A linearized, smoothed analog control offers clean power ramp-up.

In receive mode the circuit can be used in standard high performance or in reduced power consumption (user programmable). The Automatic gain control (AGC) is able to reduce the chain gain at both RF and IF locations, for optimized interferers rejection. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity and excellent linearity can be achieved.

The bill of material is reduced thanks to the high degree of integration. The radio frequency source is synthesized form an external 32 MHz crystal that does not need any external trimming capacitor network thanks to a dual network of user programmable integrated capacitors.

Figure 2. STM32WB55xx RF front-end block diagram



Notes:
- UFQFPN48 and VFQFPN68: V_{SS} through exposed pad, and V_{SSRF} pin must be connected to ground plane
- WLCSP100 and UFBGA129: V_{SSRF} pins must be connected to ground plane

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3.6.2 BLE general description

The BLE block is a master/slave processor, compliant with Bluetooth® specification 5.0 standard (2 Mbps).

It integrates a 2.4 GHz RF transceiver and a powerful Cortex®-M0+ core, on which a complete power-optimized stack for Bluetooth® Low Energy protocol runs, providing master / slave role support

- GAP: central, peripheral, observer or broadcaster roles
- ATT/GATT: client and server
- SM: privacy, authentication and authorization
- L2CAP
- Link layer: AES-128 encryption and decryption

In addition, according to Bluetooth® specification v5.0, the BLE block provides:

- Multiple roles simultaneously support
- Master/slave and multiple roles simultaneously
- LE data packet length extension (making it possible to reach 800 kbps at application level)
- LE privacy 1.2
- LE secure connections
- Flexible Internet connectivity options
- High data rate (2 Mbps)

The device allows the applications to meet the tight peak current requirements imposed by the use of standard coin cell batteries. When the high efficiency embedded SMPS step-down converter is used, the RF front end consumption (I_{tmax}) is only 8.1 mA at the highest output power (+6 dBm).

The power efficiency of the subsystem is optimized: while running with the radio and the applicative cores simultaneously using the SMPS, the Cortex®-M4 core consumption reaches 53 µA / MHz in active mode.

Ultra-low-power sleep modes and very short transition time between operating modes result in very low average current consumption during real operating conditions, resulting in longer battery life.

The BLE block integrates a full bandpass balun, thus reducing the need for external components.

The link between the Cortex®-M4 application processor (CPU1) running the application, and the BLE stack running on the dedicated Cortex®-M0+ (CPU2) is performed through a normalized API, using a dedicated IPCC.

3.6.3 802.15.4 general description

The STM32WB55xx embed a dedicated 802.15.4 hardware MAC:

- Support for 802.15.4 release 2011
- Advanced MAC frame filtering; hardwired firewall: Programmable filters based on source/destination addresses, frame version, security enabled, frame type
- 256-byte RX FIFO; Up to 8 frames capacity, additional frame information (timing, mean RSSI, LQI)
- 128-byte TX FIFO with retention
  - Content not lost, retransmissions possible under CPU2 control
- Automatic frame acknowledgment, with programmable delay
- Advanced channel access features
  - Full CSMA-CA support
  - Superframe timer
  - Beaconing support (require LSE)
  - Flexible TX control with programmable delay
- Configuration registers with retention available down to Standby mode for software/auto-restore
- Autonomous sniffer, Wakeup based on timer or CPU2 request
- Automatic frame transmission/reception/sleep periods, Interrupt to the CPU2 on particular events

3.6.4 RF pin description

The RF block contains dedicated pins, listed in *Table 4*.

Table 4. RF pin list

Name	Type	Description
RF1	I/O	RF Input/output, must be connected to the antenna through a low-pass matching network
OSC_OUT		32 MHz main oscillator, also used as HSE source
OSC_IN		
RF_TX_ MOD_EXT_PA		External PA transmit control
VDDRF	V_{DD}	Dedicated supply, must be connected to V_{DD}
VSSRF(1)	V_{SS}	To be connected to GND

1. On packages with exposed pad, this pad must be connected to GND plane for correct RF operation.

3.6.5 Typical RF application schematic

The schematic in *Figure 3* and the external components listed in *Table 4* are purely indicative. For more details refer to the “Reference design” provided in separate documents.

Figure 3. STM32WB55xx external components for the RF part

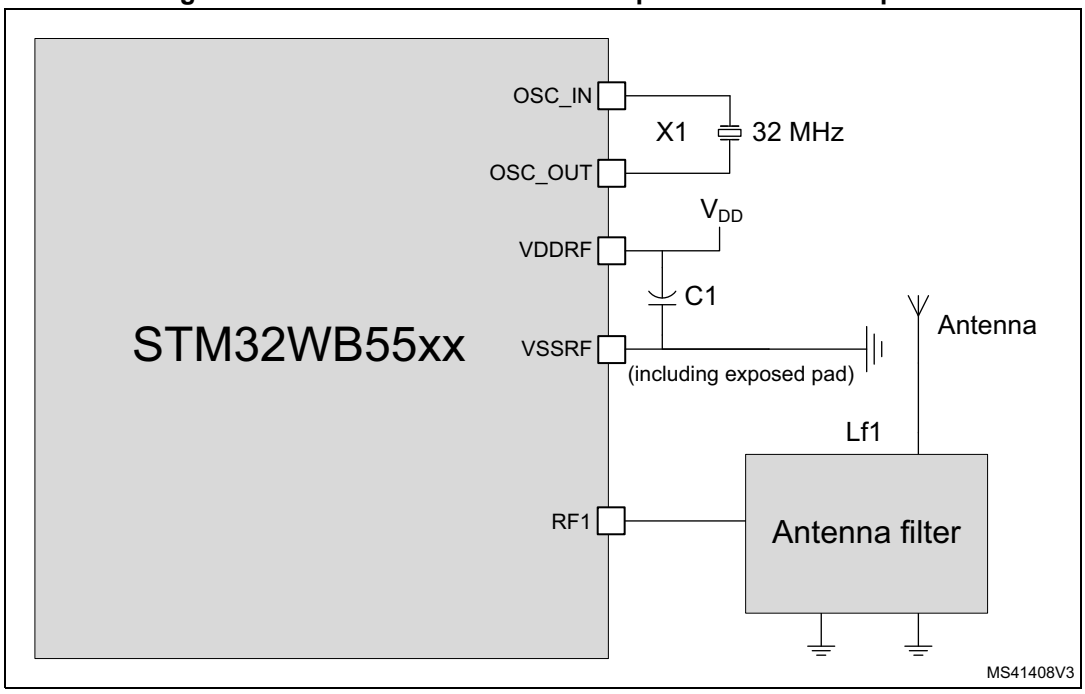


Table 5. Typical external components

Component	Description	Value
C1	Decoupling capacitance for RF	100 nF // 100 pF
X1	32 MHz crystal(1)	32 MHz
Antenna filter	Antenna filter and matching network	Refer to AN5165, on *www.st.com*
Antenna	2.4 GHz band antenna	-

1. e.g. NDK reference: NX2016SA 32 MHz EXS00A-CS06654.

3.7 Power supply management

3.7.1 Power supply distribution

The device integrate an SMPS step-down converter to improve low power performance when the V_{DD} voltage is high enough. This converter has an intelligent mode that automatically enters in bypass mode when the V_{DD} voltage falls below a specific BORx (x = 1, 2, 3 or 4) voltage.

By default, at Reset the SMPS is in bypass mode.

The device can be operated without the SMPS by just wiring its output to V_{DD}. This is the case for applications where the voltage is low, or where the power consumption is not critical.

Figure 4. Power distribution

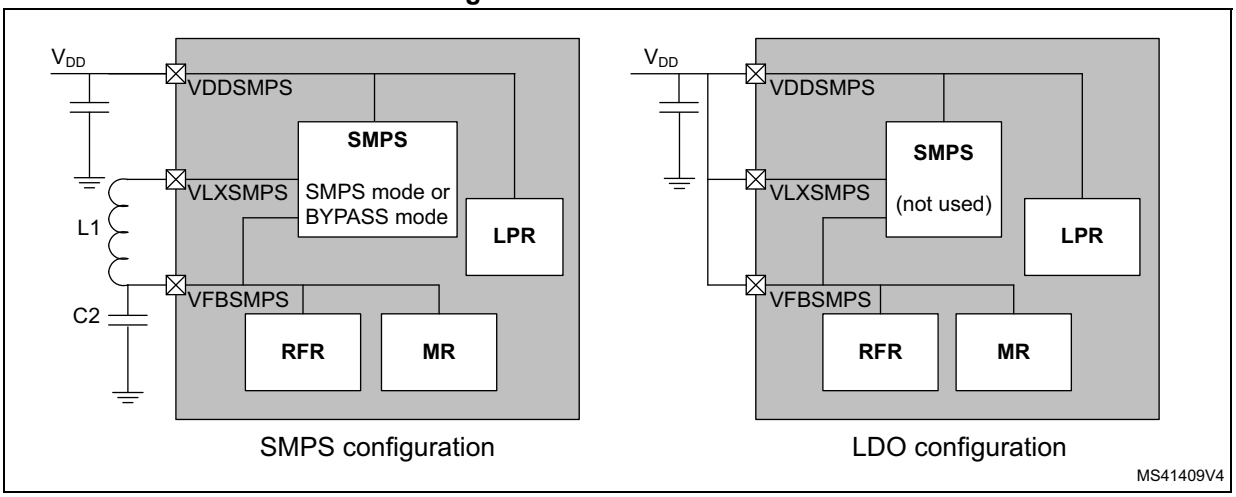


Table 6. Power supply typical components

Component	Description		Value
C2	SMPS output capacitor(1)		4.7 µF
L1(2)	SMPS inductance	For 8 MHz(3)	2.2 µH
		For 4 MHz(4)	10 µH

1. e.g. GRM155R60J475KE19.
2. An extra 10 nH inductor in series with L1 is needed to improve the receiver performance, e.g Murata LQG15WZ10NJ02D
3. e.g. Wurth 74479774222.
4. e.g. Murata LQM21FN100M70L.

The SMPS can also be switched on or set in bypass mode at any time by the application software, for example when very accurate ADC measurement are needed.

3.7.2 Power supply schemes

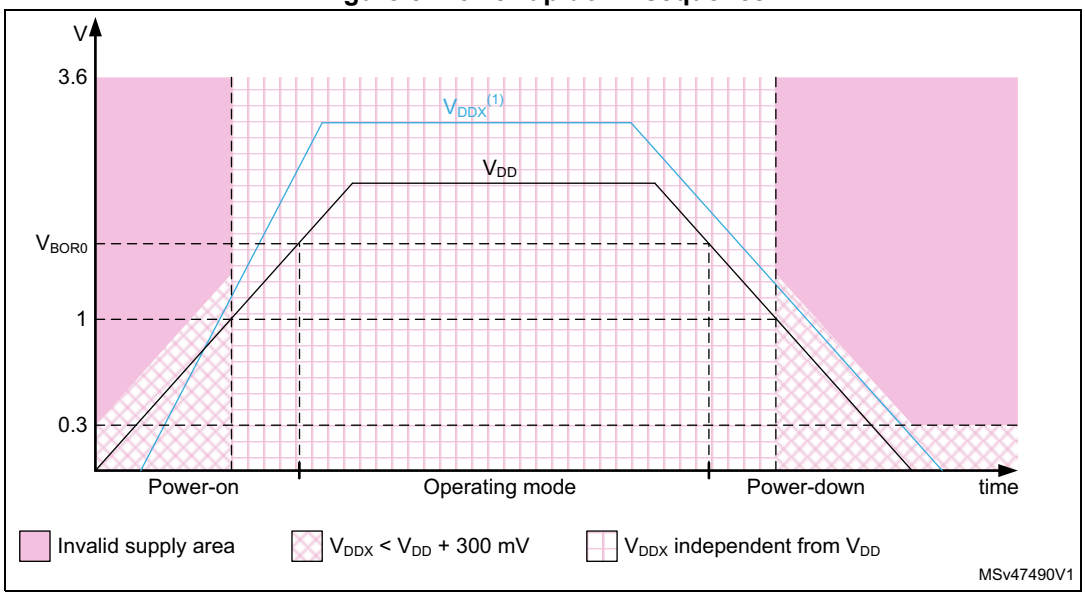
The STM32WB55xx devices have different voltage supplies (see *Figure 6*) and can operate within the following voltage ranges:

- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO}), the internal regulator and system functions such as RF, SMPS, reset, power management and internal clocks. It is provided externally through VDD pins. V_{DDRF} and V_{DDSMPS} must be always connected to VDD pins.
- V_{DDA} = 1.62 (ADC/COMPs) to 3.6 V: external analog power supply for ADC, comparators and voltage reference buffer. The V_{DDA} voltage level can be independent from the V_{DD} voltage. When not used V_{DDA} must be connected to V_{DD}.
- V_{DDUSB} = 3.0 to 3.6 V: external independent power supply for USB transceivers. When not used V_{DDUSB} must be connected to V_{DD}.
- V_{LCD} = 2.5 to 3.6 V: the LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter. This converter can generate a V_{LCD} voltage up to 3.6 V if V_{DD} is higher than 2.0 V.

During power up/ down, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V the other power supplies (V_{DDA}, V_{DDUSB}, V_{LCD}), must remain below V_{DD} + 300 mV
- When V_{DD} is above 1 V all power supplies are independent.

Figure 5. Power-up/down sequence

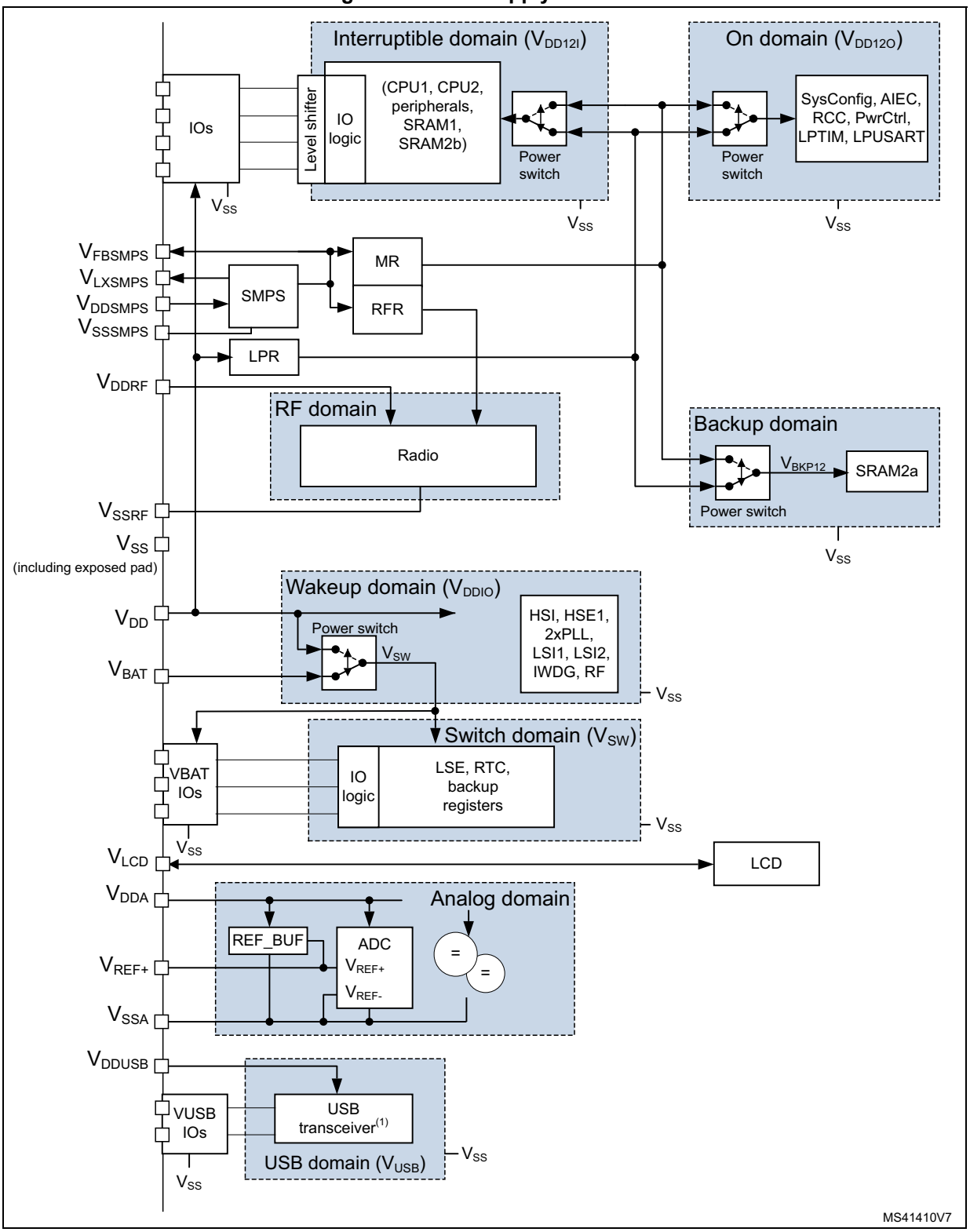


1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDUSB} and V_{LCD}.

During the power down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows the external decoupling capacitors to be discharged with different time constants during the power down transient phase.

Note: V_{DD}, V_{DDRF} and V_{DDSMPS} must be wired together, so they follow the same voltage sequence.

Figure 6. Power supply overview



1. The USB transceiver is powered by V_{DDUSB}, and the GPIOs associated with USB are powered by V_{DDUSB} when USB alternate function (PA11 and PA12) is selected. When USB alternate function is not selected the GPIOs associated with USB are powered as standard GPIOs.

3.7.3 Linear voltage regulator

Three embedded linear voltage regulators supply most of the digital and RF circuitries, the main regulator (MR), the low-power regulator (LPR) and the RF regulator (RFR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the SRAM2a in Standby with retention.
- The RFR is used to supply the RF analog part, its activity is automatically managed by the RF subsystem.

All the regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down, inducing zero consumption.

The ultralow-power STM32WB55xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

There are two voltage and frequency ranges:

- Range 1, with the CPU running up to 64 MHz
- Range 2, with a maximum CPU frequency of 16 MHz (note that HSE can be active in this mode). All peripheral clocks are also limited to 16 MHz.

VCORE can also be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode. In this case the CPU is running at up to 2 MHz, and peripherals with independent clock can be clocked by HSI16 (in this mode the RF subsystem is not available).

3.7.4 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor (PVM) that compares the independent supply voltage V_{DDA} with a fixed threshold to ensure that the peripheral is in its functional supply range.

Any BOR level can also be used to automatically switch the SMPS step-down converter in bypass mode when the V_{DD} voltage drops below a given voltage level. The mode of operation is selectable by register bit, the BOR level is selectable by option byte.

3.7.5 Low-power modes

The ultra-low-power STM32WB55xx support eight low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources.

By default, the microcontroller is in Run mode, Range 1, after a system or a power on Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep**

  In Sleep mode, only the CPU1 is stopped. All peripherals, including the RF subsystem, continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run**

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator operating current. The code can be executed from SRAM or from the Flash memory, and the CPU1 frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16. The RF subsystem is not available in this mode and must be OFF.

- **Low-power sleep**

  This mode is entered from the low-power run mode. Only the CPU1 clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode. The RF subsystem is not available in this mode and must be OFF.

- **Stop 0, Stop 1 and Stop 2**

  Stop mode achieves the lowest power consumption while retaining the content of all the SRAM and registers. The LSE (or LSI) is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  In these modes the RF subsystem can wait for incoming events in all Stop modes 0, 1, and 2.

  The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16 if the RF subsystem is disabled. If the RF subsystem or the SMPS is used the exits must be set to HSI16 only. If used, the SMPS is restarted automatically.

- **Standby**

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off.

  The RTC can remain active (Standby mode with RTC).

  The brown-out reset (BOR) always remains active in Standby mode.

  The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1, SRAM2b and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2a can be retained in Standby mode, supplied by the low-power Regulator (Standby with 32 KB SRAM2a retention mode).

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm,

periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE, or from the RF system wakeup).

The system clock after wakeup is 16 MHz, derived from the HSI16. If used, the SMPS is restarted automatically.

In this mode the RF can be used.

- **Shutdown**

  The Shutdown mode allows to achieve the ultimate lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2a, SRAM2b and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is 4 MHz, derived from the MSI.

  In this mode the RF is no longer operational.

When the RF subsystem is active, it will change the power state according to its needs (Run, Stop, Standby). This operation is transparent for the CPU1 host application and managed by a dedicated HW state machine. At any given time the effective power state reached is the higher one needed by both the CPU1 and RF sub-system.

Table 7 summarizes the peripheral features over all available modes. Wakeup capability is detailed in gray cells.

Table 7. Features over all modes(1)

Peripheral	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU1	Y		-	Y	-	-	-	-	-	-	-	-	-	-
CPU2	Y		-	Y	-	-	-	-	-	-	-	-	-	-
Radio system (BLE, 802.15.4)	Y	Y(2)	Y	-	-	Y	Y	Y	Y	Y(3)	Y(3)			
Flash memory (up to 1 MB)	Y (4)		Y	O(5)	O(5)	R	-	R	-	R	-	R	-	R
SRAM1 (up to 192 KB)	Y		Y(6)	Y	Y(6)	R	-	R	-	-	-	-	-	-
SRAM2a (32 KB)	Y		Y(6)	Y	Y(6)	R	-	R	-	R(7)	-	-	-	-
SRAM2b (32 KB)	Y		Y(6)	Y	Y(6)	R	-	R	-	-	-	-	-	-
Quad-SPI	O		O	O	O	-	-	-	-	-	-	-	-	-
Backup registers	Y		Y	Y	Y	R	-	R	-	R	-	R	-	R

Table 7. Features over all modes[1] (continued)

Peripheral	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Brown-out reset (BOR)	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O		O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor PVMx (x=1, 3)	O		O	O	O	O	O	O	O	-	-	-	-	-
SMPS	O		O	O	O	O[8]	-	-	-	-	-	-	-	-
DMAx (x = 1, 2)	O		O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O		O	O	O	O[9]	-	O[9]	-	-	-	-	-	-
Oscillator HSI48	O		O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)[10]	O		O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI1 or LSI2)	O		O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O		O	O	O	O	-	O	-	O	-	O	-	O
Multi-speed internal (MSI)[11]	48	24	O	48	O	-	-	-	-	-	-	-	-	-
PLLx VCO maximum frequency	344	128	O	-	-	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O		O	O	O	O	O[12]	O	O[12]	-	-	-	-	-
Clock security system on LSE	O		O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O		O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC tamper pins	3		3	3	3	3	O	3	O	3	O	3	O	3
LCD	O		O	O	O	O	O	O	O	-	-	-	-	-
USB FS	O	-	O	-	-	-	O	-	-	-	-	-	-	-
USART1	O		O	O	O	O[13]	O[13]	-	-	-	-	-	-	-
Low-power UART (LPUART1)	O		O	O	O	O[13]	O[13]	O[13]	O[13]	-	-	-	-	-
I2C1	O		O	O	O	O[14]	O[14]	-	-	-	-	-	-	-
I2C3	O		O	O	O	O[14]	O[14]	O[14]	O[14]	-	-	-	-	-
SPIx (x=1, 2)	O		O	O	O	-	-	-	-	-	-	-	-	-

Table 7. Features over all modes[1] (continued)

Peripheral	Run Range 1	Run Range 2	Sleep	Low-power run	Low-power sleep	Stop0/Stop1		Stop 2		Standby		Shutdown		VBAT
						-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
SAI1	O		O	O	O	-	-	-	-	-	-	-	-	-
ADC1	O		O	O	O	-	-	-	-	-	-	-	-	-
VREFBUF	O		O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1, 2)	O		O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O		O	O	O	-	-	-	-	-	-	-	-	-
Timers TIMx (x=1, 2, 16, 17)	O		O	O	O	-	-	-	-	-	-	-	-	-
Low-power Timer 1 (LPTIM1)	O		O	O	O	O	O	O	O	-	-	-	-	-
Low-power Timer 2 (LPTIM2)	O		O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O		O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O		O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O		O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O		O	O	O	-	-	-	-	-	-	-	-	-
True random number generator (RNG)	O	-	O	-	-	-	-	-	-	-	-	-	-	-
AES2 hardware accelerator	O		O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O		O	O	O	-	-	-	-	-	-	-	-	-
IPCC	O		-	O	-	-	-	-	-	-	-	-	-	-
HSEM	O		-	O	-	-	-	-	-	-	-	-	-	-
PKA	O		O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O		O	O	O	O	O	O	O	(15)	5 pins	(16)	5 pins	-

1. Legend: Y = Yes (Enabled), O = Optional (Disabled by default, can be enabled by software), R = Data retained, - = Not available.
2. Bluetooth® Low Energy not possible in this mode.
3. Standby with SRAM2a retention mode only.
4. Flash memory programming only possible in Range 1 voltage, not in Range 2 and not in Low Power mode.
5. The Flash memory can be configured in Power-down mode. By default, it is not in Power-down mode.
6. The SRAM clock can be gated on or off.

7. SRAM2a content is preserved when the bit RRS is set in PWR_CR3 register.
8. Stop 0 only. SMPS is automatically switched to Bypass or Open mode during Low power operation.
9. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
10. The HSE can be used by the RF subsystem according with the need to perform RF operation (Tx or Rx).
11. MSI maximum frequency.
12. In case RF will be used and HSE will fail.
13. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
14. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
15. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
16. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

Table 8. STM32WB55xx modes overview

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and Peripherals	Wakeup source	Consumption(1)	Wakeup time
Run	Range 1	Yes	ON(2)(3)	ON	Any	All	N/A	107 µA/MHz	N/A
	Range 2					All except RNG and USB-FS		100 µA/MHz	
LPRun	LPR	Yes	ON(2)	ON	Any except PLL	All except RF, RNG and USB-FS	N/A	103 µA/MHz	15.33 µs
Sleep	Range 1	No	ON(2)	ON(4)	Any	All	Any interrupt or event	41 µA/MHz	9 cycles
	Range 2					All except RNG and USB-FS		46 µA/MHz	
LPSleep	LPR	No	ON(2)	ON(4)	Any except PLL	All except RF, RNG and USB-FS	Any interrupt or event	45 µA/MHz	9 cycles
Stop 0	Range 1	No	OFF	ON	LSE, LSI, HSE(5), HSI16(6)	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1(7) LPUART1(7) I2Cx (x=1, 3)(8) LPTIMx (x=1, 2), SMPS All other peripherals are frozen.	Reset pin, all I/Os, RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	100 µA	1.7 µs
	Range 2								
Stop 1	LPR	No	OFF	ON	LSE, LSI, HSE(5), HSI16(6)	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1(7) LPUART1(7) I2Cx (x=1, 3)(8) LPTIMx (x=1, 2) All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) USART1 LPUART1 I2Cx (x=1, 3) LPTIMx (x=1, 2) USB	9.2 µA w/o RTC 9.6 µA w RTC	4.7 µs

Table 8. STM32WB55xx modes overview (continued)

Mode	Regulator	CPU1	Flash	SRAM	Clocks	DMA and Peripherals	Wakeup source	Consumption(1)	Wakeup time
Stop 2	LPR	No	OFF	ON	LSE, LSI	RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1(7) I2C3(8) LPTIM1 All other peripherals are frozen.	Reset pin, all I/Os RF, BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1, 2) LPUART1 I2C3 LPTIM1	1.85 µA w/o RTC 2.1 µA w RTC	5.71 µs
Standby	LPR	No	OFF	SRAM2a ON(9)	LSE, LSI	RF, BOR, RTC, IWDG All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down	RF, Reset pin 5 I/Os (WKUPx)(10) BOR, RTC, IWDG	0.32 µA w/o RTC 0.60 µA w RTC	51 µs
	OFF			OFF				0.11 µA w/o RTC 0.390 µA w RTC	
Shutdown	OFF	No	OFF	OFF	LSE	RTC All other peripherals are powered off. I/O configuration can be floating, pull-up or pull-down(11)	5 I/Os (WKUPx)(10), RTC	0.028 µA w/o RTC 0.315 µA w/ RTC	-

1. Typical current at V_{DD} = 1.8 V, 25 °C. for STOPx, SHUTDOWN and Standby, else V_{DD} = 3.3 V, 25 °C.
2. The Flash memory controller can be placed in power-down mode if the RF subsystem is not in use and all the program is run from the SRAM.
3. Flash memory programming is only possible in Range 2 voltage.
4. The SRAM1 and SRAM2 clocks can be gated off independently.
5. HSE (32 MHz) automatically used when RF activity is needed by the RF subsystem.
6. HSI16 (16 MHz) automatically used by some peripherals.
7. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, Address match or Received frame event.
8. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
9. SRAM1 and SRAM2b are OFF.
10. I/Os with wakeup from Standby/Shutdown capability: PA0, PC13, PC12, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating but the configuration is lost immediately when exiting the Shutdown mode.

3.7.6 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.8 VBAT operation

The VBAT pin allows to power the device VBAT domain (RTC, LSE and Backup registers) from an external battery, an external supercapacitor, or from V_{DD} when no external battery nor an external supercapacitor are present. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied only from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.9 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU1 resources and, consequently, reducing power supply consumption. In addition, these hardware connections result in fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, low-power run and sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 9. STM32WB55xx CPU1 peripherals interconnect matrix

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1 TIM2	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y(1)
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-

Table 9. STM32WB55xx CPU1 peripherals interconnect matrix (continued)

Source	Destination	Action	Run	Sleep	Low-power run	Low-power	Stop 0 / Stop 1	Stop 2
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y(1)
All clocks sources (internal and external)	TIM2 TIM16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) SRAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1 TIM16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y(1)
	ADC1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.10 Clocks and startup

The STM32WB55xx devices integrate many sources of clocks:

- LSE: 32.768KHz external oscillator, for accurate RTC and calibration with other embedded RC oscillators
- LSI1: 32 KHz on-chip low-consumption RC oscillator
- LSI2: almost 32 KHz on-chip high-stability RC oscillator, used by the RF subsystem
- HSE: high quality 32 MHz external oscillator with trimming, needed by the RF subsystem
- HSI16: 16 MHz high accuracy on-chip RC oscillator
- MSI: 100 KHz to 48 MHz multiple speed on-chip low power oscillator, can be trimmed using the LSE signal
- HSI48: 48 MHz on-chip RC oscillator, for USB crystal-less purpose

The clock controller (see *Figure 7*) distributes the clocks coming from the different oscillators to the core and the peripherals including the RF subsystem. It also manages clock gating for low power modes and ensures clock robustness. It features:

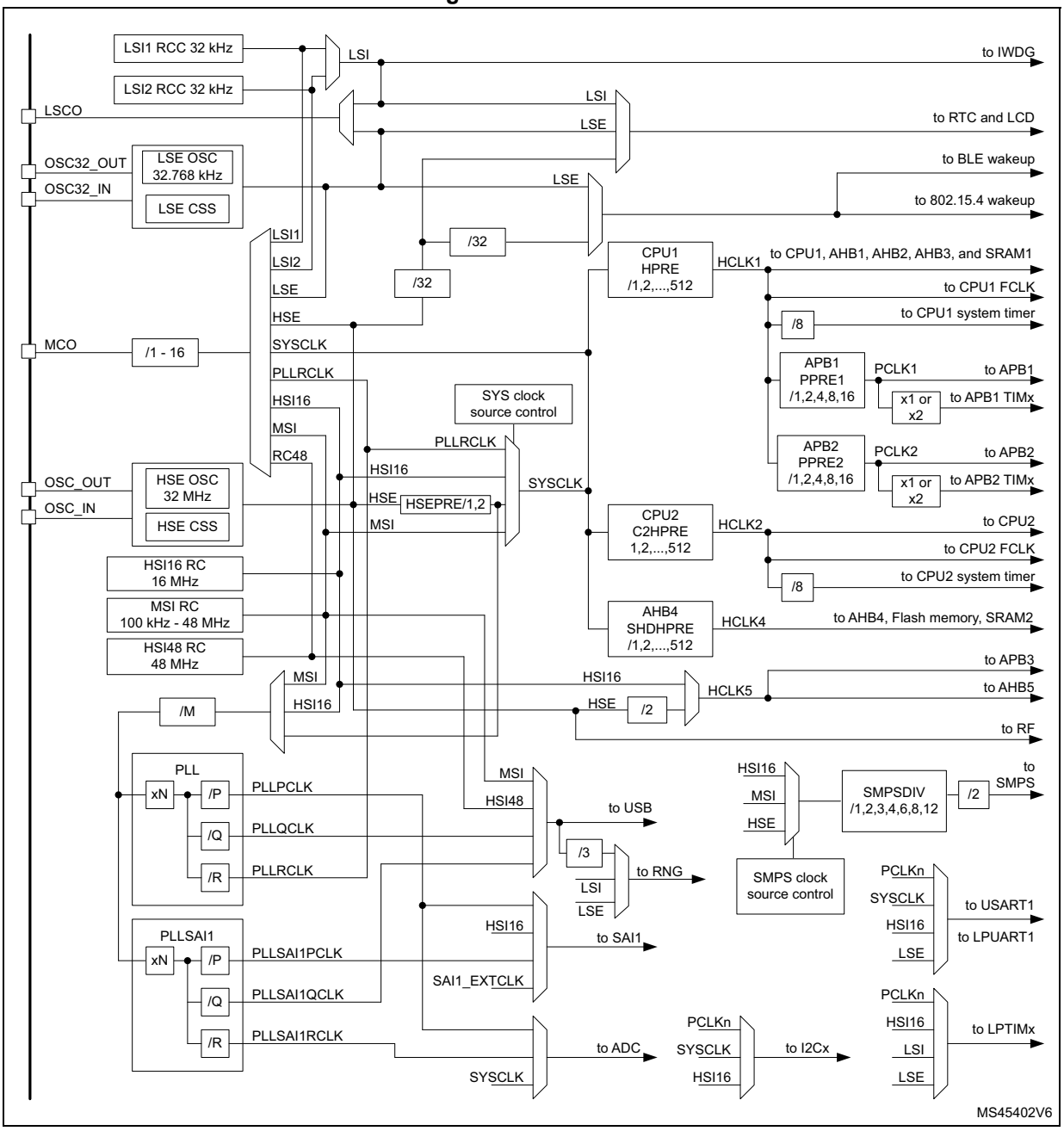
- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. The MSI can supply a PLL.
  - System PLL that can be fed by HSE, HSI16 or MSI, with a maximum frequency of 64 MHz.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5%. The LSI source can be either the LSI1 or the LSI2 on-chip oscillator.
- **Peripheral clock sources:** Several peripherals (RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Two PLLs, each

having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the RNG and the SAI.

- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software interrupt is generated if enabled. LSE failure can also be detected and an interrupt generated.
- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSIx, LSE) are available down to Stop 1 low power state.
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby.

Several prescalers allow the user to configure the AHB frequencies, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 64 MHz.

Figure 7. Clock tree



3.11 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.12 Direct memory access controller (DMA)

The device embeds two DMAs. Refer to *Table 10: DMA implementation* for the features implementation.

Direct memory access (DMA) is used to provide high-speed data transfer between peripherals and memory as well as between memories. Data can be quickly moved by DMA without any CPU action. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, a full cross matrix allows any peripheral to be mapped on any of the available DMA channels. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- fourteen independently configurable channels (requests)
- A full cross matrix between peripherals and all the DMA channels exist. There is also a HW trigger possibility through the DMAMUX.
- Priorities between requests from channels of one DMA are software programmable (four levels consisting in very high, high, medium and low) or hardware in case of equality (request 1 has priority over request 2, etc.).
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management.
- Three event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically OR-ed together in a single interrupt request for each channel.
- Memory-to-memory transfer.
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers.
- Access to Flash memory, SRAM, APB and AHB peripherals as source and destination.
- Programmable number of data to be transferred: up to 65536.

Table 10. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

A DMAMUX block makes it possible to route any peripheral source to any DMA channel.

3.13 Interrupts and events

3.13.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 63 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.13.2 Extended interrupts and events controller (EXTI)

The EXTI manages wakeup through configurable and direct event inputs. It provides wake-up requests to the Power control, and generates interrupt requests to the CPUx NVIC and events to the CPUx event input.

Configurable events/interrupts come from peripherals able to generate a pulse, and make it possible to select the Event/Interrupt trigger edge and/or a SW trigger.

Direct events/interrupts are coming from peripherals having their own clearing mechanism.

3.14 Analog to digital converter (ADC)

The device embeds a successive approximation analog-to-digital converter with the following features:

- 12-bit native resolution, with built-in calibration
- Up to 16-bit resolution with 64 decimation ratio
- 4.26 Msps maximum conversion rate with full resolution
  - Down to 39 ns sampling time
  - Increased conversion rate for lower resolution (up to 7.11 Msps for 6-bit resolution)
- Up to sixteen external channels and three internal channels: internal reference voltages, temperature sensor
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: two groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - The ADC supports multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into three data register or in SRAM with DMA controller support

- Data pre-processing: left/right alignment and per channel offset compensation
- Built-in oversampling unit for enhanced SNR
- Channel-wise programmable sampling time
- Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
- Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 input channel, which is used to convert the sensor output voltage into a digital value.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored in the system memory area, accessible in read-only mode.

Table 11. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.14.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and comparators. VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 12. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.6 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.15 Voltage reference buffer (VREFBUF)

The STM32WB55xx devices embed an voltage reference buffer that can be used as voltage reference for the ADC and also as voltage reference for external components through the VREF+ pin. The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V.

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off. The VREF+ pin is double-bonded with VDDA on UFQFPN48 package, hence the internal voltage reference buffer is not available on a dedicated pin, but user can still use the V_{DDA} value.

3.16 Comparators (COMP)

The STM32WB55xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.17 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric such as glass or plastic. The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library (free to use) and enables reliable touch sensing functionality in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 18 capacitive sensing channels
- Up to six capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to three capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.18 Liquid crystal display controller (LCD)

All device embed an LCD controller with the following characteristics:

- Highly flexible frame rate control.
- Supports Static, 1/2, 1/3, 1/4 and 1/8 duty.
- Supports Static, 1/2, 1/3 and 1/4 bias.
- Double buffered memory allows data in LCD_RAM registers to be updated at any time by the application firmware without affecting the integrity of the data displayed.
  - LCD data RAM of up to 16 x 32-bit registers which contain pixel information (active/inactive)
- Software selectable LCD output voltage (contrast) from $VLCD_{min}$ to $VLCD_{max}$.
- No need for external analog components:
  - A step-up converter is embedded to generate an internal VLCD voltage higher than V_{DD} (up to 3.6 V if V_{DD} > 2.0 V)
  - Software selection between external and internal VLCD voltage source. In case of an external source, the internal boost circuit is disabled to reduce power consumption
  - A resistive network is embedded to generate intermediate VLCD voltages
  - The structure of the resistive network is configurable by software to adapt the power consumption to match the capacitive charge required by the LCD panel
  - Integrated voltage output buffers for higher LCD driving capability.
- The contrast can be adjusted using two different methods:
  - When using the internal step-up converter, the software can adjust VLCD between $VLCD_{min}$ and $VLCD_{max}$
  - Programmable dead time (up to eight phase periods) between frames.
- Full support of low-power modes: the LCD controller can be displayed in Sleep, Low-power run, Low-power sleep and Stop modes, or can be fully disabled to reduce power consumption.
- Built in phase inversion for reduced power consumption and EMI (electromagnetic interference).
- Start of frame interrupt to synchronize the software when updating the LCD data RAM.
- Blink capability:
  - 1, 2, 3, 4, 8 or all pixels can be programmed to blink at a configurable frequency
  - Software adjustable blink frequency to achieve around 0.5 Hz, 1 Hz, 2 Hz or 4 Hz.

Used LCD segment and common pins should be configured as GPIO alternate functions and unused segment and common pins can be used for general purpose I/O or for another peripheral alternate function.

Note: When the LCD relies on the internal step-up converter, the VLCD pin should be connected to V_{SS} with a capacitor. Its typical value is 1 µF.

3.19 True random number generator (RNG)

The devices embed a true RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.20 Timers and watchdogs

The STM32WB55xx include one advanced 16-bit timer, one general-purpose 32-bit timer, two 16-bit basic timers, two low-power timers, two watchdog timers and a SysTick timer. *Table 13* compares the features of the advanced control, general purpose and basic timers.

Table 13. Timer features

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2	32-bits	Up, down, Up/down			4	No
General purpose	TIM16	16-bits	Up			2	1
General purpose	TIM17	16-bits	Up			2	1
Low power	LPTIM1 LPTIM2	16-bits	Up			1	1

3.20.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0 to 100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.20.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.20.2 General-purpose timers (TIM2, TIM16, TIM17)

There are up to three synchronizable general-purpose timers embedded in the STM32WB55xx (see *Table 13* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2
  - Full-featured general-purpose timer

  - Features four independent channels for input capture/output compare, PWM or one-pulse mode output. Can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.
  - The counter can be frozen in debug mode.
  - Independent DMA request generation, support of quadrature encoders.
- TIM16 and TIM17
  - General-purpose timers with mid-range features:
  - 16-bit auto-reload upcounters and 16-bit prescalers.
  - 1 channel and 1 complementary channel
  - All channels can be used for input capture/output compare, PWM or one-pulse mode output.
  - The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.
  - The counters can be frozen in debug mode

3.20.3 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSIx or by an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, either LSI1 or LSI2, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.20.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.20.5 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- a maskable system interrupt generation when the counter reaches 0
- a programmable clock source.

3.21 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter, supporting the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature, which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 20 backup registers are supplied through a switch that takes power either from the V_{DD} supply (when present) or from the VBAT pin.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- a 32.768 kHz external crystal (LSE)
- an external resonator or oscillator (LSE)
- one of the internal low power RC oscillators (LSI1 or LSI2, with typical frequency of 32 kHz)
- the high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by one of the LSIs, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.22 Inter-integrated circuit interface (I2C)

The device embeds two I2Cs. Refer to *Table 14* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alertc
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 7: Clock tree*.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 14. I2C implementation

I2C features(1)	I2C1	I2C3
Standard-mode (up to 100 kbit/s)	X	X
Fast-mode (up to 400 kbit/s)	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X

Table 14. I2C implementation (continued)

I2C features[1]	I2C1	I2C3
Independent clock	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X
Wakeup from Stop 2 mode on address match	-	X

1. X: supported

3.23 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32WB55xx devices feature one universal synchronous receiver transmitter.

This interface provides asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and has LIN Master/Slave capability. It provides hardware management of the CTS and RTS signals, and RS485 driver enable.

The USART is able to communicate at speeds of up to 4 Mbit/s, and also provides Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

The USART supports synchronous operation (SPI mode), and can be used as an SPI master.

The USART has a clock domain independent from the CPU clock, allowing it to wake up the MCU from Stop mode using baudrates up to 200 Kbaud.The wake up events from Stop mode are programmable and can be:

- the start bit detection
- any received data frame
- aspecific programmed data frame.

The USART interface can be served by the DMA controller.

3.24 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART, enabling asynchronous serial communication with minimum power consumption. The LPUART supports half duplex single wire communication and modem operations (CTS/RTS), allowing multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- the start bit detection
- any received data frame
- a specific programmed data frame.

Only a 32.768 kHz clock (LSE) is needed for LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an

extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interfaces can be served by the DMA controller.

3.25 Serial peripheral interface (SPI1, SPI2)

Two SPI interfaces enable communication up to 32 Mbit/s in master and up to 24 Mbit/s in slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

The SPI interfaces can be served by the DMA controller.

3.26 Serial audio interfaces (SAI1)

The device embeds a dual channel SAI peripheral that supports full duplex audio operation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- One independent audio sub-block that can be a transmitter or a receiver, with the respective FIFO
- 8-word integrated FIFOs
- Synchronous or asynchronous mode
- Master or slave configuration
- Clock generator to target independent audio frequency sampling when audio sub-block is configured in master mode
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame
- Number of bits by frame may be configurable
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/Mono audio frame capability
- Communication clock strobing edge configurable (SCK)
- Error flags with associated interrupts if enabled respectively
  - Overrun and underrun detection
  - Anticipated frame synchronization signal detection in slave mode
  - Late frame synchronization signal detection in slave mode
  - Codec not ready for the AC’97 mode in reception

- Interruption sources when enabled:
  - Errors
  - FIFO requests
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of the SAI audio sub-block.

The PDM (Pulse Density Modulation) block allows the user to manage up to three digital microphone pairs (with two different clocks). This block performs Right and Left microphone de-interleaving and time alignment through programmable delay lines in order to properly feed the SAI.

3.27 Quad-SPI memory interface (QUADSPI)

The Quad-SPI is a specialized communication interface targeting single, dual or quad SPI Flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash memory is mapped and is seen by the system as if it were an internal memory. This mode can be used for the Execute In Place (XIP)

The Quad-SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external Flash memory flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.28 Development support

3.28.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using only two pins instead of the five required by the JTAG (JTAG pins can then be reused as GPIOs with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

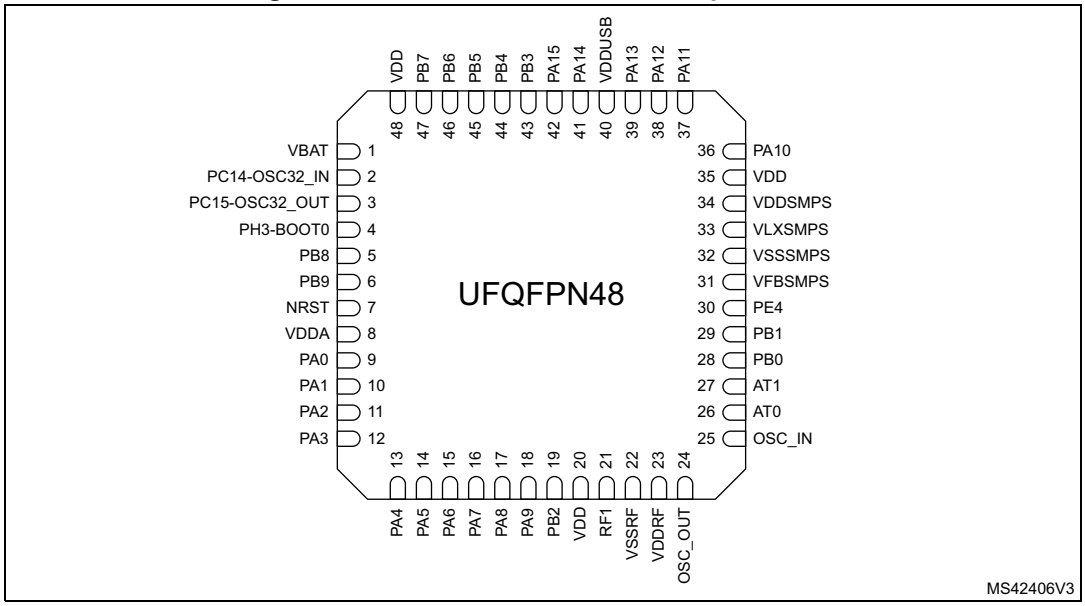
3.28.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32WB55xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

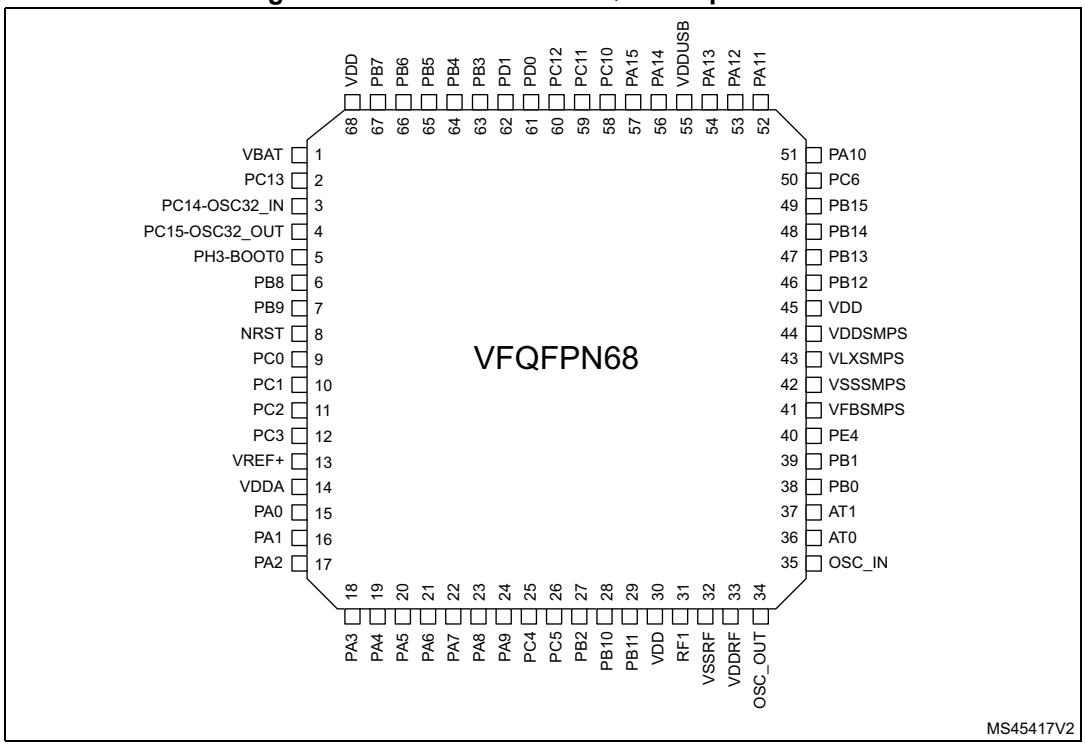
4 Pinouts and pin description

Figure 8. STM32WB55Cx UFQFPN48 pinout(1)(2)



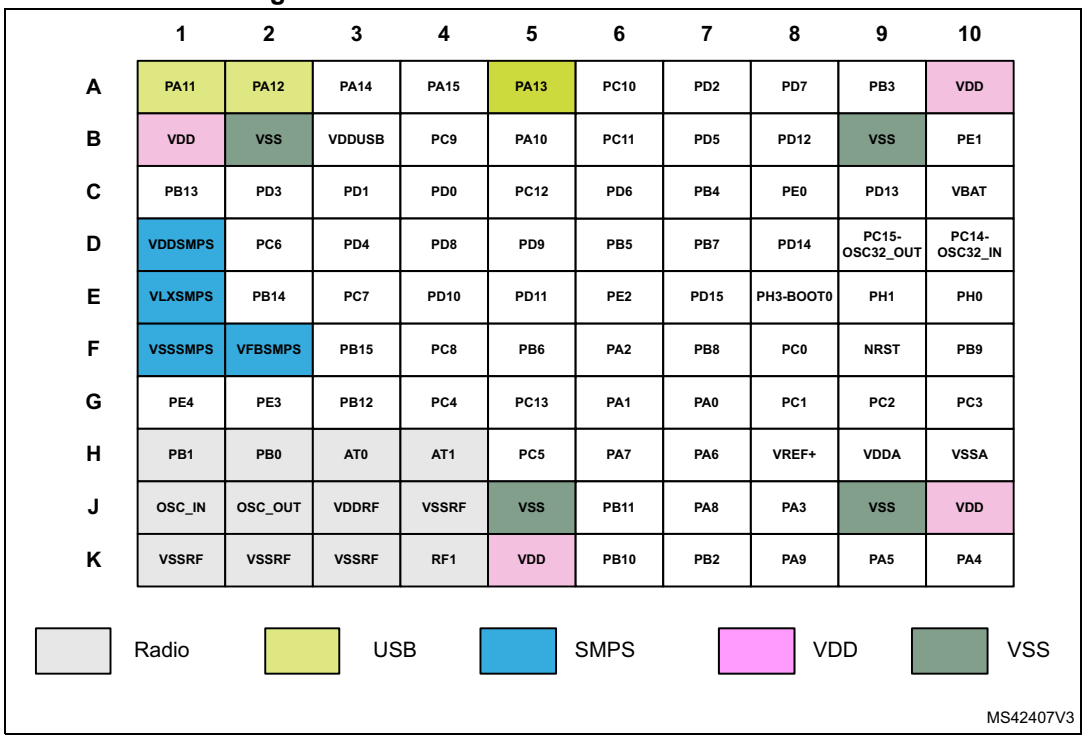
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 9. STM32WB55Rx VFQFPN68 pinout(1)(2)



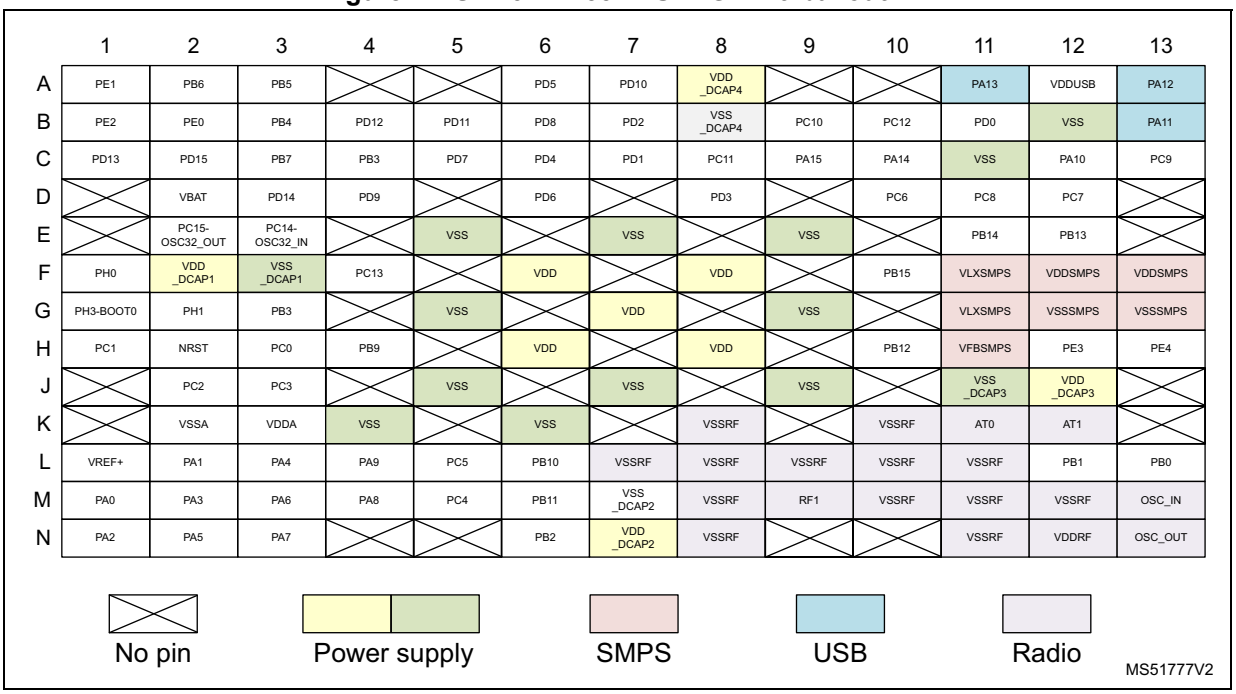
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 10. STM32WB55Vx WLCSP100 ballout(1)



1. The above figure shows the package top view.

Figure 11. STM32WB55Vx UFBGA129 ballout(1)



1. The above figure shows the package top view.

Table 15. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_l (2)	I/O, with LCD function supplied by V_{LCD}
		_u(3)	I/O, with USB function supplied by V_{DDUSB}
		_a(4) (5)	I/O, with Analog switch function supplied by V_{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 16* are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures in *Table 16* are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in *Table 16* are: FT_u, FT_lu.
4. The related I/O structures in *Table 16* are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. Analog switch for the TSC function is supplied by V_{DDIO}.

Table 16. STM32WB55xx pin and ball definitions

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	-	C8	B2	PE0	I/O	FT_l	-	TIM1_ETR, TSC_G7_IO3, LCD_SEG36, TIM16_CH1, CM4_EVENTOUT	-
-	-	B10	A1	PE1	I/O	FT_l	-	TSC_G7_IO2, LCD_SEG37, TIM17_CH1, CM4_EVENTOUT	-
-	-	E6	B1	PE2	I/O	FT_l	-	TRACECK, SAI1_PDM_CK1, TSC_G7_IO1, LCD_SEG38, SAI1_MCLK_A, CM4_EVENTOUT	-
-	-	C9	C1	PD13	I/O	FT_l	-	TSC_G6_IO4, LCD_SEG33, LPTIM2_OUT, CM4_EVENTOUT	-
-	-	D8	D3	PD14	I/O	FT_l	-	TIM1_CH1, LCD_SEG34, CM4_EVENTOUT	-
-	-	E7	C2	PD15	I/O	FT_l	-	TIM1_CH2, LCD_SEG35, CM4_EVENTOUT	-
1	1	C10	D2	VBAT	S	-	-	-	-
-	2	G5	F4	PC13	I/O	FT	(1) (2)	CM4_EVENTOUT	RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
2	3	D10	E3	PC14-OSC32_IN	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_IN
3	4	D9	E2	PC15-OSC32_OUT	I/O	FT	(1) (2)	CM4_EVENTOUT	OSC32_OUT
-	-	-	E5	VSS	S	-	-	-	-
-	-	-	F6	VDD	S	-	-	-	-
-	-	E10	F1	PH0	I/O	FT	-	CM4_EVENTOUT	-
-	-	E9	G2	PH1	I/O	FT	-	CM4_EVENTOUT	-
4	5	E8	G1	PH3-BOOT0	I/O	FT	-	CM4_EVENTOUT, LSCO	-
5	6	F7	G3	PB8	I/O	FT_fl	-	TIM1_CH2N, SAI1_PDM_CK1, I2C1_SCL, QUADSPI_BK1_IO1, LCD_SEG16, SAI1_MCLK_A, TIM16_CH1, CM4_EVENTOUT	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
6	7	F10	H4	PB9	I/O	FT_fla	-	TIM1_CH3N, SAI1_PDM_DI2, I2C1_SDA, SPI2_NSS, IR_OUT, TSC_G7_IO4, QUADSPI_BK1_IO0, LCD_COM3, SAI1_FS_A, TIM17_CH1, CM4_EVENTOUT	-
7	8	F9	H2	NRST	I/O	RST	-	-	-
-	9	F8	H3	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LCD_SEG18, LPTIM2_IN1, CM4_EVENTOUT	ADC1_IN1
-	10	G8	H1	PC1	I/O	FT_fla	-	LPTIM1_OUT, SPI2_MOSI, I2C3_SDA, LPUART1_TX, LCD_SEG19, CM4_EVENTOUT	ADC1_IN2
-	11	G9	J2	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, LCD_SEG20, CM4_EVENTOUT	ADC1_IN3
-	-	-	E7	VSS	S	-	-	-	-
-	-	-	H6	VDD	S	-	-	-	-
-	12	G10	J3	PC3	I/O	FT_a	-	LPTIM1_ETR, SAI1_PDM_DI1, SPI2_MOSI, LCD_VLCD, SAI1_SD_A, LPTIM2_ETR, CM4_EVENTOUT	ADC1_IN4
-	-	H10	K2	VSSA	S	-	-	-	-
-	13	H8	L1	VREF+	S	-	-	-	VREFBUF_OUT
8	14	H9	K3	VDDA	S	-	(3)	-	-
-	-	J9	E9	VSS	S	-	-	-	-
-	-	J10	F8	VDD	S	-	-	-	-
9	15	G7	M1	PA0	I/O	FT_a	-	TIM2_CH1, COMP1_OUT, SAI1_EXTCLK, TIM2_ETR, CM4_EVENTOUT	COMP1_INM, ADC1_IN5, RTC_TAMP2/WKUP1
10	16	G6	L2	PA1	I/O	FT_la	-	TIM2_CH2, I2C1_SMBA, SPI1_SCK, LCD_SEG0, CM4_EVENTOUT	COMP1_INP, ADC1_IN6

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
11	17	F6	N1	PA2	I/O	FT_la	-	LSCO, TIM2_CH3, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG1, COMP2_OUT, CM4_EVENTOUT	COMP2_INM, ADC1_IN7, WKUP4
12	18	J8	M2	PA3	I/O	FT_la	-	TIM2_CH4, SAI1_PDM_CK1, LPUART1_RX, QUADSPI_CLK, LCD_SEG2, SAI1_MCLK_A, CM4_EVENTOUT	COMP2_INP, ADC1_IN8
13	19	K10	L3	PA4	I/O	FT_a	-	SPI1_NSS, SAI1_FS_B, LPTIM2_OUT, LCD_SEG5, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN9
14	20	K9	N2	PA5	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, LPTIM2_ETR, SAI1_SD_B, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN10
15	21	H7	M3	PA6	I/O	FT_la	-	TIM1_BKIN, SPI1_MISO, LPUART1_CTS, QUADSPI_BK1_IO3, LCD_SEG3, TIM16_CH1, CM4_EVENTOUT	ADC1_IN11
16	22	H6	N3	PA7	I/O	FT_fla	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, LCD_SEG4, COMP2_OUT, TIM17_CH1, CM4_EVENTOUT	ADC1_IN12
17	23	J7	M4	PA8	I/O	FT_la	-	MCO, TIM1_CH1, SAI1_PDM_CK2, USART1_CK, LCD_COM0, SAI1_SCK_A, LPTIM2_OUT, CM4_EVENTOUT	ADC1_IN15
18	24	K8	L4	PA9	I/O	FT_fla	-	TIM1_CH2, SAI1_PDM_DI2, I2C1_SCL, SPI2_SCK, USART1_TX, LCD_COM1, SAI1_FS_A, CM4_EVENTOUT	COMP1_INM, ADC1_IN16
-	25	G4	M5	PC4	I/O	FT_la	-	LCD_SEG22, CM4_EVENTOUT	COMP1_INM, ADC1_IN13
-	-	-	F3	VSS_DCAP1	S	-	-	-	-
-	-	-	G7	VDD	S	-	-	-	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	26	H5	L5	PC5	I/O	FT_la	-	SAI1_PDM_DI3, LCD_SEG23, CM4_EVENTOUT	COMP1_INP, ADC1_IN14, WKUP5
19	27	K7	N6	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, LCD_VLCD, SAI1_EXTCLK, CM4_EVENTOUT	COMP1_INP
-	28	K6	L6	PB10	I/O	FT_fl	-	TIM2_CH3, I2C3_SCL, SPI2_SCK, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, CM4_EVENTOUT	-
-	29	J6	M6	PB11	I/O	FT_fl	-	TIM2_CH4, I2C3_SDA, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, CM4_EVENTOUT	-
-	-	-	G5	VSS	S	-	-	-	-
-	-	-	G9	VSS	S	-	-	-	-
20	30	K5	H8	VDD	S	-	-	-	-
-	-	-	N8	VSSRF	S	-	-	-	-
-	-	J4	L7	VSSRF	S	-	-	-	-
-	-	-	L8	VSSRF	S	-	-	-	-
-	-	-	M8	VSSRF	S	-	-	-	-
21	31	K4	M9	RF1	I/O	RF	(4)	-	-
22	32	K3	M10	VSSRF	S	-	-	-	-
-	-	K2	M11	VSSRF	S	-	-	-	-
-	-	-	K8	VSSRF	S	-	-	-	-
-	-	-	L9	VSSRF	S	-	-	-	-
-	-	-	L10	VSSRF	S	-	-	-	-
-	-	-	N11	VSSRF	S	-	-	-	-
23	33	J3	N12	VDDRF	S	-	-	-	-
-	-	K1	K10	VSSRF	S	-	-	-	-
-	-	-	M12	VSSRF	S	-	-	-	-
24	34	J2	N13	OSC_OUT	O	RF	(5)	-	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
25	35	J1	M13	OSC_IN	I	RF	(5)	-	-
-	-	-	L11	VSSRF	S	-	-	-	-
26	36	H3	K11	AT0	O	RF	(6)	-	-
27	37	H4	K12	AT1	O	RF	(6)	-	-
28	38	H2	L13	PB0	I/O	TT	(7)	COMP1_OUT, CM4_EVENTOUT, EXT_PA_TX	-
29	39	H1	L12	PB1	I/O	TT	(7)	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	-
-	-	J5	-	VSS	S	-	-	-	-
-	-	-	M7	VSS_DCAP2	S	-	-	-	-
-	-	G2	H12	PE3	I/O	FT	-	CM4_EVENTOUT	-
30	40	G1	H13	PE4	I/O	FT	-	CM4_EVENTOUT	-
31	41	F2	H11	VFBSMPS	S	-	-	-	-
-	-	-	G13	VSSSMPS	S	-	-	-	-
32	42	F1	G12	VSSSMPS	S	-	-	-	-
33	43	E1	F11	VLXSMPS	S	-	-	-	-
-	-	-	G11	VLXSMPS	S	-	-	-	-
34	44	D1	F12	VDDSMPS	S	-	-	-	-
-	-	-	F13	VDDSMPS	S	-	-	-	-
-	-	-	K4	VSS	S	-	-	-	-
35	45	B1	-	VDD	S	-	-	-	-
-	46	G3	H10	PB12	I/O	FT_l	-	TIM1_BKIN, I2C3_SMBA, SPI2_NSS, LPUART1_RTS, TSC_G1_IO1, LCD_SEG12, SAI1_FS_A, CM4_EVENTOUT	-
-	47	C1	E12	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C3_SCL, SPI2_SCK, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SAI1_SCK_A, CM4_EVENTOUT	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	48	E2	E11	PB14	I/O	FT_fl	-	TIM1_CH2N, I2C3_SDA, SPI2_MISO, TSC_G1_IO3, LCD_SEG14, SAI1_MCLK_A, CM4_EVENTOUT	-
-	49	F3	F10	PB15	I/O	FT_l	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, LCD_SEG15, SAI1_SD_A, CM4_EVENTOUT	-
-	50	D2	D10	PC6	I/O	FT_l	-	TSC_G4_IO1, LCD_SEG24, CM4_EVENTOUT	-
-	-	E3	D12	PC7	I/O	FT_l	-	TSC_G4_IO2, LCD_SEG25, CM4_EVENTOUT	-
-	-	F4	D11	PC8	I/O	FT_l	-	TSC_G4_IO3, LCD_SEG26, CM4_EVENTOUT	-
-	-	B4	C13	PC9	I/O	FT_l	-	TIM1_BKIN, TSC_G4_IO4, USB_NOE, LCD_SEG27, SAI1_SCK_B, CM4_EVENTOUT	-
-	-	-	K6	VSS	S	-	-	-	-
-	-	B2	-	VSS	S	-	-	-	-
36	51	B5	C12	PA10	I/O	FT_fl	-	TIM1_CH3, SAI1_PDM_DI1, I2C1_SDA, USART1_RX, USB_CRS_SYNC, LCD_COM2, SAI1_SD_A, TIM17_BKIN, CM4_EVENTOUT	-
37	52	A1	B13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, USB_DM, CM4_EVENTOUT	-
38	53	A2	A13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, LPUART1_RX, USART1_RTS_DE, USB_DP, CM4_EVENTOUT	-
39	54	A5	A11	PA13 (JTMS_SWDIO)	I/O	FT_u	(8)	JTMS-SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, CM4_EVENTOUT	-
40	55	B3	A12	VDDUSB	S	-	-	-	-
-	-	-	C11	VSS	S	-	-	-	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
41	56	A3	C10	PA14 (JTCK_SWCLK)	I/O	FT_l	(8)	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, LCD_SEG5, SAI1_FS_B, CM4_EVENTOUT	-
42	57	A4	C9	PA15 (JTDI)	I/O	FT_l	(8)	JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS, TSC_G3_IO1, LCD_SEG17, CM4_EVENTOUT, MCO	-
-	-	-	J11	VSS_DCAP3	S	-	-	-	-
-	58	A6	B9	PC10	I/O	FT_l	-	TRACED1, TSC_G3_IO2, LCD_COM4/LCD_SEG28/ LCD_SEG40, CM4_EVENTOUT	-
-	59	B6	C8	PC11	I/O	FT_l	-	TSC_G3_IO3, LCD_COM5/LCD_SEG29/ LCD_SEG41, CM4_EVENTOUT	-
-	60	C5	B10	PC12	I/O	FT_l	-	TRACED3, TSC_G3_IO4, LCD_COM6/LCD_SEG30/ LCD_SEG42, CM4_EVENTOUT	RTC_TAMP3/WKUP3
-	61	C4	B11	PD0	I/O	FT	-	SPI2_NSS, CM4_EVENTOUT	-
-	62	C3	C7	PD1	I/O	FT	-	SPI2_SCK, CM4_EVENTOUT	-
-	-	A7	B7	PD2	I/O	FT_l	-	TRACED2, TSC_SYNC, LCD_COM7/LCD_SEG31/LC D_SEG43, CM4_EVENTOUT	-
-	-	C2	D8	PD3	I/O	FT	-	SPI2_SCK, SPI2_MISO, QUADSPI_BK1_NCS, CM4_EVENTOUT	-
-	-	D3	C6	PD4	I/O	FT	-	SPI2_MOSI, TSC_G5_IO1, QUADSPI_BK1_IO0, CM4_EVENTOUT	-
-	-	B7	A6	PD5	I/O	FT	-	TSC_G5_IO2, QUADSPI_BK1_IO1, SAI1_MCLK_B, CM4_EVENTOUT	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
-	-	C6	D6	PD6	I/O	FT	-	SAI1_PDM_DI1, TSC_G5_IO3, QUADSPI_BK1_IO2, SAI1_SD_A, CM4_EVENTOUT	-
-	-	A8	C5	PD7	I/O	FT_l	-	TSC_G5_IO4, QUADSPI_BK1_IO3, LCD_SEG39, CM4_EVENTOUT	-
-	-	B9	B12	VSS	S	-	-	-	-
-	-	D4	B6	PD8	I/O	FT_l	-	TIM1_BKIN2, LCD_SEG28, CM4_EVENTOUT	-
-	-	D5	D4	PD9	I/O	FT_l	-	TRACED0, LCD_SEG29, CM4_EVENTOUT	-
-	-	E4	A7	PD10	I/O	FT_l	-	TRIG_INOUT, TSC_G6_IO1, LCD_SEG30, CM4_EVENTOUT	-
-	-	E5	B5	PD11	I/O	FT_l	-	TSC_G6_IO2, LCD_SEG31, LPTIM2_ETR, CM4_EVENTOUT	-
-	-	B8	B4	PD12	I/O	FT_l	-	TSC_G6_IO3, LCD_SEG32, LPTIM2_IN1, CM4_EVENTOUT	-
43	63	A9	C4	PB3 (JTDO)	I/O	FT_la	(8)	JTDO-TRACESWO, TIM2_CH2, SPI1_SCK, USART1_RTS_DE, LCD_SEG7, SAI1_SCK_B, CM4_EVENTOUT	COMP2_INM
44	64	C7	B3	PB4 (NJTRST)	I/O	FT_fla	(8)	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, TSC_G2_IO1, LCD_SEG8, SAI1_MCLK_B, TIM17_BKIN, CM4_EVENTOUT	COMP2_INP
45	65	D6	A3	PB5	I/O	FT_l	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, USART1_CK, LPUART1_TX, TSC_G2_IO2, LCD_SEG9, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, CM4_EVENTOUT	-

Table 16. STM32WB55xx pin and ball definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structures	Notes	Alternate functions	Additional functions
UFQFPN48	VFQFPN68	WLCSP100	UFBGA129						
46	66	F5	A2	PB6	I/O	FT_fla	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TSC_G2_IO3, LCD_SEG6, SAI1_FS_B, TIM16_CH1N, MCO, CM4_EVENTOUT	COMP2_INP
47	67	D7	C3	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TSC_G2_IO4, LCD_SEG21, TIM17_CH1N, CM4_EVENTOUT	COMP2_INM, PVD_IN
-	-	-	J5	VSS	S	-	-	-	-
-	-	-	J7	VSS	S	-	-	-	-
-	-	-	J9	VSS	S	-	-	-	-
-	-	-	B8	VSS_DCAP4	S	-	-	-	-
48	68	A10	-	VDD	S	-	-	-	-
-	-	-	A8	VDD_DCAP4	S	-	-	-	-
-	-	-	F2	VDD_DCAP1	S	-	-	-	-
-	-	-	J12	VDD_DCAP3	S	-	-	-	-
-	-	-	N7	VDD_DCAP2	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. As this switch only sinks a limited amount of current (3 mA), the use of the PC13, PC14 and PC15 GPIOs in output mode is limited:
   - the speed should not exceed 2 MHz with a maximum load of 30 pF
   - these GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers that are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0351, available on *www.st.com*.
3. On UFQFPN48 VDDA is connected to VREF+.
4. RF pin, use the nominal PCB layout.
5. 32 MHz oscillator pins, use the nominal PCB layout according to reference design (see AN5165).
6. Reserved, must be kept unconnected.
7. High frequency (above 100 KHz) may impact the RF performances.
8. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13 and PB4 pins and the internal pull-down on PA14 pin are activated.

Table 17. Alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
A	PA0	-	TIM2_ CH1	-	-	-	-	-	-	-	-	-	-	COMP1_ OUT	SAI1_ EXTCLK	TIM2_ ETR	CM4_ EVENTOUT
	PA1	-	TIM2_ CH2	-	-	I2C1_ SMBA	SPI1_ SCK	-	-		-	-	LCD_SEG0	-	-	-	CM4_ EVENTOUT
	PA2	LSCO	TIM2_ CH3	-	-	-	-	-	-	LPUART1 _TX	-	QUADSPI_ BK1_NCS	LCD_SEG1	COMP2_ OUT	-	-	CM4_ EVENTOUT
	PA3	-	TIM2_ CH4	-	SAI1_ PDM_CK1	-	-	-	-	LPUART1 _RX	-	QUADSPI_ CLK	LCD_SEG2	-	SAI1 _MCLK_A	-	CM4_ EVENTOUT
	PA4	-	-	-	-		SPI1_ NSS	-	-	-	-	-	LCD_SEG5	-	SAI1 _FS_B	LPTIM2_ OUT	CM4_ EVENTOUT
	PA5	-	TIM2_ CH1	TIM2_ ETR	-		SPI1_ SCK	-	-	-	-	-	-	-	SAI1 _SD_B	LPTIM2_ ETR	CM4_ EVENTOUT
	PA6	-	TIM1_ BKIN	-	-		SPI1_ MISO	-	-	LPUART1 _CTS	-	QUADSPI_ BK1_IO3	LCD_SEG3	TIM1_ BKIN	-	TIM16 _CH1	CM4_ EVENTOUT
	PA7	-	TIM1_ CH1N	-	-	I2C3_ SCL	SPI1_ MOSI	-	-	-	-	QUADSPI_ BK1_IO2	LCD_SEG4	COMP2_ OUT	-	TIM17 _CH1	CM4_ EVENTOUT
	PA8	MCO	TIM1_ CH1	-	SAI1_ PDM_CK2	-	-	-	USART1_ CK	-	-		LCD_COM0	-	SAI1 _SCK_A	LPTIM2_ OUT	CM4_ EVENTOUT
	PA9	-	TIM1_ CH2	-	SAI1_ PDM_DI2	I2C1_ SCL	SPI2_ SCK	-	USART1_ TX	-	-		LCD_COM1	-	SAI1 _FS_A	-	CM4_ EVENTOUT
	PA10	-	TIM1_ CH3	-	SAI1_ PDM_DI1	I2C1_ SDA		-	USART1_ RX	-	-	USB_CRS _SYNC	LCD_COM2	-	SAI1 _SD_A	TIM17 _BKIN	CM4_ EVENTOUT
	PA11	-	TIM1_ CH4	TIM1_ BKIN2	-	-	SPI1_ MISO	-	USART1_ CTS	-	-	USB_DM	-	TIM1_ BKIN2	-	-	CM4_ EVENTOUT
	PA12	-	TIM1_ ETR	-	-	-	SPI1_ MOSI	-	USART1_ RTS_DE	LPUART1 _RX	-	USB_DP	-	-	-	-	CM4_ EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	IR_OUT	-	USB_NOE	-	-	SAI1 _SD_B	-	CM4_ EVENTOUT
	PA14	JTCK-SWCLK	LPTIM1_ OUT	-	-	I2C1_ SMBA	-	-	-	-	-	-	LCD_SEG5	-	SAI1 _FS_B	-	CM4_ EVENTOUT
	PA15	JTDI	TIM2_ CH1	TIM2_ ETR	-		SPI1_ NSS	MCO	-	-	TSC_G3 _IO1	-	LCD_SEG17	-	-	-	CM4_ EVENTOUT

Table 17. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
B	PB0	-	-	-	-	-	-	EXT_PA_TX	-		-	-	-	COMP1_OUT	-	-	CM4_EVENTOUT
	PB1	-	-	-	-	-	-	-	-	LPUART1_RTS_DE	-	-	-	-	-	LPTIM2_IN1	CM4_EVENTOUT
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	SPI1_NSS	-	-	-	-	-	LCD_VLCD	-	SAI1_EXTCLK	-	CM4_EVENTOUT
	PB3	JTDO-TRACE SWO	TIM2_CH2	-	-	-	SPI1_SCK	-	USART1_RTS_DE	-	-	-	LCD_SEG7	-	SAI1_SCK_B	-	CM4_EVENTOUT
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	-	USART1_CTS	-	TSC_G2_IO1	-	LCD_SEG8	-	SAI1_MCLK_B	TIM17_BKIN	CM4_EVENTOUT
	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	-	USART1_CK	LPUART1_TX	TSC_G2_IO2	-	LCD_SEG9	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	CM4_EVENTOUT
	PB6	MCO	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX	-	TSC_G2_IO3	-	LCD_SEG6	-	SAI1_FS_B	TIM16_CH1N	CM4_EVENTOUT
	PB7	-	LPTIM1_IN2	-	TIM1_BKIN	I2C1_SDA	-	-	USART1_RX	-	TSC_G2_IO4	-	LCD_SEG21	-	-	TIM17_CH1N	CM4_EVENTOUT
	PB8	-	TIM1_CH2N	-	SAI1_PDM_CK1	I2C1_SCL	-	-	-	-	-	QUADSPI_BK1_IO1	LCD_SEG16	-	SAI1_MCLK_A	TIM16_CH1	CM4_EVENTOUT
	PB9	-	TIM1_CH3N	-	SAI1_PDM_DI2	I2C1_SDA	SPI2_NSS	-	-	IR_OUT	TSC_G7_IO4	QUADSPI_BK1_IO0	LCD_COM3	-	SAI1_FS_A	TIM17_CH1	CM4_EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C3_SCL	SPI2_SCK	-	-	LPUART1_RX	TSC_SYNC	QUADSPI_CLK	LCD_SEG10	COMP1_OUT	SAI1_SCK_A	-	CM4_EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C3_SDA	-	-	-	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG11	COMP2_OUT	-	-	CM4_EVENTOUT
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C3_SMBA	SPI2_NSS	-	-	LPUART1_RTS	TSC_G1_IO1	-	LCD_SEG12	-	SAI1_FS_A	-	CM4_EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2C3_SCL	SPI2_SCK	-	-	LPUART1_CTS	TSC_G1_IO2	-	LCD_SEG13	-	SAI1_SCK_A	-	CM4_EVENTOUT
	PB14	-	TIM1_CH2N	-	-	I2C3_SDA	SPI2_MISO	-	-	-	TSC_G1_IO3	-	LCD_SEG14	-	SAI1_MCLK_A	-	CM4_EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	-	-	SPI2_MOSI	-	-	-	TSC_G1_IO4	-	LCD_SEG15	-	SAI1_SD_A	-	CM4_EVENTOUT

Table 17. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
C	PC0	-	LPTIM1_ IN1	-	-	I2C3 _SCL	-	-	-	LPUART1 _RX	-	-	LCD_SEG18	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PC1	-	LPTIM1_ OUT	-	SPI2_ MOSI	I2C3 _SDA		-	-	LPUART1 _TX	-	-	LCD_SEG19	-	-	-	CM4_ EVENTOUT
	PC2	-	LPTIM1_ IN2	-	-	-	SPI2_ MISO	-	-	-	-	-	LCD_SEG20	-	-	-	CM4_ EVENTOUT
	PC3	-	LPTIM1_ ETR	-	SAI1_ PDM_DI1	-	SPI2_ MOSI	-	-	-	-	-	LCD_VLCD	-	SAI1 _SD_A	LPTIM2_ ETR	CM4_ EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	LCD_SEG22	-	-	-	CM4_ EVENTOUT
	PC5	-	-	-	SAI1_ PDM_DI3	-	-	-	-	-	-	-	LCD_SEG23	-	-	-	CM4_ EVENTOUT
	PC6	-	-	-	-	-	-	-	-	-	TSC_G4 _IO1	-	LCD_SEG24	-	-	-	CM4_ EVENTOUT
	PC7	-	-	-	-	-	-	-	-	-	TSC_G4 _IO2	-	LCD_SEG25	-	-	-	CM4_ EVENTOUT
	PC8	-	-	-	-	-	-	-	-	-	TSC_G4 _IO3	-	LCD_SEG26	-	-	-	CM4_ EVENTOUT
	PC9	-	-	-	TIM1 _BKIN	-	-	-	-	-	TSC_G4 _IO4	USB_NOE	LCD_SEG27	-	SAI1 _SCK_B	-	CM4_ EVENTOUT
	PC10	TRACE D1	-	-	-	-	-	-	-	-	TSC_G3 _IO2	-	LCD_COM4 LCD_SEG28 LCD_SEG40	-	-	-	CM4_ EVENTOUT
	PC11	-	-	-	-	-	-	-	-	-	TSC_G3 _IO3	-	LCD_COM5 LCD_SEG29 LCD_SEG41	-	-	-	CM4_ EVENTOUT
	PC12	TRACE D3	-	-	-	-	-	LSCO	-	-	TSC_G3 _IO4	-	LCD_COM6 LCD_SEG30 LCD_SEG42	-	-	-	CM4_ EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT

Table 17. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
D	PD0	-	-	-	-	-	SPI2_ NSS	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PD1	-	-	-	-	-	SPI2_ SCK	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PD2	TRACE D2	-	-	-	-	-	-	-	-	TSC_ SYNC	-	LCD_COM7 LCD_SEG31 LCD_SEG43	-	-	-	CM4_ EVENTOUT
	PD3	-	-	-	SPI2_SCK	-	SPI2_ MISO	-	-	-	-	QUADSPI_ BK1_NCS	-	-	-	-	CM4_ EVENTOUT
	PD4	-	-	-	-	-	SPI2_ MOSI	-	-	-	TSC_ G5_IO1	QUADSPI_ BK1_IO0	-	-	-	-	CM4_ EVENTOUT
	PD5	-	-	-	-	-	-	-	-	-	TSC_ G5_IO2	QUADSPI_ BK1_IO1	-	-	SAI1_ MCLK_B	-	CM4_ EVENTOUT
	PD6	-	-	-	SAI1_ PDM_DI1	-	-	-	-	-	TSC_ G5_IO3	QUADSPI_ BK1_IO2	-	-	SAI1_ SD_A	-	CM4_ EVENTOUT
	PD7	-	-	-	-	-	-	-	-	-	TSC_ G5_IO4	QUADSPI_ BK1_IO3	LCD_SEG39	-	-	-	CM4_ EVENTOUT
	PD8	-	-	TIM1 _BKIN2	-	-	-	-	-	-	-	-	LCD_SEG28	-	-	-	CM4_ EVENTOUT
	PD9	TRACE D0	-	-	-	-	-	-	-	-	-	-	LCD_SEG29	-	-	-	CM4_ EVENTOUT
	PD10	TRIG _INOUT	-	-	-	-	-	-	-	-	TSC_ G6_IO1	-	LCD_SEG30	-	-	-	CM4_ EVENTOUT
	PD11	-	-	-	-	-	-	-	-	-	TSC_ G6_IO2	-	LCD_SEG31	-	-	LPTIM2_ ETR	CM4_ EVENTOUT
	PD12	-	-	-	-	-	-	-	-	-	TSC_ G6_IO3	-	LCD_SEG32	-	-	LPTIM2_ IN1	CM4_ EVENTOUT
	PD13	-	-	-	-	-	-	-	-	-	TSC_ G6_IO4	-	LCD_SEG33	-	-	LPTIM2_ OUT	CM4_ EVENTOUT
	PD14	-	TIM1_ CH1	-	-	-	-	-	-	-	-	-	LCD_SEG34	-	-	-	CM4_ EVENTOUT
	PD15	-	TIM1_ CH2	-	-	-	-	-	-	-	-	-	LCD_SEG35	-	-	-	CM4_ EVENTOUT

Table 17. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/ TIM2/ LPTIM1	TIM1/ TIM2	SPI2/ SAI1/ TIM1	I2C1/ I2C3	SPI1/ SPI2	RF	USART1	LPUART1	TSC	USB/ QUADSPI	LCD	COMP1/ COMP2/ TIM1	SAI1	TIM2/ TIM16/ TIM17/ LPTIM2	EVENTOUT
E	PE0	-	TIM1_ ETR	-	-	-	-	-	-	-	TSC_ G7_IO3	-	LCD_SEG36	-	-	TIM16_ CH1	CM4_ EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	TSC_ G7_IO2	-	LCD_SEG37	-	-	TIM17_ CH1	CM4_ EVENTOUT
	PE2	TRACECK	-	-	SAI1_ PDM_CK1	-	-	-	-	-	TSC_ G7_IO1	-	LCD_SEG38	-	SAI1_ MCLK_A	-	CM4_ EVENTOUT
	PE3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PE4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT
	PH3	LSCO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_ EVENTOUT

5 Memory mapping

The STM32WB55xx devices feature a single physical address space that can be accessed by the application processor and by the RF subsystem.

A part of the Flash memory and of the SRAM2a and SRAM2b memories are made secure, exclusively accessible by the CPU2, protected against execution, read and write from CPU1 and DMA.

In case of shared resources the SW should implement arbitration mechanism to avoid access conflicts. This happens for peripherals Reset and Clock Controller (RCC), Power Controller (PWC), EXTI and Flash interface, and can be implemented using the built-in semaphore block (HSEM).

By default the RF subsystem and CPU2 operate in secure mode. This implies that part of the Flash and of the SRAM2 memories can only be accessed by the RF subsystem and by the CPU2. In this case the Host processor (CPU1) has no access to these resources.

The detailed memory map and the peripheral mapping of the STM32WB55xx devices can be found in the reference manual RM0434.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 12*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.

Figure 12. Pin loading conditions

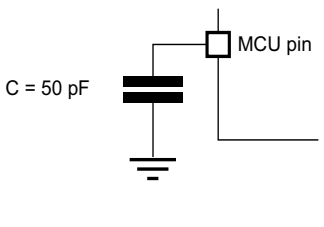
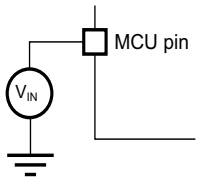
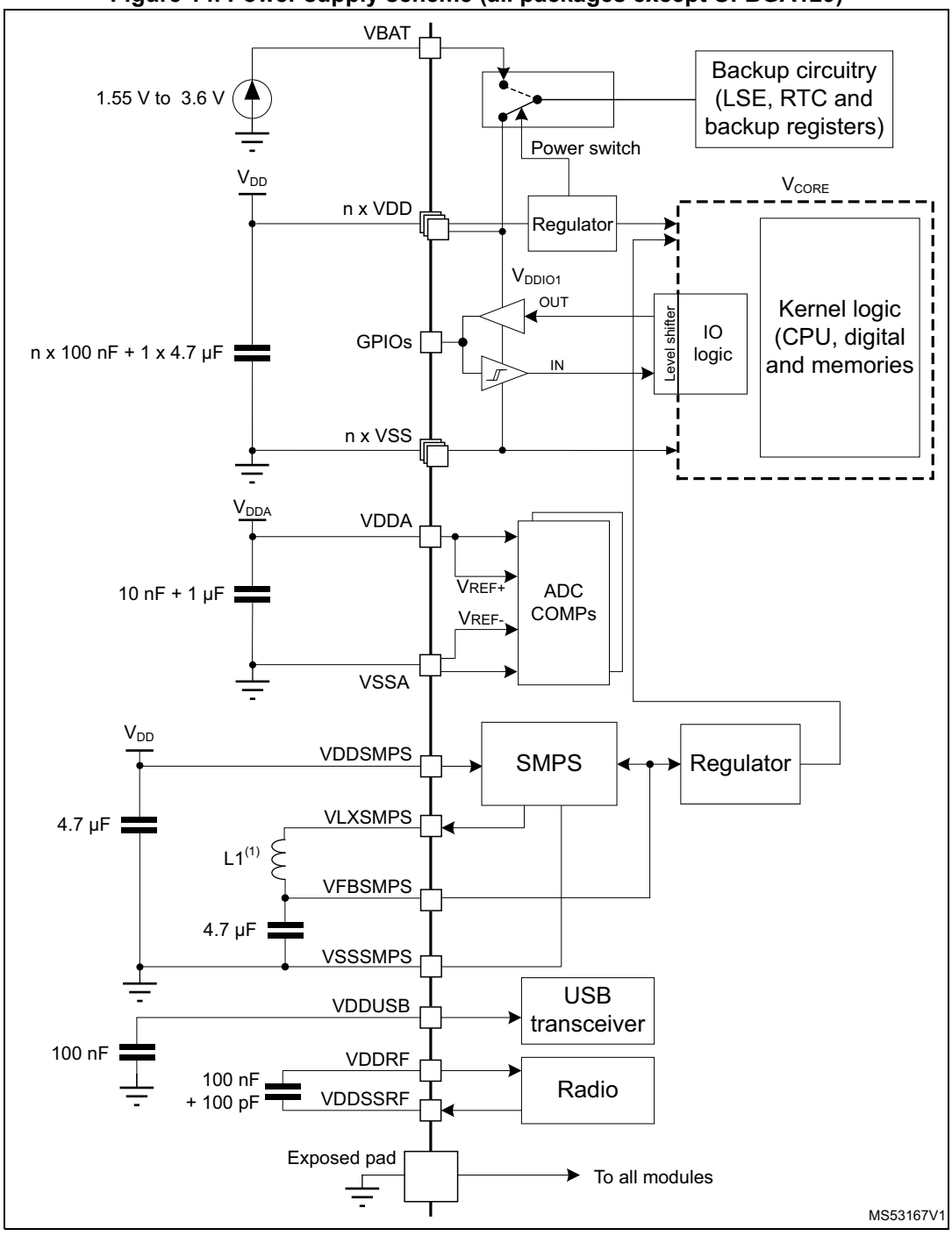


Figure 13. Pin input voltage



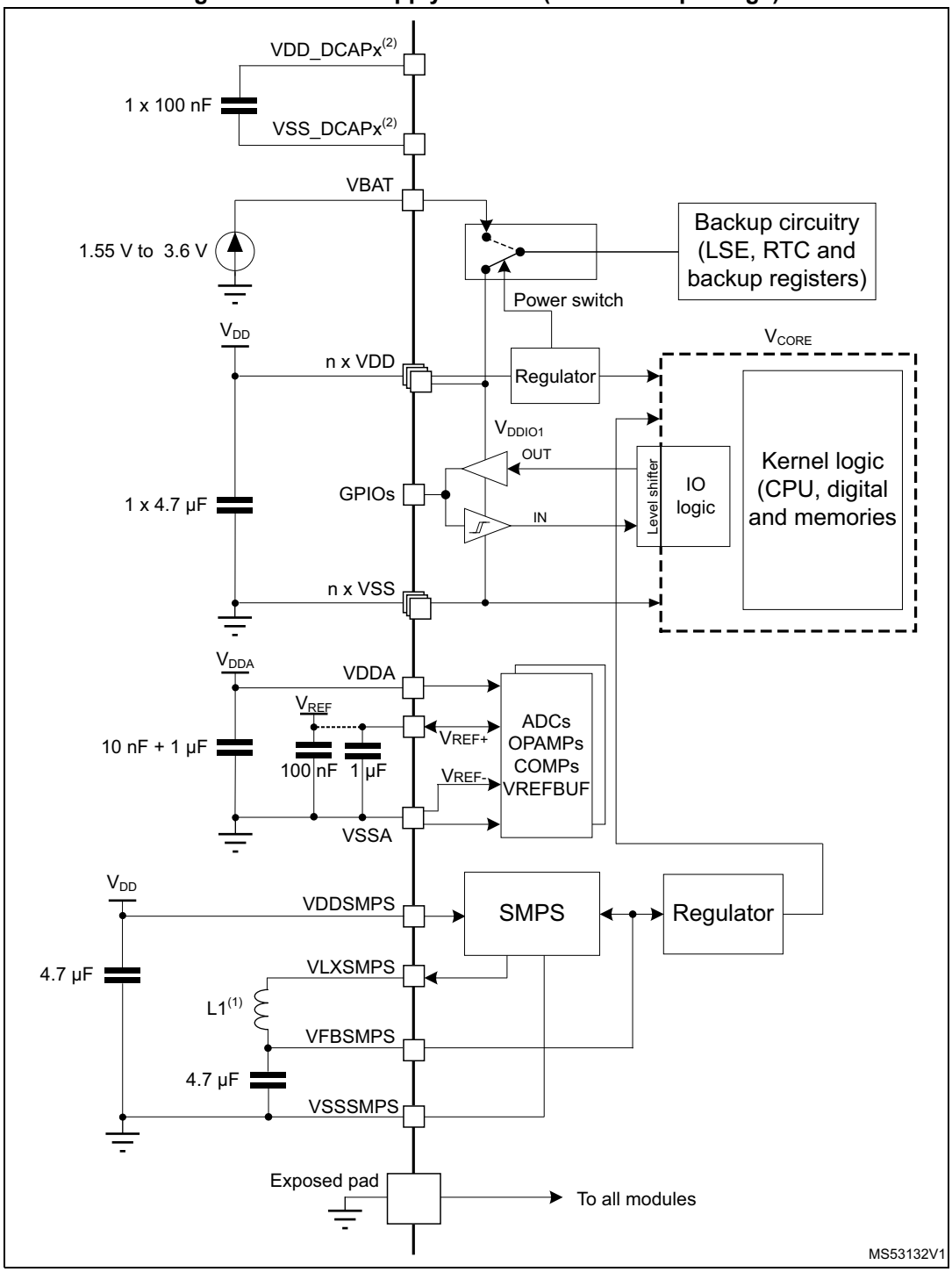
6.1.6 Power supply scheme

Figure 14. Power supply scheme (all packages except UFBGA129)



1. The value of L1 depends upon the frequency, as indicated in *Table 6*.

Figure 15. Power supply scheme (UFBGA129 package)

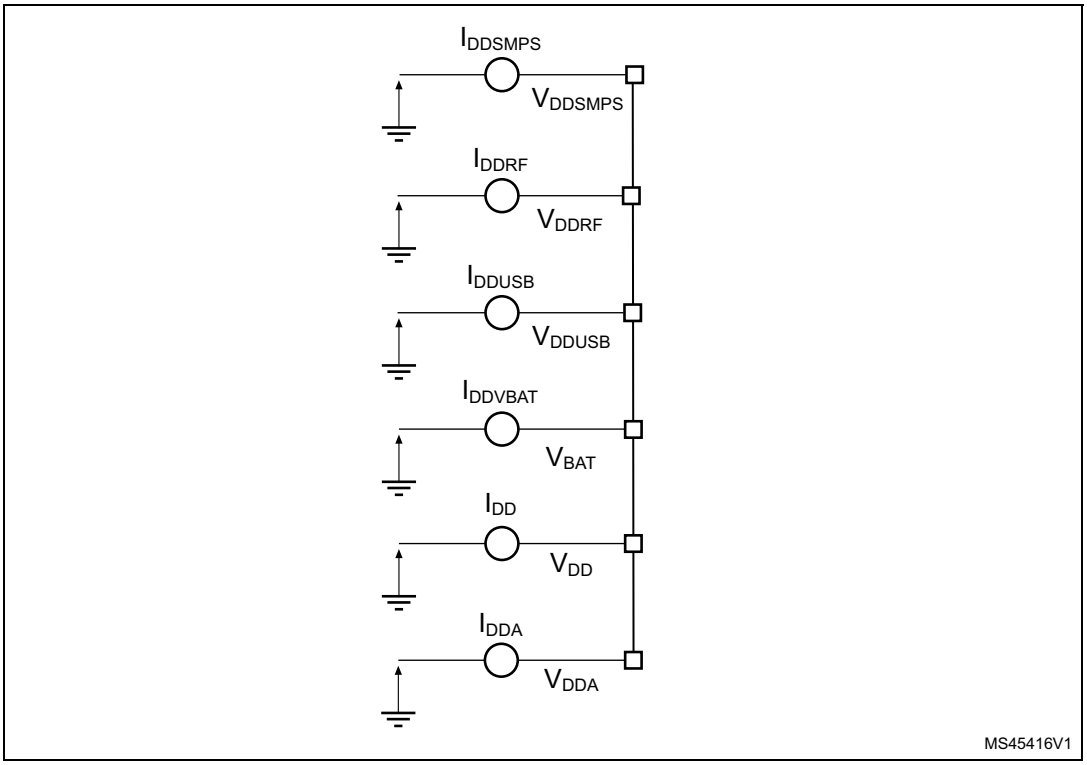


1. The value of L1 depends upon the frequency, as indicated in *Table 6*.
2. VDD_DCAPx and VSS_DCAPx balls are connected to V_{DD} and V_{SS} internally. They simplify the 2-layer board layout and especially the ground plane below the BGA.
   V_{DD} power supply can be done with a single connection to the center of the BGA on the bottom layer of the board. The decoupling 100 nF capacitors are connected between VDDCAPx and VSSCAPx without cutting the board ground plane.

Caution: Each power supply pair (V_{DD} / V_{SS}, V_{DDA} / V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown in *Figure 14*. These capacitors must be placed as close as possible to (or below) the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 16. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18*, *Table 19* and *Table 20* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 18. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}, V_{DDRF}, V_{DDSMPS}, V_{BAT}, V_{REF+})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}, V_{DDRF}, V_{DDSMPS}) + 4.0(3)(4)	
	Input voltage on TT_xx pins		4.0	
	Input voltage on any other pin		4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	
V_{REF+} - V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	V

1. All main power (V_{DD}, V_{DDRF}, V_{DDA}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 19. Current characteristics

Symbol	Ratings	Max	Unit
$\sum I_{VDD}$	Total current into sum of all V_{DD} power lines (source)(1)	130	mA
$\sum I_{VSS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	130	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, RST and B pins, except PB0 and PB1	–5 / +0(4)	
	Injected current on PB0 and PB1	-5/0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	25	

1. All main power (V_{DD}, V_{DDRF}, V_{DDA}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count packages.
3. Positive injection (when V_{IN} > V_{DD}) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by V_{IN} < V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 18: Voltage characteristics* for the maximum allowed input voltage values.

5. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	130	

6.3 Operating conditions

6.3.1 Summary of main performance

Table 21. Main performance at V_{DD} = 3.3 V

Parameter			Test conditions	Typ	Unit
I_{CORE}	Core current consumption		VBAT (V_{BAT} = 1.8 V, V_{DD} = 0 V)	0.002	µA
			Shutdown (V_{DD} = 1.8 V)	0.013	
			Standby (V_{DD} = 1.8 V, 32 Kbytes RAM retention)	0.320	
			Stop2	1.85	
			Sleep (16 MHz)	740	
			LP run (2 MHz)	320	
			Run (64 MHz)	5000	
			Radio RX	4500	
			Radio TX 0 dBm output power	5200	
I_{PERI}	Peripheral current consumption	BLE	Advertising (Tx = 0 dBm; Period 1.28 s; 31 bytes, 3 channels)	13	
			Advertising (Tx = 0 dBm, 6 bytes; period 10.24 s, 3 channels)	4	
		LP timers	-	6	
		I2C3	-	7.1	
		LPUART	-	7.7	
		RTC	-	2.5	

6.3.2 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	64	
f_{PCLK2}	Internal APB2 clock frequency	-	0	64	
V_{DD}	Standard operating voltage	-	1.71(1)	3.6	V
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		VREFBUF used	2.4		
		ADC, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	

Table 22. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{FBSMPS}	SMPS Feedback voltage	-	1.4	3.6	V
V_{DDRF}	Minimum RF voltage	-	1.71	3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	–0.3	V_{DD} + 0.3	
		All I/O except TT_xx	–0.3	min (min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 3.6 V, 5.5 V)(2)(3)	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	UFQFPN48	-	803	mW
		VFQFPN68	-	425	
		WLCSP100	-	558	
		UFBGA129	-	481	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)		105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	–40	105	
		Low-power dissipation(5)		125	
T_J	Junction temperature range	Suffix 6 version	–40	105	
		Suffix 7 version		125	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 3.6 V and 5.5V.
3. For operation with voltage higher than min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Section 7.5: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Section 7.5: Thermal characteristics*).

6.3.3 RF BLE characteristics

RF characteristics are given at 1 Mbps, unless otherwise specified.

Table 23. RF transmitter BLE characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{op}	Frequency operating range	-	2402	-	2480	MHz
F_{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	250	-	KHz
Rgfsk	On Air data rate	-	-	1	2	Mbps
PLLres	RF channel spacing	-	-	2	-	MHz

Table 24. RF transmitter BLE characteristics (1 Mbps)(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power		SMPS Bypass or ON (V_{FBSMPS} = 1.7 V and V_{DD} > 1.95 V)	-	6.0	-	dBm
			SMPS Bypass or ON (V_{FBSMPS} = 1.4 V and V_{DD} > 1.71 V), Code 29	-	3.7	-	
	0 dBm output power		-	-	0	-	
	Minimum output power		-	-	-20	-	
P_{band}	Output power variation over the band		Tx = 0 dBm - Typical	-0.5	-	0.4	dB
BW20dB	20 dB signal bandwidth		-	-	670	-	KHz
IBSE	In band spurious emission	2 MHz	Bluetooth® Low Energy: -20 dBm	-	-50	-	dBm
		≥ 3 MHz	Bluetooth® Low Energy: -30 dBm	-	-53	-	
f_d	Frequency drift		Bluetooth® Low Energy: ±50 kHz	-50	-	+50	KHz
maxdr	Maximum drift rate		Bluetooth® Low Energy: ±20 KHz / 50 µs	-20	-	+20	KHz/ 50 µs
fo	Frequency offset		Bluetooth® Low Energy: ±150 kHz	-150	-	+150	KHz
Δf1	Frequency deviation average		Bluetooth® Low Energy: between 225 and 275 kHz	225	-	275	
Δfa	Frequency deviation Δf2 (average) / Δf1 (average)		Bluetooth® Low Energy:> 0.80	0.80	-	-	-
OBSE(2)	Out of band spurious emission	< 1 GHz	-	-	-61	-	dBm
		≥ 1 GHz	-	-	-46	-	

1. :Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

Table 25. RF transmitter BLE characteristics (2 Mbps)(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
P_{rf}	Maximum output power		SMPS Bypass or ON (V_{FBSMPS} = 1.7 V and V_{DD} > 1.95 V)	-	6.0	-	dBm
			SMPS Bypass or ON (V_{FBSMPS} = 1.4 V and V_{DD} > 1.71 V), Code 29	-	3.7	-	
	0 dBm output power		-	-	0	-	
	Minimum output power		-	-	-20	-	
P_{band}	Output power variation over the band		Tx = 0 dBm - Typical	-0.5	-	0.4	dB
BW20dB	20 dB signal bandwidth		-	-	670	-	KHz
IBSE	In band spurious emission	4 MHz	Bluetooth® Low Energy: -20 dBm	-	-56	-	dBm
		5 MHz	Bluetooth® Low Energy: -20 dBm	-	-57	-	
		≥ 6 MHz	Bluetooth® Low Energy: -30 dBm		-58		
f_d	Frequency drift		Bluetooth® Low Energy: ±50 kHz	-50	-	50	KHz
maxdr	Maximum drift rate		Bluetooth® Low Energy: ±20 KHz / 50 µs	-20	-	20	KHz/ 50 µs
fo	Frequency offset		Bluetooth® Low Energy: ±150 kHz	-150	-	150	KHz
Δf1	Frequency deviation average		Bluetooth® Low Energy: between 450 and 550 kHz	450	-	550	
Δfa	Frequency deviation Δf2 (average) / Δf1 (average)		Bluetooth® Low Energy:> 0.80	0.80	-	-	-
OBSE(2)	Out of band spurious emission	< 1 GHz	-	-	-61	-	dBm
		≥ 1 GHz	-	-	-46	-	

1. :Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

Table 26. RF receiver BLE characteristics (1 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens(1)	High sensitivity mode (SMPS Bypass)	PER <30.8% Bluetooth® Low Energy: max -70 dBm	-96	
	High sensitivity mode (SMPS ON)		-95.5	
$Rssi_{maxrange}$	RSSI maximum value	-	-7	
$Rssi_{minrange}$	RSSI minimum value	-	-94	
$Rssi_{accu}$	RSSI accuracy	-	2	dB
C/Ico	Co-channel rejection	Bluetooth® Low Energy: 21 dB	8	
C/I	Adjacent channel interference	Adj ≥ 5 MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj ≤ -5 MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj = 4 MHz Bluetooth® Low Energy: -27 dB	-48	
		Adj = -4 MHz Bluetooth® Low Energy: -15 dB	-33	
		Adj = 3 MHz Bluetooth® Low Energy: -27 dB	-46	
		Adj = 2 MHz Bluetooth® Low Energy: -17 dB	-39	
		Adj = -2 MHz Bluetooth® Low Energy: -15 dB	-35	
		Adj = 1 MHz Bluetooth® Low Energy: 15 dB	-2	
		Adj = -1 MHz Bluetooth® Low Energy: 15 dB	2	
C/Image	Image rejection (F_{image} = -3 MHz)	Bluetooth® Low Energy: -9 dB	-29	
P_IMD	Intermodulation	|f2-f1| = 3 MHz Bluetooth® Low Energy: -50 dBm	-34	dBm
		|f2-f1| = 4 MHz Bluetooth® Low Energy: -50 dBm	-30	
		|f2-f1| = 5 MHz Bluetooth® Low Energy: -50 dBm	-32	

Table 26. RF receiver BLE characteristics (1 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	dBm
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-5	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-2	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	7	

1. With ideal TX.

Table 27. RF receiver BLE characteristics (2 Mbps)

Symbol	Parameter	Test conditions	Typ	Unit
Prx_max	Maximum input signal	PER <30.8% Bluetooth® Low Energy: min -10 dBm	0	dBm
Psens(1)	High sensitivity mode (SMPS Bypass)	PER <30.8% Bluetooth® Low Energy: max -70 dBm	-93	
	High sensitivity mode (SMPS ON)		-92.5	
$Rssi_{maxrange}$	RSSI maximum value	-	-7	
$Rssi_{minrange}$	RSSI minimum value	-	-94	
$Rssi_{accu}$	RSSI accuracy	-	2	dB
C/Ico	Co-channel rejection	Bluetooth® Low Energy spec: 21 dB	9	
C/I	Adjacent channel interference	Adj ≥ 8MHz Bluetooth® Low Energy: -27 dB	-53	
		Adj ≤ -8 MHz Bluetooth® Low Energy: -27 dB	-50	
		Adj = 6 MHz Bluetooth® Low Energy: -27 dB	-49	
		Adj = -6 MHz Bluetooth® Low Energy: -15 dB	-46	
		Adj = 4 MHz Bluetooth® Low Energy: -17 dB	-42	
		Adj = 2 MHz Bluetooth® Low Energy:15 dB	-3	
		Adj = -2 MHz Bluetooth® Low Energy:15 dB	-3	
C/Image	Image rejection (F_{image} = -4 MHz)	Bluetooth® Low Energy: -9 dB	-26	

Table 27. RF receiver BLE characteristics (2 Mbps) (continued)

Symbol	Parameter	Test conditions	Typ	Unit
P_IMD	Intermodulation	|f2-f1| = 6 MHz Bluetooth® Low Energy: -50 dBm	-29	dBm
		|f2-f1| = 8 MHz Bluetooth® Low Energy: -50 dBm	-30	
		|f2-f1| = 10 MHz Bluetooth® Low Energy: -50 dBm	-29	
P_OBB	Out of band blocking	30 to 2000 MHz Bluetooth® Low Energy: -30 dBm	-3	
		2003 to 2399 MHz Bluetooth® Low Energy: -35 dBm	-9	
		2484 to 2997 MHz Bluetooth® Low Energy: -35 dBm	-3	
		3 to 12.75 GHz Bluetooth® Low Energy: -30 dBm	4	

1. With ideal TX.

Table 28. RF BLE power consumption for V_{DD} = 3.3 V

Symbol	Parameter	Typ	Unit
I_{txmax}	TX maximum output power consumption (SMPS Bypass)	12.7	mA
	TX maximum output power consumption (SMPS On, V_{FBSMPS} = 1.7 V)	7.8	
I_{tx0dbm}	TX 0 dBm output power consumption (SMPS Bypass)	8.8	
	TX 0 dBm output power consumption (SMPS On, V_{FBSMPS} = 1.4 V)	5.2	
I_{rxlo}	Rx consumption (SMPS Bypass)	7.9	
	Rx consumption (SMPS On, V_{FBSMPS} = 1.4 V)	4.5	

6.3.4 RF 802.15.4 characteristics

Table 29. RF transmitter 802.15.4 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{op}	Frequency operating range	-	2405	-	2480	MHz
F_{xtal}	Crystal frequency	-	-	32	-	
ΔF	Delta frequency	-	-	5	-	
Roqpsk	On Air data rate	-	-	250	-	Kbps
PLLres	RF channel spacing	-	-	5	-	MHz

Table 29. RF transmitter 802.15.4 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Prf	Maximum output power(1)	SMPS Bypass or ON (V_{FBSMPS} = 1.7 V) and V_{DD} > 1.95 V)	-	5.7	-	dBm
		SMPS Bypass or ON (V_{FBSMPS} = 1.4 V and V_{DD} > 1.71 V)	-	3.7	-	
	0 dBm output power	-	-	0	-	
	Minimum output power	-	-	-20	-	
Pband	Output power variation over the band	Tx = 0 dBm - Typical	-0.5	-	0.4	dB
EVMrms	EVM rms	Pmax	-	8	-	%
Txpd	Transmit power density	|f - fc| > 3.5 MHz	-	-35	-	dB

1. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 30. RF receiver 802.15.4 characteristics

Symbol	Parameter	Conditions	Typ	Unit
Prx_max	Maximum input signal	Min: -20 dBm and PER < 1%	-10	dBm
Rsens	Sensitivity (SMPS Bypass)	Max: -85 dBm and PER < 1%	-100	
	Sensitivity (SMPS ON)		-98	
C/adj	Adjacent channel rejection	-	35	dB
C/alt	Alternate channel rejection	-	46	

Figure 17. Typical link quality indicator code vs. Rx level

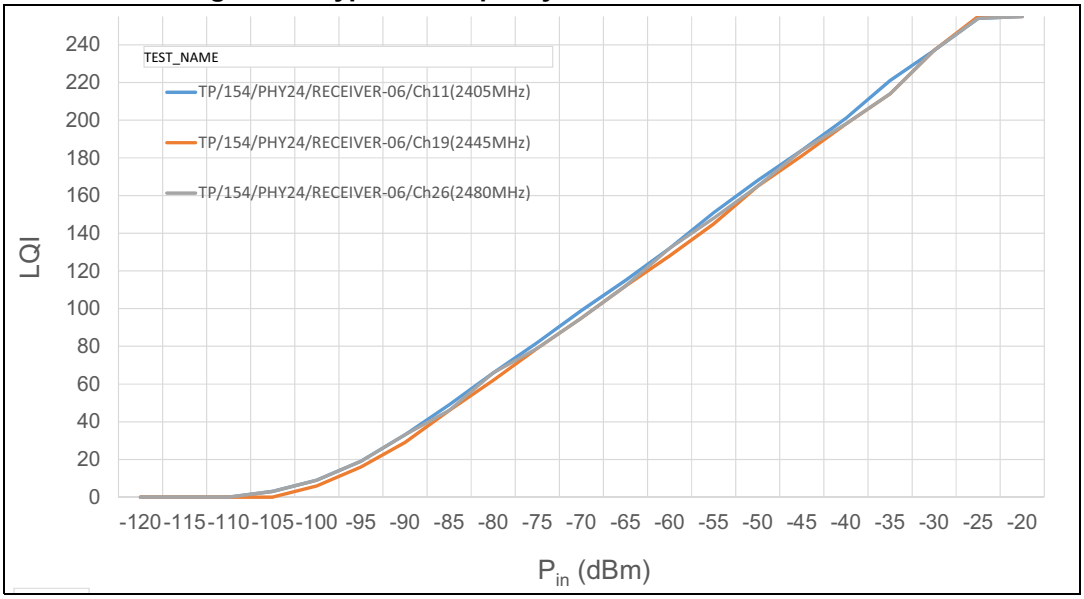


Figure 18. Typical energy detection (T = 27°C, V_{DD} = 3.3 V)

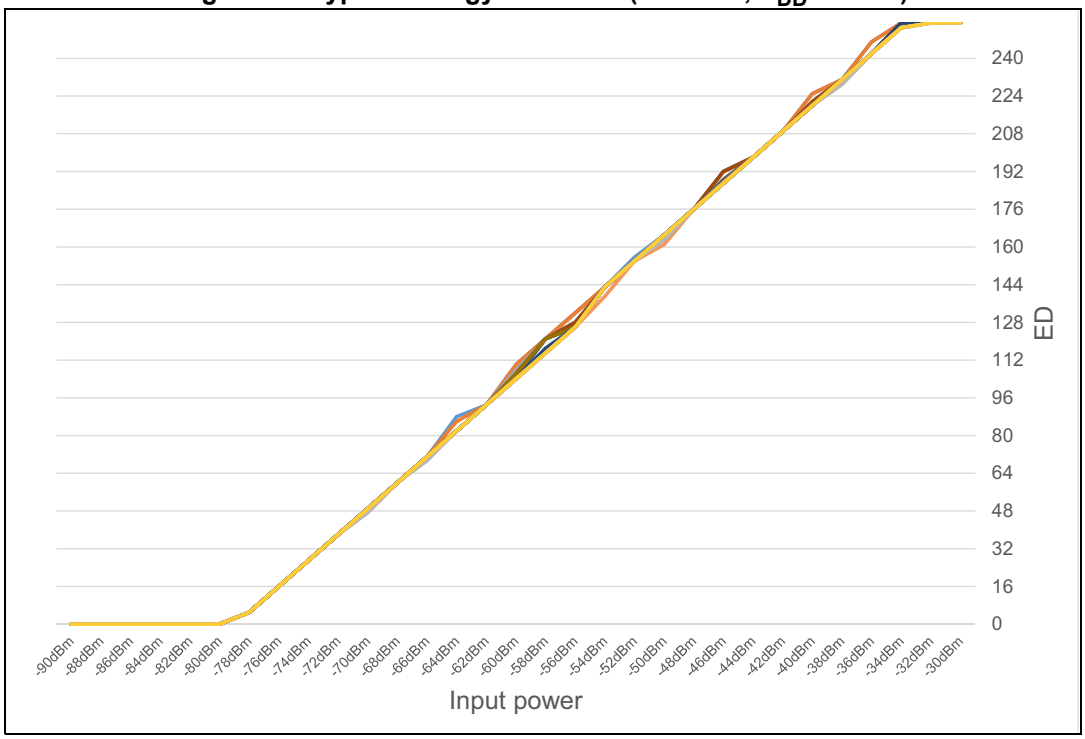


Table 31. RF 802.15.4 power consumption for V_{DD} = 3.3 V

Symbol	Parameter	Typ	Unit
I_{txmax}	TX maximum output power consumption (SMPS Bypass)	11.7	mA
	TX maximum output power consumption (SMPS On, V_{FBSMPS} = 1.7 V)	6.5	
I_{tx0dbm}	TX 0 dBm output power consumption (SMPS Bypass)	9.1	
	TX 0 dBm output power consumption (SMPS On, V_{FBSMPS} = 1.4 V)	4.5	
I_{rxlo}	Rx consumption (SMPS Bypass)	9.2	
	Rx consumption (SMPS On)	4.5	

6.3.5 Operating conditions at power-up / power-down

The parameters given in *Table 32* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 32. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	-	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	
	V_{DDUSB} fall time rate		10	∞	
t_{VDDRF}	V_{DDRF} rise time rate	-	-	∞	
	V_{DDRF} fall time rate		-	∞	

6.3.6 Embedded reset and power control block characteristics

The parameters given in *Table 33* are derived from tests performed under the ambient temperature conditions summarized in *Table 22: General operating conditions*.

Table 33. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$t_{RSTTEMPO}$[2]	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}[2]	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.70	V
		Falling edge	1.60	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.10	2.14	
		Falling edge	1.96	2.00	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.10	2.15	2.19	
		Falling edge	2.00	2.05	2.10	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	
		Falling edge	2.31	2.36	2.41	

Table 33. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	
		Falling edge	1.6	1.64	1.68	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM1}	PVM1 hysteresis	-	-	10	-	
I_{DD} (PVM1)[2]	PVM1 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3)[2]	PVM3 consumption from V_{DD}	-	-	2	-	

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

6.3.7 Embedded voltage reference

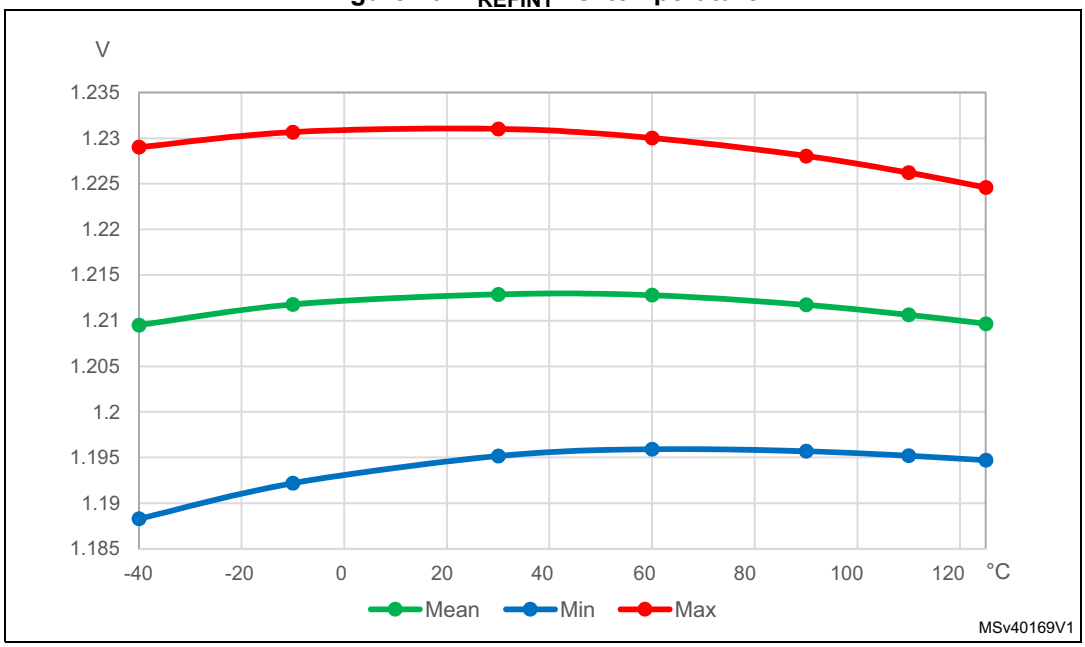
The parameters given in *Table 34* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 34. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +125 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Temperature coefficient	–40 °C < T_A < +125 °C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25 °C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 19. V_{REFINT} vs. temperature



6.3.8 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 16: Current consumption measurement scheme*.

Typical and maximum current consumption

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- For Flash memory and shared peripherals $f_{PCLK} = f_{HCLK} = f_{HCLKS}$

The parameters given in *Table 35* to *Table 46* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 35. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ				Max(1)			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE}$ = 32 MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	Range 2	16 MHz	1.90	1.90	2.00	2.20	2.40	2.52	2.96	mA
				2 MHz	0.960	0.985	1.10	1.25	1.25	1.57	2.05	
			Range 1	64 MHz	8.15	8.25	8.40	8.60	9.30	9.60	10.02	
				32 MHz	4.20	4.25	4.40	4.65	4.25	4.63	5.17	
				16 MHz	2.25	2.30	2.40	2.65	2.65	2.91	3.52	
			SMPS Range 1	64 MHz	5.00	5.00	5.10	5.20	-	-	-	
				32 MHz	3.15	3.15	3.25	3.35	-	-	-	
				16 MHz	2.30	2.30	2.35	2.45	-	-	-	
I_{DD}(LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2 MHz	0.335	0.360	0.470	0.670	0.480	0.910	1.47	
				1 MHz	0.170	0.210	0.325	0.520	0.270	0.730	1.31	
				400 kHz	0.0815	0.120	0.230	0.425	0.140	0.590	1.18	
				100 kHz	0.0415	0.076	0.190	0.385	0.070	0.550	1.14	

1. Guaranteed by characterization results, unless otherwise specified.

Table 36. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ				Max(1)			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE}$ = 32 MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	Range 2	16 MHz	2.00	2.05	2.15	2.30	2.57	3.04	3.64	mA
				2 MHz	0.970	1.00	1.10	1.25	1.62	1.90	2.55	
			Range 1	64 MHz	8.80	8.90	9.00	9.20	10.50	10.80	11.30	
				32 MHz	4.50	4.55	4.70	4.90	4.63	4.89	5.62	
				16 MHz	2.40	2.40	2.55	2.70	2.50	2.70	3.21	
			SMPS Range 1	64 MHz	5.25	5.30	5.35	5.45	-	-	-	
				32 MHz	3.25	3.25	3.35	3.45	-	-	-	
				16 MHz	2.35	2.35	2.40	2.45	-	-	-	
I_{DD}(LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2 MHz	0.265	0.285	0.385	0.550	0.440	0.940	1.620	
				1 MHz	0.135	0.170	0.270	0.430	0.290	0.760	1.480	
				400 kHz	0.066	0.097	0.195	0.360	0.200	0.670	1.380	
				100 kHz	0.031	0.0625	0.160	0.325	0.170	0.470	1.330	

1. Guaranteed by characterization results, unless otherwise specified.

Table 37. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), V_{DD}= 3.3 V

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, f_{HSI16} + PLL ON above 32 MHz All peripherals disable	Range 2 f_{HCLK} = 16 MHz	Reduced code(1)	1.90	mA	119	µA/MHz
				Coremark	1.85		116	
				Dhrystone 2.1	1.85		116	
				Fibonacci	1.75		109	
				While(1)	1.60		100	
			Range 1 f_{HCLK} = 64 MHz	Reduced code(1)	8.15	mA	127	µA/MHz
				Coremark	8.00		125	
				Dhrystone 2.1	8.10		127	
				Fibonacci	7.60		119	
				While(1)	6.85		107	
			Range 1, SMPS On f_{HCLK} = 64 MHz	Reduced code(1)	5.00	mA	78	µA/MHz
				Coremark	4.95		77	
				Dhrystone 2.1	4.95		77	
				Fibonacci	4.75		74	
				While(1)	4.40		69	
			Range 1, SMPS On f_{HCLK} = 64 MHz, When RF Tx level = 0 dBm(2)	Reduced code(1)	4.07	mA	64	µA/MHz
				Coremark	3.99		62	
				Dhrystone 2.1	4.04		63	
				Fibonacci	3.79		59	
				While(1)	3.42		53	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz All peripherals disable		Reduced code(1)	320	µA	160	µA/MHz
				Coremark	350		175	
				Dhrystone 2.1	350		175	
				Fibonacci	390		195	
				While(1)	225		113	

1. Reduced code used for characterization results provided in *Table 35* and *Table 36*.
2. Value computed. MCU consumption when RF TX and SMPS are ON.

Table 38. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, V_{DD} = 3.3 V

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, f_{HSI16} + PLL ON above 32 MHz All peripherals disable	Range 2 f_{HCLK} = 16 MHz	Reduced code(1)	2.00	mA	125	µA/MHz
				Coremark	1.75		109	
				Dhrystone 2.1	1.95		122	
				Fibonacci	1.85		116	
				While(1)	1.85		116	
			Range 1 f_{HCLK} = 64 MHz	Reduced code(1)	8.80	mA	138	µA/MHz
				Coremark	7.50		117	
				Dhrystone 2.1	8.60		134	
				Fibonacci	7.90		123	
				While(1)	8.00		125	
			Range 1, SMPS On f_{HCLK} = 64 MHz	Reduced code(1)	5.25	mA	82	µA/MHz
				Coremark	4.65		73	
				Dhrystone 2.1	5.15		80	
				Fibonacci	4.85		76	
				While(1)	4.90		77	
			Range 1, SMPS On f_{HCLK} = 64 MHz, When RF Tx level = 0 dBm(2)	Reduced code(1)	4.39	mA	69	µA/MHz
				Coremark	3.74		58	
				Dhrystone 2.1	4.29		67	
				Fibonacci	3.94		62	
				While(1)	3.99		62	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz All peripherals disable		Reduced code(1)	255	µA	128	µA/MHz
				Coremark	205		103	
				Dhrystone 2.1	250		125	
				Fibonacci	230		115	
				While(1)	220		110	

1. Reduced code used for characterization results provided in *Table 35* and *Table 36*.
2. Value computed. MCU consumption when RF TX and SMPS are ON.

Table 39. Current consumption in Sleep and Low-power sleep modes, Flash memory ON

Symbol	Parameter	Conditions			TYP				MAX(1)			Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSI16}$ up to 16 MHz included, $f_{HCLK} = f_{HSE}$ up to 32 MHz f_{HSI16} + PLL ON above 32 MHz All peripherals disabled	Range 2	16 MHz	0.740	0.765	0.865	1.05	0.840	1.210	1.810	mA
			Range 1	64 MHz	2.65	2.70	2.80	3.00	3.00	3.33	3.91	
				32 MHz	1.40	1.45	1.60	1.80	1.55	1.86	2.49	
				16 MHz	0.845	0.875	0.990	1.20	0.970	1.40	2.02	
			SMPS Range 1	64 MHz	2.60	2.60	2.65	2.75	-	-	-	
				32 MHz	1.90	1.95	2.00	2.10	-	-	-	
				16 MHz	1.70	1.70	1.75	1.80	-	-	-	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ All peripherals disabled		2 MHz	0.090	0.125	0.235	0.430	0.130	0.600	1.19	
				1 MHz	0.058	0.093	0.205	0.400	0.090	0.570	1.16	
				400 kHz	0.044	0.0725	0.185	0.380	0.070	0.540	1.11	
				100 kHz	0.0315	0.0635	0.0175	0.370	0.055	0.530	1.13	

1. Guaranteed by characterization results, unless otherwise specified.

Table 40. Current consumption in Low-power sleep modes, Flash memory in Power down

Symbol	Parameter	Conditions		TYP				MAX(1)			Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	25 °C	85 °C	105 °C	
I_{DD}(LPSleep)	Supply current in low-power sleep	$f_{HCLK} = f_{MSI}$ All peripheral	2 MHz	94.0	115	200	335	135	610	1201	µA
			1 MHz	56.5	86.0	170	305	94.2	560	1171	
			400 kHz	40.5	66.5	150	285	68.0	540	1129	
			100 kHz	27.5	57.5	140	275	54.6	539	1131	

1. Guaranteed by characterization results, unless otherwise specified.

Table 41. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	LCD disabled BLE disabled	1.8 V	1.00	1.85	3.15	5.95	21.5	50.0	1.58	4.12	56.9	132.7	µA
			2.4 V	1.10	1.85	3.20	6.00	22.0	51.0	-	-	-	-	
			3.0 V	1.10	1.85	3.25	6.10	22.0	52.0	1.60	4.17	57.9	135.6	
			3.6 V	1.15	1.95	3.35	6.25	23.0	53.0	1.69	4.40	58.6	135.7	
		LCD enabled(2) and clocked by LSI BLE disabled	1.8 V	1.20	2.00	3.35	6.10	22.0	50.5	1.76	4.30	57.1	133.3	
			2.4 V	1.20	2.00	3.40	6.20	22.0	51.0	-	-	-	-	
			3.0 V	1.25	2.10	3.45	6.30	22.5	52.0	1.85	4.41	58.1	135.8	
			3.6 V	1.30	2.15	3.60	6.55	23.0	53.5	1.97	4.66	59.4	136.6	
I_{DD} (Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled, BLE disabled	RTC clocked by LSI, LCD disabled	1.8 V	1.30	2.10	3.45	6.25	22.0	50.5	1.91	4.50	57.2	133.0	
			2.4 V	1.45	2.25	3.55	6.40	22.5	51.5	-	-	-	-	
			3.0 V	1.50	2.30	3.70	6.55	22.5	52.5	2.11	4.64	58.3	136.1	
			3.6 V	1.75	2.50	3.95	6.85	23.5	53.5	2.26	5.12	59.7	136.9	
		RTC clocked by LSI, LCD enabled(2)	1.8 V	1.35	2.20	3.55	6.30	22.0	50.5	1.99	4.57	57.4	133.8	
			2.4 V	1.50	2.35	3.65	6.50	22.5	51.5	-	-	-	-	
			3.0 V	1.70	2.45	3.85	6.65	23.0	52.5	2.17	4.87	58.4	136.3	
			3.6 V	1.80	2.60	4.05	6.95	23.5	54.0	2.41	5.11	59.9	137.1	
		RTC clocked by LSE quartz(3) in low drive mode	1.8 V	1.35	2.20	3.50	6.25	22.0	50.5	1.91	4.29	57.1	133.5	
			2.4 V	1.45	2.25	3.65	6.40	22.5	51.5	-	-	-	-	
			3.0 V	1.55	2.45	3.80	6.65	23.0	52.5	2.01	4.31	58.0	135.9	
			3.6 V	1.70	2.55	4.05	6.95	23.5	54.0	2.16	4.40	81.6	137.0	

Table 41. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode bypass mode	Wakeup clock is HSI16, voltage Range 2. See(4).	3.0 V	-	389	-	-	-	-	-	-	-	-	µA
		Wakeup clock is MSI = 32 MHz, voltage Range 1. See(4).	3.0 V	-	320	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See(4).	3.0 V	-	528	-	-	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in *Table 49: Low-power mode wakeup timings*.

Table 42. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	BLE disabled LCD disabled	1.8 V	5.05	9.20	15.5	28.0	96.0	210	7.00	28.4	343.7	738.6	µA
			2.4 V	5.10	9.25	15.5	28.5	96.5	215	-	-	-	-	
			3.0 V	5.15	9.30	15.5	28.5	97.0	215	7.07	28.5	346.8	746.0	
			3.6 V	5.25	9.45	16.0	29.0	97.5	215	7.30	28.8	351.0	749.4	
		BLE disabled LCD enabled(2), clocked by LSI	1.8 V	5.05	9.30	15.5	28.5	96.0	210	7.10	28.7	344.4	739.0	
			2.4 V	5.10	9.35	16.0	28.5	96.5	215	-	-	-	-	
			3.0 V	5.20	9.65	16.0	28.5	97.0	215	7.26	29.6	345.0	747.0	
			3.6 V	5.55	9.85	16.0	29.0	98.5	215	7.62	29.8	349.0	750.8	
I_{DD} (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC enabled, BLE disabled	RTC clocked by LSI LCD disabled	1.8 V	5.30	9.35	16.0	28.5	96.5	215	7.30	29.5	343.7	739.2	
			2.4 V	5.40	9.45	16.0	28.5	97.0	215	-	-	-	-	
			3.0 V	5.70	9.55	16.5	29.0	98.5	220	7.69	29.7	347.2	746.1	
			3.6 V	5.85	10.0	16.5	29.5	96.5	215	8.08	29.8	349.9	751.1	
		RTC clocked by LSI LCD enabled(2)	1.8 V	5.25	9.60	16.0	28.5	96.5	215	7.10	29.0	344.3	739.9	
			2.4 V	5.30	9.75	16.0	29.0	97.0	215	-	-	-	-	
			3.0 V	5.85	9.80	16.5	29.0	97.5	215	7.53	29.8	347.4	746.2	
			3.6 V	5.90	10.5	16.5	29.0	98.5	220	8.18	29.9	350.6	751.8	
		RTC clocked by LSE quartz(3) in Low drive mode	1.8 V	5.35	9.55	16.0	28.5	96.5	215	6.00	28.7	343.9	738.7	
			2.4 V	5.40	9.70	16.0	29.0	96.5	215	-	-	-	-	
			3.0 V	5.75	9.70	16.0	29.0	97.5	215	7.40	28.9	346.6	743.8	
			3.6 V	5.90	10.0	16.5	29.5	99.0	220	7.58	29.2	349.0	749.9	

Table 42. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (wakeup from Stop1)	Supply current during wakeup from Stop 1 bypass mode	Wakeup clock HSI16, voltage Range 2. See (4).	3.0 V	-	129	-	-	-	-	-	-	-	-	µA
		Wakeup clock MSI = 32 MHz, voltage Range 1. See (4).	3.0 V	-	124	-	-	-	-	-	-	-	-	
		Wakeup clock MSI = 4 MHz, voltage Range 2. See (4).	3.0 V	-	207	-	-	-	-	-	-	-	-	

1. Guaranteed based on test during characterization, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 49: Low-power mode wakeup timings*.

Table 43. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Stop 0)	Supply current in Stop 0 mode, RTC disabled, BLE disabled, LCD disabled	--	1.8 V	95.5	100	110	120	195	315	110.0	114.2	458.1	874.8	µA
			2.4 V	97.5	105	110	125	195	315	-	-	-	-	
			3.0 V	98.5	105	110	125	195	320	117.3	134.3	461.8	880.0	
			3.6 V	100	105	115	125	200	320	165.0	135.7	494.0	884.1	
	Supply current during wakeup from Stop 0 Bypass mode	Wakeup clock HSI16, voltage Range 2. See (2).	3.0 V	-	331	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 32 MHz, voltage Range 1. See (2).	3.0 V	-	349	-	-	-	-	-	-	-	-	
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See (2).	3.0 V	-	196	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in *Table 49: Low-power mode wakeup timings*.

Table 44. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC disabled	BLE disabled No independent watchdog	1.8 V	0.270	0.320	0.515	0.920	3.45	8.20	0.300	0.828	7.850	19.300	µA
			2.4 V	0.270	0.350	0.540	0.955	3.50	8.80	-	-	-	-	
			3.0 V	0.270	0.370	0.575	1.00	3.85	9.50	0.380	0.945	8.505	21.200	
			3.6 V	0.300	0.410	0.645	1.15	4.20	10.50	0.400	1.040	8.980	22.400	
		BLE disabled With independent watchdog	1.8 V	0.265	0.525	0.710	1.10	3.90	8.40	0.520	1.095	8.041	19.500	
			2.4 V	0.280	0.595	0.790	1.20	4.00	9.05	-	-	-	-	
			3.0 V	0.290	0.670	0.855	1.35	4.15	9.80	0.730	1.253	8.774	21.400	
			3.6 V	0.295	0.770	0.990	1.50	4.60	11.00	0.851	1.356	9.360	22.840	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers and SRAM2a retained), RTC enabled BLE disabled	RTC clocked by LSI, no independent watchdog	1.8 V	0.500	0.600	0.780	1.20	3.70	8.45	0.680	1.165	8.143	19.660	
			2.4 V	0.630	0.705	0.910	1.30	3.80	9.10	-	-	-	-	
			3.0 V	0.725	0.825	1.050	1.50	3.95	9.90	0.930	1.463	8.977	21.440	
			3.6 V	0.860	0.970	1.200	1.70	4.25	11.00	1.050	1.628	9.634	23.080	
		RTC clocked by LSI, with independent watchdog	1.8 V	0.565	0.655	0.830	1.25	3.75	8.55	0.734	1.196	8.187	19.710	
			2.4 V	0.635	0.790	0.975	1.40	4.10	9.20	-	-	-	-	
			3.0 V	0.725	0.915	1.100	1.55	4.50	10.00	1.028	1.573	9.072	21.810	
			3.6 V	0.870	1.050	1.300	1.80	4.90	11.00	1.144	1.723	9.730	23.200	
		RTC clocked by LSE quartz (2) in low drive mode	1.8 V	0.525	0.625	0.840	1.25	3.75	8.60	0.600	1.061	8.029	19.610	
			2.4 V	0.665	0.755	0.960	1.35	4.05	9.25	-	-	-	-	
			3.0 V	0.775	0.880	1.100	1.55	4.40	10.00	0.600	1.100	8.719	21.570	
			3.6 V	0.935	1.050	1.300	1.80	5.00	11.00	0.750	1.171	9.460	23.030	

Table 44. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (SRAM2a)(3)	Supply current to be subtracted in Standby mode when SRAM2a is not retained	-	1.8 V	0.160	0.210	0.380	0.660	2.30	5.15	-	-	-	-	µA
			2.4 V	0.165	0.245	0.375	0.650	2.15	5.20	-	-	-	-	
			3.0 V	0.155	0.250	0.385	0.630	2.25	5.20	-	-	-	-	
			3.6 V	0.155	0.235	0.375	0.670	2.20	5.20	-	-	-	-	
I_{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is HSI16. See (4). SMPS OFF	3.0 V	-	1.73	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. The supply current in Standby with SRAM2a mode is: I_{DD}(Standby) + I_{DD}(SRAM2a). The supply current in Standby with RTC with SRAM2a mode is: I_{DD}(Standby + RTC) + I_{DD}(SRAM2a).
4. Wakeup with code execution from Flash memory. Average value given for a typical wakeup time as specified in *Table 49*.

Table 45. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP						MAX(1)				Unit
		-	V_{DD}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	85 °C	105 °C	
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	0.039	0.013	0.030	0.100	0.635	1.950	-	-	2.099	6.200	µA
			2.4 V	0.059	0.014	0.055	0.120	0.785	2.350	-	-	-	-	
			3.0 V	0.064	0.037	0.070	0.180	1.000	2.900	-	0.185	2.670	7.490	
			3.6 V	0.071	0.093	0.140	0.280	1.300	3.700	-	0.247	3.120	8.450	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE quartz (2) in low drive mode	1.8 V	0.320	0.315	0.355	0.420	0.985	2.300	-	0.572	2.702	6.180	
			2.4 V	0.425	0.405	0.460	0.540	1.200	2.800	-	-	-	-	
			3.0 V	0.535	0.535	0.595	0.700	1.500	3.450	-	0.664	2.990	7.800	
			3.6 V	0.695	0.720	0.790	0.940	2.000	4.350	-	0.790	3.730	9.140	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 46. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP						MAX(1)						Unit
		-	V_{BAT}	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	
I_{DD}(VBAT)	Backup domain supply current	RTC disabled	1.8 V	1.00	2.00	4.00	10.0	52.0	145	-	-	-	-	-	-	nA
			2.4 V	1.00	2.00	5.00	12.0	60.0	165	-	-	-	-	-	-	
			3.0 V	2.00	4.00	7.00	16.0	75.0	225	-	-	-	-	-	-	
			3.6 V	7.00	15.0	23.0	42.0	170	450	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	295	305	315	325	380	480	-	-	-	-	-	-	
			2.4 V	385	395	400	415	475	595	-	-	-	-	-	-	
			3.0 V	495	505	515	530	600	765	-	-	-	-	-	-	
			3.6 V	630	645	660	685	830	1150	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 47. Current under Reset condition

Symbol	Conditions	TYP						MAX(1)						Unit
		0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	0 °C	25 °C	40 °C	55 °C	85 °C	105 °C	
$I_{DD(RST)}$	1.8 V	-	410	-	-	-	-	-	-	-	-	-	-	µA
	2.4 V	-	-	-	-	-	-	-	-	-	-	-	-	
	3.0 V	-	550	-	-	-	-	-	750	-	-	-	-	
	3.6 V	-	750	-	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 69: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 48: Peripheral current consumption*, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the I/O supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{IO} + C_{EXT}$
- C_{IO} is the I/O pin capacitance
- C_{EXT} is the PCB board capacitance plus any connected external device pin capacitance.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 48*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 18: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 48*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 48. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB1	Bus Matrix(1)	2.40	2.00	1.80	µA/MHz
	TSC	1.25	1.05	1.05	
	CRC	0.465	0.375	0.380	
	DMA1	1.90	1.55	1.80	
	DMA2	2.00	1.65	1.80	
	DMAMUX	4.15	3.40	4.45	
	All AHB1 Peripherals	12.0	10.0	11.5	
AHB2(2)	AES1	4.00	3.30	3.90	
	ADC independent clock domain	2.55	2.10	2.10	
	ADC clock domain	2.25	1.90	1.90	
	All AHB2 Peripherals	7.45	6.20	6.60	
AHB3	QSPI	7.60	6.25	7.10	
AHB Shared	TRNG independent clock domain	3.80	N/A	N/A	
	TRNG clock domain	2.00	N/A	N/A	
	SRAM2	0.170	0.135	0.135	
	FLASH	8.35	6.90	8.45	
	AES2	6.95	5.75	7.00	
	PKA	4.40	3.65	4.25	
	All AHB Shared Peripherals	17.5	14.5	16.0	

Table 48. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	RTCA	1.10	0.88	1.25	µA/MHz
	CRS	0.24	0.20	0.20	
	USB FS independent clock domain	3.20	N/A	N/A	
	USB FS clock domain	2.05	N/A	N/A	
	I2C1 independent clock domain	2.50	4.40	4.40	
	I2C1 clock domain	4.80	4.00	5.50	
	I2C3 independent clock domain	2.10	3.50	3.55	
	I2C3 clock domain	3.70	3.10	3.55	
	LCD	1.35	1.10	2.10	
	SPI2	1.65	1.40	2.25	
	LPTIM1 independent clock domain	2.10	3.40	3.00	
	LPTIM1 clock domain	3.60	3.00	3.80	
	TIM2	5.65	4.70	4.90	
	LPUART1 independent clock domain	2.70	4.15	3.85	
	LPUART1 clock domain	4.45	3.70	5.25	
	LPTIM2 clock domain	3.95	3.25	4.50	
	LPTIM2 independent clock domain	2.20	3.70	3.80	
	WWDG	0.335	0.285	0.965	
	All APB1 Peripherals	27.0	22.5	25.5	
APB2	AHB to APB2(3)	1.10	0.885	1.35	
	TIM1	8.20	6.80	7.25	
	TIM17	2.85	2.40	2.40	
	TIM16	2.75	2.30	2.55	
	USART1 independent clock domain	4.40	7.80	7.00	
	USART1 clock domain	8.80	7.30	7.75	
	SPI1	1.75	1.45	1.45	
	SAI1 independent clock domain	2.50	1.50	3.50	
	SAI1 clock domain	2.40	N/A	N/A	
	All APB2 on	28.0	23.0	25.5	
ALL		97.5	80.5	90.0	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. GPIOs consumption during read and write accesses.
3. The AHB to APB2 bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.9 Wakeup time from Low-power modes and voltage scaling transition times

The wakeup times given in *Table 49* are the latency between the event and the execution of the first user instruction.

The device goes in Low-power mode after the WFE (Wait For Event) instruction.

Table 49. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		9	10	No. of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with memory in power-down during low-power sleep mode (FPDS = 1 in PWR_CR1) and with clock MSI = 2 MHz		9	10	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash memory	Range 1	Wakeup clock MSI = 32 MHz	2.38	2.96	µs
			Wakeup clock HSI16 = 16 MHz	1.69	2.00	
		Range 2	Wakeup clock HSI16 = 16 MHz	1.70	2.01	
			Wakeup clock MSI = 4 MHz	7.43	8.59	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 32 MHz	2.63	3.00	
			Wakeup clock HSI16 = 16 MHz	1.80	2.00	
		Range 2	Wakeup clock HSI16 = 16 MHz	1.82	2.02	
			Wakeup clock MSI = 4 MHz	7.58	8.70	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash memory SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	4.67	5.56	
			Wakeup clock HSI16 = 16 MHz	5.09	6.03	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.08	6.00	
			Wakeup clock MSI = 4 MHz	8.36	9.28	
	Wake up time from Stop 1 mode to Run in SRAM1 SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	4.88	5.55	
			Wakeup clock HSI16 = 16 MHz	5.29	5.95	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.28	5.96	
			Wakeup clock MSI = 4 MHz	8.49	9.30	
	Wake up time from Stop 1 mode to Low-power run mode in Flash memory	Regulator in Low-power mode (LPR = 1 in PWR_CR1)	Wakeup clock MSI = 4 MHz	7.96	9.59	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			8.00	9.47	

Table 49. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash memory SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	5.27	6.07	µs
			Wakeup clock HSI16 = 16 MHz	5.71	6.52	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.72	6.52	
			Wakeup clock MSI = 4 MHz	9.10	9.93	
	Wake up time from Stop 2 mode to Run mode in SRAM1 SMPS bypassed	Range 1	Wakeup clock MSI = 32 MHz	5.20	5.94	
			Wakeup clock HSI16 = 16 MHz	5.64	6.42	
		Range 2	Wakeup clock HSI16 = 16 MHz	5.64	6.43	
			Wakeup clock MSI = 4 MHz	9.05	9.85	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode SMPS Bypassed	Range 1	Wakeup clock HSI16 = 16 MHz	51.0	58.1	µs

1. Guaranteed by characterization results (V_{DD} = 3 V, .T = 25 °C).

Table 50. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode(2)	Code run with MSI 2 MHz	15.33	16.30	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with HSI16	21.4	28.9	

1. Guaranteed by characterization results (V_{DD} = 3 V, T = 25 °C).
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 51. Wakeup time using LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPUART}$	Wakeup time needed to calculate the maximum LPUART baud rate allowing to wakeup up from Stop mode when LPUART clock source is HSI16	Stop mode 0	-	1.7	µs
		Stop mode 1/2	-	8.5	

1. Guaranteed by design.

6.3.10 External clock source characteristics

High-speed external user clock generated from an external source

The high-speed external (HSE) clock must be supplied with a 32 MHz crystal oscillator.

The STM32WB55xx include internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one.

The characteristics in *Table 52* and *Table 53* are measured over recommended operating conditions, unless otherwise specified. Typical values are referred to T_A = 25 °C and V_{DD} = 3.0 V.

Table 52. HSE crystal requirements(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{NOM}	Oscillator frequency	-	-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.	-	-	20	ppm
C_L	Load capacitance	-	6	-	8	pF
ESR	Equivalent series resistance	-	-	-	100	Ω
P_D	Drive level	-	-	-	100	µW

1. 32 MHz XTAL is specified for two specific references: NX2016SA and NX1612SA.

Table 53. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SUA(HSE)}$	Startup time for 80% amplitude stabilization	V_{DDRF} stabilized, XOTUNE=000000, -40 to +125 °C range	-	1000	-	µs
$t_{SUR(HSE)}$	Startup time for XOREADY signal	V_{DDRF} stabilized, XOTUNE=000000, -40 to +125 °C range	-	250	-	
$I_{DDRF(HSE)}$	HSE current consumption	HSEGMC=000, XOTUNE=000000	-	50	-	µA
$XOT_{g(HSE)}$	XOTUNE granularity	Capacitor bank	-	1	5	ppm
$XOT_{fp(HSE)}$	XOTUNE frequency pulling		±20	±40	-	
$XOT_{nb(HSE)}$	XOTUNE number of tuning bits		-	6	-	bit
$XOT_{st(HSE)}$	XOTUNE setting time		-	-	0.1	ms

Note: For information about the trimming of the oscillator, refer to application note AN5042 "HSE trimming for RF applications using the STM32WB Series".

Low-speed external user clock generated from an external source

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. The information provided in this section is based on design simulation results obtained with typical external components specified in *Table 54*. In the application, the

resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time.

Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

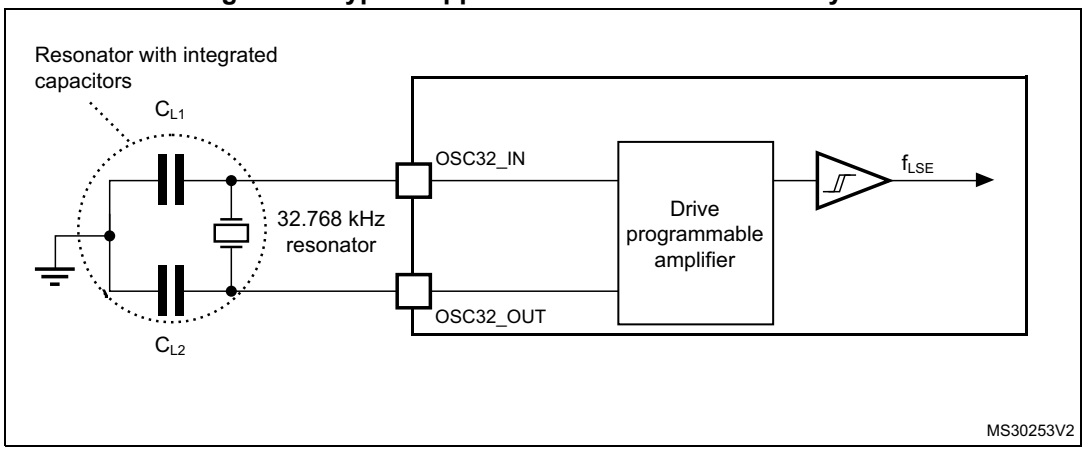
Table 54. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$G_{mcritmax}$	Maximum critical crystal g_m	LSEDRV[1:0] = 00 Low drive capability	-	-	0.50	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.70	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.70	
$t_{SU(LSE)}$(2)	Startup time	V_{DD} stabilized	-	2	-	s

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stable 32 MHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal refer to application note AN2867 "Oscillator design guide for STM8S, STM8A and STM32 microcontrollers" available from www.st.com.

Figure 20. Typical application with a 32.768 kHz crystal



Note: No external resistors are required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics detailed in *Section 6.3.17*. The recommend clock input waveform is shown in *Figure 21*.

Figure 21. Low-speed external clock source AC timing diagram

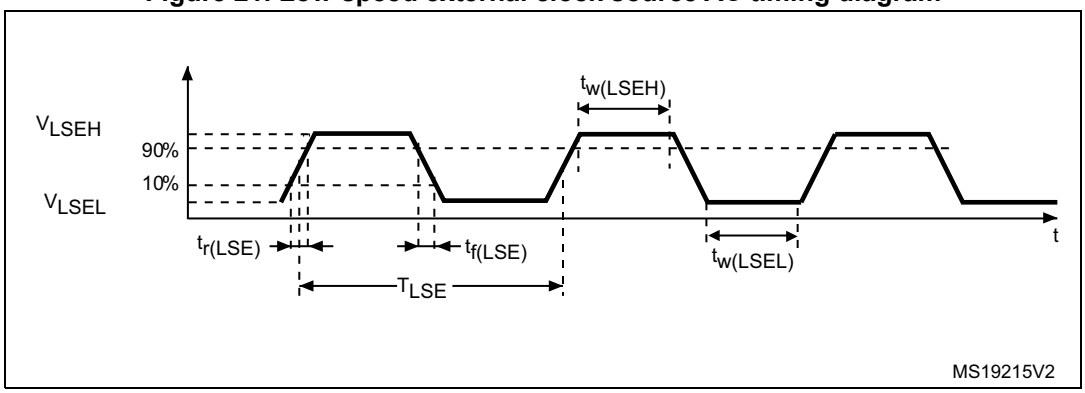


Table 55. Low-speed external user clock characteristics(1) – Bypass mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	21.2	32.768	44.4	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDx}	-	V_{DDx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns
f_{tolLSE}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling	-500	-	+500	ppm

1. Guaranteed by design.

6.3.11 Internal clock source characteristics

The parameters given in *Table 56* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. The provided curves are characterization results, not tested in production.

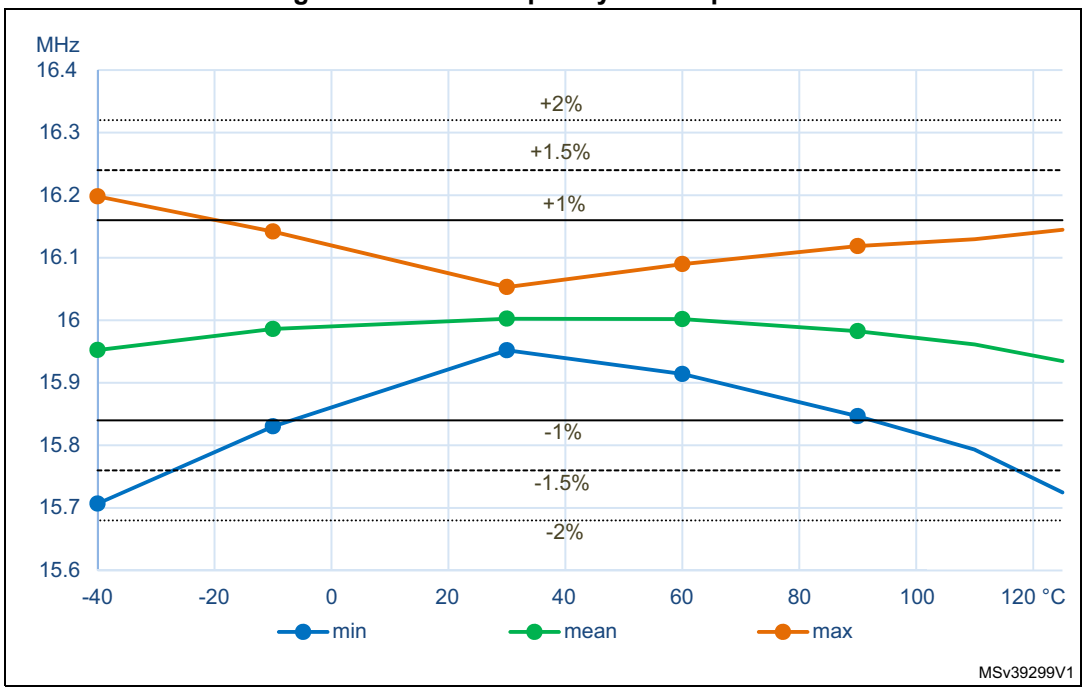
High-speed internal (HSI16) RC oscillator

Table 56. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	
		T_A= -40 to 125 °C	-2	-	1.5	
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 22. HSI16 frequency vs. temperature



Multi-speed internal (MSI) RC oscillator

Table 57. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	789.6	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
Δ_{TEMP}(MSI)(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

Table 57. MSI oscillator characteristics(1) (continued)

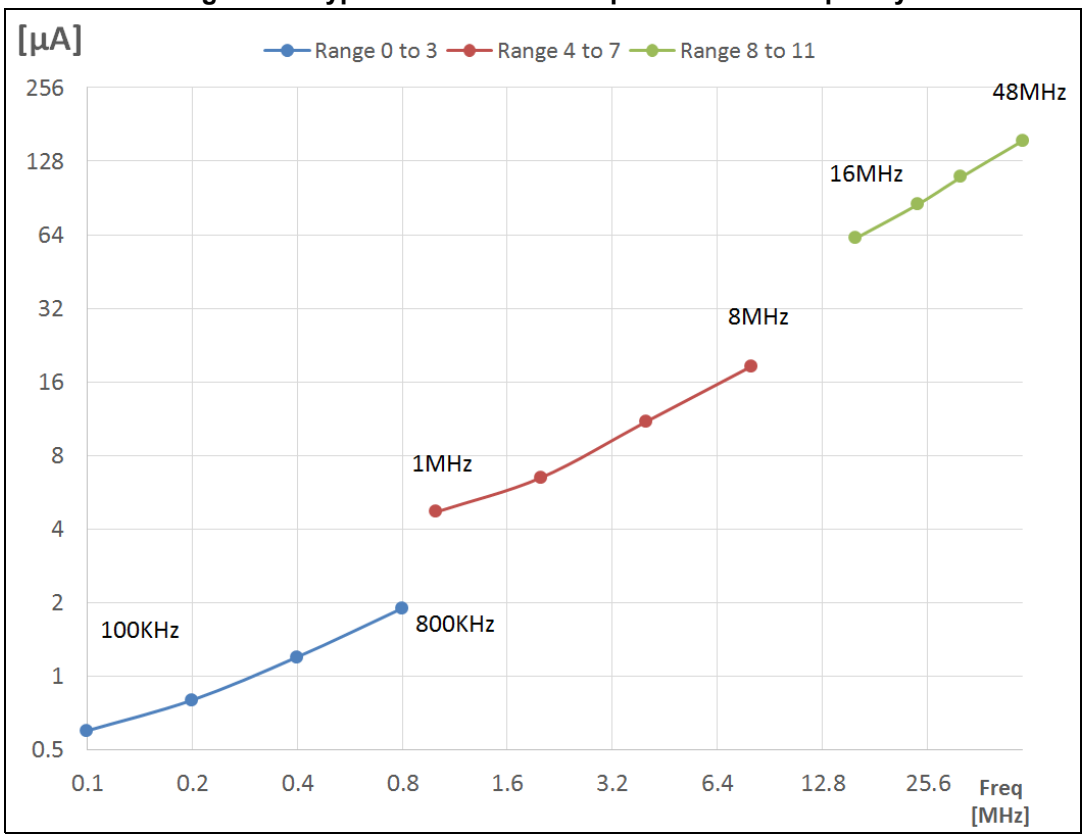
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
Δ_{VDD}(MSI)(2)	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD} = 1.62 to 3.6 V	-1.2	-	0.5	%
				V_{DD} = 2.4 to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD} = 1.62 to 3.6 V	-2.5	-	0.7	
				V_{DD} = 2.4 to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD} = 1.62 to 3.6 V	-5	-	1	
				V_{DD} = 2.4 to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}$ (MSI)(2)(6)	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		-	1	2	
			T_A= -40 to 125 °C		-	2	4	
P_USB Jitter(MSI)(6)	Period jitter for USB clock(4)	PLL mode Range 11	For next transition	-	-	-	3.458	ns
			For paired transition	-	-	-	3.916	
MT_USB Jitter(MSI)(6)	Medium term jitter for USB clock(5)	PLL mode Range 11	For next transition	-	-	-	2	
			For paired transition	-	-	-	1	
CC jitter(MSI)(6)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(6)	RMS period jitter	PLL mode Range 11		-	-	50	-	
t_{SU}(MSI)(6)	MSI oscillator start-up time	Range 0		-	-	10	20	µs
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
t_{STAB}(MSI)(6)	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 57. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{DD}(MSI)^{(6)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Average period of MSI at 48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI at 48 MHz clock.
5. Only accumulated jitter of MSI at 48 MHz is extracted over 28 cycles.
   For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI at 48 MHz, for 1000 captures over 28 cycles.
   For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI at 48 MHz, for 1000 captures over 56 cycles.
6. Guaranteed by design.

Figure 23. Typical current consumption vs. MSI frequency



High-speed internal 48 MHz (HSI48) RC oscillator

Table 58. HSI48 oscillator characteristics(1)

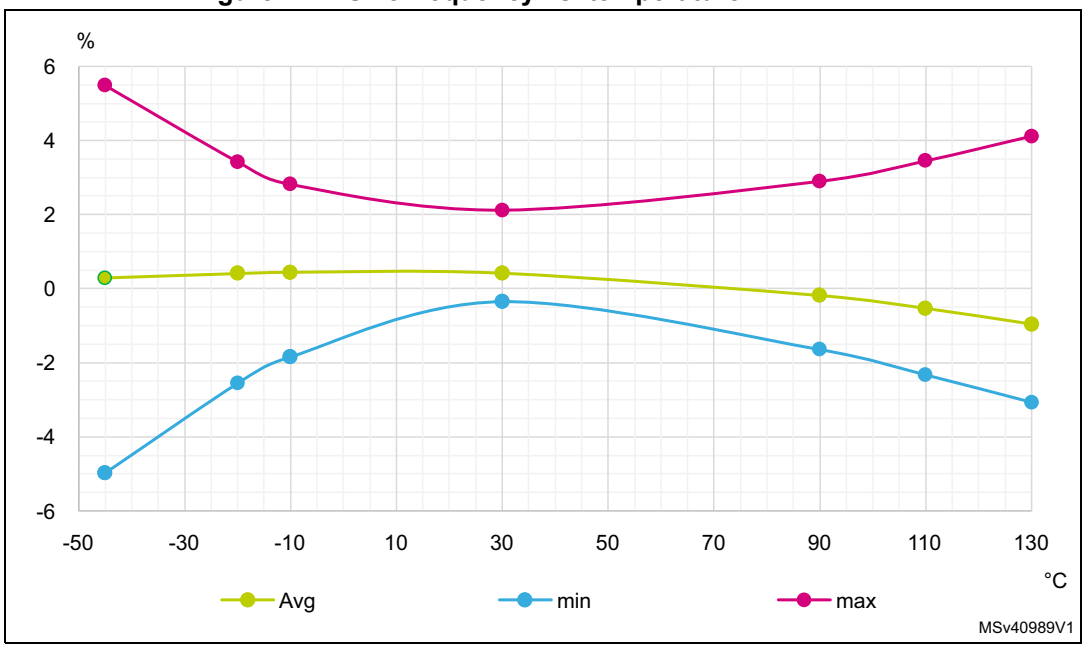
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD} = 3.0 V, T_A = 30 °C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	
DuCy(HSI48)	Duty cycle	-	45(2)	-	55(2)	
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA

Table 58. HSI48 oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	±0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	±0.25(2)	-	

1. V_{DD} = 3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 24. HSI48 frequency vs. temperature



Low-speed internal (LSI) RC oscillator

Table 59. LSI1 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI1 frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI1)$(2)	LSI1 oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI1)$(2)	LSI1 oscillator stabilization time	5% of final frequency	-	125	180	
$I_{DD}(LSI1)$(2)	LSI1 oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 60. LSI2 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI2}	LSI2 frequency	V_{DD} = 3.0 V, T_A = 30 °C	21.6	-	44.2	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	21.2	-	44.4	
$t_{SU}(LSI2)$(2)	LSI2 oscillator start-up time	-	0.7	-	3.5	ms
$I_{DD}(LSI2)$(2)	LSI2 oscillator power consumption	-	-	500	1180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.12 PLL characteristics

The parameters given in *Table 61* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 61. PLL, PLLSAI1 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2	-	64	MHz
		Voltage scaling Range 2	2	-	16	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	64	
		Voltage scaling Range 2	8	-	16	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	64	
		Voltage scaling Range 2	8	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 64 MHz	-	40	-	ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 96 MHz	-	200	260	µA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the two PLLs.

6.3.13 Flash memory characteristics

Table 62. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	90.8	µs
t_{prog_row}	One row (64 double word) programming time	Normal programming	5.2	5.5	ms
		Fast programming	3.8	4.0	
t_{prog_page}	One page (4 KByte) programming time	Normal programming	41.8	43.0	
		Fast programming	30.4	31.0	
t_{ERASE}	Page (4 KByte) erase time	-	22.0	24.5	
t_{ME}	Mass erase time	-	22.1	25.0	
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 6 µs)	-	
		Erase mode	7 (for 67 µs)	-	

1. Guaranteed by design.

Table 63. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 64*. They are based on the EMS levels and classes defined in application note AN1709 “EMC design guide for STM8, STM32 and Legacy MCUs”, available on *www.st.com*.

Table 64. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flow must include the management of runaway conditions such as:

- corrupted program counter
- unexpected reset
- critical data corruption (e.g. control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard, which specifies the test board and the pin loading.

Table 65. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Peripheral ON SMPS OFF or ON [f_{HSE} / f_{CPUM4}, f_{CPUM0}]	Unit
				32 MHz / 64 MHz, 32 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, WLCSP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	1	dBµV
			30 MHz to 130 MHz	4	
			130 MHz to 1 GHz	-1	
			1 GHz to 2 GHz	7	
			EMI level	1.5	-

6.3.15 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 66. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1 JS-002	C2a(2)	500(2)	
			C1(3)	250(3)	

1. Guaranteed by characterization results.
2. UFQFPN48, VFQPN68 and WLCSP100 packages.
3. UFBGA129 package.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 67. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II

6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA / 0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 68*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 68. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PB0, PB1	-5	N/A(2)	mA
	Injected current on PB0, PB1 pins	-5	0	

1. Guaranteed by characterization results.
2. Injection not possible.

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 69* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 69. I/O static characteristics

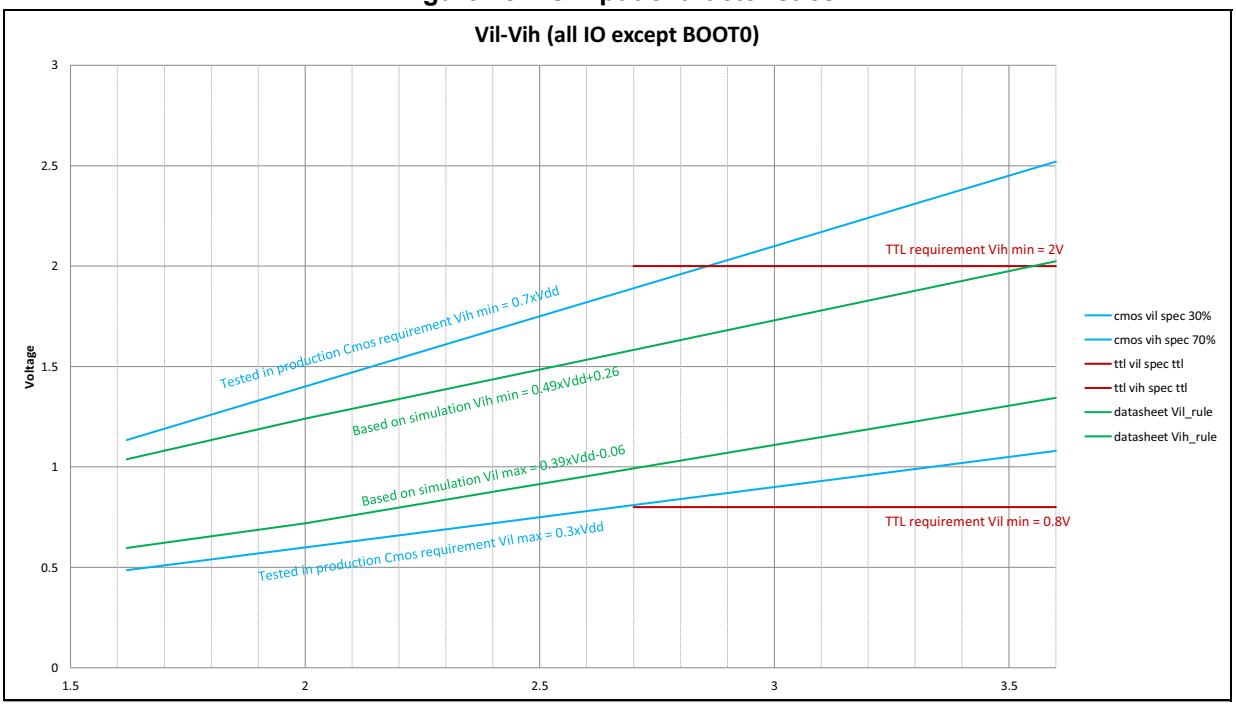
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage(1)	1.62 V < V_{DD} < 3.6 V	-	-	0.3 x V_{DD}	V
	I/O input low level voltage(2)				0.39 x V_{DD} - 0.06	
V_{IH}	I/O input high level voltage(1)		0.7 x V_{DD}	-	-	
	I/O input high level voltage(2)		0.49 x V_{DD} + 0.26	-	-	
V_{hys}	TT_xx, FT_xxx and NRST I/O input hysteresis		-	200	-	mV
I_{lkg}	FT_xx input leakage current	0 ≤ V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) +1 V(2)(3)(4)	-	-	650	
		Max(V_{DDXXX}) +1 V < V_{IN} ≤ 5.5 V(2)(3)(4)(5)(6)	-	-	200(7)	
	FT_lu, FT_u and PC3 IO input leakage current	0 ≤ V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX}) +1 V(2)(3)	-	-	2500	
		Max(V_{DDXXX}) +1 V < V_{IN} ≤ 5.5 V(1)(3)(4)(8)	-	-	250	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(3)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(3)	-	-	2000	
R_{PU}	Weak pull-up equivalent resistor(1)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(1)	V_{IN} = V_{DD}	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Tested in production.
2. Guaranteed by design, not tested in production.
3. Represents the pad leakage of the I/O itself. The total product pad leakage is given by $I_{Total\_Ileak\_max}$ = 10 µA + number of I/Os where V_{IN} is applied on the pad x $I_{lkg(Max)}$.
4. Max(V_{DDXXX}) is the maximum value among all the I/O supplies.
5. V_{IN} must be lower than [Max(V_{DDXXX}) + 3.6 V].
6. Refer to *Figure 25: I/O input characteristics*.

7. To sustain a voltage higher than Min(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled. All FT_xx IO except FT_lu, FT_u and PC3.
8. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS, whose contribution to the series resistance is minimal (~10%).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in *Figure 25* .

Figure 25. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL} / V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 18: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 18: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT or TT unless otherwise specified).

Table 70. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	CMOS port(3) $\|I_{IO}\|$ = 8 mA $V_{DD} \geq 2.7$ V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 0.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	TTL port(3) $\|I_{IO}\|$ = 8 mA $V_{DD} \geq 2.7$ V	-	0.4	
V_{OH}(2)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	-	1.3	
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 1.3	-	
V_{OL}(2)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DD} \geq 1.62$ V	-	0.4	
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DD} - 0.45	-	
V_{OLFM+}(2)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with “f” option)	$\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DD} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DD} ≥ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings Σ I_{IO}.
2. Guaranteed by design.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Table 71*.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 71. I/O AC characteristics(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5	MHz
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	1	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	1.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	ns
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	52	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ ≤2.7 V	-	37	

Table 71. I/O AC characteristics[1][2] (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	MHz
			C=50 pF, 1.62 V ≤ V_{DD} ≤ ≤2.7 V	-	10	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	9	ns
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	16	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	9	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	50	MHz
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	25	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100[3]	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.8	ns
			C=50 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	11	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.5	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	5	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	120[3]	MHz
			C=30 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	50	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	180[3]	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	75[3]	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C=30 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	6	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.7	
			C=10 pF, 1.62 V ≤ V_{DD} ≤ 2.7 V	-	3.3	

1. The maximum frequency is defined with (T_r+ T_f) ≤ 2/3 T, and Duty cycle comprised between 45 and 55%.
2. The fall and rise time are defined, respectively, between 90 and 10%, and between 10 and 90% of the output waveform.
3. This value represents the I/O capability but the maximum system frequency is limited to 64 MHz.

6.3.18 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

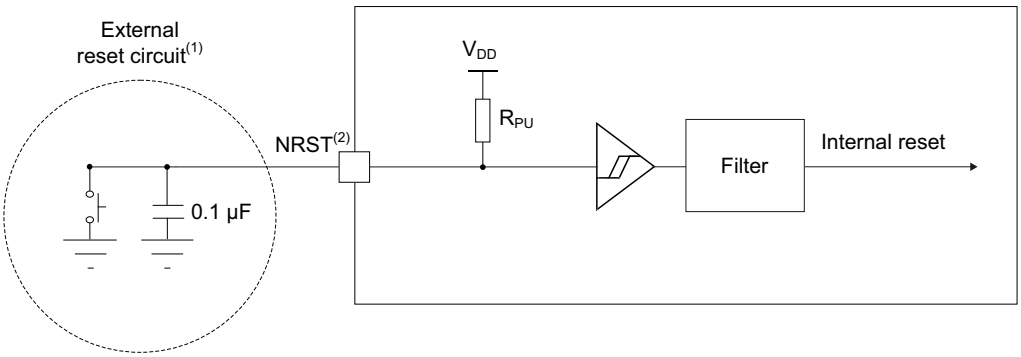
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 72. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10%).

Figure 26. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 72*, otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.19 Analog switches booster

Table 73. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

6.3.20 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in *Table 74* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 22: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 74. ADC characteristics(1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	-	-	64	MHz
		Range 2	-	-	16	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	4.26	Msps
		Resolution = 10 bits	-	-	4.92	
		Resolution = 8 bits	-	-	5.81	
		Resolution = 6 bits	-	-	7.11	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	3.36	
		Resolution = 10 bits	-	-	4.00	
		Resolution = 8 bits	-	-	4.57	
		Resolution = 6 bits	-	-	7.11	
f_{TRIG}	External trigger frequency	f_{ADC} = 64 MHz Resolution = 12 bits	-	-	4.26	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{CMIN}	Input common mode	Differential mode	$(V_{REF+}+V_{REF-})/2 - 0.18$	$(V_{REF+}+V_{REF-})/2$	$(V_{REF+}+V_{REF-})/2 + 0.18$	V
V_{AIN} (4)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 64 MHz	1.8125			µs
		-	116			$1 / f_{ADC}$

Table 74. ADC characteristics(1) (2) (3) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 64 MHz	0.039	-	10.0	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 64 MHz Resolution = 12 bits	0.234	-	1.019	µs
		Resolution = 12 bits	t_s + 12.5 cycles for successive approximations = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 4.26 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 4.26 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 4.26 Msps	-	250	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. SMPS in bypass mode.
4. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

Table 75. ADC sampling time[1][2]

Resolution (bits)	RAIN (kΩ)	Fast channel		Slow channel	
		Minimum sampling time (ns)	Sampling cycles	Minimum sampling time (ns)	Sampling cycles
12	0	33	6.5	57	6.5
	0.05	37	6.5	62	6.5
	0.1	42	6.5	67	6.5
	0.2	51	6.5	76	6.5
	0.5	78	6.5	104	12.5
	1	123	12.5	151	12.5
	5	482	47.5	526	47.5
	10	931	92.5	994	92.5
	20	1830	247.5	1932	247.5
	50	4527	640.5	4744	640.5
	100	9021	640.5	9430	640.5
10	0	27	2.5	47	6.5
	0.05	30	2.5	51	6.5
	0.1	34	6.5	55	6.5
	0.2	41	6.5	62	6.5
	0.5	64	6.5	85	6.5
	1	100	12.5	124	12.5
	5	395	47.5	431	47.5
	10	763	92.5	816	92.5
	20	1500	247.5	1584	247.5
	50	3709	640.5	3891	640.5
	100	7391	640.5	7734	640.5
8	0	21	2.5	37	2.5
	0.05	24	2.5	40	6.5
	0.1	27	2.5	43	6.5
	0.2	32	6.5	49	6.5
	0.5	50	6.5	67	6.5
	1	78	6.5	97	6.5
	5	308	47.5	337	24.5
	10	595	92.5	637	47.5
	20	1169	247.5	1237	92.5
	50	2891	247.5	3037	247.5
	100	5762	640.5	6038	640.5

Table 75. ADC sampling time[1][2] (continued)

Resolution (bits)	RAIN (kΩ)	Fast channel		Slow channel	
		Minimum sampling time (ns)	Sampling cycles	Minimum sampling time (ns)	Sampling cycles
6	0	15	2.5	26	2.5
	0.05	17	2.5	28	2.5
	0.1	19	2.5	31	2.5
	0.2	23	2.5	35	2.5
	0.5	36	6.5	48	6.5
	1	56	6.5	69	6.5
	5	221	24.5	242	24.5
	10	427	47.5	458	47.5
	20	839	92.5	890	92.5
	50	2074	247.5	2184	247.5
	100	4133	640.5	4342	640.5

1. Guaranteed by design.
2. V_{DD} = 1.62 V, C_{pcb} = 4.7 pF, 125 °C, booster enabled.

Table 76. ADC accuracy - Limited test conditions 1(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 76. ADC accuracy - Limited test conditions 1(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 77. ADC accuracy - Limited test conditions 2(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, V_{DDA} ≥ 2 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Table 77. ADC accuracy - Limited test conditions 2(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, V_{DDA} ≥ 2 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 78. ADC accuracy - Limited test conditions 3(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 78. ADC accuracy - Limited test conditions 3(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 64 MHz, Sampling rate ≤ 4.26 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 79. ADC accuracy - Limited test conditions 4(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 16 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 79. ADC accuracy - Limited test conditions 4(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 16 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 27. ADC accuracy characteristics

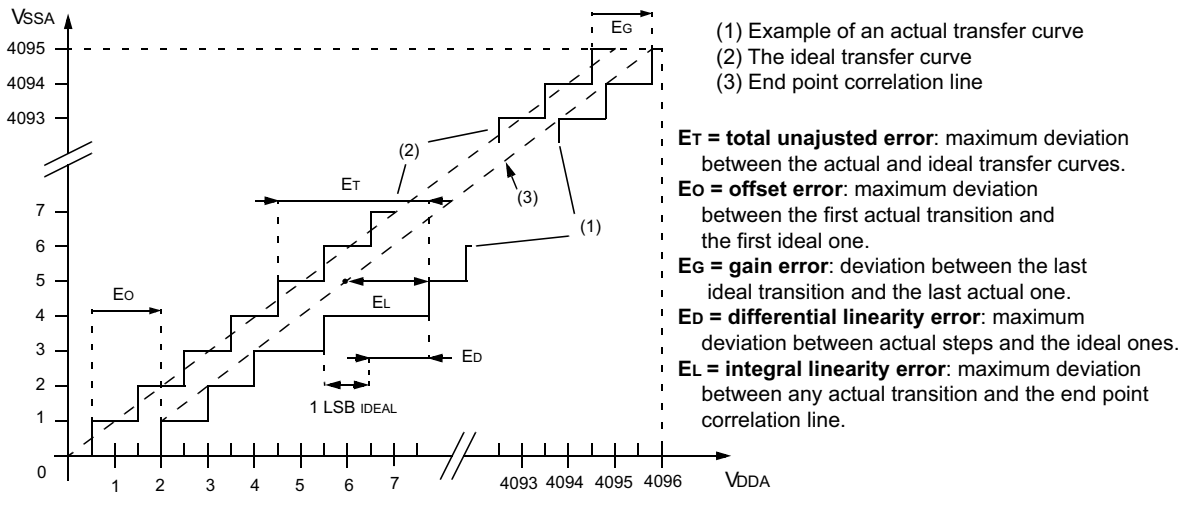
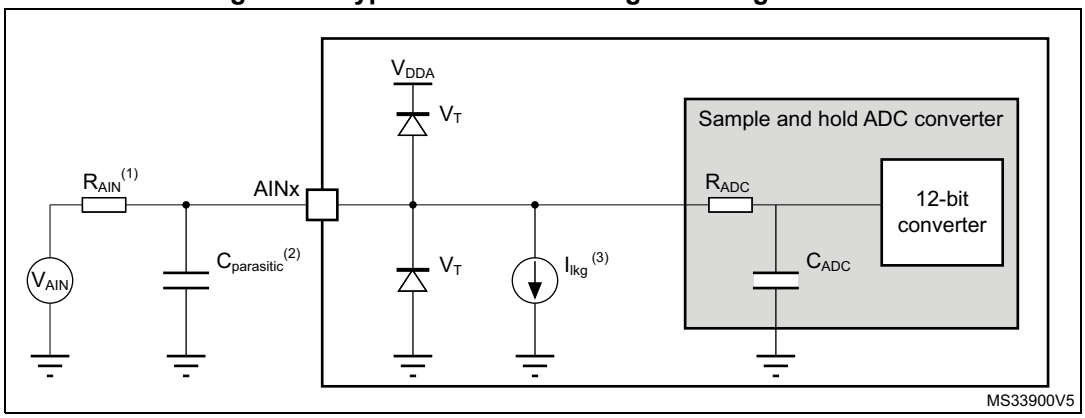


Figure 28. Typical connection diagram using the ADC



1. Refer to *Table 74: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 69: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 69: I/O static characteristics* for the values of Ilkg.

General PCB design guidelines

Power supply decoupling has to be performed as shown in *Figure 14: Power supply scheme (all packages except UFBGA129)*. The 10 nF capacitor needs to be ceramic (good quality), placed as close as possible to the chip.

6.3.21 Voltage reference buffer characteristics

Table 80. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	2.046(3)	2.048	2.049(3)	
			V_{RS} = 1	2.498(3)	2.5	2.502(3)	
		Degraded mode(2)	V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent series resistor of C_{load}	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA

Table 80. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < T_J < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < T_J < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(4)		-	300	350	µs
		CL = 1.1 µF(4)		-	500	650	
		CL = 1.5 µF(4)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (5)	-	-	-	8	-	mA
I_{DDA} (VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA		-	16	25	µA
		I_{load} = 500 µA		-	18	30	
		I_{load} = 4 mA		-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer cannot maintain accurately the output voltage that will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF in-rush current during start-up phase and scaling change, the V_{DDA} voltage must be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.22 Comparator characteristics

Table 81. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D(3)	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	55	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range		-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 34: Embedded internal voltage reference*.
3. Guaranteed by characterization results.

6.3.23 Temperature sensor characteristics

Table 82. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV / °C
V_{30}	Voltage at 30 °C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor buffer start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 11: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.24 V_{BAT} monitoring characteristics

Table 83. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 84. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.25 SMPS step-down converter characteristics

The SMPS step-down converter characteristic are given at 4 MHz clock, with a 20 mA load (unless otherwise specified), using a 10 µH inductor and a 4.7 µF capacitor.

6.3.26 LCD controller characteristics

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the VLCD pin to decouple this converter.

Table 85. LCD controller characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage		-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0		-	2.62	-	
V_{LCD1}	LCD internal reference voltage 1		-	2.76	-	
V_{LCD2}	LCD internal reference voltage 2		-	2.89	-	
V_{LCD3}	LCD internal reference voltage 3		-	3.04	-	
V_{LCD4}	LCD internal reference voltage 4		-	3.19	-	
V_{LCD5}	LCD internal reference voltage 5		-	3.32	-	
V_{LCD6}	LCD internal reference voltage 6		-	3.46	-	
V_{LCD7}	LCD internal reference voltage 7		-	3.62	-	
C_{ext}	V_{LCD} external capacitance	Buffer OFF (BUFEN=0 is LCD_CR register)	0.2	-	2	µF
		Buffer ON (BUFEN=1 is LCD_CR register)	1	-	2	
I_{LCD}(2)	Supply current from V_{DD} at V_{DD} = 2.2 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	3	-	µA
	Supply current from V_{DD} at V_{DD} = 3.0 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	1.5	-	
I_{VLCD}	Supply current from V_{LCD} (V_{LCD} = 3 V)	Buffer OFF (BUFFEN = 0, PON = 0)	-	0.5	-	µA
		Buffer ON (BUFFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High resistor value for Low drive resistive network		-	5.5	-	MΩ
R_{LN}	Total Low resistor value for High drive resistive network		-	240	-	kΩ

Table 85. LCD controller characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{44}	Segment/Common highest level voltage		-	V_{LCD}	-	V
V_{34}	Segment/Common 3/4 level voltage		-	3/4 V_{LCD}	-	
V_{23}	Segment/Common 2/3 level voltage		-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage		-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage		-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage		-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage		-	0	-	

1. Guaranteed by design.
2. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio = 64, all pixels active, no LCD connected.

6.3.27 Timer characteristics

The parameters given in the following tables are guaranteed by design. Refer to *Section 6.3.17* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 86. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 64 MHz	0	40	
Res_{TIM}	Timer resolution	TIM1, TIM16, TIM17	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	0.015625	1024	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	-	67.10	s

1. TIMx, is used as a general term where x stands for 1, 2, 16 or 17.

Table 87. IWDG min/max timeout period at 32 kHz (LSI1)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock vs. the LSI clock, hence there is always a full RC period of uncertainty.

6.3.28 Clock recovery system (CRS)

The devices embed a special block for the automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range.

This automatic trimming is based on the external synchronization signal, which can be derived from USB Sart Of Frame (SOF) signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software.

For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

6.3.29 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

Table 88. Minimum I2CCLK frequency in all I²C modes

Symbol	Parameter	Condition		Min	Unit
$f_{(I2CCLK)}$	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON, DNF = 0	9	
			Analog filter OFF, DNF = 1	9	
		Fast-mode Plus	Analog filter ON, DNF = 0	19	
			Analog filter OFF, DNF = 1	16	

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (see the reference manual).

The SDA and SCL I/O requirements are met with the following restriction: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. The 20 mA output drive requirement in Fast-mode Plus is supported partially.

This limits the maximum load C_{load} supported in Fast-mode Plus, given by these formulas:

- $t_r(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
- $R_p(min) = [V_{DD} - V_{OL}(max)] / I_{OL}(max)$

where R_p is the I2C lines pull-up. Refer to *Section 6.3.17* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter, refer to *Table 89* for its characteristics.

Table 89. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	110(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in *Table 90* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 22: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.17* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 90. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode $1.65 < V_{DD} < 3.6$ V Voltage Range 1	-	-	32	MHz
		Master transmitter mode $1.65 < V_{DD} < 3.6$ V Voltage Range 1			32	
		Slave receiver mode $1.65 < V_{DD} < 3.6$ V Voltage Range 1			32	
		Slave mode transmitter/full duplex $2.7 < V_{DD} < 3.6$ V Voltage Range 1			32(2)	
		Slave mode transmitter/full duplex $1.65 < V_{DD} < 3.6$ V Voltage Range 1			20.5(2)	
		Voltage Range 2			8	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	$4xT_{PCLK}$	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	$2xT_{PCLK}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{PCLK} - 1.5$	T_{PCLK}	$T_{PCLK} + 1$	
$t_{su(MI)}$	Data input setup time	Master mode	1.5	-	-	ns
$t_{su(SI)}$		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	
$t_{dis(SO)}$	Data output disable time		9	-	16	
$t_{v(SO)}$	Data output valid time	Slave mode $2.7 < V_{DD} < 3.6$ V Voltage Range 1	-	14.5	15.5	ns
		Slave mode $1.65 < V_{DD} < 3.6$ V Voltage Range 1	-	15.5	24	
		Slave mode $1.65 < V_{DD} < 3.6$ V Voltage Range 2	-	19.5	26	
$t_{v(MO)}$		Master mode (after enable edge)	-	2.5	3	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	8	-	-	
$t_{h(MO)}$		Master mode (after enable edge)	1	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$, which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty(SCK) = 50 %.

Figure 29. SPI timing diagram - slave mode and CPHA = 0

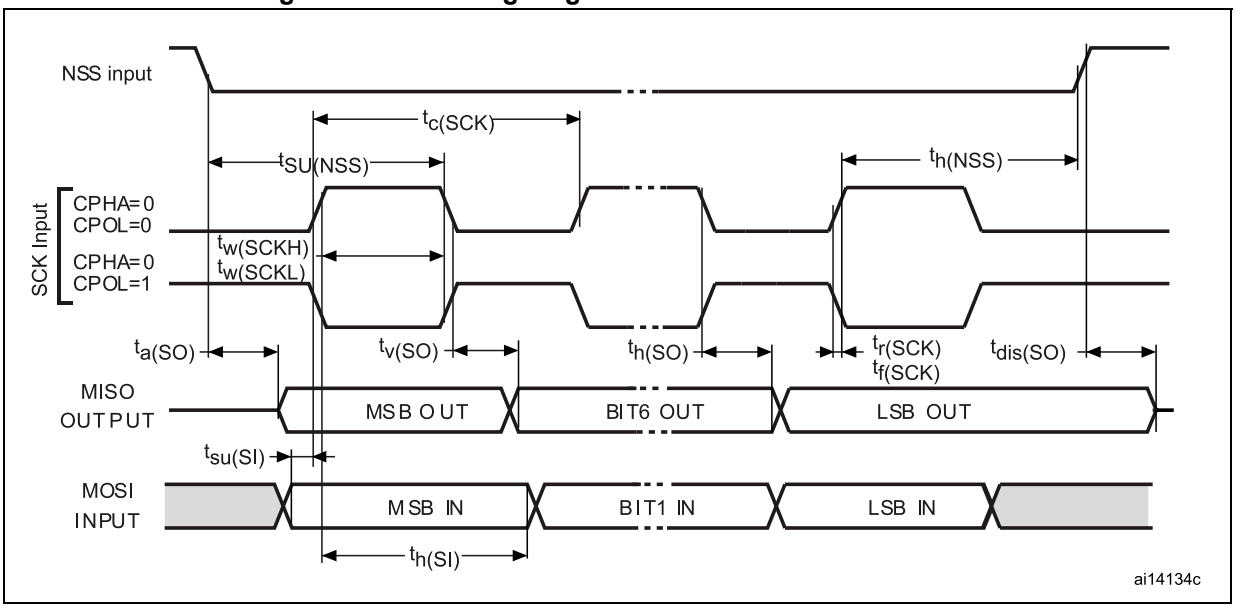
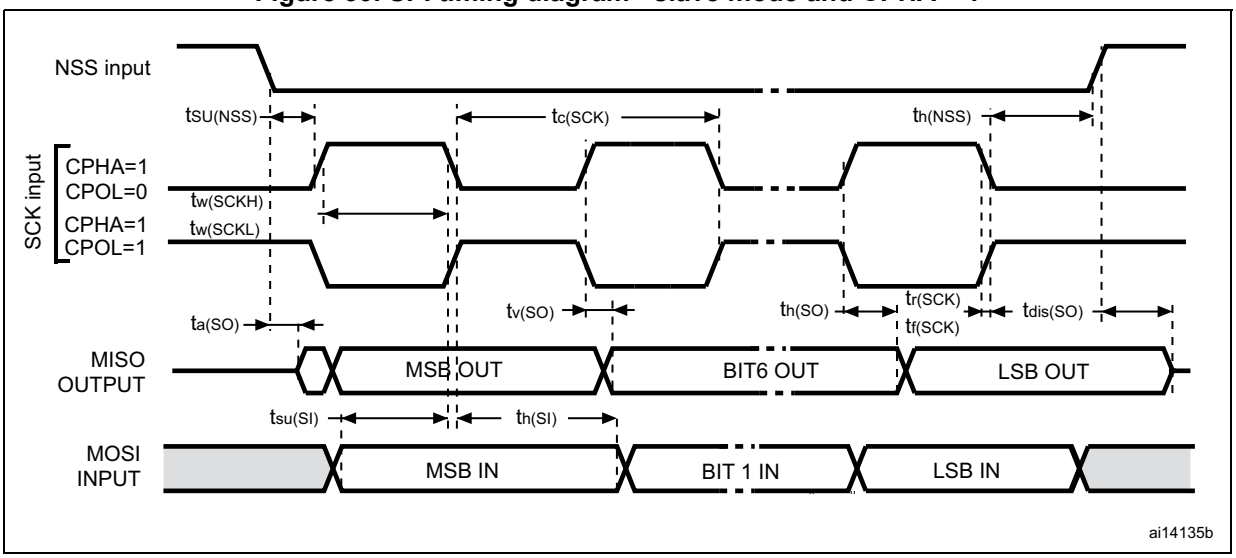
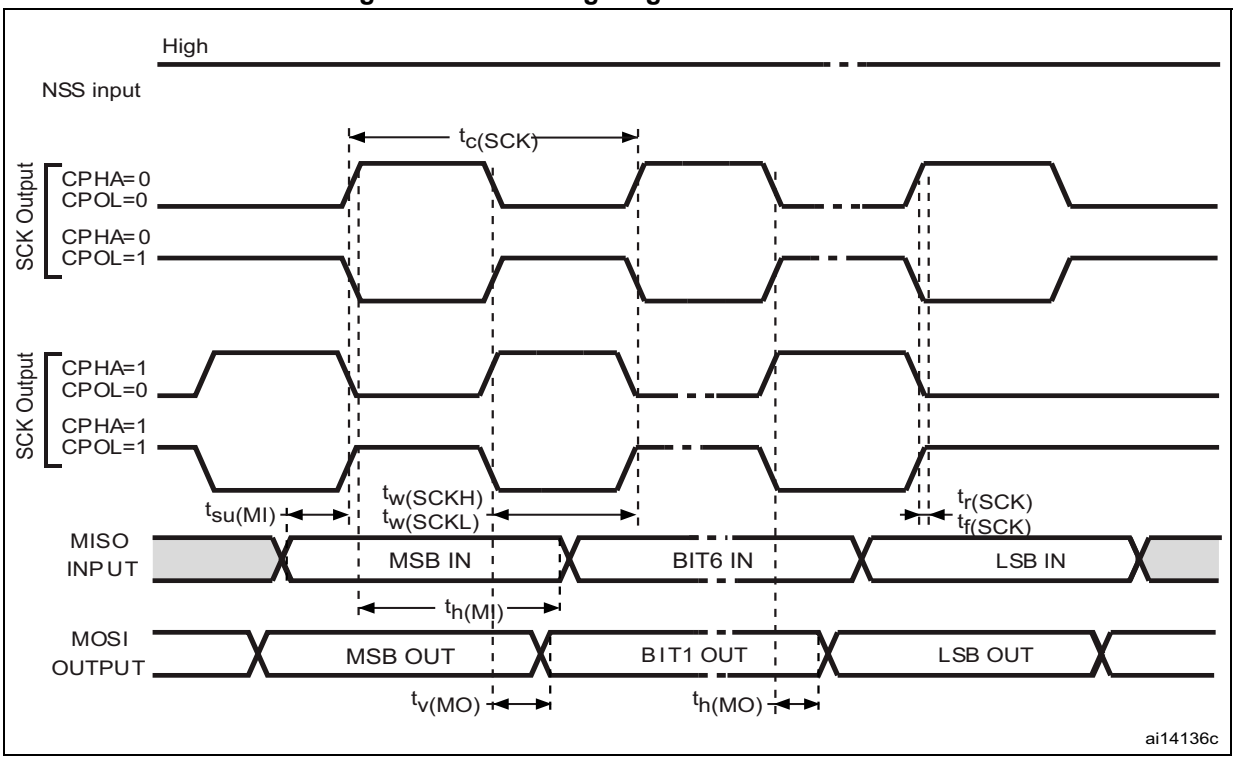


Figure 30. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 31. SPI timing diagram - master mode



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Quad-SPI characteristics

Unless otherwise specified, the parameters given in *Table 91* and *Table 92* for Quad-SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are set at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17* for more details on the input/output alternate function characteristics.

Table 91. Quad-SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad-SPI clock frequency	1.65 < V_{DD}< 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.65 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.65 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	16	
$t_{w(CKH)}$	Quad-SPI clock high and low time	f_{AHBCLK}= 48 MHz, presc=1	$t_{(CK)}/2$ - 0.5	-	$t_{(CK)}/2$ + 1	ns
$t_{w(CKL)}$			$t_{(CK)}/2$ - 1	-	$t_{(CK)}/2$ + 0.5	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	2	-	-	
		Voltage Range 2	3.5	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	4.5	-	-	
		Voltage Range 2	6	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	1	1.5	
		Voltage Range 2	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

Table 92. Quad-SPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad-SPI clock frequency	1.65 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1		-	-	40	MHz
		2.0 < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1		-	-	50	
		1.65 < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1		-	-	48	
		1.65 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2		-	-	16	
$t_{w(CKH)}$	Quad-SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc=0		$t_{(CK)}/2$	-	$t_{(CK)}/2 + 1$	ns
$t_{w(CKL)}$				$t_{(CK)}/2 - 1$	-	$t_{(CK)}/2$	
$t_{sr(IN)}$	Data input setup time on rising edge	Voltage Range 1		2.5	-	-	
		Voltage Range 2		3.5			
$t_{sf(IN)}$	Data input setup time on falling edge	Voltage Range 1		2.5	-	-	
		Voltage Range 2		1.5			
$t_{hr(IN)}$	Data input hold time on rising edge	Voltage Range 1		5.5	-	-	
		Voltage Range 2		6.5			
$t_{hf(IN)}$	Data input hold time on falling edge	Voltage Range 1		5	-	-	
		Voltage Range 2		6			
$t_{vr(OUT)}$	Data output valid time on rising edge	Voltage Range 1	DHHC=0	-	4	5.5	
			DHHC=1		$t_{(CK)}/2 + 1$	$t_{(CK)}/2 + 1.5$	
		Voltage Range 2			4.5	7	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	DHHC=0	-	4	6	
			DHHC=1		$t_{(CK)}/2 + 1$	$t_{(CK)}/2 + 2$	
		Voltage Range 2			6	7.5	
$t_{hr(OUT)}$	Data output hold time on rising edge	Voltage Range 1	DHHC=0	2	-	-	
			DHHC=1	$t_{(CK)}/2 + 0.5$	-	-	
		Voltage Range 2		3.5	-	-	
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	DHHC=0	3	-	-	
			DHHC=1	$t_{(CK)}/2 + 0.5$	-	-	
		Voltage Range 2		5	-	-	

1. Guaranteed by characterization results.

Figure 32. Quad-SPI timing diagram - SDR mode

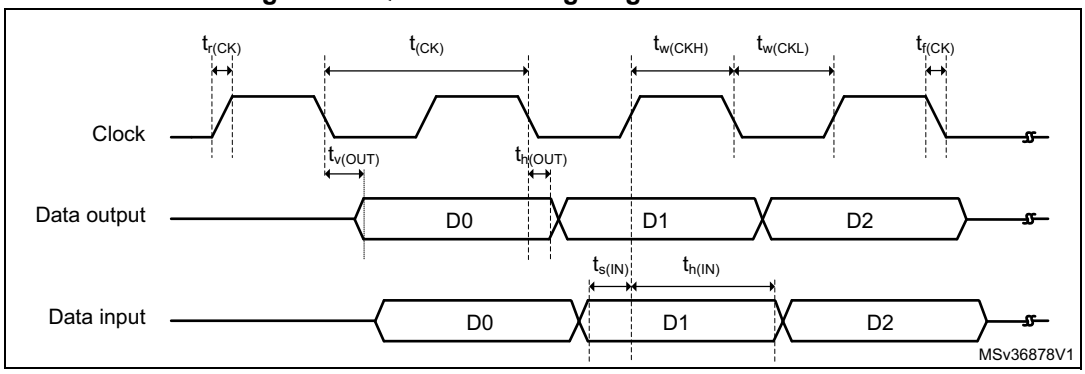
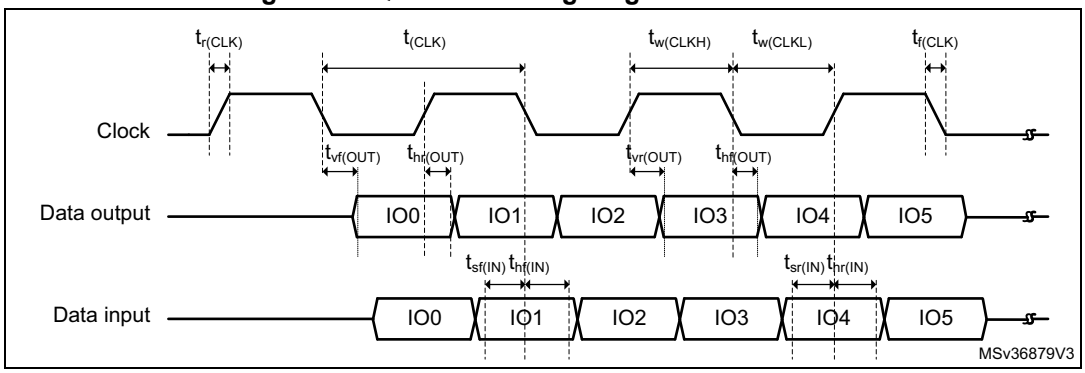


Figure 33. Quad-SPI timing diagram - DDR mode



SAI characteristics

Unless otherwise specified, the parameters given in *Table 93* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement are performed at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.17* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 93. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	23.5	
		Master transmitter 1.65 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	16	
		Master receiver Voltage Range 1	-	16	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	26	
		Slave transmitter 1.65 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	20	
		Slave receiver Voltage Range 1	-	32	
		Voltage Range 2	-	8	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	21	ns
		Master mode 1.65 V ≤ V_{DD} ≤ 3.6 V	-	30	
$t_{h(FS)}$	FS hold time	Master mode	10	-	
$t_{su(FS)}$	FS setup time	Slave mode	1.5	-	
$t_{h(FS)}$	FS hold time	Slave mode	2.5	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	6.5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	
		Slave transmitter (after enable edge) 1.65 V ≤ V_{DD} ≤ 3.6 V	-	25	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	18.5	
		Master transmitter (after enable edge) 1.65 V ≤ V_{DD} ≤ 3.6 V	-	25	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 34. SAI master timing waveforms

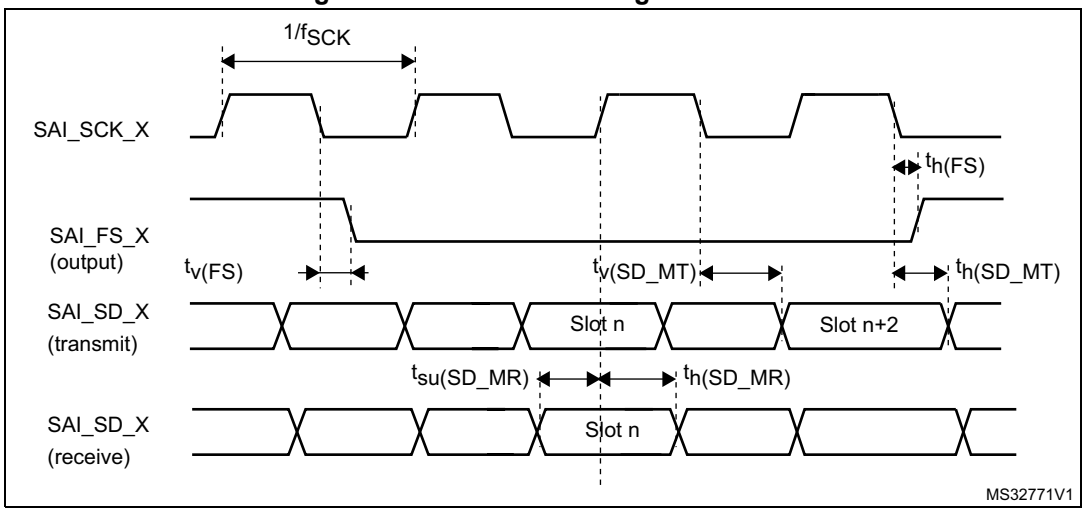
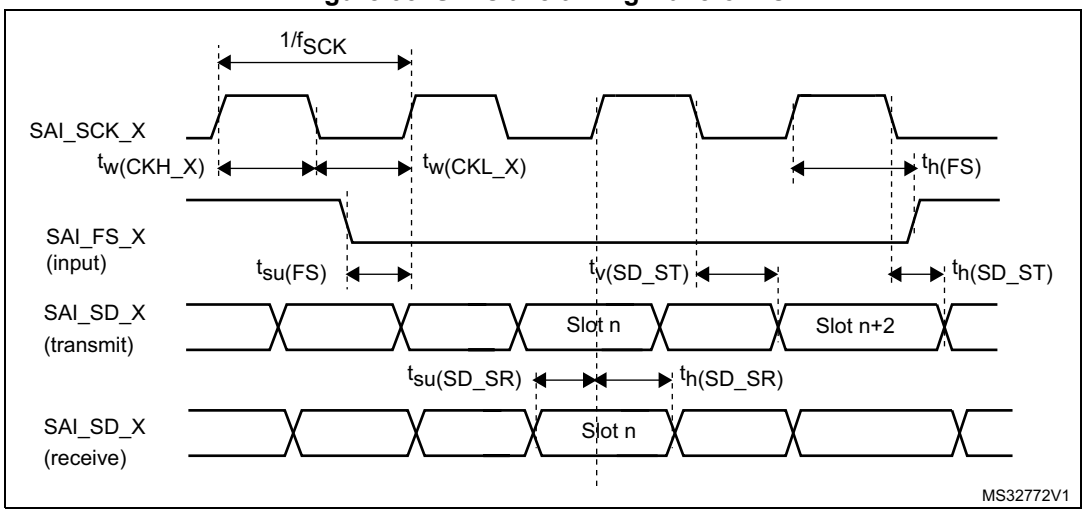


Figure 35. SAI slave timing waveforms



USB characteristics

The STM32WB55xx USB interface is fully compliant with the USB specification version 2.0, and is USB-IF certified (for Full-speed device operation).

Table 94. USB electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage	-	3.0(2)	-	3.6	V
$T_{crystal\_less}$	USB crystal-less operation temperature	-	-15	-	85	°C
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}(3)	Output driver impedance(4)	Driving high and low	28	36	44	

1. T_A = -40 to 125 °C unless otherwise specified.
2. The STM32WB55xx USB functionality is ensured down to 2.7 V, but the full USB electrical characteristics are degraded in the 2.7 to 3.0 V voltage range.
3. Guaranteed by design.
4. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 95* and *Table 96* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Table 95. JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/t_{c(TCK)}$	TCK clock frequency	2.7 < V_{DD} < 3.6 V	-	-	29	MHz
		1.65 < V_{DD} < 3.6 V	-	-	21	
$t_{isu(TMS)}$	TMS input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	2	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	2	-	-	
$t_{ov(TDO)}$	TDO output valid time	2.7 < V_{DD} < 3.6 V	-	13.5	16.5	
		1.65 < V_{DD} < 3.6 V	-	13.5	23	
$t_{oh(TDO)}$	TDO output hold time	-	11	-	-	

Table 96. SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/t_{c(SWCLK)}$	SWCLK clock frequency	$2.7 < V_{DD} < 3.6$ V	-	-	55	MHz
		$1.65 < V_{DD} < 3.6$ V	-	-	35	
$t_{isu(TMS)}$	SWDIO input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	SWDIO input hold time	-	2	-	-	
$t_{ov(TDO)}$	SWDIO output valid time	$2.7 < V_{DD} < 3.6$ V	-	16	18	
		$1.65 < V_{DD} < 3.6$ V	-	16	28	
$t_{oh(TDO)}$	SWDIO output hold time	-	13	-	-	

Refer to *Section 6.3.17* for more details on the input/output alternate function characteristics (CK, SD, WS).

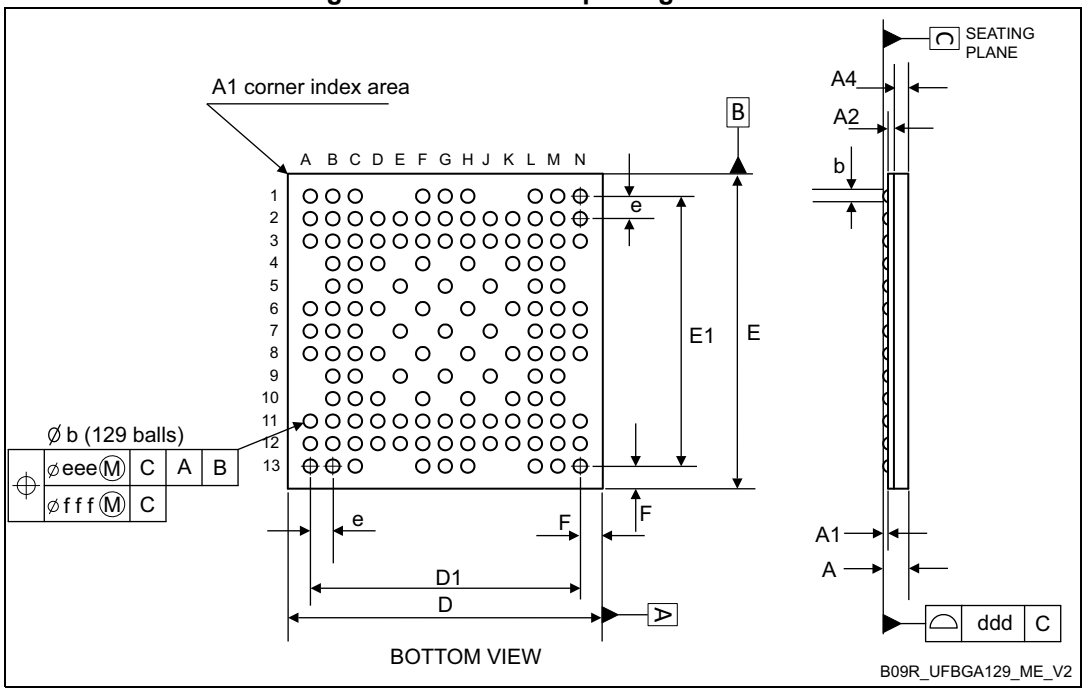
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 UFBGA129 package information

This UFBGA is a 129-ball, 7 x 7 mm, 0.5 mm fine pitch, square ball grid array package.

Figure 36. UFBGA129 package outline



1. Drawing is not to scale.
2. - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
   - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 97. UFBGA129 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.60	-	-	0.024
A1	-	-	0.11	-	-	0.004
A2	-	0.13	-	-	0.005	-
A4	-	0.32	-	-	0.013	-
b[3]	0.24	0.29	0.34	0.009	0.011	0.013

Table 97. UFBGA129 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	6.85	7.00	7.15	0.270	0.276	0.281
E	6.85	7.00	7.15	0.270	0.276	0.281
D1	-	6.00	-	-	0.236	-
E1	-	6.00	-	-	0.236	-
e	-	0.50	-	-	0.020	-
F	-	0.50	-	-	0.020	-
ddd	-	-	0.08	-	-	0.003
eee[4]	-	-	0.15	-	-	0.006
fff[5]	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to four decimal digits.
2. - UFBGA stands for Ultra Thin Profile Fine Pitch Ball Grid Array.
   - Ultra thin profile: 0.50 < A ≤ 0.65mm / Fine pitch: e < 1.00mm pitch.
   - The total profile height (Dim A) is measured from the seating plane to the top of the component
   - The maximum total package height is calculated by the following methodology:
   A Max = A1 Typ + A2 Typ + A4 Typ + $\sqrt{(A1^2+A2^2+A4^2}$ tolerance values).
3. The typical balls diameters before mounting is 0.20 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

Figure 37. UFBGA129 recommended footprint

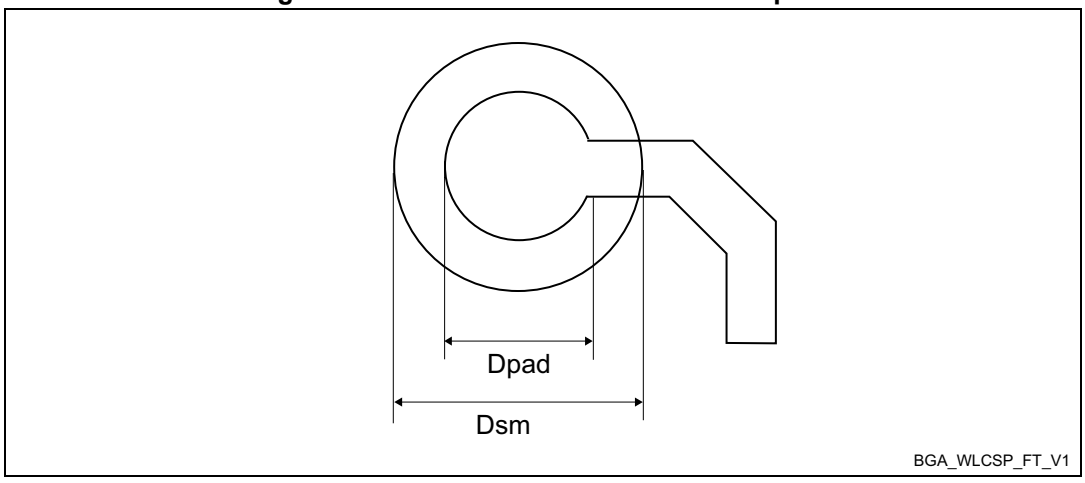


Table 98. UFBGA129 recommended PCB design rules

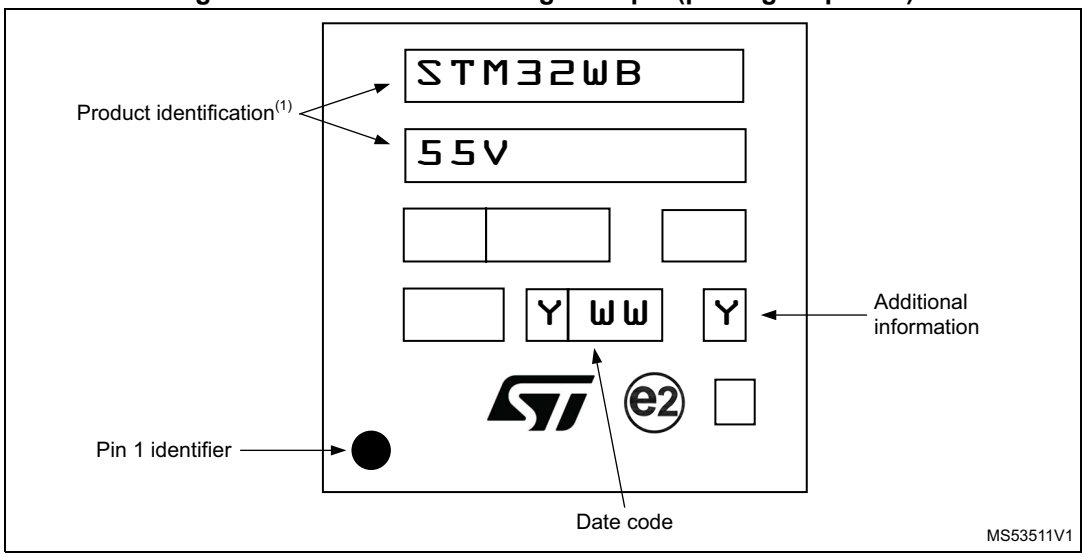
Dimension	Recommended values
Pitch	0.5 mm
Dpad	0,360 mm
Dsm	0.460 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.360 mm
Stencil thickness	0.100 mm

Device marking for UFBGA129

Figure 38 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 38. UFBGA129 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 WLCSP100 package information

WLCSP100 is a 100-ball, 4.390 x 4.371 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 39. WLCSP100 outline

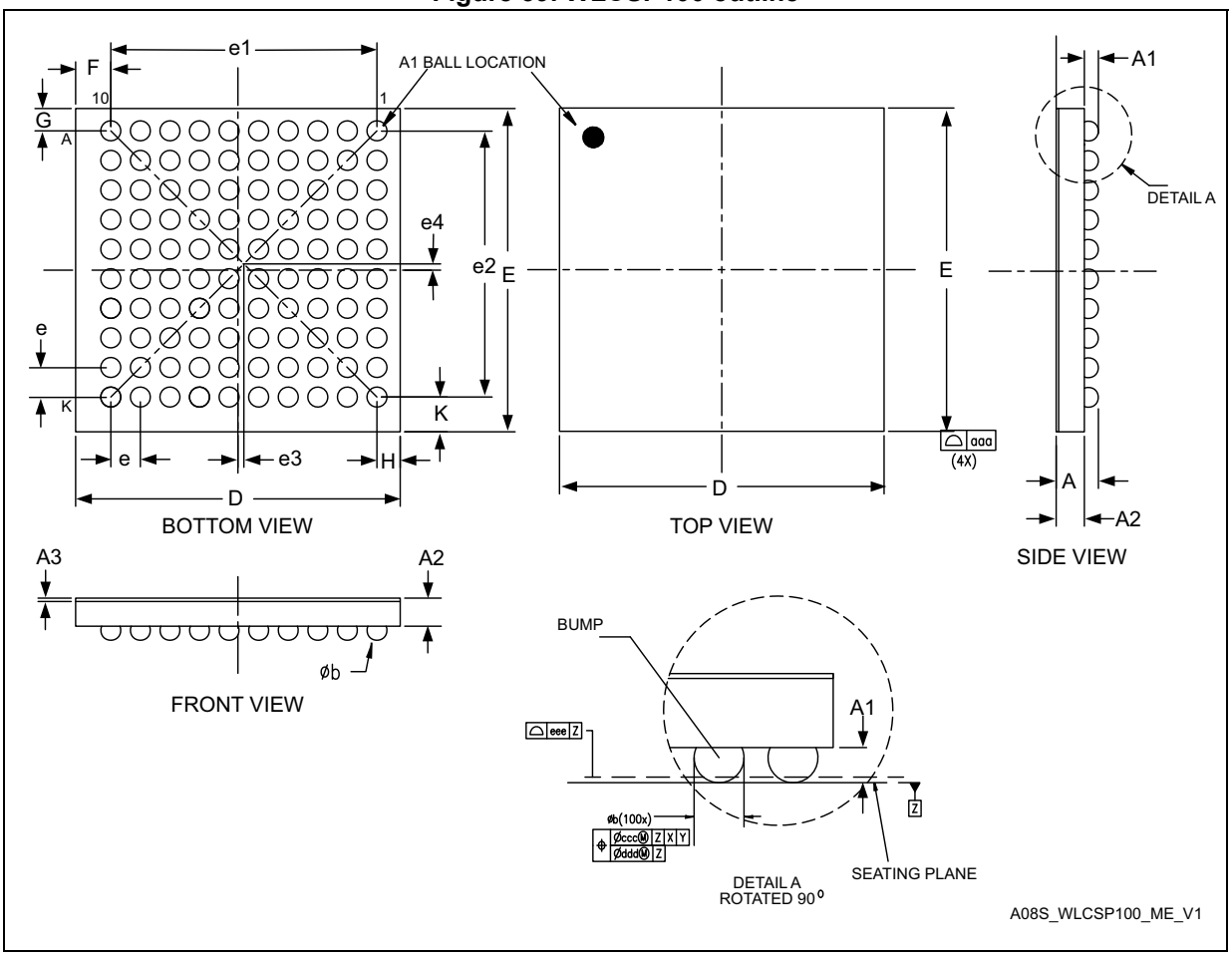
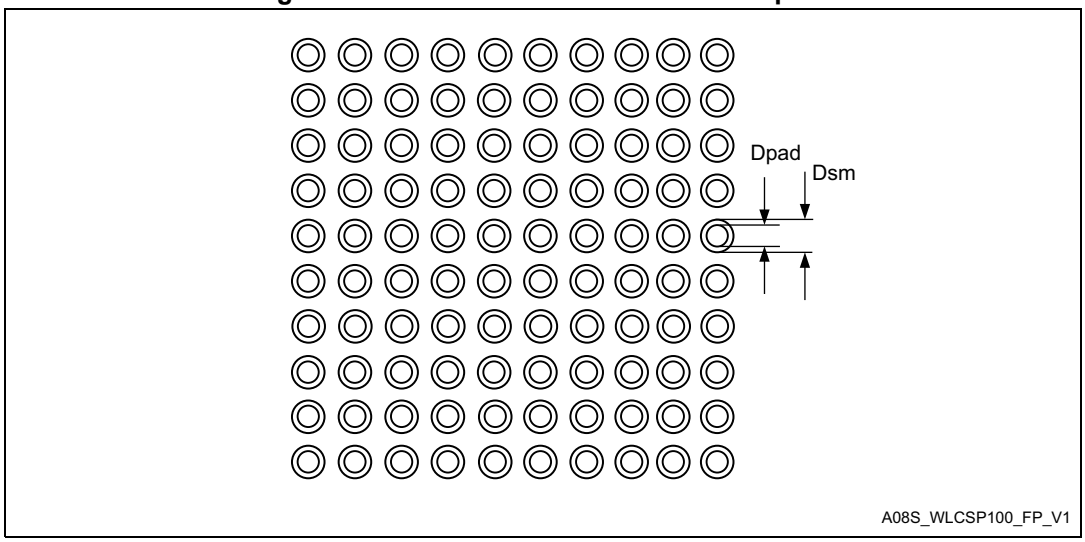


Table 99. WLCSP100 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025[2]	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.0110
D	4.38	4.40	4.42	0.1715	0.1728	0.1742
E	4.36	4.38	4.40	0.1707	0.1721	0.1735
e	-	0.40	-	-	0.0157	-
e1	-	3.60	-	-	0.1417	-
e2	-	3.60	-	-	0.1417	-
e3	-	0.08	-	-	0.0031	-
e4	-	0.08	-	-	0.0033	-
F	-	0.480[3]	-	-	0.0187	-
G	-	0.306[3]	-	-	0.0119	-
H	-	0.32	-	-	0.0124	-
K	-	0.47	-	-	0.0185	-
aaa	-	-	0.10	-	-	0.0039
bbb	-	-	0.10	-	-	0.0039
ccc	-	-	0.10	-	-	0.0039
ddd	-	-	0.05	-	-	0.0020
eee	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to the third decimal place.
2. Nominal dimension rounded to the third decimal place results from process capability.
3. Calculated dimensions are rounded to third decimal place.

Figure 40. WLCSP100 recommended footprint



1. Dimensions are expressed in millimeters.

Table 100. WLCSP100 recommended PCB design rules

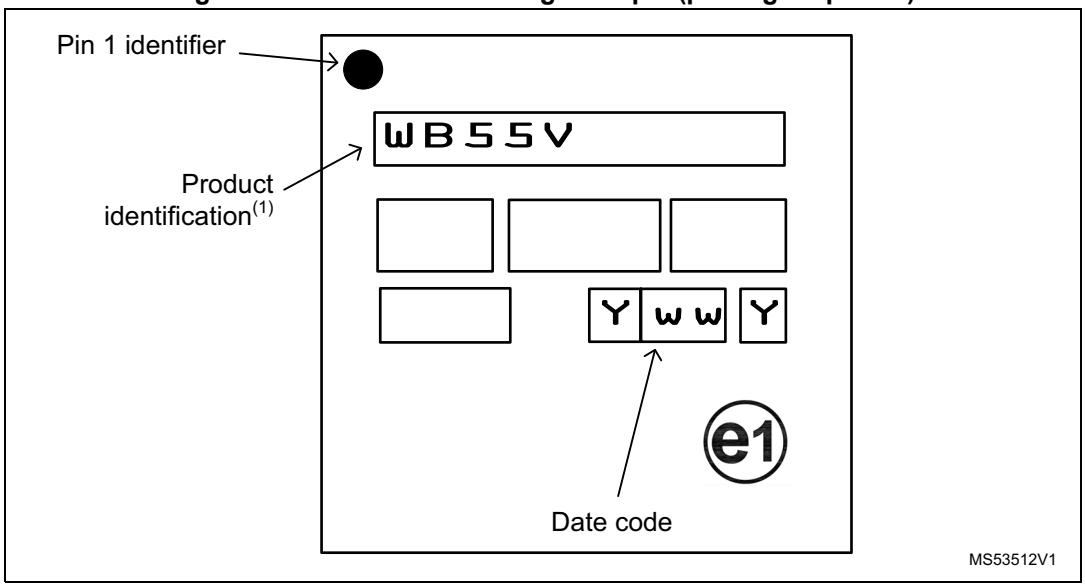
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for WLCSP100

Figure 41 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 41. WLCSP100 marking example (package top view)

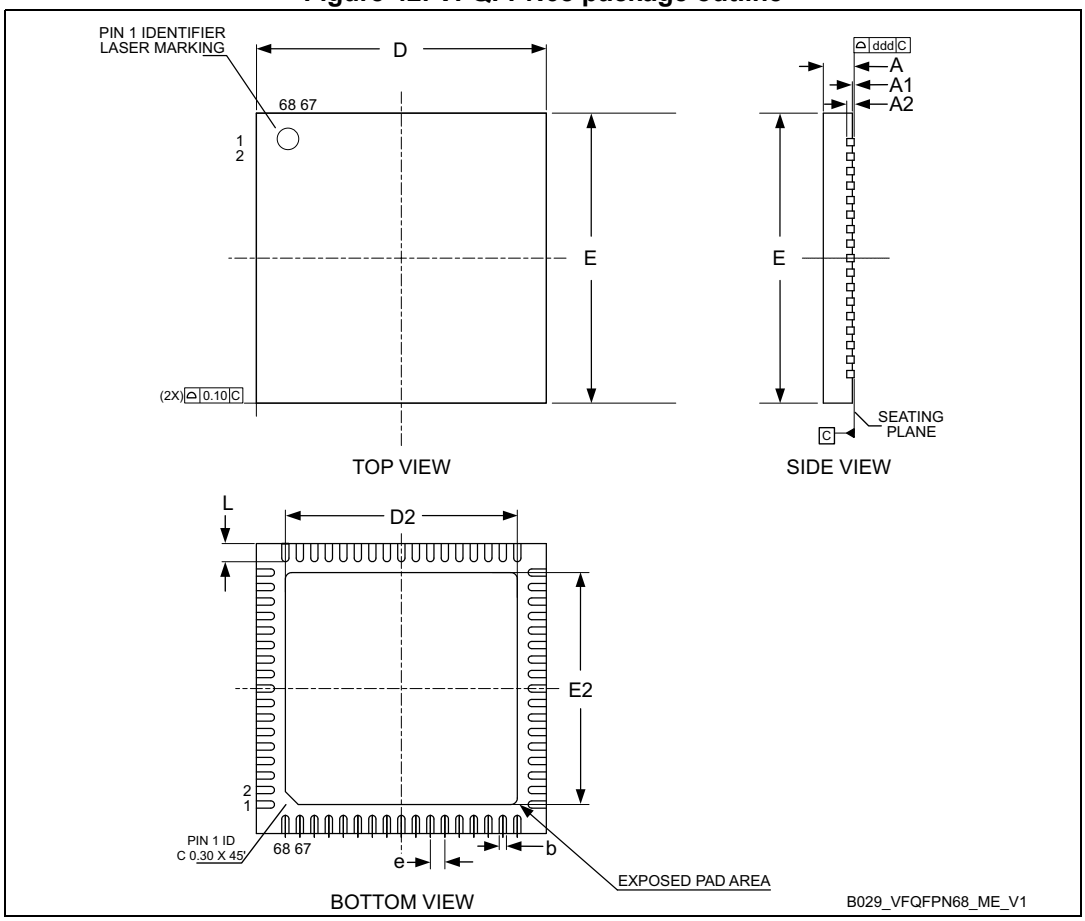


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 VFQFPN68 package information

VFQFPN68 is a 8 x 8 mm, 0.4 mm pitch, very thin fine pitch quad flat package.

Figure 42. VFQFPN68 package outline



1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead. Sawed version. Very thin profile: 0.80 < A ≤ 1.00 mm.
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

Table 101. VFQFPN68 mechanical data

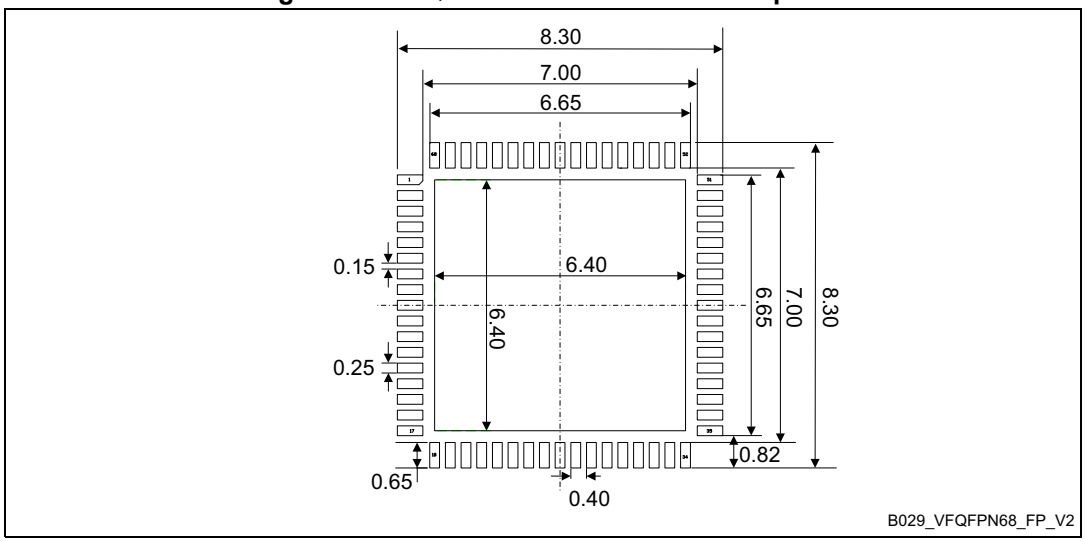
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05	0	0.0008	0.0020
A3	-	0.20	-	-	0.0008	-
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	7.85	8.00	8.15	0.3091	0.3150	0.3209
D2	6.30	6.40	6.50	0.2480	0.2520	0.2559

Table 101. VFQFPN68 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	7.85	8.00	8.15	0.3091	0.3150	0.3209
E2	6.30	6.40	6.50	0.2480	0.2520	0.2559
e	-	0.40	-	-	0.0157	-
L	0.40	0.50	0.60	0.0157	0.0197	0.0236
ddd	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 43. VFQFPN68 recommended footprint



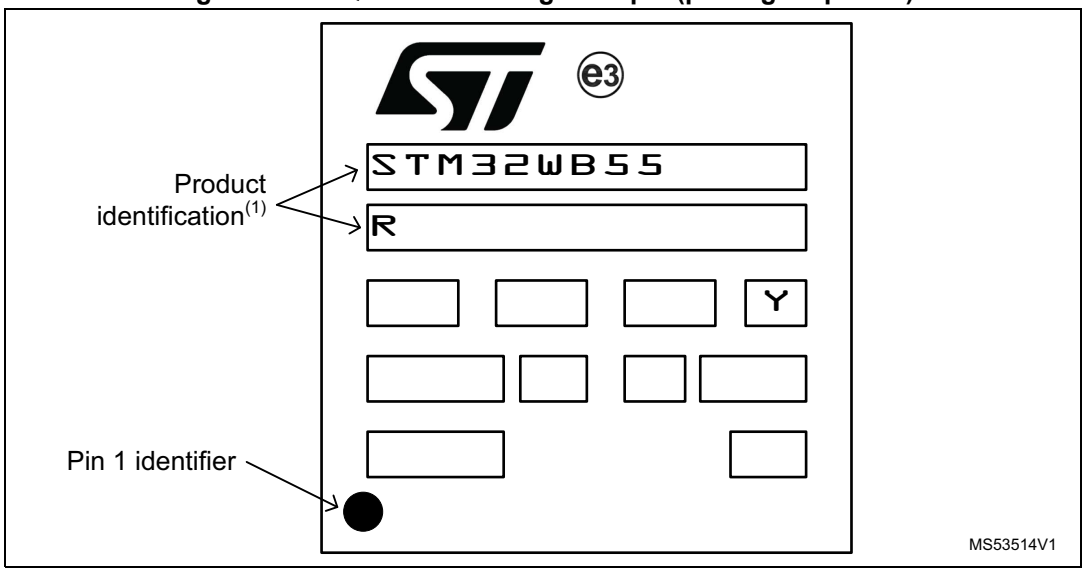
1. Dimensions are expressed in millimeters.

Device marking for VFQFPN68

Figure 43 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 44. VFQFPN68 marking example (package top view)

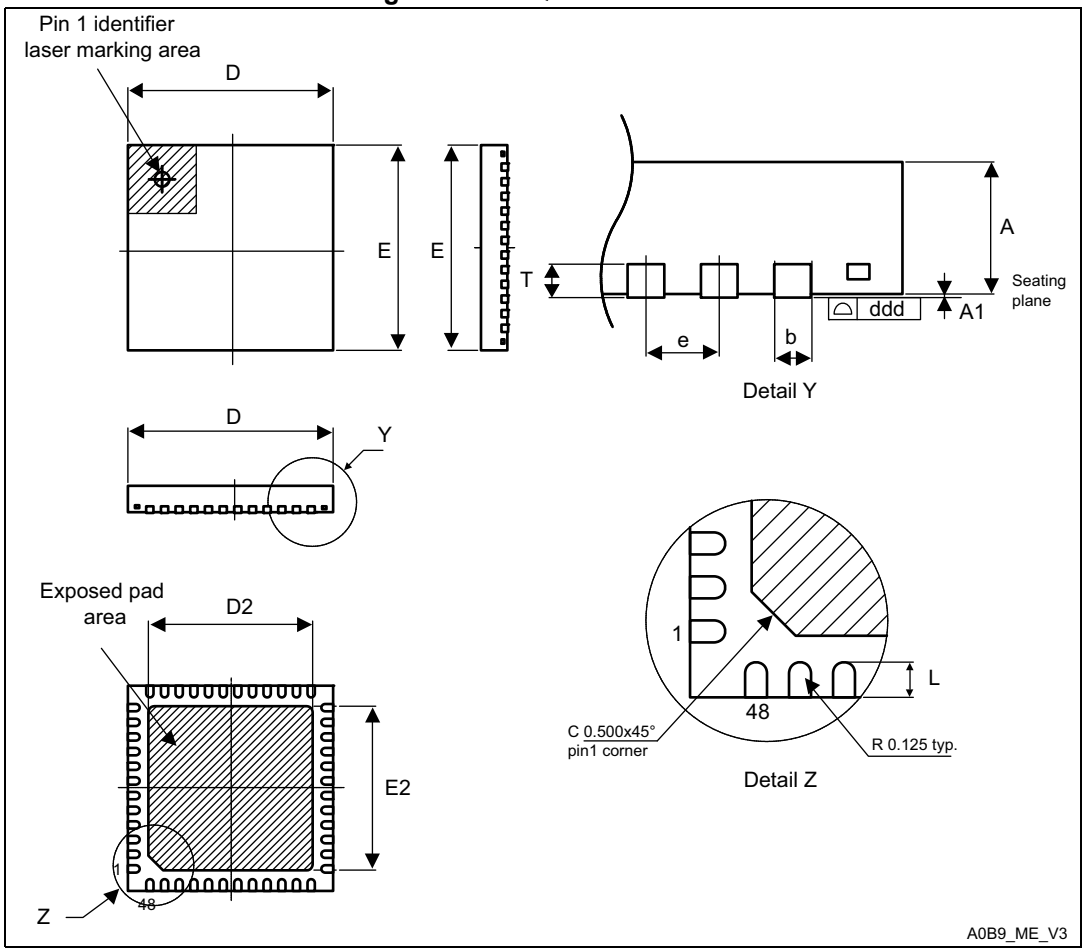


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 45. UFQFPN48 outline



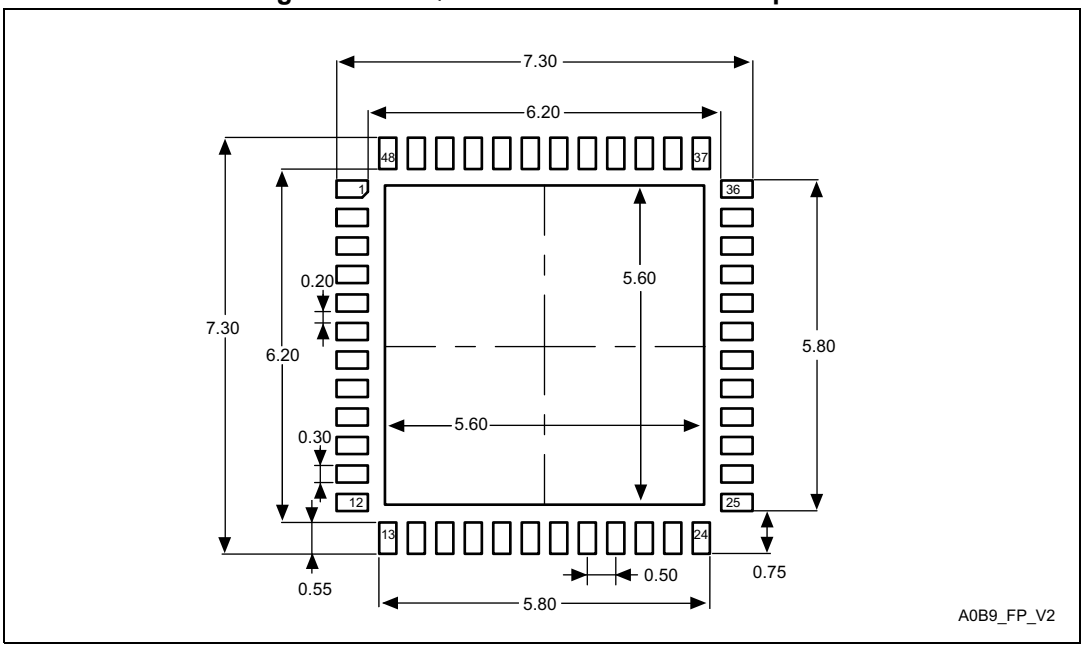
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package, it must be electrically connected to the PCB ground.

Table 102. UFQFPN48 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 46. UFQFPN48 recommended footprint



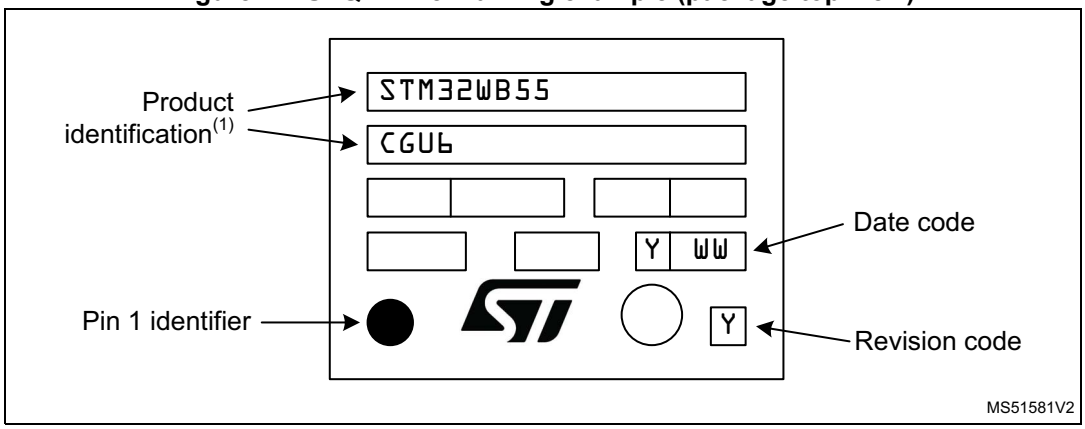
1. Dimensions are expressed in millimeters.

Device marking for UFQFPN48

Figure 47 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. UFQFPN48 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C / W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watt. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

- $P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Note: When the SMPS is used, a portion of the power consumption is dissipated into the external inductor, therefore reducing the chip power dissipation. This portion depends mainly on the inductor ESR characteristics.

Note: As the radiated RF power is quite low (< 4 mW), it is not necessary to remove it from the chip power consumption.

Note: RF characteristics (such as sensitivity, Tx power, consumption) are provided up to 85 °C.

Table 103. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFQFPN48 - 7 mm x 7 mm	24.9	°C/W
	Thermal resistance junction-ambient VFQFPN68 - 8 mm x 8 mm	47.0	
	Thermal resistance junction-ambient WLCSP100 - 0.4 mm pitch	35.8	
	Thermal resistance junction-ambient UFBGA129 - 0.5 mm pitch	41.5	
Θ_{JB}	**Thermal resistance junction-case** UFQFPN48 - 7 mm x 7 mm	13.0	°C/W
	Thermal resistance junction-case VFQFPN68 - 8 mm x 8 mm	36.1	
	Thermal resistance junction-case WLCSP100 - 0.4 mm pitch	N/A	
	Thermal resistance junction-case UFBGA129 - 0.5 mm pitch	16.2	

Table 103. Package thermal characteristics (continued)

Symbol	Parameter	Value	Unit
Θ_{JC}	**Thermal resistance junction-board** UFQFPN48 - 7 mm x 7 mm	1.3	°C/W
	Thermal resistance junction-board VFQFPN68 - 8 mm x 8 mm	13.7	
	Thermal resistance junction-board WLCSP100 - 0.4 mm pitch	N/A	
	Thermal resistance junction-board UFBGA129 - 0.5 mm pitch	34.9	

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32WB55xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_A max = 82 °C (measured according to JESD51-2), I_{DD} max = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INT} max = 50 mA × 3.5 V = 175 mW

P_{IO} max = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INT} max = 175 mW and P_{IO} max = 272 mW

P_D max = 175 + 272 = 447 mW

Using the values obtained in *Table 103* T_J max is calculated as follows:

– For VFQFPN68, 47 °C / W

T_J max = 82 °C + (47 °C / W × 447 mW) = 82 °C + 21 °C = 103 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C), see *Section 8*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8*).

Note: With this given P_D max user can find the T_A max allowed for a given device temperature range (order code suffix 7).

Suffix 7: T_A max = T_J max - (47 °C / W × 447 mW) = 125 °C - 21 °C = 103 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications running at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_A max = 100 °C (measured according to JESD51-2), I_{DD} max = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INT} max = 50 mA × 3.5 V = 175 mW

P_{IO} max = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 175 mW and P_{IO} max = 64 mW

P_D max = 175 + 64 = 239 mW

Thus: P_D max = 239 mW

Using the values obtained in *Table 103* T_J max is calculated as follows:

– For UFQFPN48, 24.9 °C / W

T_J max = 100 °C + (24.9 °C / W × 239 mW) = 100 °C + 6 °C = 106 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8*), unless user reduces the power dissipation to be able to use suffix 6 parts.

8 Ordering information

Example: STM32 WB 55 V G V 6 TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth®

Device subfamily

55 = Die 5, full set of features

Pin count

C = 48 pins

R = 68 pins

V = 100 or 129 pins

Flash memory size

C = 256 KB

E = 512 KB

G = 1 MB

Package

U = UFQFPN48 7 x 7 mm

V = VFQFPN68 8 x 8 mm

Y = WLCSP100 0.4 mm pitch

Q = UFBGA129 0.5 mm pitch

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

Packing

TR = tape and reel

xxx = programmed parts

9 Revision history

Table 104. Document revision history

Date	Revision	Changes
25-Jul-2017	1	Initial release.
04-Apr-2018	2	Updated document title, *Features*, *Section 1: Introduction*, *Section 2: Description*, *Section 3.1: Architecture*, *Section 3.3.2: Memory protection unit*, *Section 3.3.3: Embedded Flash memory*, *Section 3.4: Security and safety*, *Section 3.6: RF subsystem*, *Section 3.6.1: RF front-end block diagram*, *Section 3.6.2: BLE general description*, *Section 3.7.1: Power supply distribution*, *Section 3.7.2: Power supply schemes*, *Section 3.7.4: Power supply supervisor*, *Section 3.10: Clocks and startup*, *Section 3.14: Analog to digital converter (ADC)*, *Section 3.19: True random number generator (RNG)*, *Section 5: Memory mapping*, *Section 6.3.25: SMPS step-down converter characteristics* and *Section 7.5.2: Selecting the product temperature range*. Updated *Table 2: STM32WB55xx devices features and peripheral counts*, *Table 6: Power supply typical components*, *Table 7: Features over all modes*, *Table 8: STM32WB55xx modes overview*, *Table 13: Timer features*, *Table 15: Legend/abbreviations used in the pinout table*, *Table 16: STM32WB55xx pin and ball definitions*, *Table 17: Alternate functions*, *Table 23: RF transmitter BLE characteristics*, *Table 26: RF receiver BLE characteristics (1 Mbps)* and added footnote to it, *Table 28: RF BLE power consumption for VDD = 3.3 V*, *Table 31: RF 802.15.4 power consumption for VDD = 3.3 V*, *Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V*, *Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V*, *Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down*, *Table 41: Current consumption in Stop 2 mode*, *Table 42: Current consumption in Stop 1 mode*, *Table 43: Current consumption in Stop 0 mode*, *Table 44: Current consumption in Standby mode*, *Table 45: Current consumption in Shutdown mode*, *Table 48: Peripheral current consumption*, *Table 103: Package thermal characteristics* and *Table 97: STM32WB55xx ordering information scheme*. Added *Table 47: Current under Reset condition*. Updated *Figure 1: STM32WB55xx block diagram*, *Figure 2: STM32WB55xx RF front-end block diagram*, *Figure 4: Power distribution*, *Figure 6: Power supply overview*, *Figure 7: Clock tree*, *Figure 8: STM32WB55Cx UFQFPN48 pinout*[(1)(2)], *Figure 9: STM32WB55Rx VFQFPN68 pinout*[(1)(2)], *Figure 10: STM32WB55Vx WLCSP100 ballout*[(1)] and *Figure 14: Power supply scheme (all packages except UFBGA129)*.

Table 104. Document revision history (continued)

Date	Revision	Changes
08-Oct-2018	3	Changed document classification to Public. Updated *Features*, *Section 3.6.2: BLE general description*, *Section 3.7.2: Power supply schemes*, *Section 3.7.3: Linear voltage regulator*, *Section 3.10: Clocks and startup*, *Section 6.3.10: External clock source characteristics*, *Section 6.3.20: Analog-to-Digital converter characteristics*, *Section 6.3.29: Communication interfaces characteristics*, *Section 7.2: WLCSP100 package information* and *Section 7.5: Thermal characteristics*. Replaced V_{DDIOx} with V_{DD} throughout the whole document. Updated *Table 5: Typical external components*, footnote *2* of *Table 7: Features over all modes*, *Table 8: STM32WB55xx modes overview* and its footnote *5*, *Table 12: Internal voltage reference calibration values*, *Table 16: STM32WB55xx pin and ball definitions* and its footnote *5*, *Table 17: Alternate functions*, *Table 20: Thermal characteristics*, *Table 21: Main performance at VDD = 3.3 V*, *Table 21: Main performance at VDD = 3.3 V*, *Table 22: General operating conditions*, *Table 23: RF transmitter BLE characteristics* and its footnote, *Table 26: RF receiver BLE characteristics (1 Mbps)*, *Table 28: RF BLE power consumption for VDD = 3.3 V*, *Table 29: RF transmitter 802.15.4 characteristics* and its footnote *1*, *Table 30: RF receiver 802.15.4 characteristics*, *Table 31: RF 802.15.4 power consumption for VDD = 3.3 V*, *Table 34: Embedded internal voltage reference*, *Table 35: Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V*, *Table 36: Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, VDD = 3.3 V*, *Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V*, *Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V*, *Table 39: Current consumption in Sleep and Low-power sleep modes, Flash memory ON*, *Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down*, *Table 41: Current consumption in Stop 2 mode*, *Table 42: Current consumption in Stop 1 mode*, *Table 43: Current consumption in Stop 0 mode*, *Table 44: Current consumption in Standby mode*, *Table 45: Current consumption in Shutdown mode*, *Table 46: Current consumption in VBAT mode*, *Table 47: Current under Reset condition*, *Table 48: Peripheral current consumption*, *Table 49: Low-power mode wakeup timings*, *Table 50: Regulator modes transition times*, *Table 51: Wakeup time using LPUART*, *Table 53: HSE oscillator characteristics* and added footnote to it, *Table 60: LSI2 oscillator characteristics*, *Table 62: Flash memory characteristics*, *Table 64: EMS characteristics*, *Table 66: ESD absolute maximum ratings*, *Table 68: I/O current injection susceptibility*, *Table 69: I/O static characteristics* and its footnotes, *Table 70: Output voltage characteristics*, *Table 71: I/O AC characteristics* and its footnotes *1* and *2*, *Table 72: NRST pin characteristics*, *Table 76: ADC accuracy - Limited test conditions 1*, *Table 77: ADC accuracy - Limited test conditions 2*, *Table 78: ADC accuracy - Limited test conditions 3*, *Table 79: ADC accuracy - Limited test conditions 4*, *Table 81: COMP characteristics*, *Table 89: I2C analog filter characteristics*, *Table 90: SPI characteristics*, *Table 91: Quad-SPI characteristics in SDR mode*, *Table 92: Quad-SPI characteristics in DDR mode* and *Table 93: SAI characteristics*.

Table 104. Document revision history (continued)

Date	Revision	Changes
08-Oct-2018	3 (cont'd)	Updated *Figure 2: STM32WB55xx RF front-end block diagram*, *Figure 14: Power supply scheme (all packages except UFBGA129)*, *Figure 18: Typical energy detection (T = 27°C, VDD = 3.3 V)* and *Figure 25: I/O input characteristics*. Added *Figure 5: Power-up/down sequence*, *Figure 17: Typical link quality indicator code vs. Rx level* and *Figure 18: Typical energy detection (T = 27°C, VDD = 3.3 V)*. Added *Table 24: RF transmitter BLE characteristics (1 Mbps)*, *Table 25: RF transmitter BLE characteristics (2 Mbps)*, *Table 27: RF receiver BLE characteristics (2 Mbps)*, *Table 52: HSE crystal requirements* and *Table 88: Minimum I2CCLK frequency in all I2C modes*. Added *Device marking for UFQFPN48*. Removed former *Figure 22: I/O AC characteristics definition*(1) and *Figure 27: SMPS efficiency - VDDSMPS = 3.6 V*.
20-Feb-2019	4	Updated document title. Product status moved to Production data. Introduced BGA129 package, hence updated image on cover page, *Table 16: STM32WB55xx pin and ball definitions* and *Section 8: Ordering information*, and added *Figure 11: STM32WB55Vx UFBGA129 ballout*(1) and *Section 7.1: UFBGA129 package information*. Updated *Features*, *Section 3.3.4: Embedded SRAM*, *Section 3.17: Touch sensing controller (TSC)* and *Section 3.24: Low-power universal asynchronous receiver transmitter (LPUART)*. Added *Section 6.3.28: Clock recovery system (CRS)*. Added *Table 75: ADC sampling time*. Removed former *Table 75: Maximum ADC RAIN* and *Table 84: SMPS step-down converter characteristics*. Updated captions of figures *8*, *9* and *10*. Updated *Figure 43: VFQFPN68 recommended footprint*.

Table 104. Document revision history (continued)

Date	Revision	Changes
20-Feb-2019	4 (cont'd)	Updated *Table 2: STM32WB55xx devices features and peripheral counts*, *Table 8: STM32WB55xx modes overview* and its footnotes, *Table 21: Main performance at VDD = 3.3 V*, *Table 22: General operating conditions*, *Table 23: RF transmitter BLE characteristics*, *Table 24: RF transmitter BLE characteristics (1 Mbps)*, *Table 25: RF transmitter BLE characteristics (2 Mbps)*, *Table 26: RF receiver BLE characteristics (1 Mbps)*, *Table 27: RF receiver BLE characteristics (2 Mbps)*, *Table 28: RF BLE power consumption for VDD = 3.3 V*, *Table 29: RF transmitter 802.15.4 characteristics*, *Table 31: RF 802.15.4 power consumption for VDD = 3.3 V*, *Table 35: Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF), VDD = 3.3 V*, *Table 36: Current consumption in Run and Low-power run modes, code with data processing running from SRAM1, VDD = 3.3 V*, *Table 37: Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF), VDD= 3.3 V*, *Table 38: Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1, VDD = 3.3 V*, *Table 39: Current consumption in Sleep and Low-power sleep modes, Flash memory ON*, *Table 40: Current consumption in Low-power sleep modes, Flash memory in Power down*, *Table 41: Current consumption in Stop 2 mode*, *Table 42: Current consumption in Stop 1 mode*, *Table 43: Current consumption in Stop 0 mode*, *Table 44: Current consumption in Standby mode*, *Table 45: Current consumption in Shutdown mode*, *Table 46: Current consumption in VBAT mode*, *Table 47: Current under Reset condition*, *Table 48: Peripheral current consumption* and its footnotes, *Table 49: Low-power mode wakeup timings*, *Table 50: Regulator modes transition times* and its footnote *1*, *Table 64: EMS characteristics*, *Table 65: EMI characteristics*, *Table 66: ESD absolute maximum ratings*, *Table 68: I/O current injection susceptibility*, *Table 74: ADC characteristics*, *Table 76: ADC accuracy - Limited test conditions 1*, *Table 77: ADC accuracy - Limited test conditions 2*, *Table 78: ADC accuracy - Limited test conditions 3*, *Table 79: ADC accuracy - Limited test conditions 4* and *Table 103: Package thermal characteristics*.
04-Oct-2019	5	Updated *Features*, *Section 2: Description*, *Section 6.1.6: Power supply scheme*, *Section 6.2: Absolute maximum ratings* and *Section 7.2: WLCSP100 package information*. Updated *Table 6: Power supply typical components*, *Table 7: Features over all modes*, *Table 11: Temperature sensor calibration values*, *Table 16: STM32WB55xx pin and ball definitions*, *Table 17: Alternate functions*, *Table 21: Main performance at VDD = 3.3 V*, *Table 26: RF receiver BLE characteristics (1 Mbps)*, *Table 34: Embedded internal voltage reference*, *Table 61: PLL, PLLSAI1 characteristics* and *Table 66: ESD absolute maximum ratings*. Updated *Figure 6: Power supply overview* and *Figure 33: Quad-SPI timing diagram - DDR mode*. Added *Figure 15: Power supply scheme (UFBGA129 package)* and *Figure 21: Low-speed external clock source AC timing diagram*. Added *Table 55: Low-speed external user clock characteristics – Bypass mode*.

Table 104. Document revision history (continued)

Date	Revision	Changes
19-Feb-2020	6	Updated *Features*, *Section 2: Description*, *I/O system current consumption*, *Section 3.17: Touch sensing controller (TSC)*, *Section 7.1: UFBGA129 package information*, *Section 7.2: WLCSP100 package information*, *Section 7.3: VFQFPN68 package information*, *Section 7.4: UFQFPN48 package information*, *Section 7.5: Thermal characteristics* and *Section 8: Ordering information*. Added *JTAG/SWD interface characteristics*, *Device marking for UFBGA129*, *Device marking for WLCSP100* and *Device marking for VFQFPN68*. Updated *Table 2: STM32WB55xx devices features and peripheral counts*, *Table 7: Features over all modes*, *Table 16: STM32WB55xx pin and ball definitions*, *Table 17: Alternate functions*, *Table 18: Voltage characteristics*, *Table 22: General operating conditions*, *Table 26: RF receiver BLE characteristics (1 Mbps)*, *Table 27: RF receiver BLE characteristics (2 Mbps)*, *Table 30: RF receiver 802.15.4 characteristics*, *Table 47: Current under Reset condition*, *Table 60: LSI2 oscillator characteristics* and *Table 103: Package thermal characteristics*. Added footnote *5* to *Table 15: Legend/abbreviations used in the pinout table*. Updated *Figure 2: STM32WB55xx RF front-end block diagram*, *Figure 6: Power supply overview*, *Figure 7: Clock tree*, *Figure 11: STM32WB55Vx UFBGA129 ballout*(1), *Figure 14: Power supply scheme (all packages except UFBGA129)*, *Figure 36: UFBGA129 package outline* and *Figure 47: UFQFPN48 marking example (package top view)*.