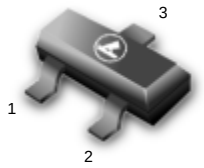
30V P-Channel Enhancement-Mode MOSFET

LP3407LT1G
S-LP3407LT1G

V_{DS}	-30V
I_D (V_{GS} = -10V)	-4.1A
$R_{DS(ON)}$ (V_{GS} = -10V)	< 70mΩ
$R_{DS(ON)}$ (V_{GS} = -4.5V)	< 100mΩ



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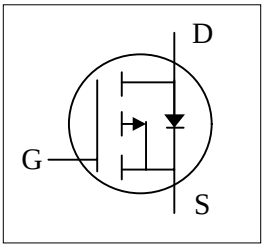


FEATURES

The LP3407LT1G uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use as a load switch or in PWM applications.

S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

ORDERING INFORMATION

Device	Marking	Shipping
LP3407LT1G S-LP3407LT1G	A07	3000/Tape&Reel
LP3407LT3G S-LP3407LT3G	A07	10000/Tape&Reel

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	-4.1	A
	T_A=70°C		-3.5	
Pulsed Drain Current [C]		I_{DM}	-25	
Power Dissipation [B]	T_A=25°C	P_D	1.4	W
	T_A=70°C		0.9	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	70	90	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		100	125	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	63	80	°C/W

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	μA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA	-1	-2	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-25			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-4.1A			70	mΩ
		T_J=125°C			95	
		V_{GS}=-4.5V, I_D=-3A			100	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-4A		10		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz	415	520	625	pF
C_{oss}	Output Capacitance		70	100	130	pF
C_{rss}	Reverse Transfer Capacitance		40	65	90	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	3.5	7.5	11.5	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-4A	7.4	9.2	11	nC
Q_g(4.5V)	Total Gate Charge		3.7	4.6	6	nC
Q_{gs}	Gate Source Charge		1.3	1.6	1.9	nC
Q_{gd}	Gate Drain Charge		1.3	2.2	3.1	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=3.6Ω, R_{GEN}=3Ω		7.5		ns
t_r	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off DelayTime			19		ns
t_f	Turn-Off Fall Time			7		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-4A, dI/dt=100A/μs	8.8	11	13	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-4A, dI/dt=100A/μs	4	5.3	6.4	nC

TYPICAL ELECTRICAL CHARACTERISTICS

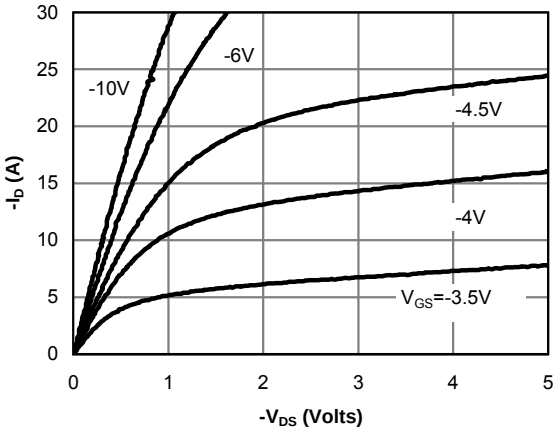


Fig 1: On-Region Characteristics (Note E)

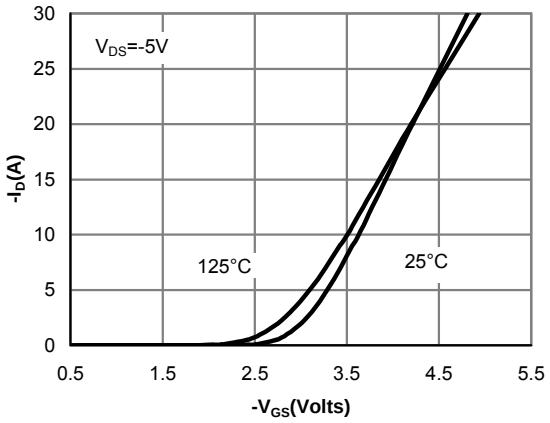


Figure 2: Transfer Characteristics (Note E)

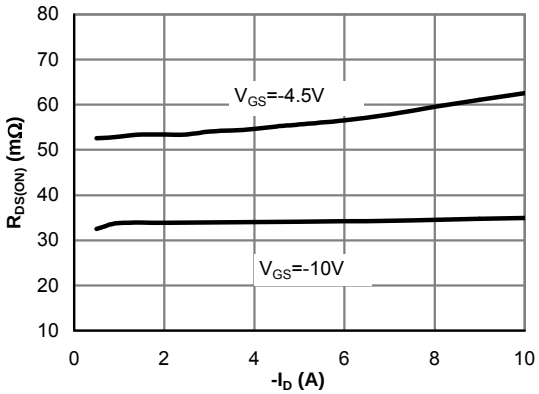


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

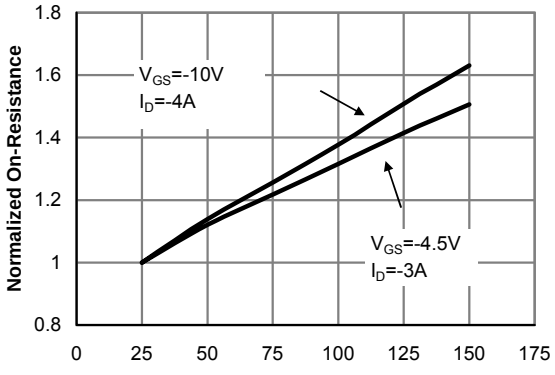


Figure 4: On-Resistance vs. Junction Temperature (Note E)

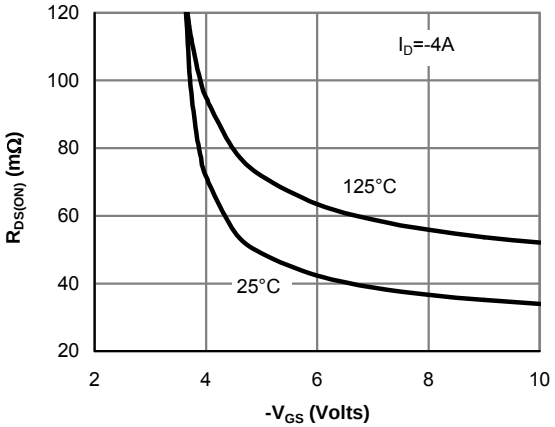


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

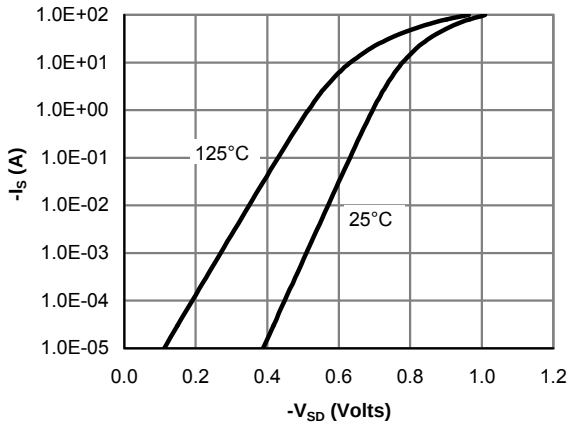


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL CHARACTERISTICS

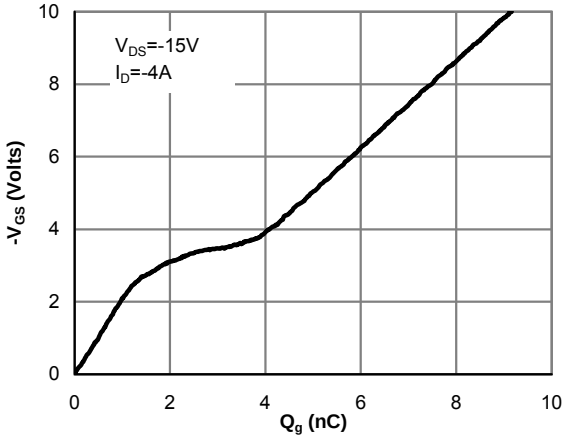


Figure 7: Gate-Charge Characteristics

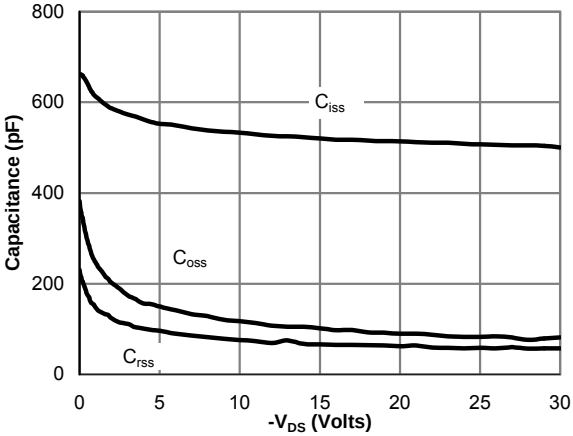


Figure 8: Capacitance Characteristics

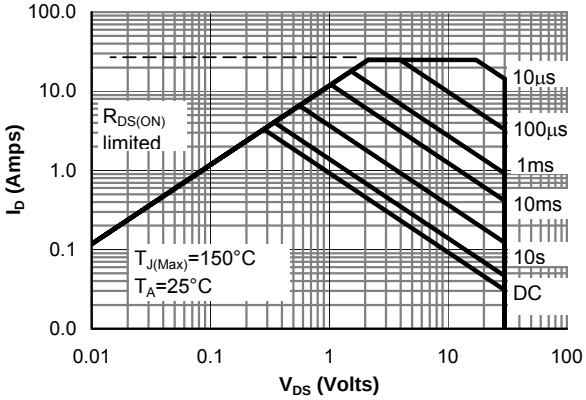


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

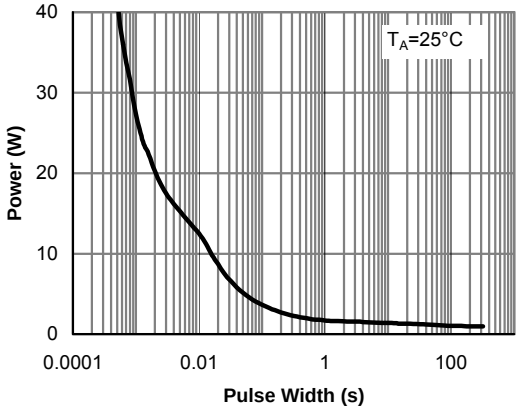


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

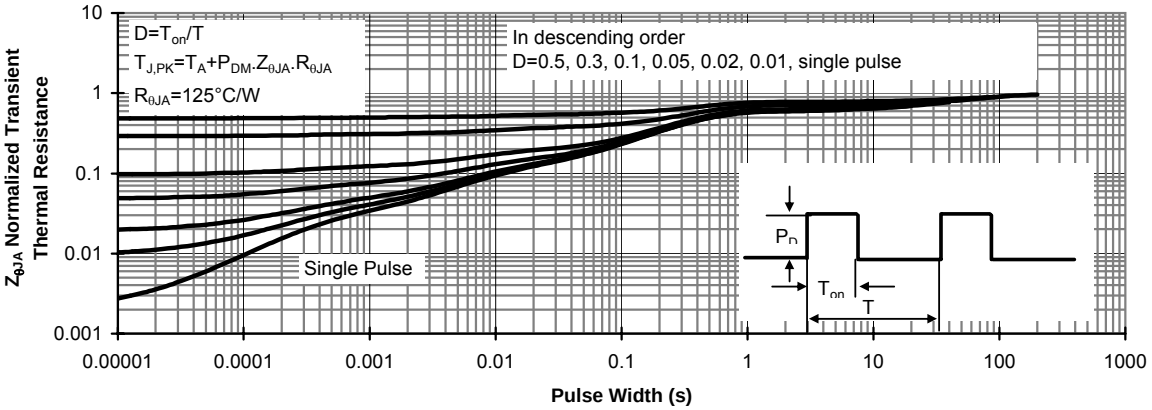
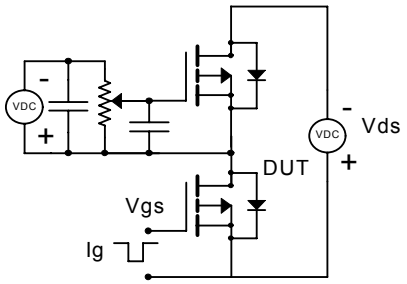
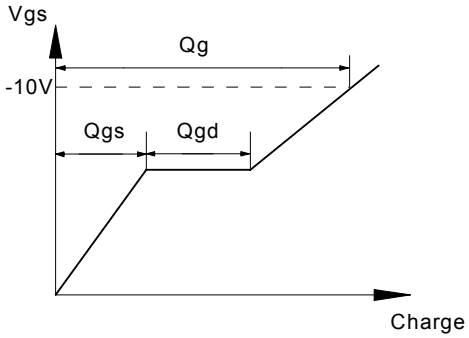


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

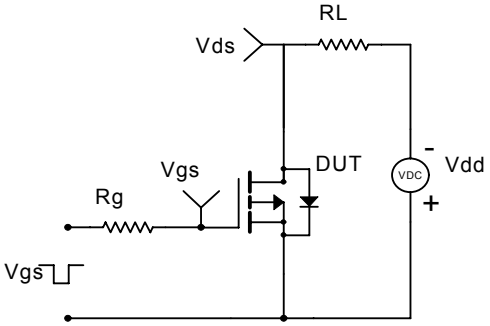
LP3407LT1G , S-LP3407LT1G

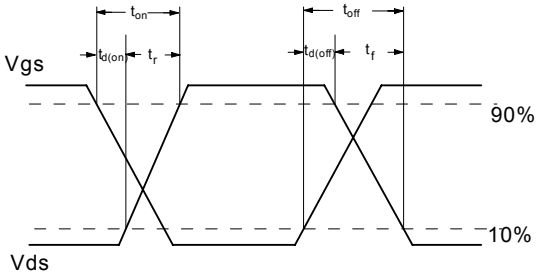
Gate Charge Test Circuit & Waveform



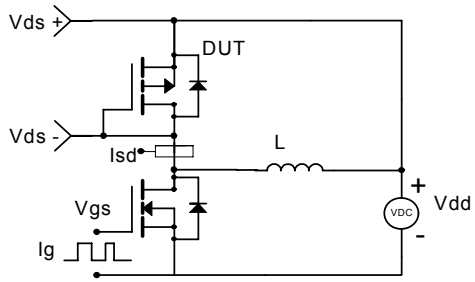


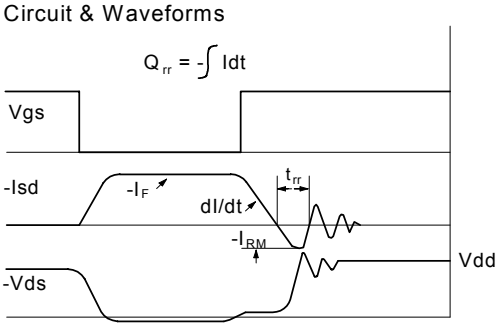
Resistive Switching Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





LP3407LT1G , S-LP3407LT1G

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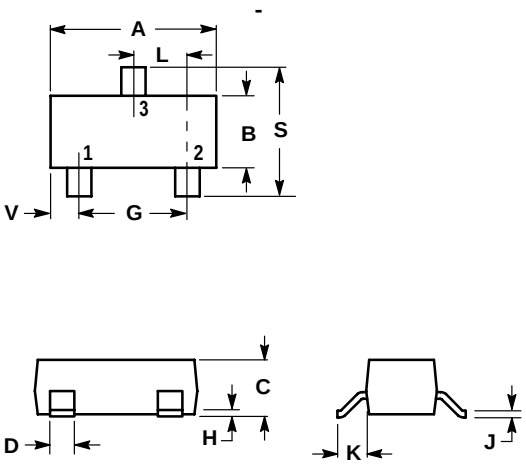

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60