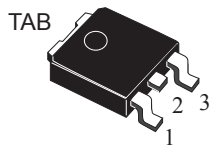
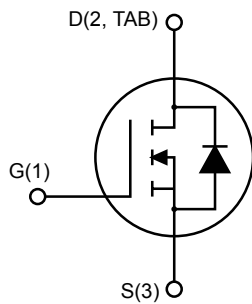


## N-channel 100 V, 60 mΩ typ., 23 A, STripFET™ II Power MOSFET in a DPAK package


**DPAK**


AM01475v1\_noZen

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STD15NF10T4	100 V	65 mΩ	23 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

### Applications

- Switching applications

### Description

This Power MOSFET series has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

#### Product status link

[STD15NF10T4](#)

#### Product summary

<b>Order code</b>	STD15NF10T4
<b>Marking</b>	D15NF10
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{DGR}$	Gate-source voltage ( $R_{GS} = 20\text{ k}\Omega$ )	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	23	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	16	A
$I_{DM}^{(1)}$	Drain current (pulsed)	92	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	180	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	9	V/ns
$T_{stg}$	Storage temperature range	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 10\text{ A}$ ,  $V_{DD} = 30\text{ V}$
3.  $I_{SD} \leq 13\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DS} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.14	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

$T_{CASE} = 25\text{ °C}$  unless otherwise specified

**Table 3. On-/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, T_C = 125\text{ °C}^{(1)}$			10	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DD} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$		60	65	m $\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	870		pF
$C_{oss}$	Output capacitance		-	125		pF
$C_{riss}$	Reverse transfer capacitance		-	50		pF
$Q_g$	Total gate charge	$V_{DD} = 80\text{ V}, I_D = 24\text{ A}$	-	30	40	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	6		nC
$Q_{gd}$	Gate-drain charge	(see Figure 12. Test circuit for gate charge behavior)	-	10		nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}, I_D = 12\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	60	-	ns
$t_r$	Rise time		-	45	-	ns
$t_{d(off)}$	Turn-off delay time		-	49	-	ns
$t_f$	Fall time		-	17	-	ns

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		23	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		92	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}, V_{GS} = 0\text{ V}$	-		1.5	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{rr}$	Reverse recovery time	$I_{SD} = 24 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	100		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 30 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$	-	375		nC
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 16. Switching time waveform</a> )	-	7.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

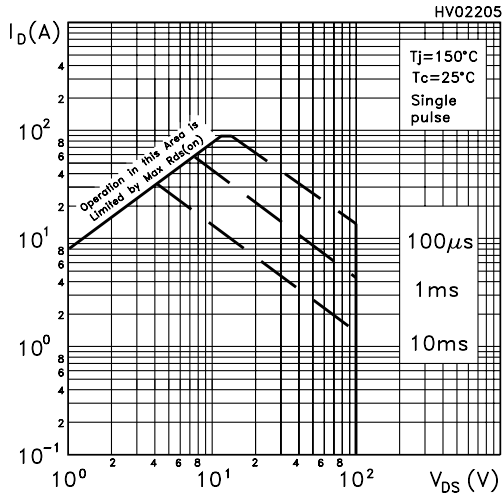


Figure 2. Thermal impedance

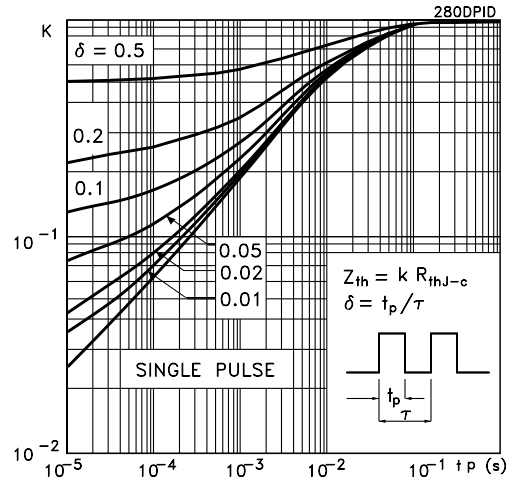


Figure 3. Output characteristics

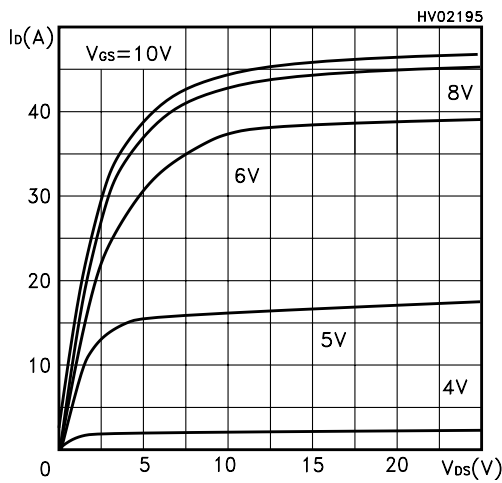
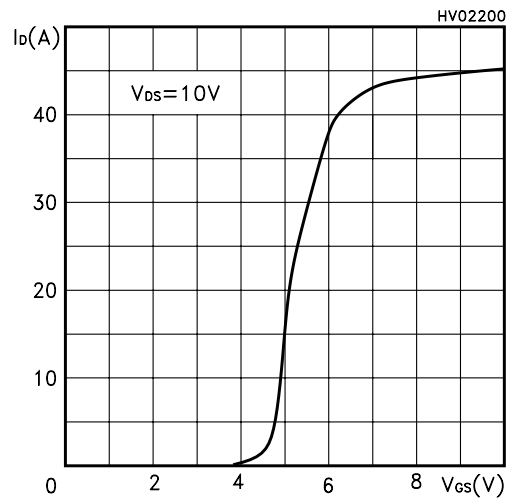
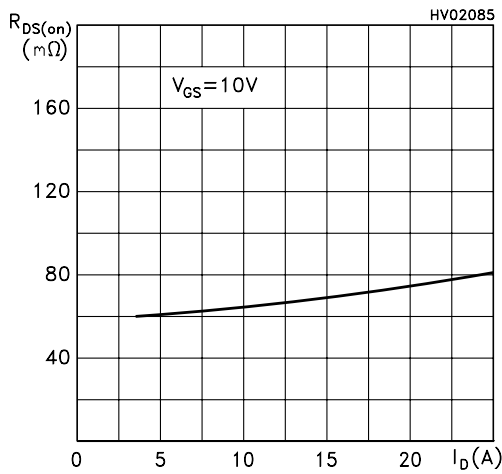


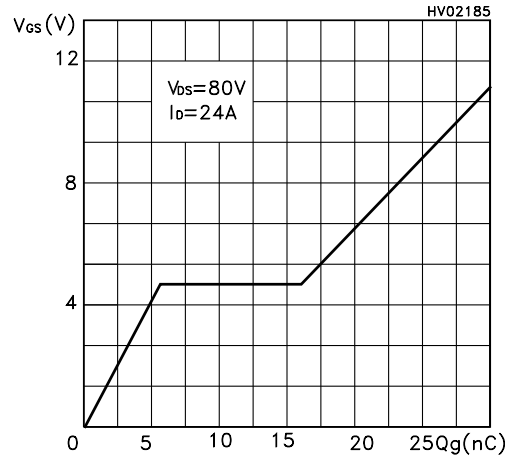
Figure 4. Transfer characteristics



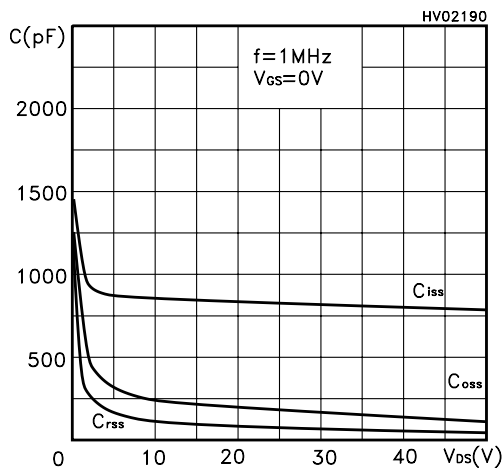
**Figure 5. Static drain-source on-resistance**



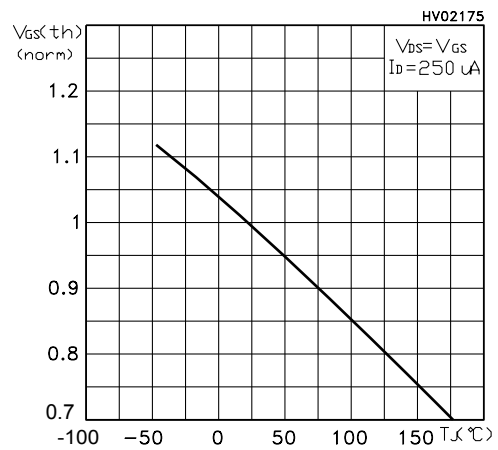
**Figure 6. Gate charge vs gate-source voltage**



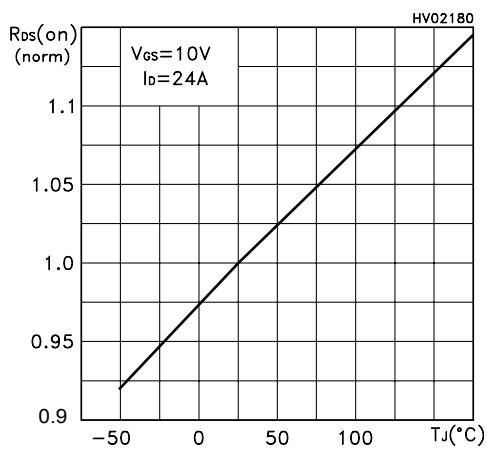
**Figure 7. Capacitance variations**



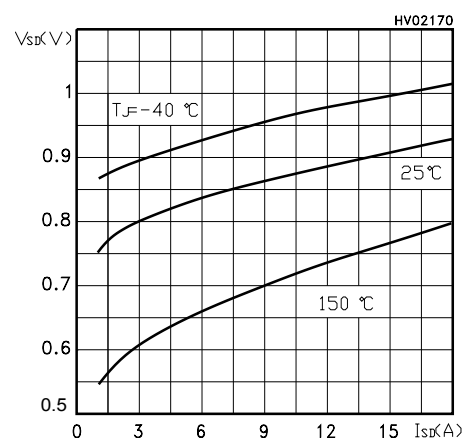
**Figure 8. Normalized gate threshold voltage vs temperature**



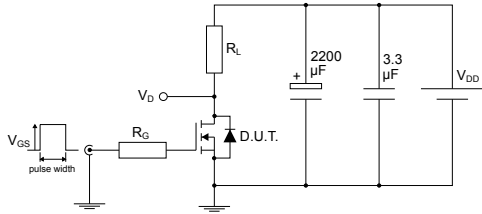
**Figure 9. Normalized on-resistance vs temperature**



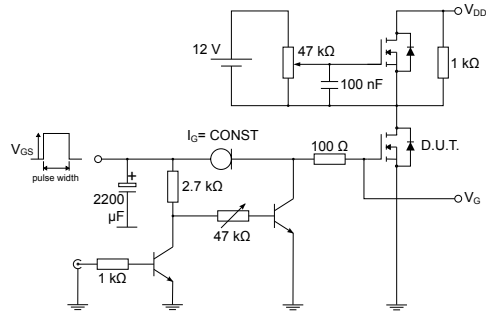
**Figure 10. Source-drain diode forward characteristics**



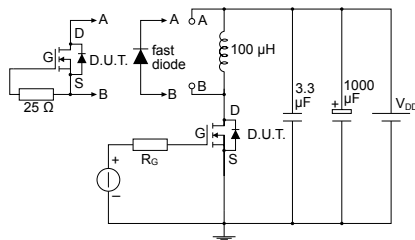
### 3 Test circuits

**Figure 11. Test circuit for resistive load switching times**


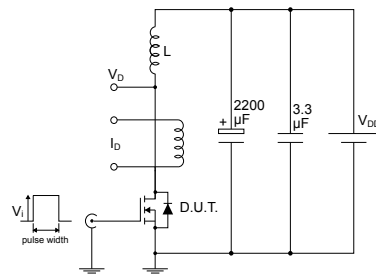
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**Figure 12. Test circuit for gate charge behavior**


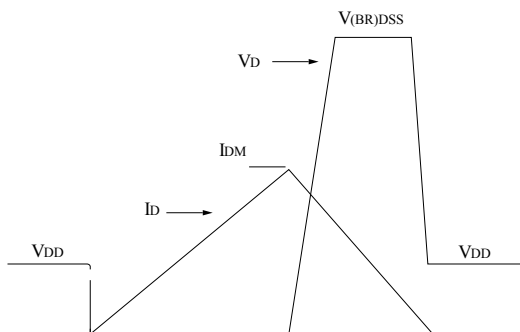
AM01469v1

**Figure 13. Test circuit for inductive load switching and diode recovery times**


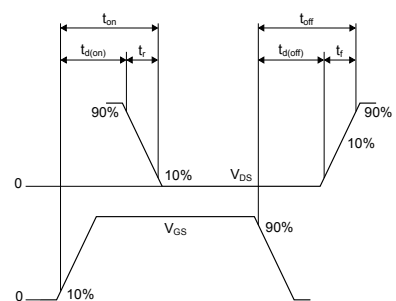
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**Figure 14. Unclamped inductive load test circuit**


AM01471v1

**Figure 15. Unclamped inductive waveform**


AM01472v1

**Figure 16. Switching time waveform**


AM01473v1

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## 4 Package information

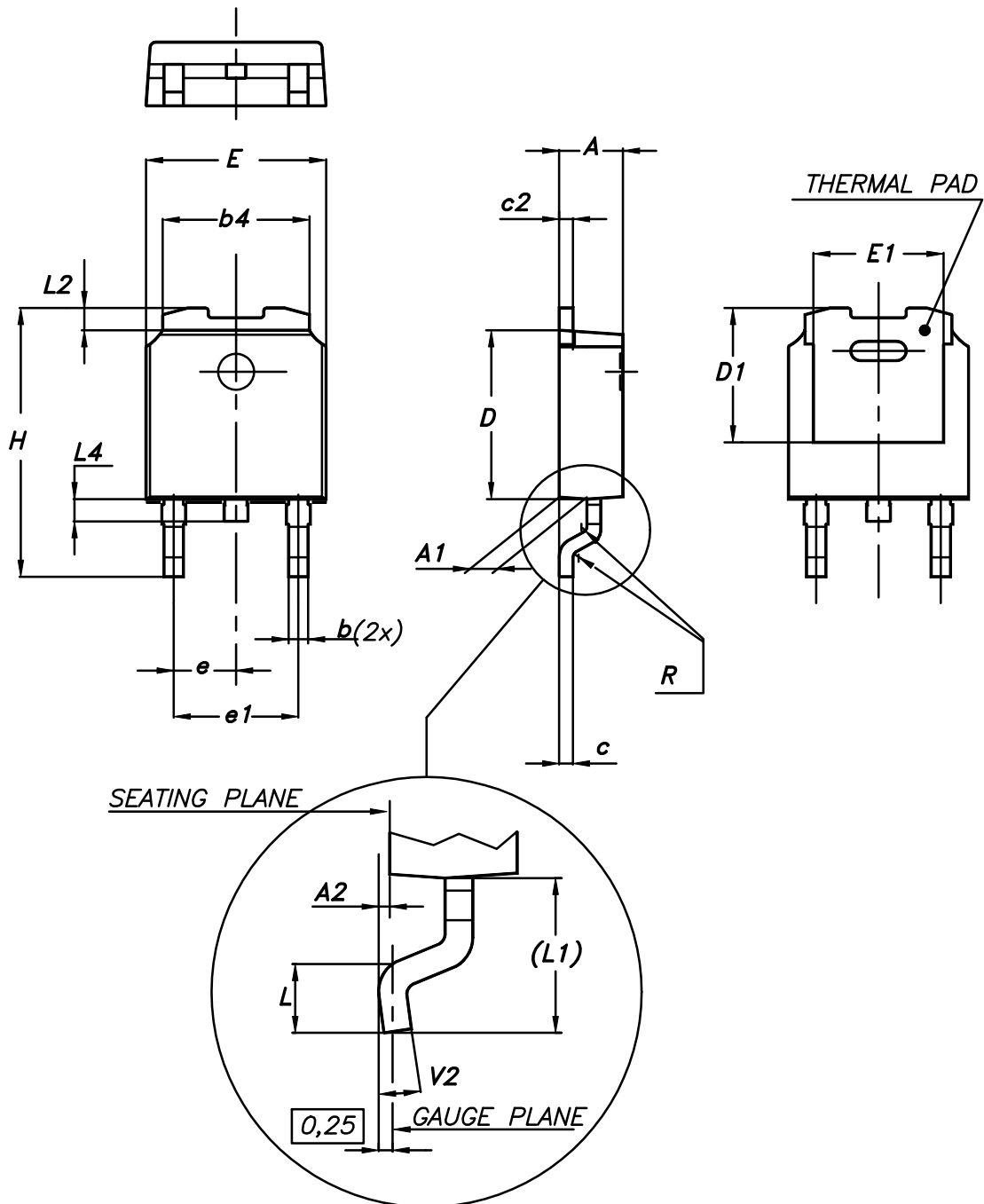
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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.



### 4.1 DPAK (TO-252) type A package information

Figure 17. DPAK (TO-252) type A package outline



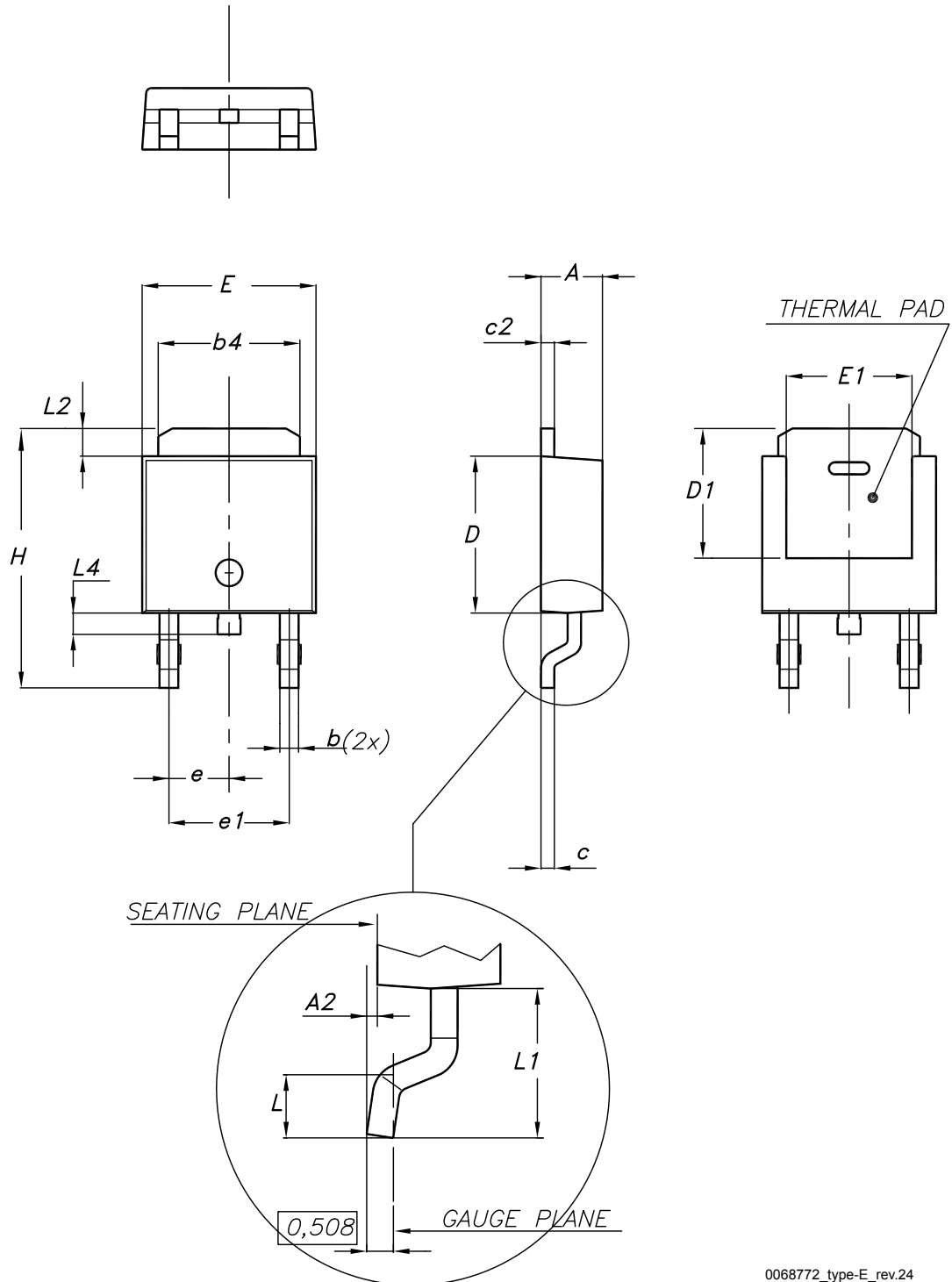
0068772\_A\_24

**Table 7. DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

## 4.2 DPAK (TO-252) type E package information

Figure 18. DPAK (TO-252) type E package outline

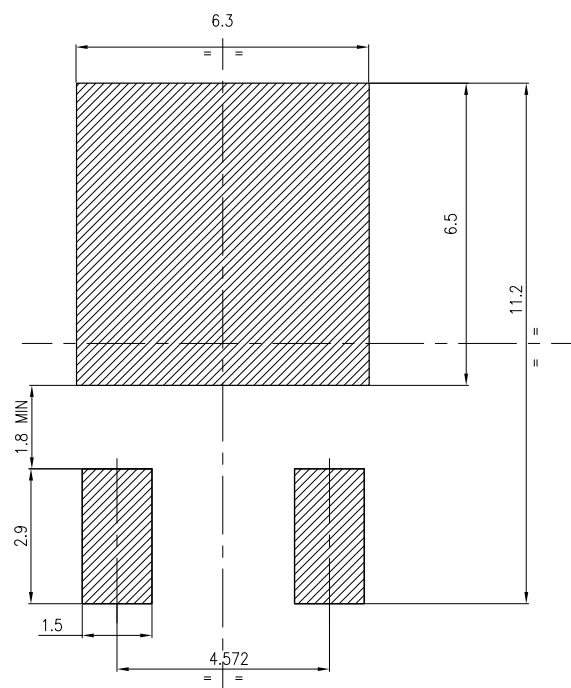


0068772\_type-E\_rev.24

**Table 8. DPAK (TO-252) type E mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

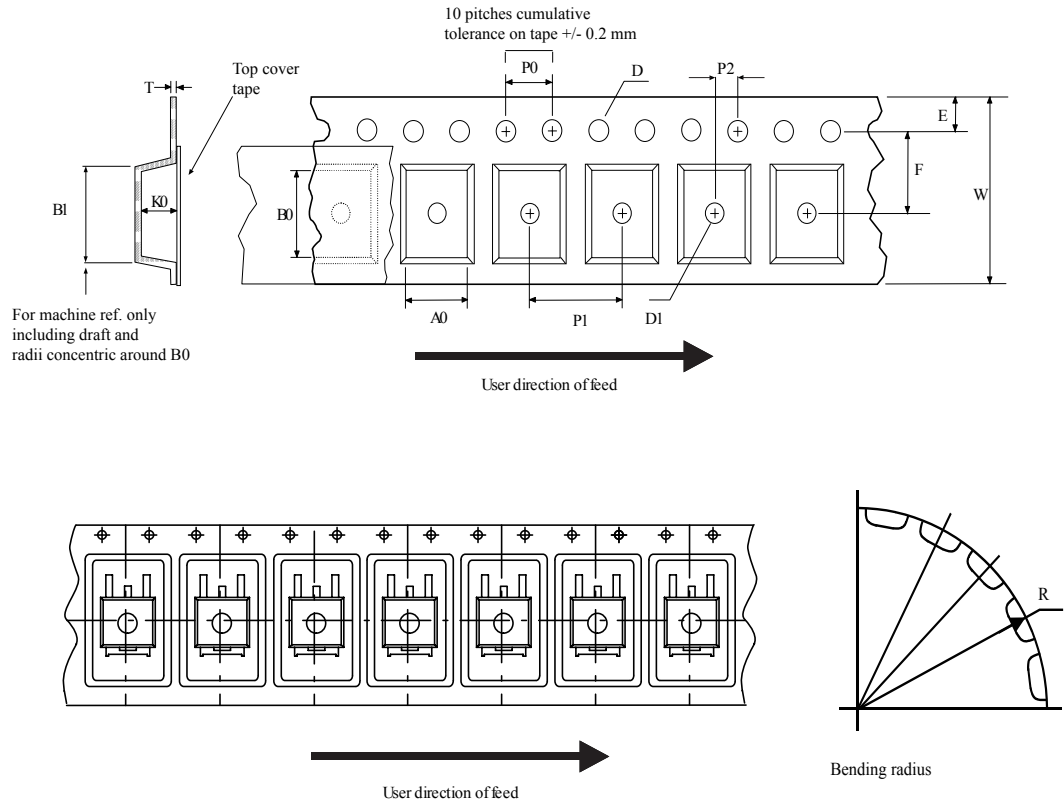
**Figure 19. DPAK (TO-252) recommended footprint (dimensions are in mm)**



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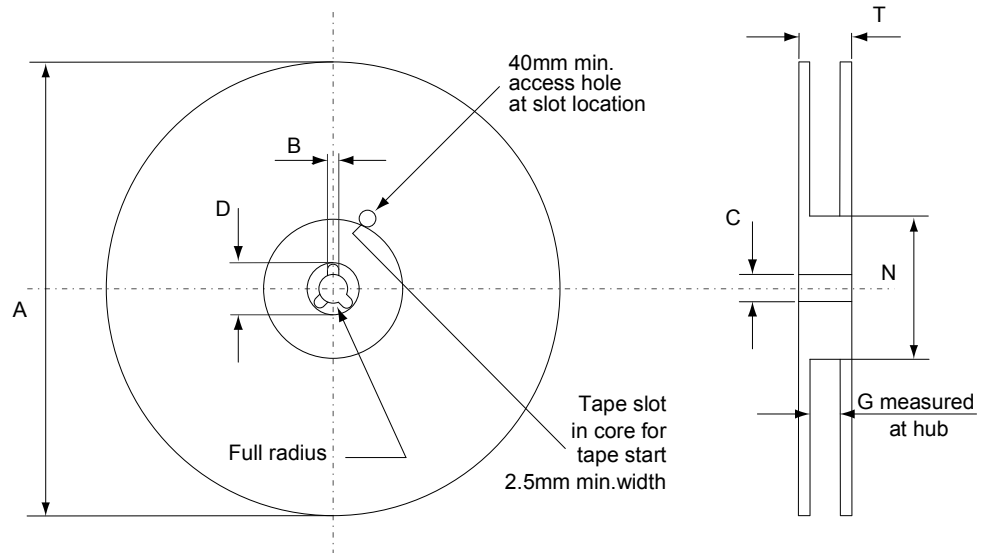
### 4.3 DPAK (TO-252) packing information

Figure 20. DPAK (TO-252) tape outline



AM08852v1

**Figure 21. DPAK (TO-252) reel outline**



AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
19-Apr-2018	1	Initial release. The document status is production data.

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