BROADCOM®

Data Sheet

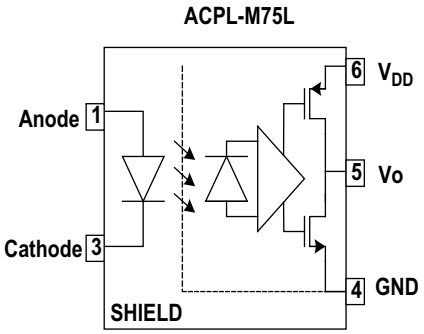
ACPL-M75L

High-Speed 15 MBd CMOS Optocoupler

Description

The Broadcom® ACPL-M75L is a 15 MBd CMOS optocoupler in a SOIC-5 package. This optocoupler utilizes the latest CMOS IC technology to achieve outstanding performance with very low power consumption. The basic building blocks of the ACPL-M75L are high-speed LEDs and CMOS detector ICs. Each detector incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



NOTE: A 0.1-µF bypass capacitor must be connected between pins 4 and 6.

Truth Table

LED	V_O, Output
OFF	H
ON	L

Features

- +3.3V and +5V CMOS compatibility
- 25 ns max. pulse width distortion
- 55 ns max. propagation delay
- 40 ns max. propagation delay skew
- High speed: 15 MBd min
- 10 kV/µs minimum Common-Mode Rejection (CMR)
- –40°C to +105°C temperature range
- Safety and regulatory approvals:
  - UL recognized: 3750 V_{rms} for 1 min. per UL 1577
  - CSA component acceptance Notice #5
  - IEC/EN/DIN EN 60747-5-5 approved Option 060

Applications

- Digital field bus isolation:
  - RS485, RS232, CANbus
- Multiplexed data transmission
- Computer peripheral interface
- Microprocessor system interface
- DC/DC converter
- Servo motor

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments. The components are not AEC-Q100 qualified and not recommended for automotive applications.

Ordering Information

ACPL-M75L will be UL Recognized with 3750 V_{rms} for 1 minute per UL1577.

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-M75L	-000E	SO-5	X			100 per tube
	-500E		X	X		1500 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

Use part number ACPL-M75L-500E to order a product with a Small Outline SO-5 package in Tape and Reel packaging in RoHS compliant.

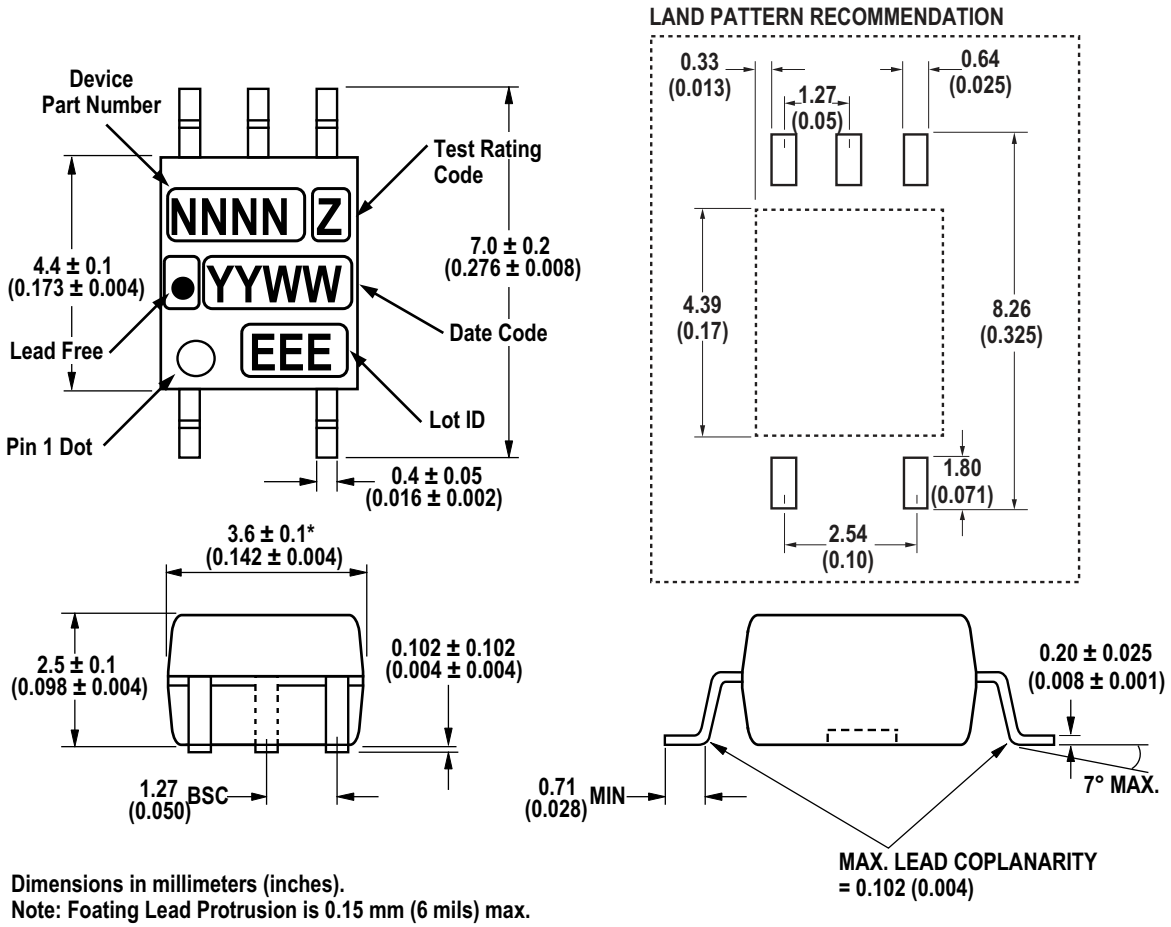
Example 2:

Use part number ACPL-M75L-000E to order a product with a Small Outline SO-5 package in tube packaging and in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawing

ACPL-M75L (JEDEC MO-155 Package)



Dimensions in millimeters (inches).
Note: Foating Lead Protrusion is 0.15 mm (6 mils) max.

*** Maximum Mold flash on each side is 0.15 mm (0.006).**

Reflow Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-M75L has been approved by the following organizations:

- **UL** – Recognized under UL 1577, component recognition program, File E55361.
- **CSA** – Approval under CSA Component Acceptance Notice #5, File CA 88324.
- **IEC/EN/DIN EN 60747-5-5**

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (Clearance)	L(I01)	≥5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	≥5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	≥175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics (Option 060)

Description	Symbol	Option 060	Unit
Installation Classification per DIN VDE 0110/1.89, Table 1 For Rated Mains Voltage ≤150 V_{rms} For Rated Mains Voltage ≤300 V_{rms}		 I-IV I-III	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1s, Partial Discharge < 5 pC	V_{PR}	1063	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10s, Partial Discharge < 5 pC	V_{PR}	907	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60s)	V_{IOTM}	6000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Thermal Derating curve, Figure 11.) Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 150 150 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500V	R_{IO}	≥10^9	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	–55	+125	°C
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD}	0	6.0	V
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V
Average Forward Input Current	I_F	—	10.0	mA
Average Output Current	I_O	—	10.0	mA
Lead Solder Temperature	260°C for 10s, 1.6 mm below seating plane			
Solder Reflow Temperature Profile	See Reflow Soldering Profile.			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Ambient Operating Temperature	T_A	–40	+105	°C
Supply Voltages	V_{DD}	4.5	5.5	V
		3.0	3.6	V
Input Current (ON)	I_F	4	8	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Supply Voltage Slew Rate[a]	S_R	0.5	500	V/ms

a. Slew rate of supply voltage ramping is recommended to ensure no glitch more than 1V to appear at the output pin.

Electrical Specifications

Over recommended temperature (T_A = –40°C to +105°C), 3.0V ≤ V_{DD} ≤ 3.6V and 4.5V ≤ V_{DD} ≤ 5.5V.
All typical specifications are at T_A = +25°C, V_{DD} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Forward Voltage	V_F	1.3	1.5	1.8	V	I_F = 6 mA
Input Reverse Breakdown Voltage	BV_R	5.0	—	—	V	I_R = 10 µA
Logic High Output Voltage	V_{OH}	V_{DD} – 1	V_{DD} – 0.3	—	V	I_F = 0, I_O = –4 mA, V_{DD} = 3.3V
		V_{DD} – 1	V_{DD} – 0.2	—	V	I_F = 0, I_O = –4 mA, V_{DD} = 5V
Logic Low Output Voltage	V_{OL}	—	0.2	0.8	V	I_F = 6 mA, I_O = 4 mA, V_{DD} = 3.3V
		—	0.35	0.8	V	I_F = 6 mA, I_O = 4 mA, V_{DD} = 5V
Input Threshold Current	I_{TH}	—	1	3	mA	I_{OL} = 20 µA
Logic Low Output Supply Current	I_{DDL}	—	4.5	6.5	mA	I_F = 6 mA
Logic High Output Supply Current	I_{DDH}	—	4	6	mA	I_F = 0

Switching Specifications

Over recommended temperature (T_A = –40°C to +105°C), 3.0V ≤ V_{DD} ≤ 3.6V and 4.5V ≤ V_{DD} ≤ 5.5V.
All typical specifications are at T_A = +25°C, V_{DD} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Propagation Delay Time to Logic Low Output[a]	t_{PHL}	—	25	55	ns	I_F = 6 mA, C_L= 15 pF CMOS signal levels
Propagation Delay Time to Logic High Output[a]	t_{PLH}	—	21	55	ns	I_F = 6 mA, C_L= 15 pF, CMOS signal levels
Pulse Width	t_{PW}	66.7	—	—	ns	
Pulse Width Distortion[b]	|PWD |	0	4	25	ns	I_F = 6 mA, C_L= 15 pF, CMOS signal levels
Propagation Delay Skew[c]	t_{PSK}	—	—	40	ns	I_F = 6 mA, C_L= 15 pF CMOS signal levels
Output Rise Time (10% to 90%)	t_R	—	3.5	—	ns	I_F = 6 mA, C_L= 15 pF CMOS signal levels
Output Fall Time (90% to 10%)	t_F	—	3.5	—	ns	I_F = 6 mA, C_L= 15 pF CMOS signal levels
Common Mode Transient Immunity at Logic High Output[d]	| CM_H |	10	15	—	kV/µs	V_{CM} = 1000V, T_A = 25°C, I_F = 0 mA (Figure 18)
		30	35	—	kV/µs	Using Broadcom's Application Circuit (Figure 13)
Common Mode Transient Immunity at Logic Low Output[e]	| CM_L |	10	15	—	kV/µs	V_{CM} = 1000V, T_A = 25°C, I_F = 6 mA (Figure 18)
		30	35	—	kV/µs	Using Broadcom's Application Circuit (Figure 13)

a. t_{PHL} propagation delay is measured from the 50% V_{DD} level on the rising edge of the input pulse to the 50% V_{DD} level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% V_{DD} level on the falling edge of the input pulse to the 50% V_{DD} level of the rising edge of the V_O signal

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to ensure that the output remains in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to ensure that the output remains in a low logic state.

Package Characteristics

All typical specifications are at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input-Output Insulation	I_{I-O}	—	—	1.0	µA	45% RH, t = 5s, V_{I-O} = 3 kV DC, T_A = 25°C
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	3750		—	V_{rms}	RH ≤ 50%, t = 1 min., T_A = 25°C
Input-Output Resistance	R_{I-O}	—	10^{12}	—	Ω	V_{I-O} = 500 V dc
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz, T_A = 25°C

a. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{rms} for 1 second (Leakage detection current limit, I_{I-O} ≤ 5 µA).

Figure 1: Typical Input Diode Forward Characteristic

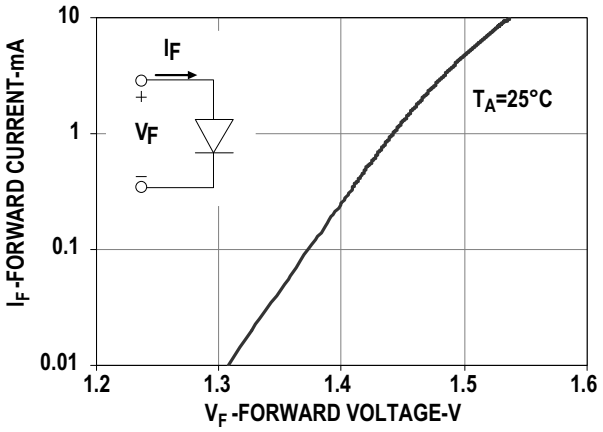


Figure 2: Typical Input Threshold Current vs. Temperature

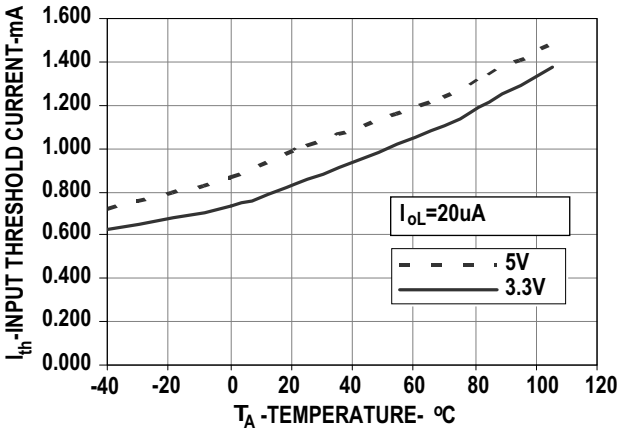


Figure 3: Typical Logic High O/P Supply Current vs. Temperature

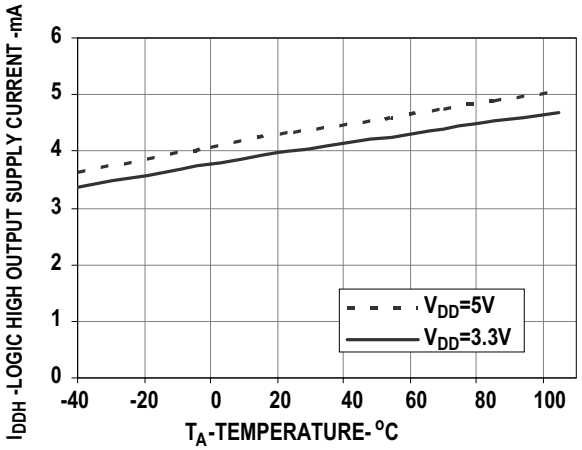


Figure 4: Typical Logic Low O/P Supply Current vs. Temperature

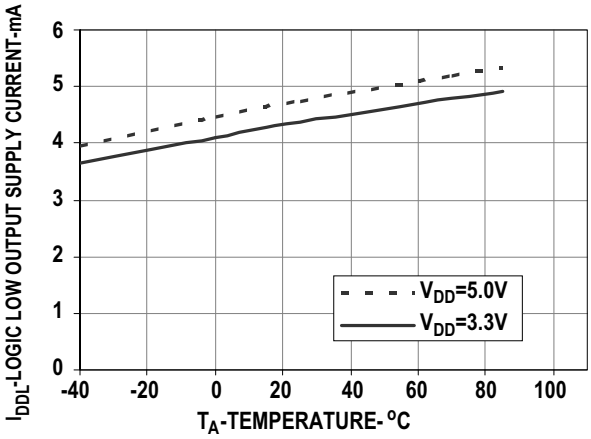


Figure 5: Typical Switching Speed vs. Pulse Input Current at 5V Supply Voltage

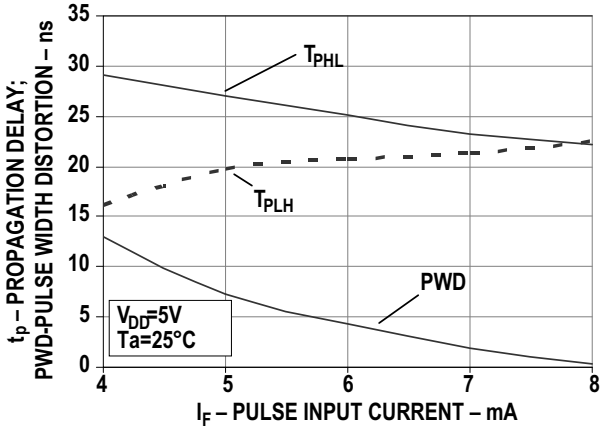


Figure 6: Typical Switching Speed vs. Pulse Input Current at 3.3V Supply Voltage

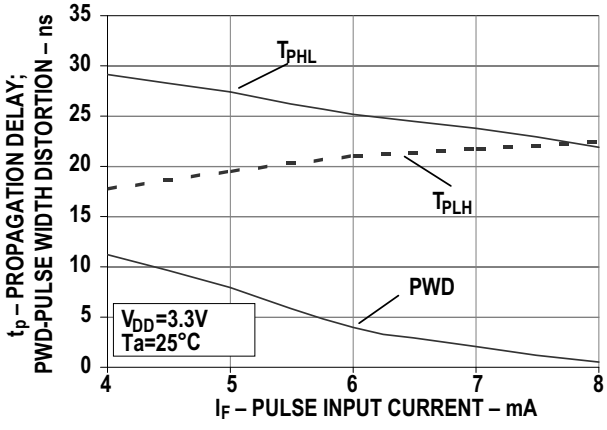


Figure 7: Typical V_F vs. Temperature

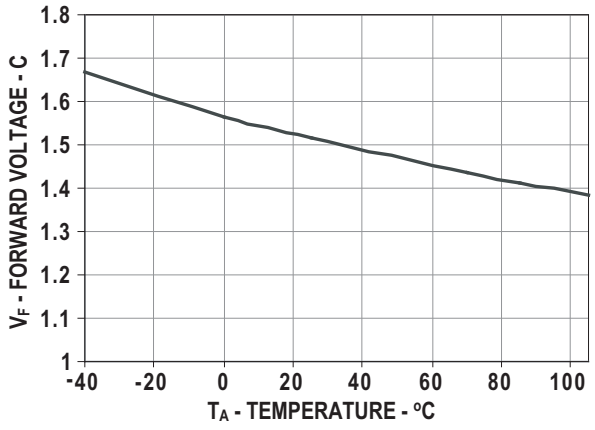
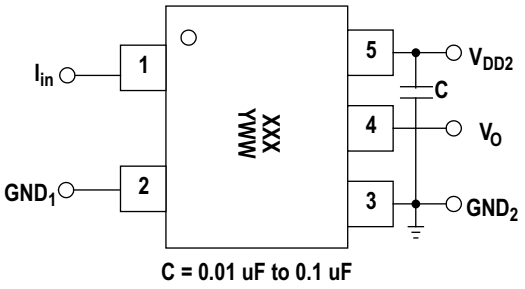


Figure 8: Recommended Printed Circuit Board Layout



Application Information

Bypassing and PC Board Layout

The ACPL-M75L optocoupler is extremely easy to use. ACPL-M75L provides CMOS logic output due to the high-speed CMOS IC technology used.

The external components required for proper operation are the input limiting resistor and the output bypass capacitor. Capacitor values should be between 0.01 µF and 0.1 µF. They should be placed as close as possible to the power supply and ground pins of the optocoupler.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high.

Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 9).

Figure 9: Propagation Delay and Skew Waveform

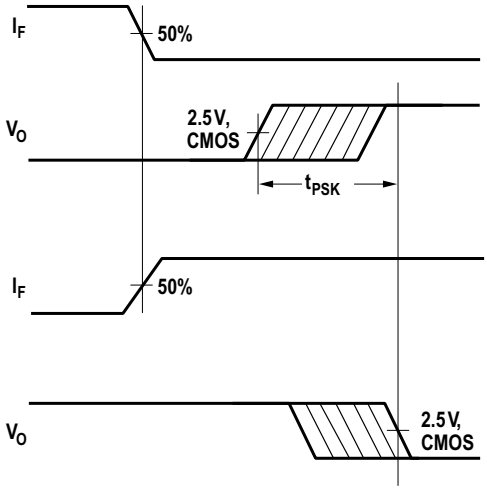
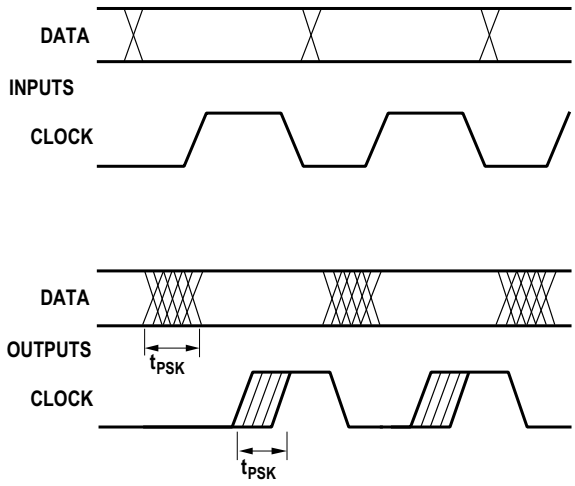


Figure 10: Parallel Data Transmission Example



Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often PWD determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20% to 30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern.

If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers that are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}. As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate.

Figure 10 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 10 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap; otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs might start to change before the clock signal has arrived.

From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

Figure 11: Connection of Peaking Capacitor (C_{peak}) in Parallel of the Input Limiting Resistor (R_{limit}) to Improve Speed Performance

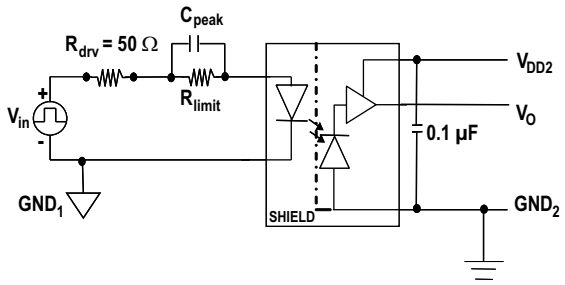
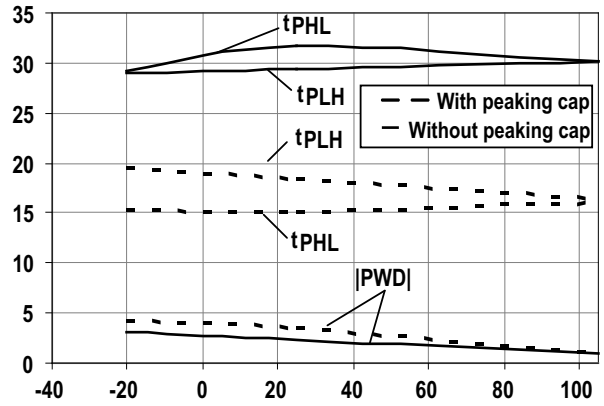
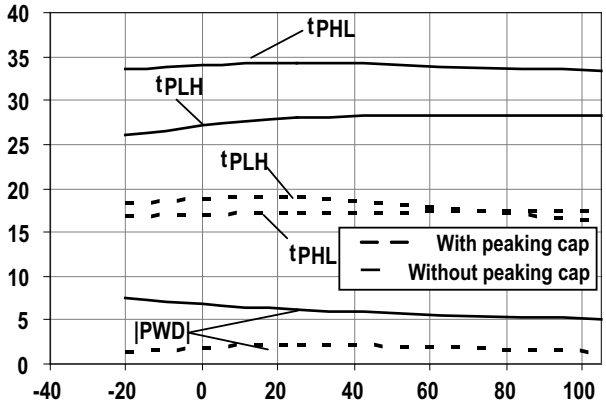


Figure 12: Improvement of tp and PWD with Added 100 pF Peaking Capacitor in Parallel of Input Limiting Resistor



(i) V_{DD} = 5V, C_{peak} = 100 pF, R_{limit} = 530Ω



(ii) V_{DD} = 3.3V, C_{peak} = 100 pF, R_{limit} = 250Ω

Powering Sequence

V_{DD} needs to achieve a minimum level of 3V before powering up the output connecting component.

Input Limiting Resistors

ACPL-M75L is direct current driven (Figure 8), and thus eliminate the need for input power supply. To limit the amount of current flowing through the LED, it is recommended that a 530Ω resistor is connected in series with anode of LED (i.e., Pin 1 for ACPL-M75L) at 5V input signal. At 3.3V input signal, it is recommended to connect 250Ω resistor in series with anode of LED. The recommended limiting resistors is based on the assumption that the driver output impedence is 50Ω (as shown in Figure 11).

Speed Improvement

A peaking capacitor can be placed across the input current limit resistor (Figure 11) to achieve enhanced speed performance. The value of the peaking cap is dependent to the rise and fall time of the input signal and supply voltages and LED input driving current (I_F). Figure 12 shows significant improvement of propagation delay and pulse width distortion with added peak capacitor at driving current of 6 mA for both 3.3V and 5V power supply.

Common Mode Rejection for ACPL-M75L

Figure 13 shows the recommended drive circuit for the ACPL-M75L for optimal common-mode rejection performance.

Two LED-current setting resistors are used instead of one. This is to balance the common mode impedance at LED anode and cathode. Common-mode transients can capacitively couple from the LED anode (or cathode) to the output-side ground causing current to be shunted away from the LED (which can be bad if the LED is on) or conversely cause current to be injected into the LED (bad if the LED is meant to be off). Figure 14 shows the parasitic capacitances which exists between LED anode/cathode and output ground (C_{LA} and C_{LC}). Also shown in Figure 14 on the input side is an AC-equivalent circuit.

Table 1 indicates the directions of I_{LP} and I_{LN} flow depending on the direction of the common-mode transient. For transients occurring when the LED is on, common-mode rejection (CM_L, since the output is in the *low* state) depends upon the amount of LED current drive (I_F). For conditions where I_F is close to the switching threshold (I_{TH}), CM_L also depends on the extent that I_{LP} and I_{LN} balance each other. In other words, any condition where common-mode transients cause a momentary decrease in I_F (that is, when $dV_{CM}/dt > 0$ and $|I_{FP}| > |I_{FN}|$, refer to Table 1) will cause common-mode failure for transients that are fast enough.

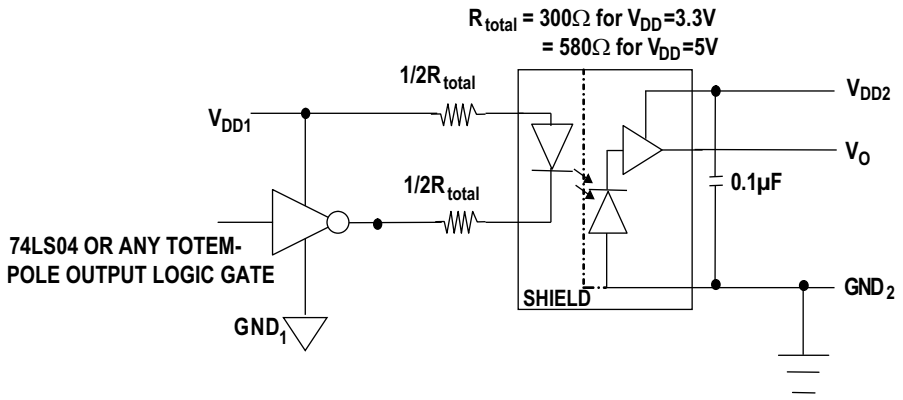
Likewise for common-mode transients that occur when the LED is off (i.e., CM_H, since the output is *high*), if an imbalance between I_{LP} and I_{LN} results in a transient I_F equal to or greater than the switching threshold of the optocoupler, the transient *signal* might cause the output to spike below 2V (which constitutes a CM_H failure).

By using the recommended circuit in Figure 13, good CMR can be achieved. The resistors recommended in Figure 13 include both the output impedence of the logic driver circuit and the external limiting resistor. The balanced I_{LED}-setting resistors help equalize the common-mode voltage change at anode and cathode to reduce the amount by which I_{LED} is modulated from transient coupling through C_{LA} and C_{LC}.

Table 1: Effects of Common Mode Pulse Direction on Transient I_{LED}

If dV_{CM}/dt Is:	Then I_{LP} Flows:	And I_{LN} Flows:	If $\|I_{LP}\| < \|I_{LN}\|$, LED I_F Current Is Momentarily:	If $\|I_{LP}\| > \|I_{LN}\|$, LED I_F Current Is Momentarily:
positive (>0)	away from LED anode through C_{LA}	away from LED cathode through C_{LC}	increased	decreased
negative (<0)	toward LED anode through C_{LA}	toward LED cathode through C_{LC}	decreased	increased

Figure 13: Recommended Drive Circuit for ACPL-M75L for High-CMR



CMR with Other Drive Circuits

CMR performance with drive circuits other than that shown in Figure 13 can be enhanced by following these guidelines:

1. Use of drive circuits where current is shunted from the LED in the LED *off* state (as shown in Figure 15 and Figure 16). This is beneficial for good CM_H.
2. Use of typical I_{FH} = 6 mA per data sheet recommendation.

Using any one of the drive circuits in Figure 15 to Figure 17 with I_F = 6 mA will result in a typical CMR of 10 kV/s for ACPL-M75L, as long as the PC board layout practices are followed.

Figure 15 shows a circuit that can be used with any totem-pole-output TTL/LSTTL/HCMOS logic gate. The buffer PNP transistor allows the circuit to be used with logic devices that have low current-sinking capability. It also helps maintain the driving-gate power-supply current at a constant level to minimize ground shifting for other devices connected to the input-supply ground.

When using an open-collector TTL or open-drain CMOS logic gate, the circuit in Figure 16 can be used. When using a CMOS gate to drive the optocoupler, the circuit shown in Figure 17, where the resistor is recommended to connect to the anode of the LED, can be used.

Figure 14: AC Equivalent of ACPL-M75L

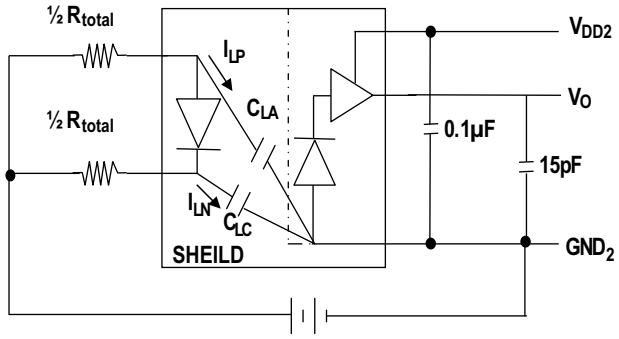


Figure 15: TTL Interface Circuit for the ACPI-M75L Families

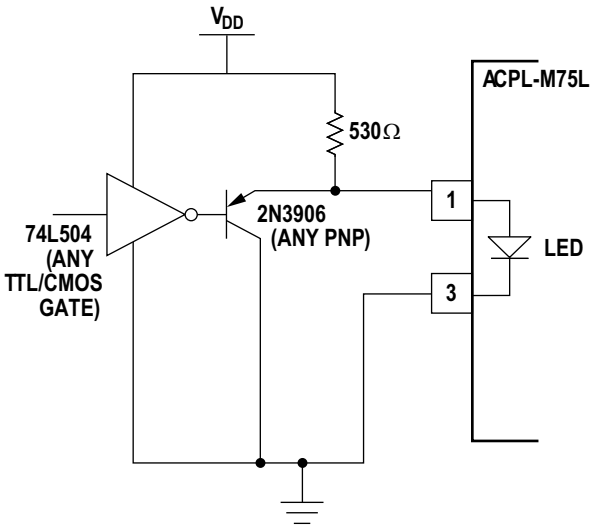


Figure 16: TTL Open-Collector/Open Drain Gate Drive Circuit for ACPL-M75L Families

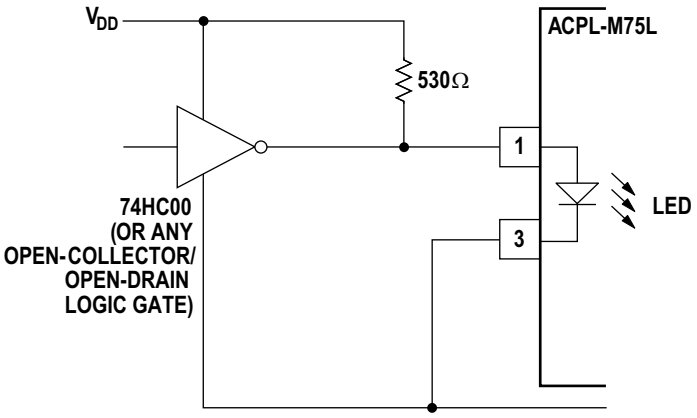


Figure 17: CMOS Gate Drive Circuit for ACPL-M75L Families

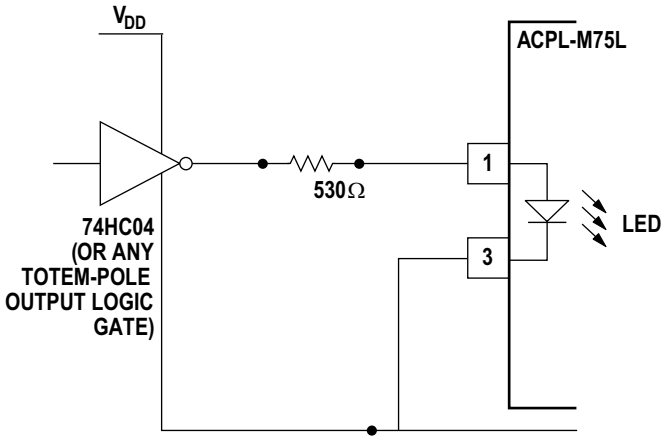
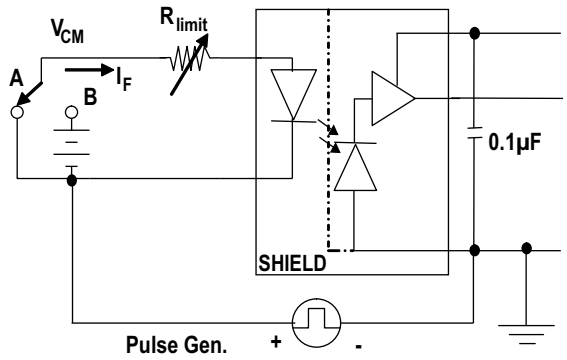
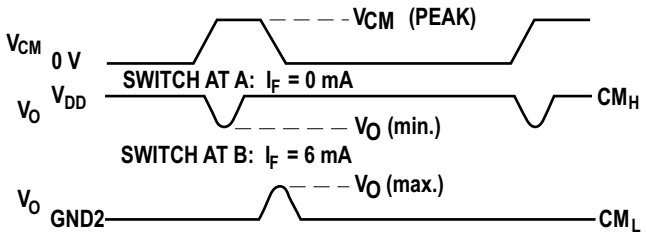


Figure 18: Test Circuit for Common Mode Transient Immunity and Typical Waveforms





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