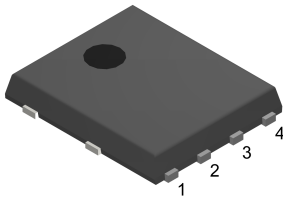
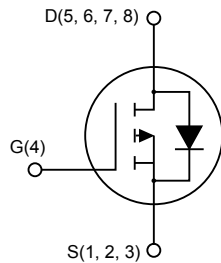


## P-channel 40 V, 11.5 mΩ typ., 60 A STripFET F6 Power MOSFET in a PowerFLAT 5x6 package


**PowerFLAT 5x6**


AM01475v4


**Product status link**
[STL60P4LLF6](#)
**Product summary**

<b>Order code</b>	STL60P4LLF6
<b>Marking</b>	60P4LLF6
<b>Package</b>	PowerFLAT 5x6
<b>Packing</b>	Tape and reel

*Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.*

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL60P4LLF6	40 V	14 mΩ	60 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	60	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	42	A
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	240	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	13	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	9.3	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	52	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$P_{TOT}^{(2)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
	Derating factor <sup>(2)</sup>	0.03	W/°C
$T_{stg}$	Storage temperature	-55 to 175	°C
$T_J$	Maximum junction temperature	175	°C

1. The value is limited by  $R_{thj-case}$ .
2. The value is limited by  $R_{thj-pcb}$ .
3. Pulse width is limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb, single operation	31.3	°C/W

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$ .

**Note:** For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$ , $T_C = 125\text{ °C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 6.5\text{ A}$		11.5	14	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 6.5\text{ A}$		15	19	

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	3525	-	pF
$C_{oss}$	Output capacitance		-	344	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	238	-	pF
$Q_g$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 13\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see Figure 13. Gate charge test circuit)	-	34	-	nC
$Q_{gs}$	Gate-source charge		-	11.3	-	nC
$Q_{gd}$	Gate-drain charge		-	13.8	-	nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 6.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 12. Switching times test circuit for resistive load)	-	49.4	-	ns
$t_r$	Rise time		-	60.6	-	ns
$t_{d(off)}$	Turn-off-delay time		-	170	-	ns
$t_f$	Fall time		-	20	-	ns

*Note:* For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 6.5\text{ A}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	29		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 24\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	27.6		nC
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	1.9		A

1. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

Note: For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

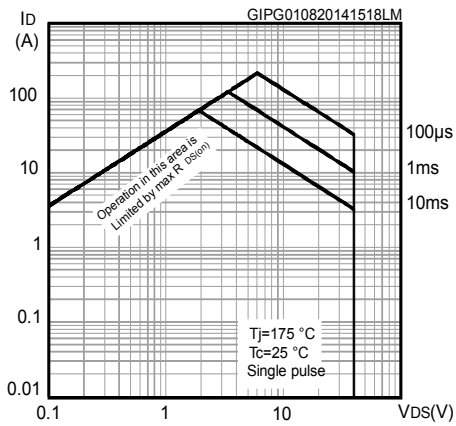


Figure 2. Thermal impedance

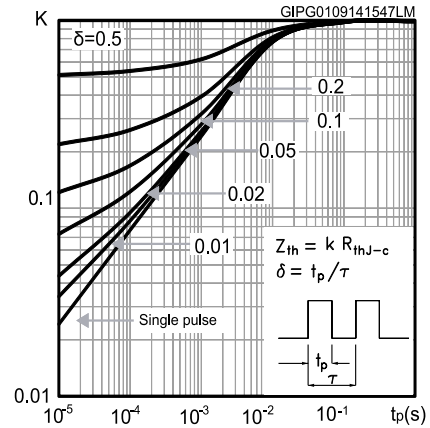


Figure 3. Output characteristics

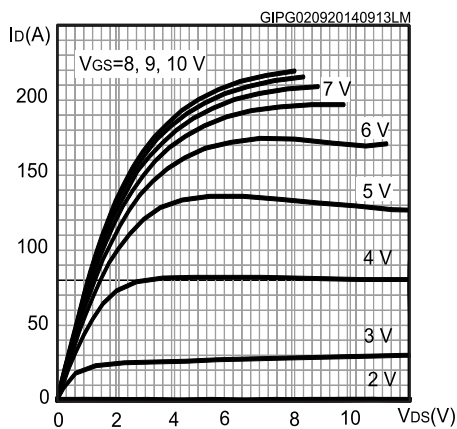


Figure 4. Transfer characteristics

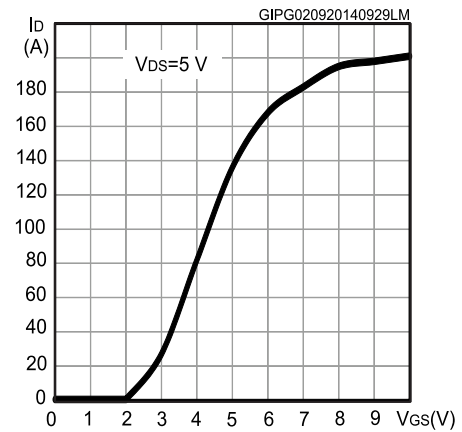


Figure 5. Normalized gate threshold voltage vs temperature

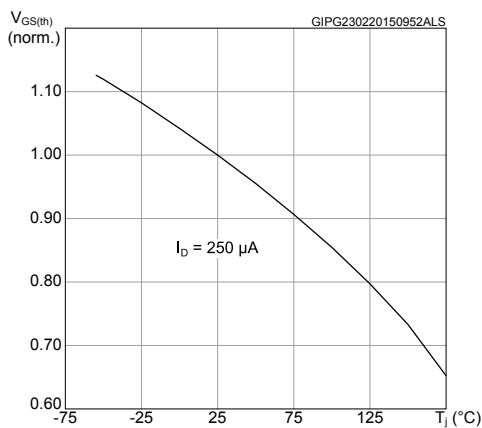
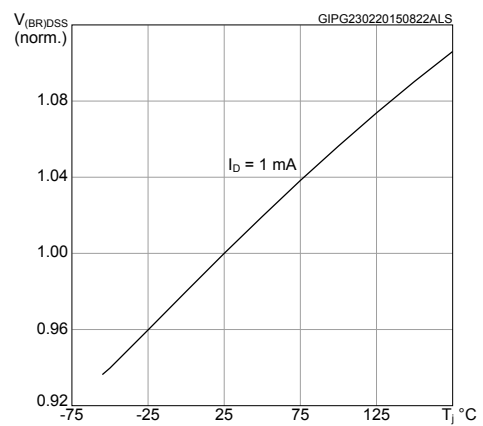
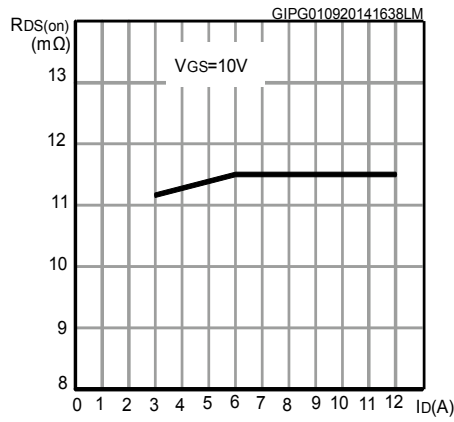


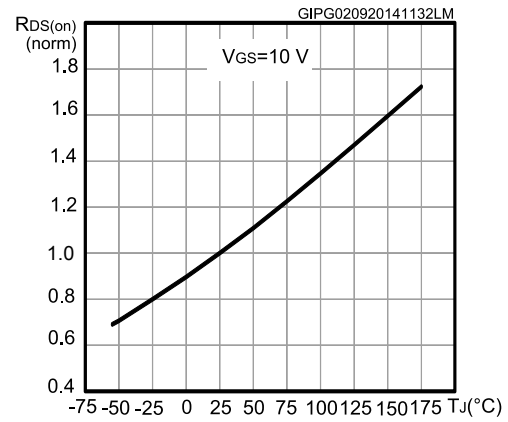
Figure 6. Normalized  $V_{(BR)DSS}$  vs temperature



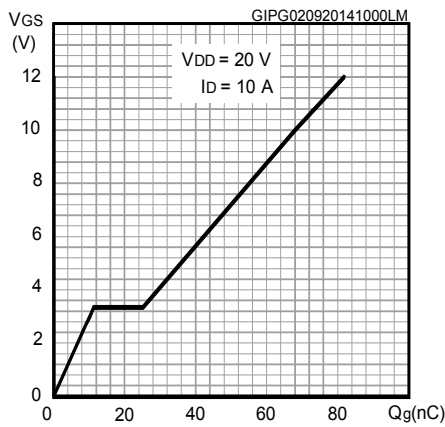
**Figure 7. Static drain-source on-resistance**



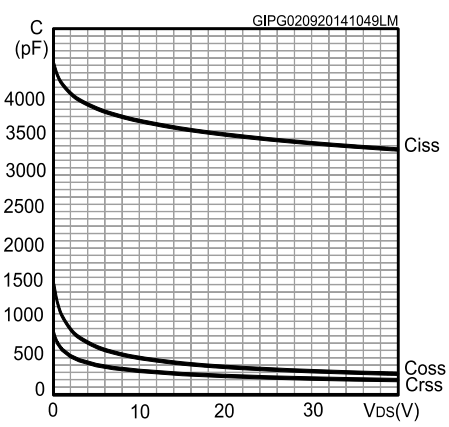
**Figure 8. Normalized on-resistance vs. temperature**



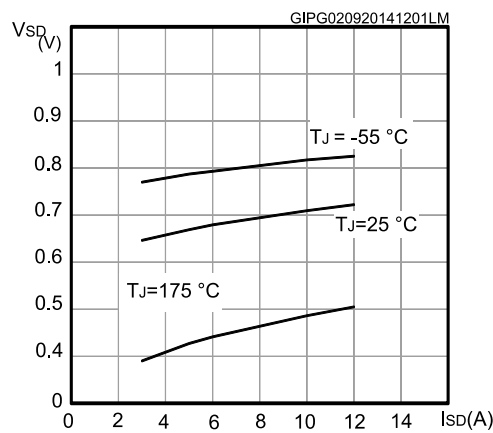
**Figure 9. Gate charge vs gate-source voltage**



**Figure 10. Capacitance variations voltage**



**Figure 11. Source-drain diode forward characteristics**



### 3 Test circuits

Figure 12. Switching times test circuit for resistive load

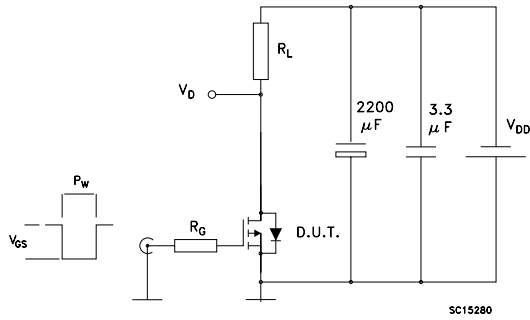


Figure 13. Gate charge test circuit

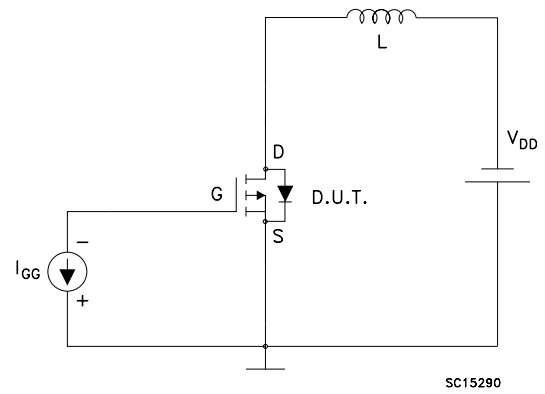
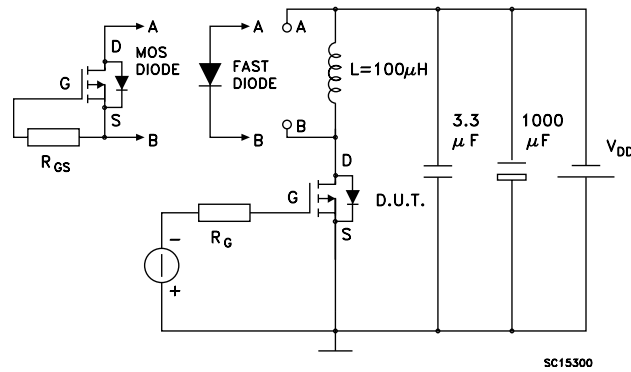


Figure 14. Test circuit for inductive load switching and diode recovery times

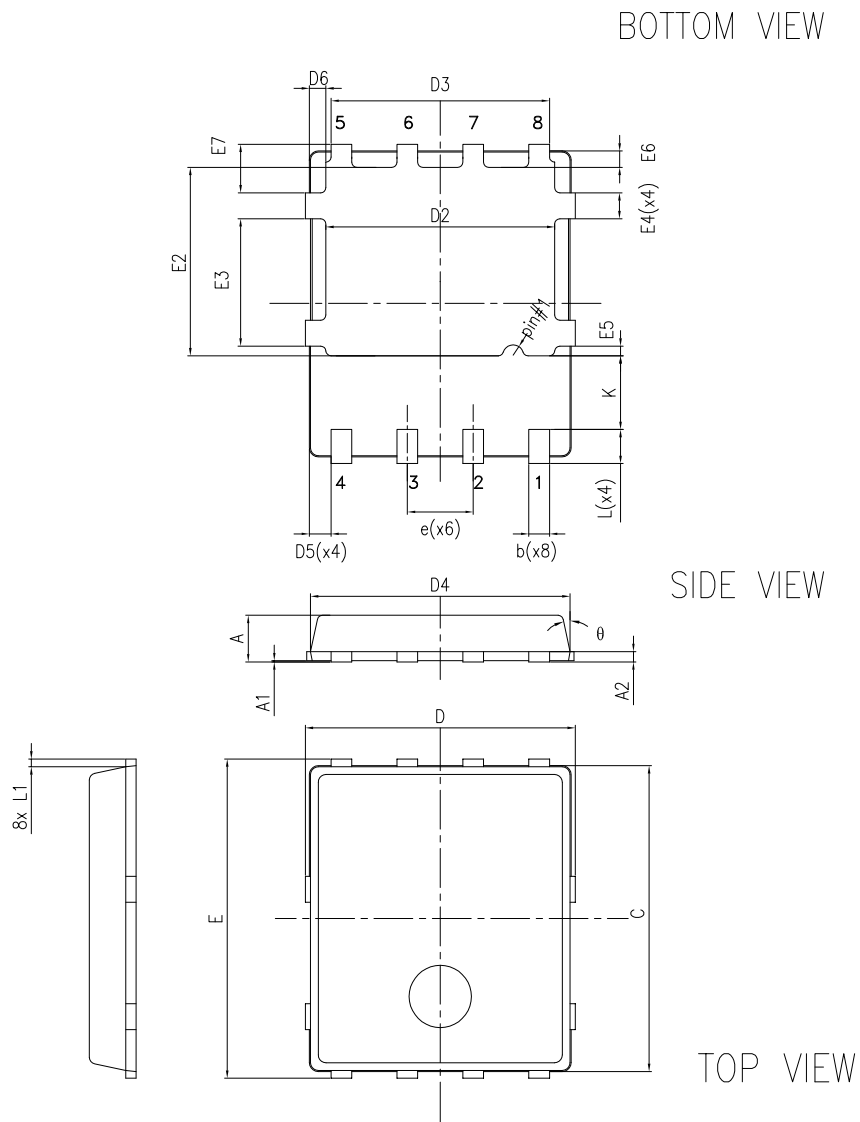


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 PowerFLAT 5x6 type R package information

**Figure 15. PowerFLAT 5x6 type R package outline**



A0ER\_8231817\_Rev20

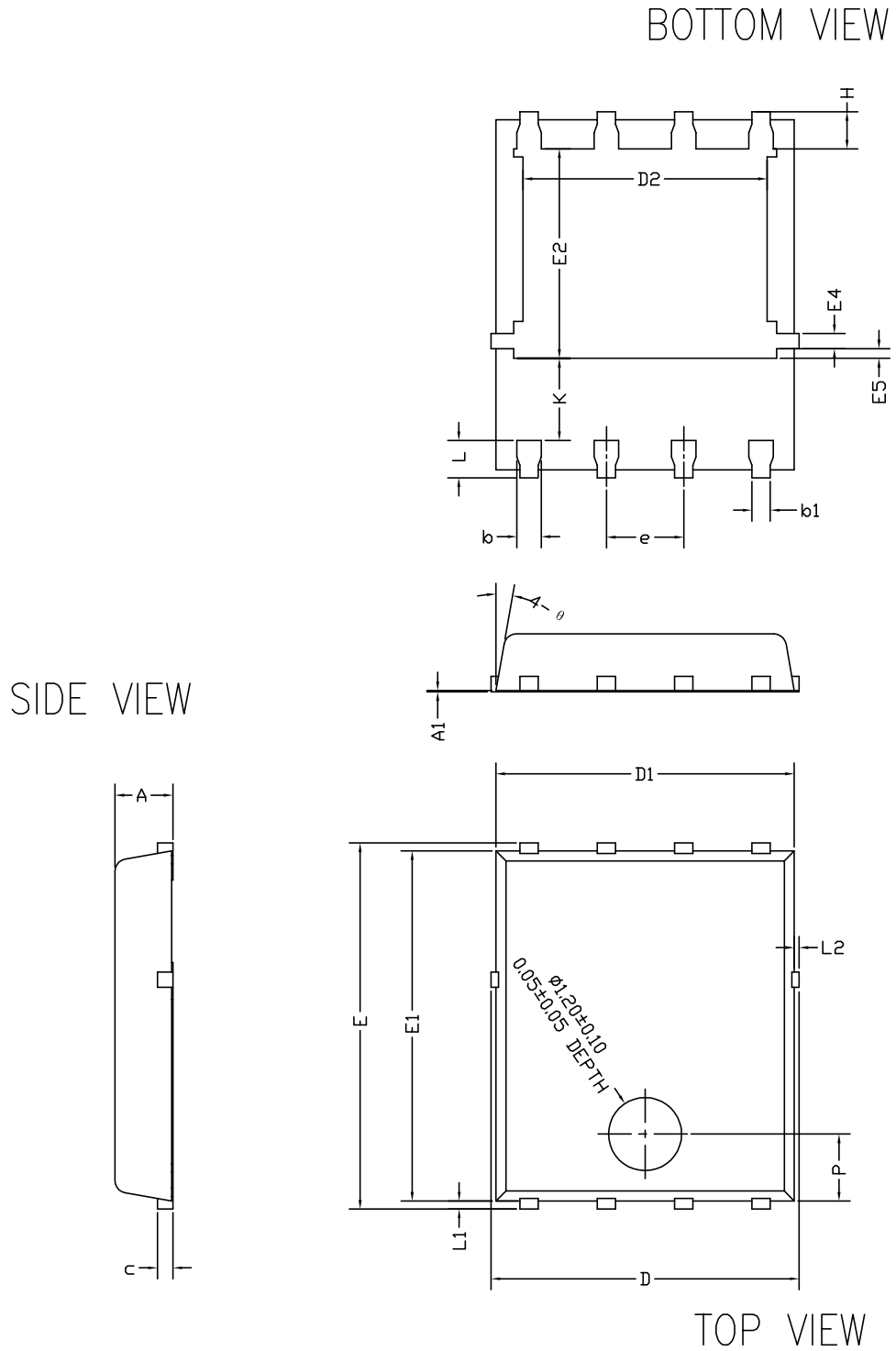


**Table 7. PowerFLAT 5x6 type R mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

## 4.2 PowerFLAT 5x6 type R SUBCON package information

Figure 16. PowerFLAT 5x6 type R SUBCON package outline

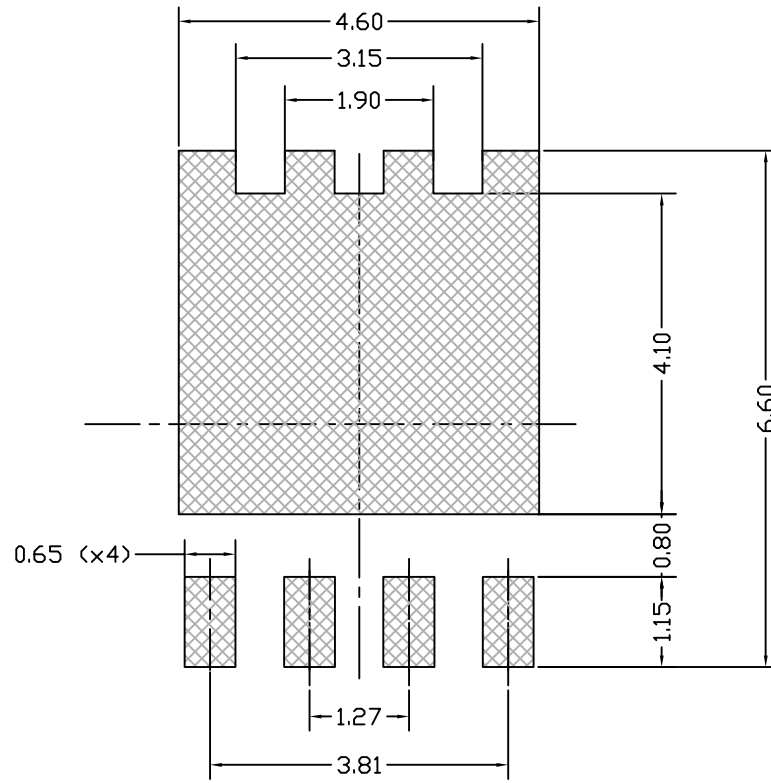


8472137\_SUBCON\_998G\_Type\_R\_REV4

**Table 8. PowerFLAT 5x6 type R SUBCON package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
E4	0.15	0.25	0.35
E5	0.06	0.16	0.26
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
$\theta$	8°	10°	12°

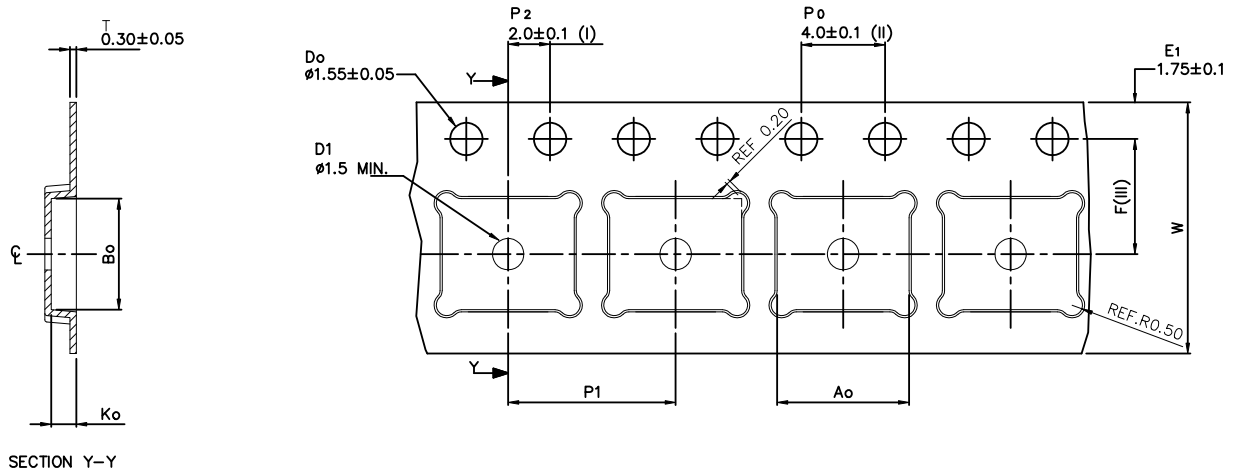
Figure 17. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817\_FOOTPRINT\_simp\_Rev\_20

### 4.3 PowerFLAT 5x6 packing information

Figure 18. PowerFLAT 5x6 tape (dimensions are in mm)



A <sub>0</sub>	6.30	+/- 0.1
B <sub>0</sub>	5.30	+/- 0.1
K <sub>0</sub>	1.20	+/- 0.1
F	5.50	+/- 0.1
P <sub>1</sub>	8.00	+/- 0.1
W	12.00	+/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

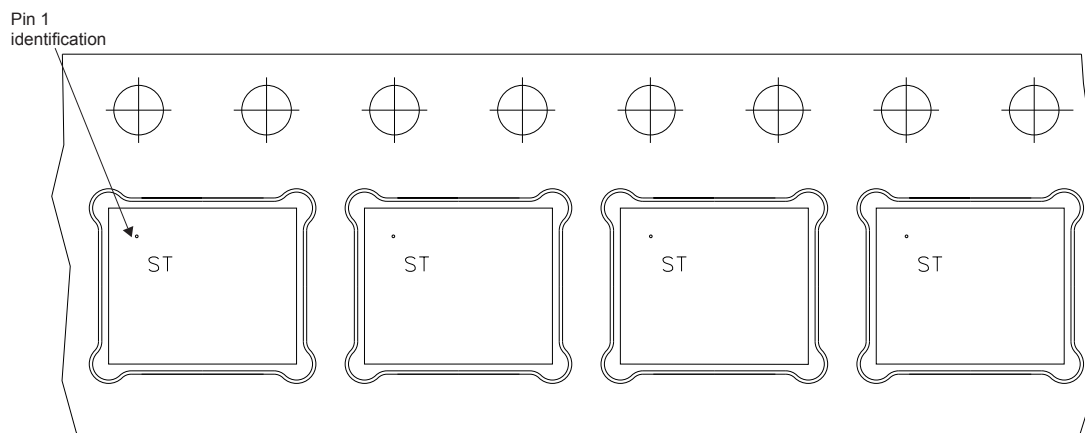
(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

(III) Measured from centreline of sprocket hole to centreline of pocket

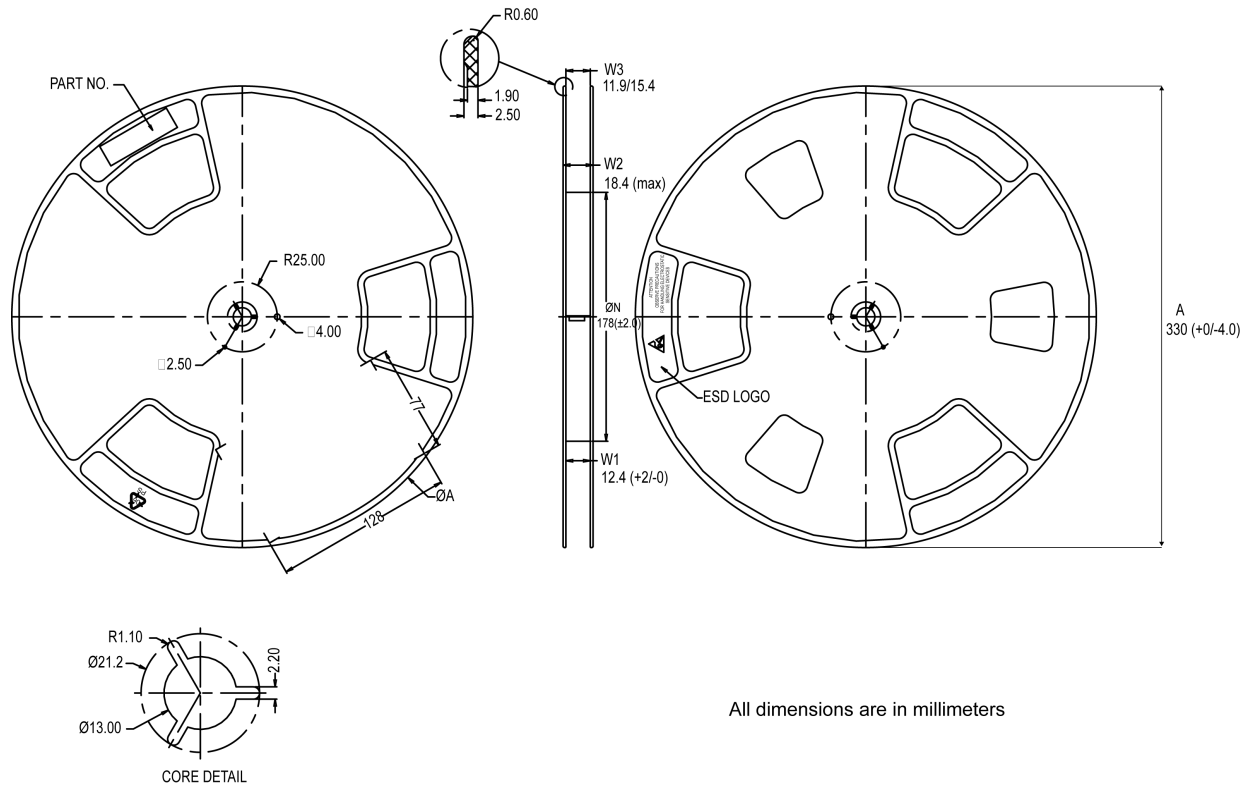
Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

8234350\_Tape\_rev\_C

Figure 19. PowerFLAT 5x6 package orientation in carrier tape



**Figure 20. PowerFLAT 5x6 reel**



All dimensions are in millimeters

8234350\_Reel\_rev\_C

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
04-Sep-2014	1	Initial release.
16-Dec-2014	2	Document status promoted from preliminary data to production data. Minor text changes.
24-Feb-2020	3	Updated <a href="#">Section 4 Package information</a> . Minor text changes.

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