- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
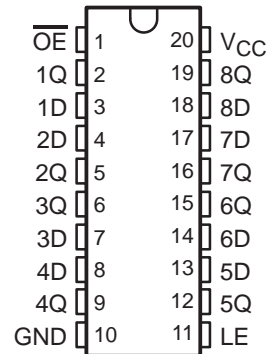 - 200-V Machine Model (A115-A)

SN54LVTH373 . . . J OR W PACKAGE
SN74LVTH373 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{OE}$	1	20 V_{CC}
1Q	2	19 8Q
1D	3	18 8D
2D	4	17 7D
2Q	5	16 7Q
3Q	6	15 6Q
3D	7	14 6D
4D	8	13 5D
4Q	9	12 5Q
GND	10	11 LE

SN54LVTH373 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1D, 1Q, $\overline{OE}$, V_{CC}, 8Q

2D 4	18 8D
2Q 5	17 7D
3Q 6	16 7Q
3D 7	15 6Q
4D 8	14 6D

Top numbers: 3 2 1 20 19
Bottom numbers: 9 10 11 12 13

Bottom pins: 4Q, GND, LE, 5Q, 5D

description/ordering information

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.
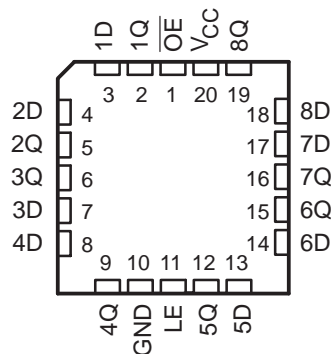
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – DW	Tube	SN74LVTH373DW	LVTH373
		Tape and reel	SN74LVTH373DWR	
	SOP – NS	Tape and reel	SN74LVTH373NSR	LVTH373
	SSOP – DB	Tape and reel	SN74LVTH373DBR	LXH373
	TSSOP – PW	Tube	SN74LVTH373PW	LXH373
		Tape and reel	SN74LVTH373PWR	
−55°C to 125°C	CDIP – J	Tube	SNJ54LVTH373J	SNJ54LVTH373J
	CFP – W	Tube	SNJ54LVTH373W	SNJ54LVTH373W
	LCCC - FK	Tube	SNJ54LVTH373FK	SNJ54LVTH373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)
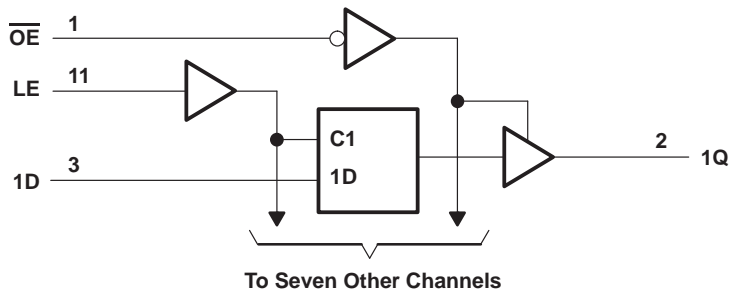
To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high-impedance
  or power-off state, V_O (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O: SN54LVTH373 .... 96 mA
                                          SN74LVTH373 .... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH373 .... 48 mA
                                                      SN74LVTH373 .... 64 mA
Input clamp current, I_{IK} (V_I < 0) .... –50 mA
Output clamp current, I_{OK} (V_O < 0) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package .... 70°C/W
                                            DW package .... 58°C/W
                                            NS package .... 60°C/W
                                            PW package .... 83°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and V_O > V_{CC}.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVTH373		SN74LVTH373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH373 MIN	TYP†	MAX	SN74LVTH373 MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 2.7$ V,	$I_I = -18$ mA			−1.2			−1.2	V
V_{OH}		$V_{CC} = 2.7$ V to 3.6 V,	$I_{OH} = -100$ µA	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7$ V,	$I_{OH} = -8$ mA	2.4			2.4			
		$V_{CC} = 3$ V	$I_{OH} = -24$ mA	2						
			$I_{OH} = -32$ mA				2			
V_{OL}		$V_{CC} = 2.7$ V	$I_{OL} = 100$ µA			0.2			0.2	V
			$I_{OL} = 24$ mA			0.5			0.5	
		$V_{CC} = 3$ V	$I_{OL} = 16$ mA			0.4			0.4	
			$I_{OL} = 32$ mA			0.5			0.5	
			$I_{OL} = 48$ mA			0.55				
			$I_{OL} = 64$ mA						0.55	
I_I		$V_{CC} = 0$ or 3.6 V,	$V_I = 5.5$ V			10			10	µA
	Control inputs	$V_{CC} = 3.6$ V,	$V_I = V_{CC}$ or GND			±1			±1	
	Data inputs	$V_{CC} = 3.6$ V	$V_I = V_{CC}$			1			1	
			$V_I = 0$			−5			−5	
I_{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V						±100	µA
$I_{I(hold)}$	Data inputs	$V_{CC} = 3$ V	$V_I = 0.8$ V	75			75			µA
			$V_I = 2$ V	−75			−75			
		$V_{CC} = 3.6$ V‡,	$V_I = 0$ to 3.6 V						500 −750	
I_{OZH}		$V_{CC} = 3.6$ V,	$V_O = 3$ V			5			5	µA
I_{OZL}		$V_{CC} = 3.6$ V,	$V_O = 0.5$ V			−5			−5	µA
I_{OZPU}		$V_{CC} = 0$ to 1.5 V, $V_O = 0.5$ V to 3 V, $\overline{OE}$ = don't care				±100*			±100	µA
I_{OZPD}		$V_{CC} = 1.5$ V to 0, $V_O = 0.5$ V to 3 V, $\overline{OE}$ = don't care				±100*			±100	µA
I_{CC}		$V_{CC} = 3.6$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}§		$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		$V_I = 3$ V or 0			3			3		pF
C_o		$V_O = 3$ V or 0			7			7		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°$C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH373				SN74LVTH373				UNIT
		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3		3		3		3		ns
t_{su}	Setup time, data before LE↓	1.1		0.4		1.1		0.4		ns
t_h	Hold time, data after LE↓	1.7		2		1.4		1.4		ns

switching characteristics over recommended free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH373				SN74LVTH373					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	D	Q	1.4	4.1		4.7	1.5	2.6	3.9		4.5	ns
t_{PHL}			1.4	4.1		4.7	1.5	2.6	3.9		4.5	
t_{PLH}	LE	Q	1.6	4.4		5.1	1.7	2.7	4.2		4.9	ns
t_{PHL}			1.6	4.4		5.1	1.7	2.7	4.2		4.9	
t_{PZH}	$\overline{OE}$	Q	1.2	5		6.1	1.3	3	4.8		5.9	ns
t_{PZL}			1.2	5		5.7	1.3	3	4.8		5.5	
t_{PHZ}	$\overline{OE}$	Q	1.6	5.5		5.7	1.9	3	4.6		4.9	ns
t_{PLZ}			0.8	4.8		4.9	1.9	3	4.5		4.6	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
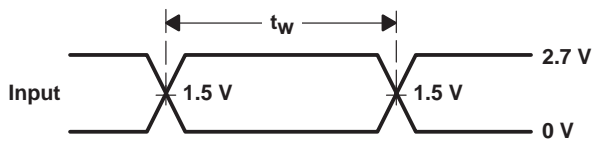
VOLTAGE WAVEFORMS
PULSE DURATION
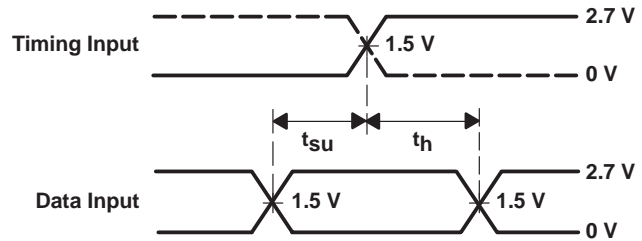
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
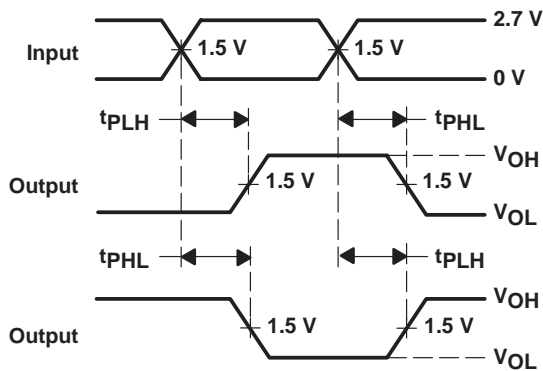
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
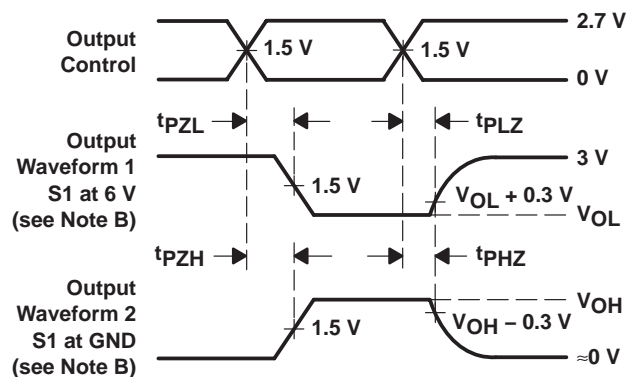
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9950901Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9950901Q2A SNJ54LVTH 373FK	Samples
5962-9950901QRA	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-9950901QRA SNJ54LVTH373J	Samples
5962-9950901QSA	ACTIVE	CFP	W	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-9950901QSA SNJ54LVTH373W	Samples
SN74LVTH373DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH373	Samples
SN74LVTH373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH373	Samples
SN74LVTH373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH373	Samples
SN74LVTH373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH373	Samples
SN74LVTH373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH373	Samples
SN74LVTH373PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH373	Samples
SN74LVTH373PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH373	Samples
SN74LVTH373PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH373	Samples
SN74LVTH373PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH373	Samples
SNJ54LVTH373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9950901Q2A SNJ54LVTH 373FK	Samples
SNJ54LVTH373J	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-9950901QRA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54LVTH373J	
SNJ54LVTH373W	ACTIVE	CFP	W	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-9950901QS A SNJ54LVTH373W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LVTH373, SN74LVTH373 :

• Catalog: SN74LVTH373

• Enhanced Product: SN74LVTH373-EP, SN74LVTH373-EP

• Military: SN54LVTH373

NOTE: Qualified Version Definitions:

    • Catalog - TI's standard catalog product

    • Enhanced Product - Supports Defense, Aerospace and Medical Applications

    • Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVTH373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVTH373NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVTH373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH373DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVTH373DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVTH373NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVTH373PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

J (R−GDIP−T**)

14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

20   11

4,50
4,30

6,60
6,20

Ⓓ

1   10

6,60
6,40

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

△ | 0,10
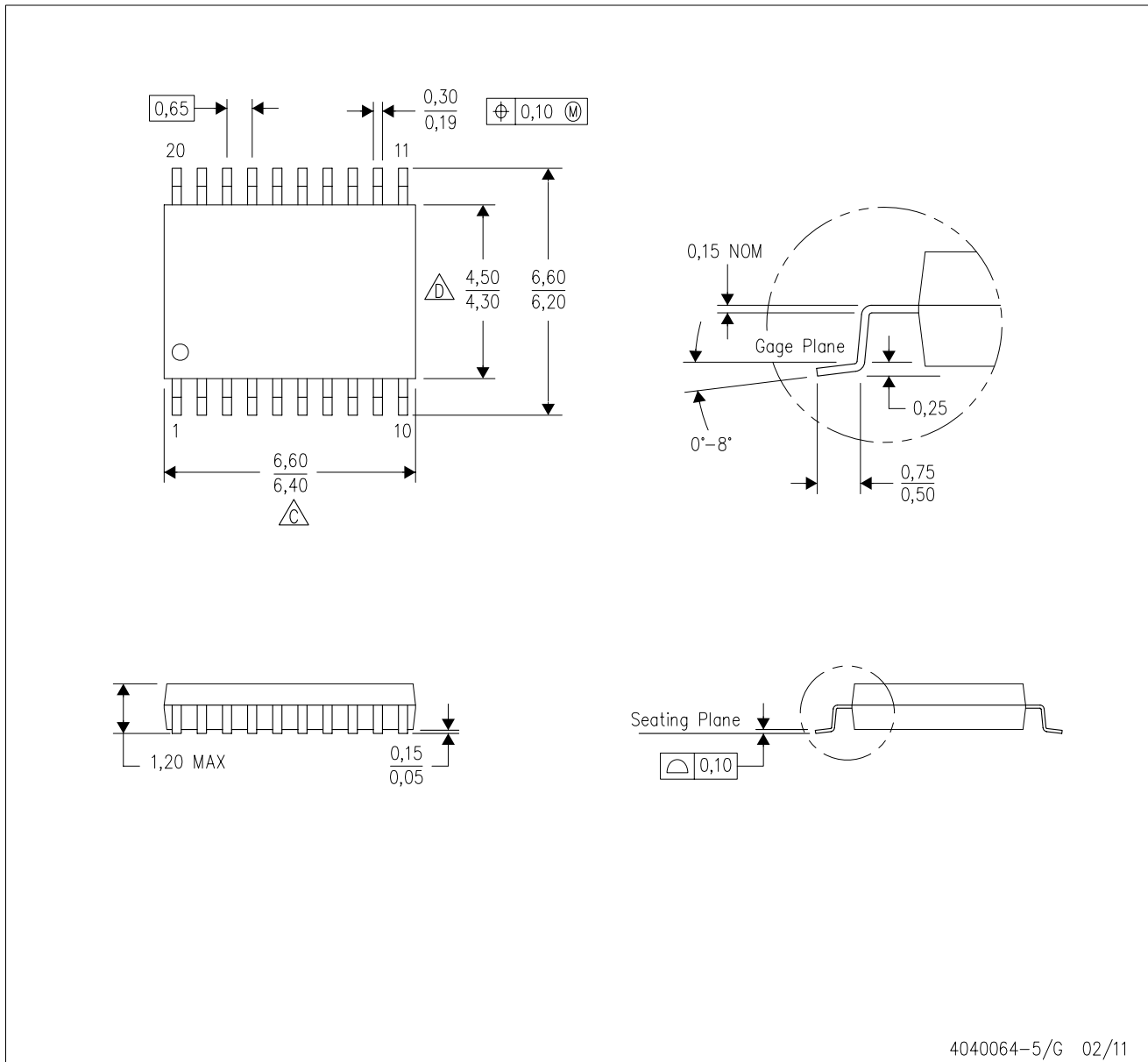
4040064−5/G 02/11

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
        Ⓒ   Body length does not include mold flash, protrusions, or gate burrs.   Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
        Ⓓ   Body width does not include interlead flash.   Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−5/G   08/15

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS INSTRUMENTS
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SEATING PLANE

C

0.1 C

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

18X 1.27

20

2X 11.43

13.0 / 12.6 NOTE 3

10

11

B

7.6 / 7.4 NOTE 4

20X 0.51 / 0.31

0.25 Ⓜ C A B

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

DW0020A

SOIC

20X (2)

1

SYMM

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

10

SYMM

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK

0.045 (1,14)
0.026 (0,66)

0.100 (2,45)
0.045 (1,14)

0.300 (7,62)
0.245 (6,22)

Base and Seating Plane

0.009 (0,23)
0.004 (0,10)

0.320 (8,13) MAX

1   20

0.022 (0,56)
0.015 (0,38)

0.050 (1,27)

0.540 (13,72) MAX

0.005 (0,13) MIN
4 Places

10   11

0.370 (9,40)
0.250 (6,35)

0.370 (9,40)
0.250 (6,35)

4040180−4/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within Mil−Std 1835 GDFP2−F20

FK (S−CQCC−N**)
28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS−004

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8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

18X 0.65

20

7.5
6.9
NOTE 3

2X
5.85

10

11

20X 0.38 / 0.22

⊕ 0.1 Ⓜ C A B

B

5.6
5.0
NOTE 4

C

◠ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95
0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL
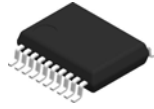
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

20X (1.85)

1

20X (0.45)

SYMM

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DB0020A

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM	PINS **	14	16	20	24
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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