SN74LVCR162245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES047E – AUGUST 1995 – REVISED MARCH 2005

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 2.7 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 8.5 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**

DGG OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	1$\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2$\overline{OE}$

DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.
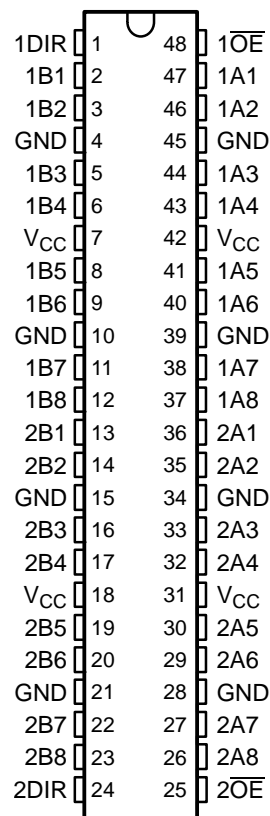
The SN74LVCR162245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses effectively are isolated.

All outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by $\overline{OE}$ or DIR.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74LVCR162245DL	LVCR162245
		Tape and reel	SN74LVCR162245DLR	
	TSSOP – DGG	Tape and reel	SN74LVCR162245DGGR	LVCR162245
	VFBGA – GQL	Tape and reel	SN74LVCR162245KR	LEP245
	VFBGA – ZQL (Pb-free)		74LVCR162245ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
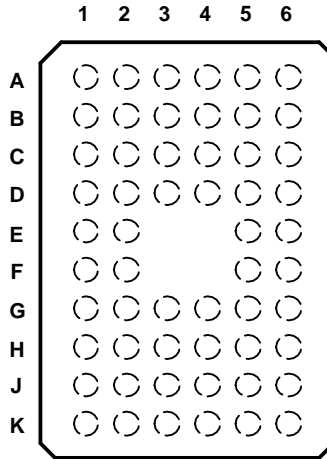
Widebus is a trademark of Texas Instruments.

TEXAS INSTRUMENTS
www.ti.com

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

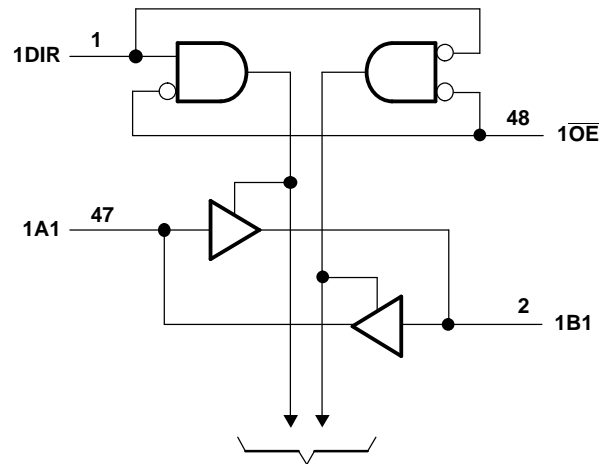**GQL OR ZQL PACKAGE**
(TOP VIEW)

TERMINAL ASSIGNMENTS[1]

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CC}	V_{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CC}	V_{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{OE}$

(1) NC - No internal connection

FUNCTION TABLE
(EACH 8-BIT SECTION)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

![Texas Instruments logo] TEXAS INSTRUMENTS
www.ti.com

SN74LVCR162245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES047E – AUGUST 1995 – REVISED MARCH 2005

LOGIC DIAGRAM (POSITIVE LOGIC)

To Seven Other Channels
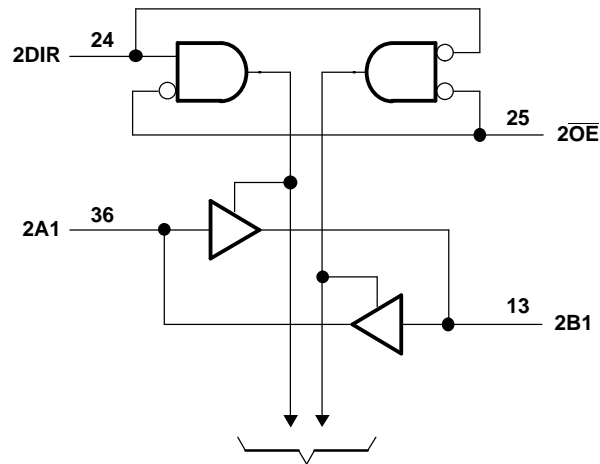
Pin numbers shown are for the DGG and DL packages.

SN74LVCR162245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES047E − AUGUST 1995 − REVISED MARCH 2005

TEXAS INSTRUMENTS
www.ti.com

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range	Except I/O ports[2]	−0.5	V_{CC} + 4.6	V
		I/O ports[2][3]	−0.5	V_{CC} + 0.5	
V_O	Output voltage range[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DGG package		70	°C/W
		DL package		63	
		GQL/ZQL package		42	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−8	mA
		V_{CC} = 3 V		−12	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		8	mA
		V_{CC} = 3 V		12	
$\Delta t/\Delta V$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}[1]	MIN	TYP[2]	MAX	UNIT
V_{OH}		$I_{OH} = -100$ µA		MIN to MAX	$V_{CC} - 0.2$			V
		$I_{OH} = -4$ mA,	$V_{IH} = 2$ V	2.7 V	2.2			
		$I_{OH} = -8$ mA,	$V_{IH} = 2$ V		2			
		$I_{OH} = -6$ mA,	$V_{IH} = 2$ V	3 V	2.4			
		$I_{OH} = -12$ mA,	$V_{IH} = 2$ V		2			
V_{OL}		$I_{OL} = 100$ µA		MIN to MAX			0.2	V
		$I_{OL} = 4$ mA,	$V_{IL} = 0.8$ V	2.7 V			0.4	
		$I_{OL} = 8$ mA,	$V_{IL} = 0.8$ V				0.6	
		$I_{OL} = 6$ mA,	$V_{IL} = 0.8$ V	3 V			0.55	
		$I_{OL} = 12$ mA,	$V_{IL} = 0.8$ V				0.8	
I_I		$V_I = V_{CC}$ or GND		3.6 V			±5	µA
$I_{I(hold)}$		$V_I = 0.8$ V		3 V	75			µA
		$V_I = 2$ V			-75			
		$V_I = 0$ to 3.6 V		3.6 V			±500	µA
I_{OZ}[3]		$V_O = 0$ V or (V_{CC} to 5.5 V)		3.6 V			±10	µA
I_{CC}		$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			20	µA
		3.6 V $\leq V_I \leq 5.5$ V [4]					20	
ΔI_{CC}		One input at $V_{CC} - 0.6$ V,	Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		2.5		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		3.5		pF

(1) For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
(2) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
(3) For the total leakage current in an I/O port, please consult the $I_{I(hold)}$ specification for the input voltage condition 0 V $< V_I < V_{CC}$, and the I_{OZ} specification for the input voltage conditions $V_I = 0$ V or $V_I = V_{CC}$ to 5.5 V. The bus-hold current, at input voltage greater than V_{CC}, is negligible.
(4) This applies in the disabled state only.

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)
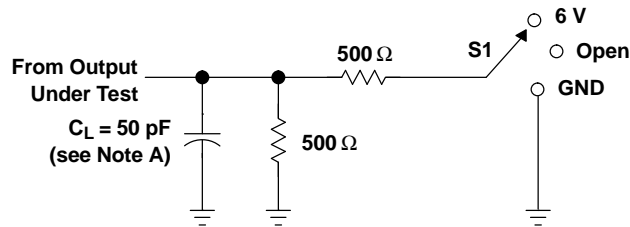
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3$ V ± 0.3 V		$V_{CC} = 2.7$ V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1.5	7.5	1.5	8.5	ns
t_{en}	$\overline{OE}$	A or B	1.5	9	1.5	10	ns
t_{dis}	$\overline{OE}$	A or B	1.5	7.5	1.5	8.5	ns

Operating Characteristics

$V_{CC} = 3.3$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50$ pF, $f = 10$ MHz	20	pF
	Outputs disabled		2	

SN74LVCR162245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES047E – AUGUST 1995 – REVISED MARCH 2005

TEXAS INSTRUMENTS
www.ti.com

PARAMETER MEASUREMENT INFORMATION

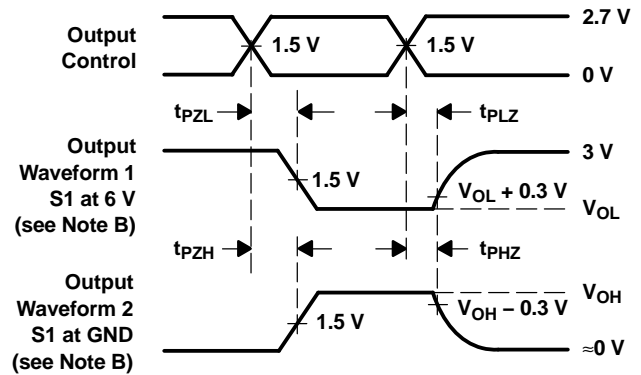| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR OUTPUTS
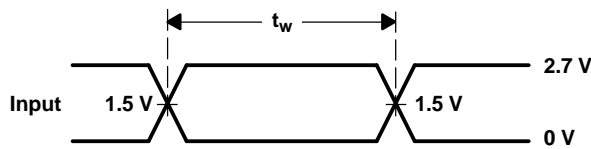
**VOLTAGE WAVEFORMS
PULSE DURATION**
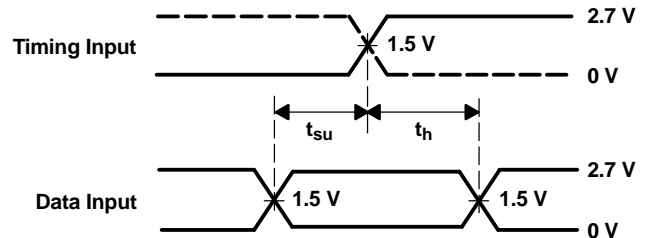
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
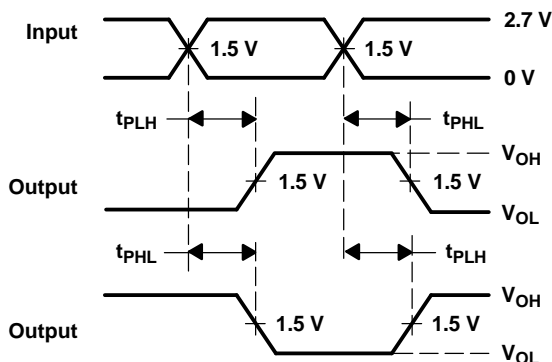
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
     B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
     C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
     D. The outputs are measured one at a time, with one transition per measurement.
     E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
     F. t_{PZL} and t_{PZH} are the same as t_{en}.
     G. t_{PLH} and t_{PHL} are the same as t_{pd}.
     H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVCR162245ZQLR	NRND	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LEP245	
SN74LVCR162245DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR162245	Samples
SN74LVCR162245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR162245	Samples
SN74LVCR162245DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR162245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVCR162245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74LVCR162245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVCR162245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVCR162245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	350.0	350.0	43.0
SN74LVCR162245DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVCR162245DLR	SSOP	DL	48	1000	367.0	367.0	55.0

DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

$\frac{0.0135\ (0,343)}{0.008\ (0,203)}$ ⊕ 0.005 (0,13) Ⓜ

48   25

$\frac{0.420\ (10,67)}{0.395\ (10,03)}$

$\frac{0.299\ (7,59)}{0.291\ (7,39)}$

1   24

$\frac{0.630\ (16,00)}{0.620\ (15,75)}$

$\frac{0.010\ (0,25)}{0.005\ (0,13)}$

Gage Plane

0°−8°

0.010 (0,25)

$\frac{0.040\ (1,02)}{0.020\ (0,51)}$

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−3/F   05/13
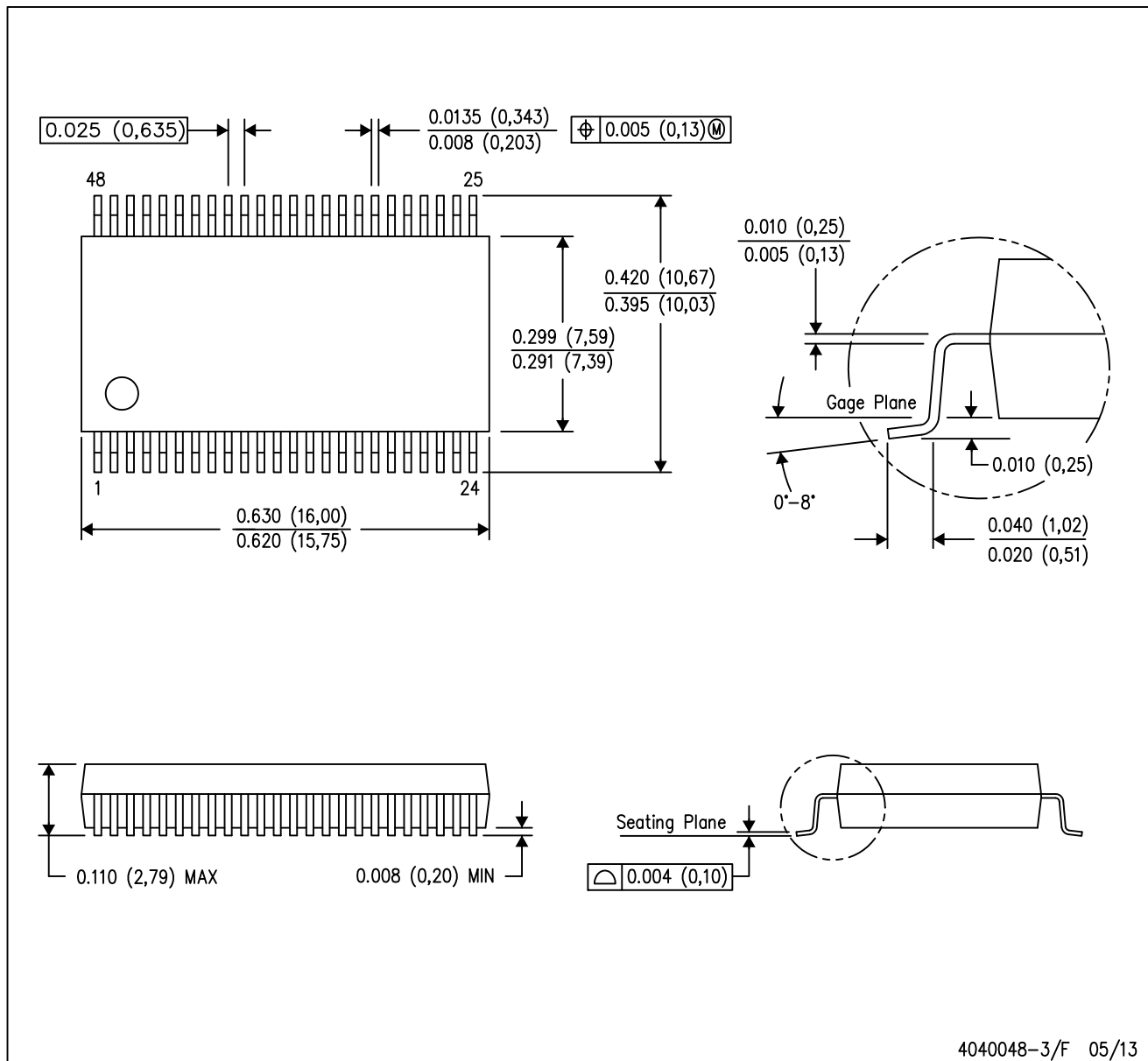
NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

PowerPAD is a trademark of Texas Instruments.

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97
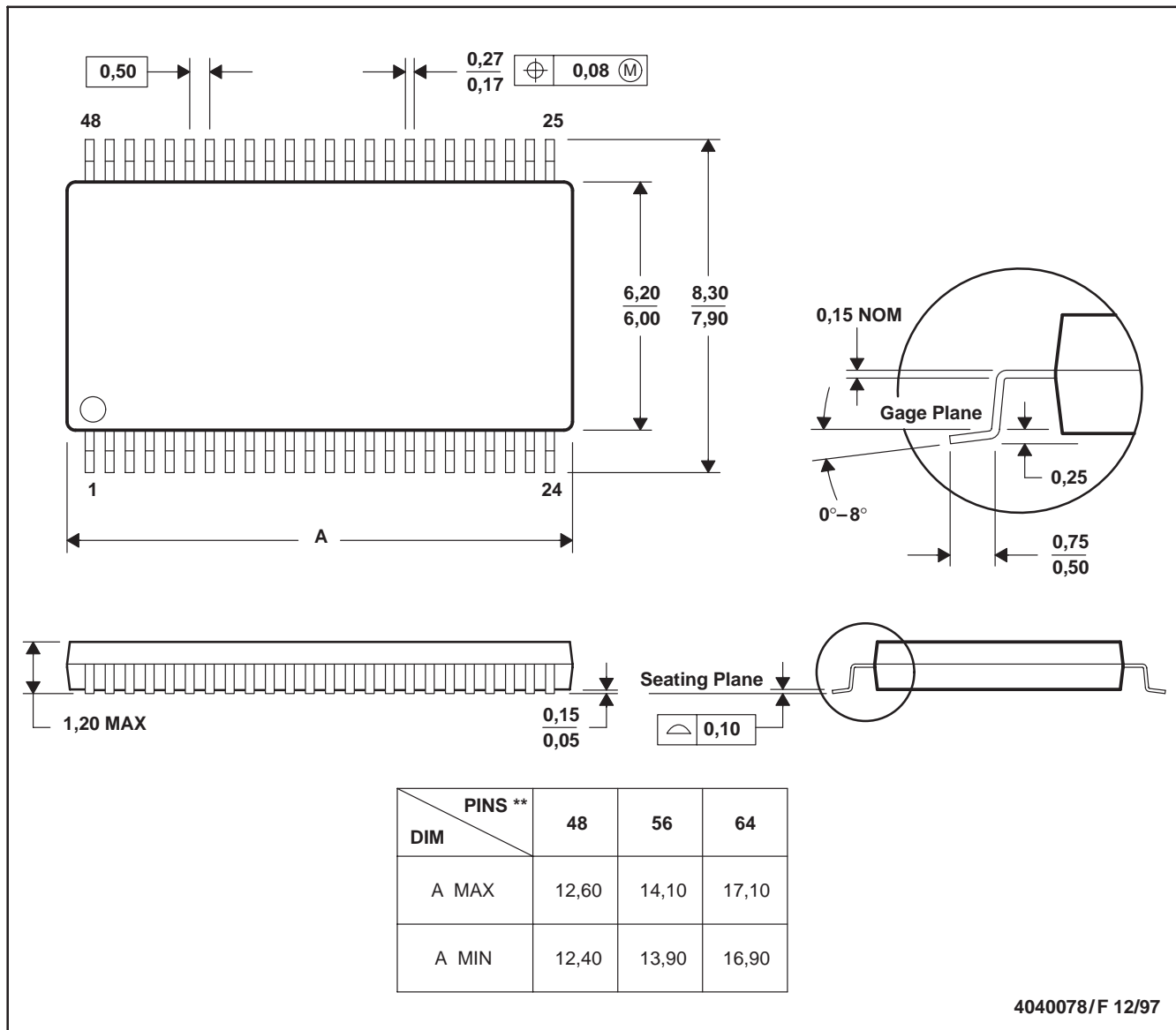
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

B ← 4.6 / 4.4 → A

BALL A1 CORNER

7.1 / 6.9

1 MAX

C

SEATING PLANE

0.35 / 0.15 TYP

BALL TYP

⌒ 0.1 C

3.25 TYP

SYMM ₵

(0.625) TYP

(0.575) TYP

K
J
H
G
F
E
D
C
B
A

1 2 3 4 5 6

5.85 TYP

SYMM ₵

NOTE 3

56X ⌀ 0.45 / 0.35

⊕ | ⌀ 0.15 Ⓜ | C | B | A
⊕ | ⌀ 0.08 Ⓜ | C |

0.65 TYP

BALL A1 CORNER

0.65 TYP
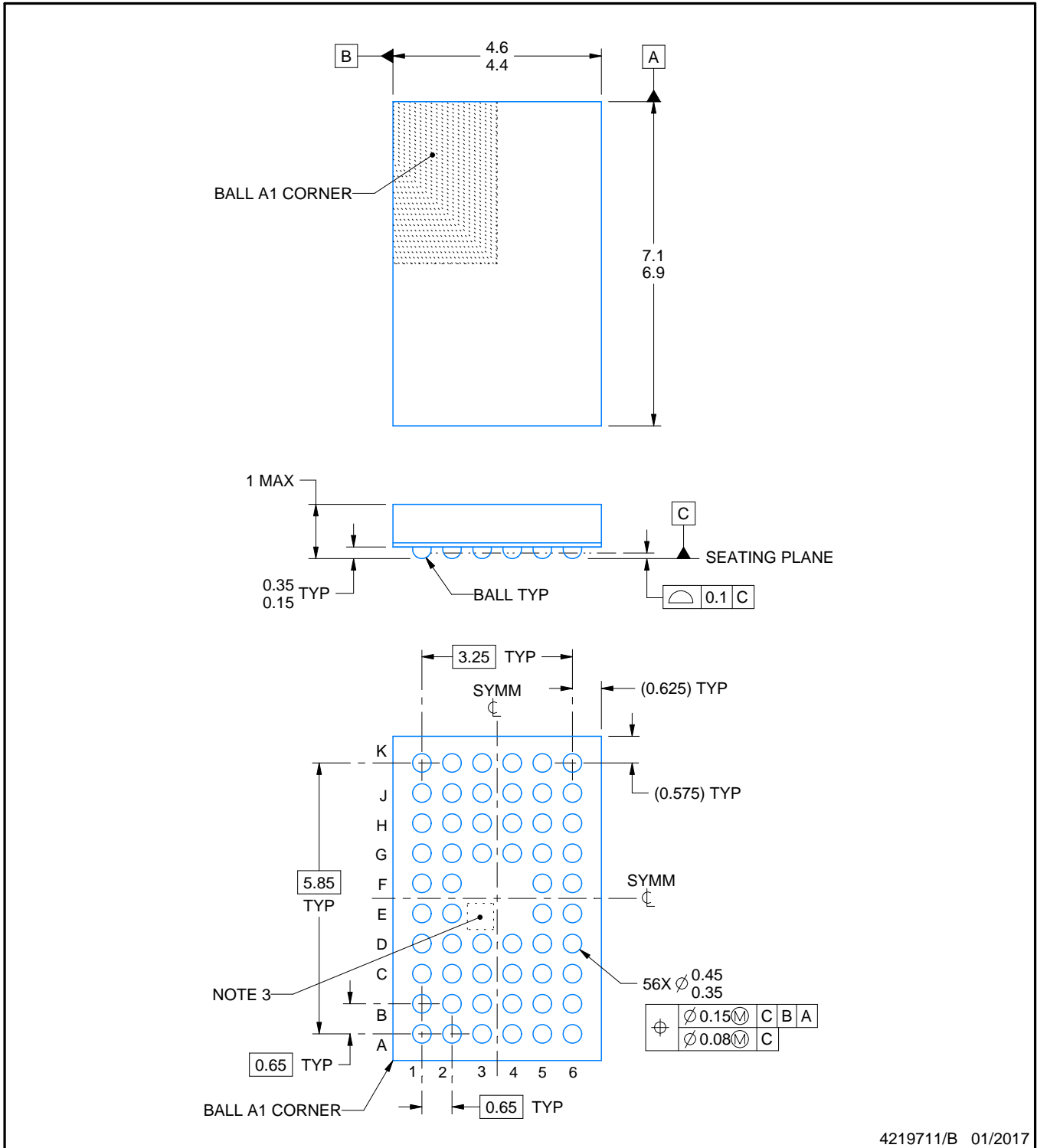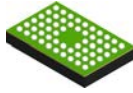
4219711/B   01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.

ZQL0056A

56X (∅ 0.33)

(0.65) TYP

(0.65) TYP

1 2 3 4 5 6

A B C D E F G H J K

SYMM ℄

SYMM ℄
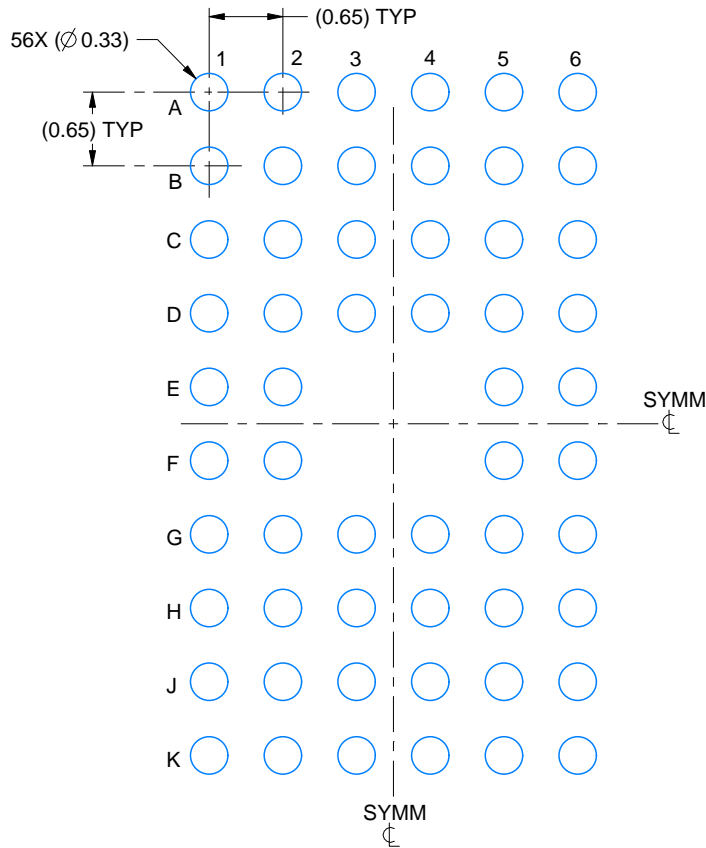
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

0.05 MAX

EXPOSED METAL

(∅ 0.33)
METAL

**NON-SOLDER MASK
DEFINED
(PREFERRED)**

0.05 MIN

METAL UNDER
SOLDER MASK

EXPOSED METAL

(∅ 0.33)
SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**
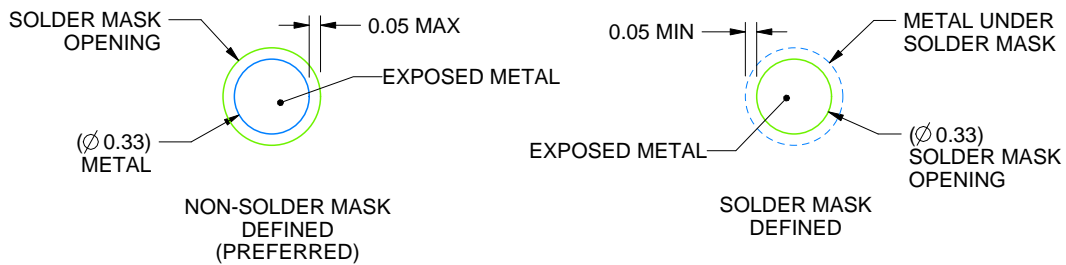
SOLDER MASK DETAILS
NOT TO SCALE

4219711/B   01/2017

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

ZQL0056A

PLASTIC BALL GRID ARRAY
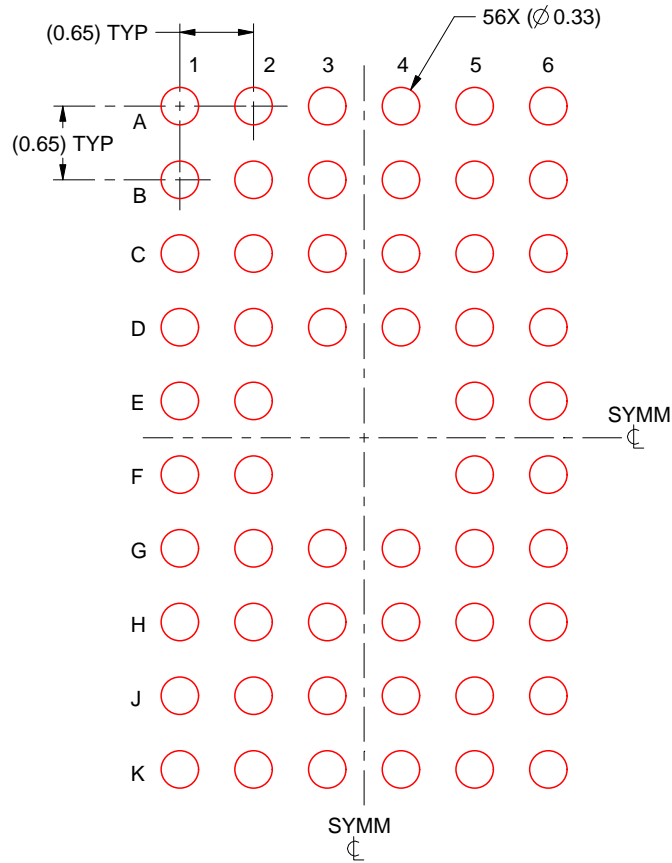
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4219711/B 01/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.