SNx4LVC74A Dual Positive-Edge-Triggered D-Type Flip-Flops With Clear and Preset

1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Maximum t_{pd} of 5.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Medical, Healthcare, and Fitness
- Telecom Infrastructures
- TVs, Set-Top Boxes, and Audio
- Test and Measurement
- Industrial Transport
- Wireless Infrastructure
- Enterprise Switching
- Motor Drives
- Factory Automation and Control

3 Description

The SNx4LVC74A devices integrate two positive-edge triggered D-type flip-flops in one convenient device.

The SN54LVC74A is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC74A is designed for 1.65-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

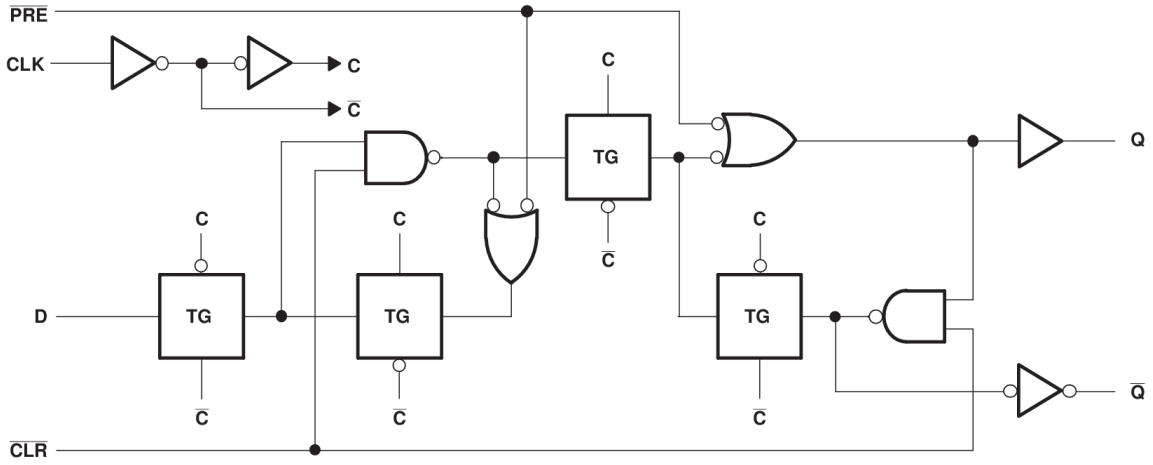
The data I/Os and control inputs are overvoltage tolerant. This feature allows the use of these devices for down-translation in a mixed-voltage environment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNJ54LVC74AFK	LCCC (20)	8.89 mm × 8.89 mm
SNJ54LVC74AJ	CDIP (14)	19.56 mm × 6.67 mm
SNJ54LVC74AW	CFP (14)	9.21 mm × 5.97 mm
SN74LVC74AD	SOIC (14)	8.65 mm × 3.91 mm
SN74LVC74ADB	SSOP (14)	6.20 mm × 5.30 mm
SN74LVC74ANS	SO (14)	10.30 mm × 5.30 mm
SN74LVC74APW	TSSOP (14)	5.00 mm × 4.40 mm
SN74LVC74ARGY	VQFN (14)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Flip-Flop (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision T (July 2013) to Revision U — **Page**

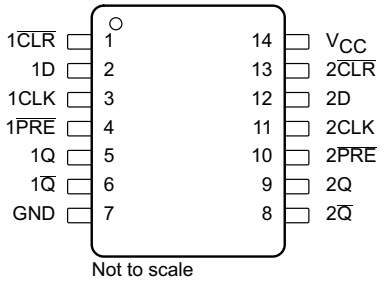
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Package thermal impedance, $R_{\theta JA}$, values in *Thermal Information: SN74LVC74A* From: 86 To: 93.7 (D), From: 96 To: 107.3 (DB), From: 76 To: 90.3 (NS), From: 113 To: 121.7 (PW), and From: 47 To: 54.9 (RGY) ... 5

Changes from Revision S (May 2005) to Revision T — **Page**

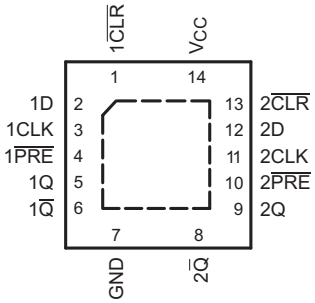
- Extended maximum temperature operating range from 85°C to 125°C ... 4

5 Pin Configuration and Functions

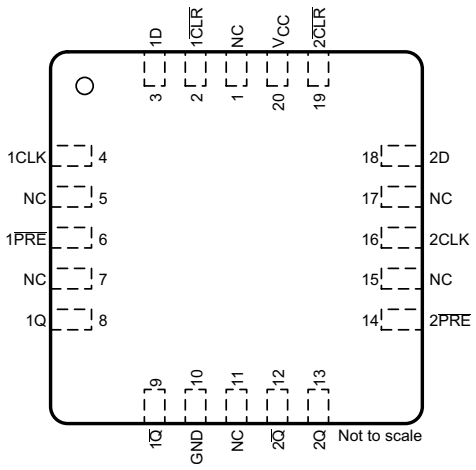
D, DB, J, PW, NS, or W Package
14-Pin SOIC, SSOP, CDIP, TSSOP, SO, or CFP
Top View



RGY Package
14-Pin VQFN With Exposed Thermal Pad
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, CFP, PDIP, SO, SOIC, SSOP, TSSOP, VQFN	LCCC		
1CLK	3	4	I	Channel 1 clock input
1$\overline{CLR}$	1	2	I	Channel 1 clear input. Pull low to set Q output low.
1D	2	3	I	Channel 1 data input
1$\overline{PRE}$	4	6	I	Channel 1 preset input. Pull low to set Q output high.
1Q	5	8	O	Channel 1 output
1$\overline{Q}$	6	9	O	Channel 1 inverted output
2CLK	11	16	I	Channel 2 clock input
2$\overline{CLR}$	13	19	I	Channel 2 clear input. Pull low to set Q output low.
2D	12	18	I	Channel 2 data input
2$\overline{PRE}$	10	14	I	Channel 2 preset input. Pull low to set Q output high.
2Q	9	13	O	Channel 2 output
2$\overline{Q}$	8	12	O	Channel 2 Inverted output
GND	7	10	—	Ground
NC	—	1, 5, 7, 11, 15, 17	—	No connect
V_{CC}	14	20	—	Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	6.5	V
Input voltage, V_I(2)		–0.5	6.5	V
Output voltage, V_O(2)(3)		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	V_I < 0		–50	mA
Output clamp current, I_{OK}	V_O < 0		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see(1)

				MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	SN54LVC74A	2	3.6	V
			SN74LVC74A	1.65	3.6	
		Data retention only		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	SN74LVC74A	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	SN74LVC74A	1.7		
		V_{CC} = 2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V	SN74LVC74A		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	SN74LVC74A		0.7	
		V_{CC} = 2.7 V to 3.6 V			0.8	
V_I	Input voltage			0	5.5	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V	SN74LVC74A		–4	mA
		V_{CC} = 2.3 V	SN74LVC74A		–8	
		V_{CC} = 2.7 V			–12	
		V_{CC} = 3 V			–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V	SN74LVC74A		4	mA
		V_{CC} = 2.3 V	SN74LVC74A		8	
		V_{CC} = 2.7 V			12	
		V_{CC} = 3 V			24	
Δt/Δv	Input transition rise or fall rate				10	ns/V

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Recommended Operating Conditions (continued)

see[1]

			MIN	MAX	UNIT
T_A	Operating free-air temperature	SN54LVC74A	–55	125	°C
		SN74LVC74A	–40	125	

6.4 Thermal Information: SN74LVC74A

THERMAL METRIC[1]		SN74LVC74A					UNIT
		D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.7	107.3	90.3	121.7	54.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.8	59.2	48.1	50.3	52.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	54.6	49.1	63.4	30.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.3	24.1	17.9	6.2	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.7	54.1	48.8	62.8	30.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	12.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA	V_{CC} = 1.65 V to 3.6 V and T_A = –55°C to 125°C (SN54LVC74A only)	V_{CC} – 0.2			V
			V_{CC} = 2.7 V to 3.6 V and T_A = –40°C to 125°C (SN74LVC74A only)	V_{CC} – 0.2			
		I_{OH} = –4 mA, V_{CC} = 1.65 V, and T_A = –40°C to 125°C (SN74LVC74A only)		1.2			
		I_{OH} = –8 mA, V_{CC} = 2.3 V, and T_A = –40°C to 125°C (SN74LVC74A only)		1.7			
		I_{OH} = –12 mA	V_{CC} = 2.7 V	2.2			
			V_{CC} = 3 V	2.4			
		I_{OH} = –24 mA, V_{CC} = 3 V		2.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA	V_{CC} = 1.65 V to 3.6 V, and T_A = –40°C to 125°C (SN74LVC74A only)			0.2	V
			V_{CC} = 2.7 V to 3.6 V and T_A = –55°C to 125°C (SN54LVC74A only)			0.2	
		I_{OL} = 4 mA, V_{CC} = 1.65 V, and T_A = –40°C to 125°C (SN74LVC74A only)				0.45	
		I_{OL} = 8 mA, V_{CC} = 2.3 V, and T_A = –40°C to 125°C (SN74LVC74A only)				0.7	
		I_{OL} = 12 mA, V_{CC} = 2.7 V				0.4	
		I_{OL} = 24 mA, V_{CC} = 3 V				0.55	
I_I	Input current	V_I = 5.5 V or GND, V_{CC} = 3.6 V				±5	µA
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0, V_{CC} = 3.6 V				10	µA
ΔI_{CC}	Change in supply current	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND, and V_{CC} = 2.7 V to 3.6 V				500	µA
C_i	Input capacitance	V_I = V_{CC} or GND, V_{CC} = 3.3 V, T_A = 25°C			5		pF

6.6 Timing Requirements: SN54LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Figure 3)

				MIN	MAX	UNIT
f_{clock}	Clock frequency	V_{CC} = 2.7 V			83	MHz
		V_{CC} = 3.3 V ± 0.3 V			100	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low		3.3		ns
		CLK high or low		3.3		
t_{su}	Setup time before CLK↑	Data	V_{CC} = 2.7 V	3.4		ns
			V_{CC} = 3.3 V ± 0.3 V	3		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	V_{CC} = 2.7 V	2.2		
			V_{CC} = 3.3 V ± 0.3 V	2		
t_h	Hold time, data after CLK↑			1		ns

6.7 Timing Requirements: SN74LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Figure 3)

				MIN	MAX	UNIT
f_{clock}	Clock frequency	V_{CC} = 1.8 V or 2.5 V			83	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	V_{CC} = 1.8 V ± 0.15 V	4.1		ns
			V_{CC} = 2.5 V ± 0.2 V	3.3		
		CLK high or low	V_{CC} = 1.8 V ± 0.15 V	4.1		
			V_{CC} = 2.5 V ± 0.2 V	3.3		
t_{su}	Setup time before CLK↑	Data	V_{CC} = 1.8 V ± 0.15 V	3.6		ns
			V_{CC} = 2.5 V ± 0.2 V	2.3		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	V_{CC} = 1.8 V ± 0.15 V	2.7		
			V_{CC} = 2.5 V ± 0.2 V	1.9		
t_h	Hold time, data after CLK↑	V_{CC} = 1.8 V or 2.5 V		1		ns

6.8 Timing Requirements: SN74LVC74A, –40°C to 125°C and –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted; see Figure 3)

					MIN	MAX	UNIT
f_{clock}	Clock frequency	T_A = –40°C to 125°C	V_{CC} = 2.7 V			83	MHz
			V_{CC} = 3.3 V ± 0.3 V			100	
		T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V				150	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	V_{CC} = 2.7 V or 3.3 V		3.3		ns
		CLK high or low	V_{CC} = 2.7 V or 3.3 V		3.3		
t_{su}	Setup time before CLK↑	Data	T_A = –40°C to 125°C	V_{CC} = 2.7 V	3.4		ns
				V_{CC} = 3.3 V ± 0.3 V	3		
			T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		3		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	T_A = –40°C to 125°C	V_{CC} = 2.7 V	2.2		
				V_{CC} = 3.3 V ± 0.3 V	2		
			T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		2		
t_h	Hold time, data after CLK↑	V_{CC} = 2.7 V or 3.3 V			1		ns

6.9 Switching Characteristics: SN54LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Figure 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}	Maximum clock frequency	—	—	V_{CC} = 2.7 V	83		MHz
				V_{CC} = 3.3 V ± 0.3 V	100		
t_{pd}	Propagation (delay) time	CLK	Q or $\overline{Q}$	V_{CC} = 2.7 V		6	ns
				V_{CC} = 2.7 V	1	5.2	
		$\overline{PRE}$ or $\overline{CLR}$		V_{CC} = 3.3 V ± 0.3 V		6.4	
				V_{CC} = 3.3 V ± 0.3 V	1	5.4	

6.10 Switching Characteristics: SN74LVC74A

over recommended operating free-air temperature range (unless otherwise noted; see Figure 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}	Maximum clock frequency	—	—		83		MHz
t_{pd}	Propagation (delay) time	CLK$\overline{PRE}$	Q or $\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	1	7.1	ns
				V_{CC} = 2.5 V ± 0.2 V	1	4.4	
		or $\overline{CLR}$		V_{CC} = 1.8 V ± 0.15 V	1	6.9	
				V_{CC} = 2.5 V ± 0.2 V	1	4.6	

6.11 Switching Characteristics: SN74LVC74A, –40°C to 125°C and –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted; see Figure 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
f_{max}	Maximum clock frequency	—	—	T_A = –40°C to 125°C	V_{CC} = 2.7 V	83		MHz
					V_{CC} = 3.3 V ± 0.3 V	100		
				T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		150		
t_{pd}	Propagation (delay) time	CLK	Q or $\overline{Q}$	T_A = –40°C to 125°C	V_{CC} = 2.7 V	1	6	ns
					V_{CC} = 3.3 V ± 0.3 V		5.2	
				T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		1	5.2	
		$\overline{PRE}$ or $\overline{CLR}$		T_A = –40°C to 125°C	V_{CC} = 2.7 V	1	6.4	
					V_{CC} = 3.3 V ± 0.3 V		5.4	
				T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V		1	5.4	
$t_{sk(o)}$	Skew (time), output	—	—	T_A = –40°C to 85°C and V_{CC} = 3.3 V ± 0.3 V			1	ns

6.12 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	f = 10 MHz	V_{CC} = 1.8 V	24	pF
			V_{CC} = 2.5 V	24	
			V_{CC} = 3.3 V	26	

6.13 Typical Characteristics

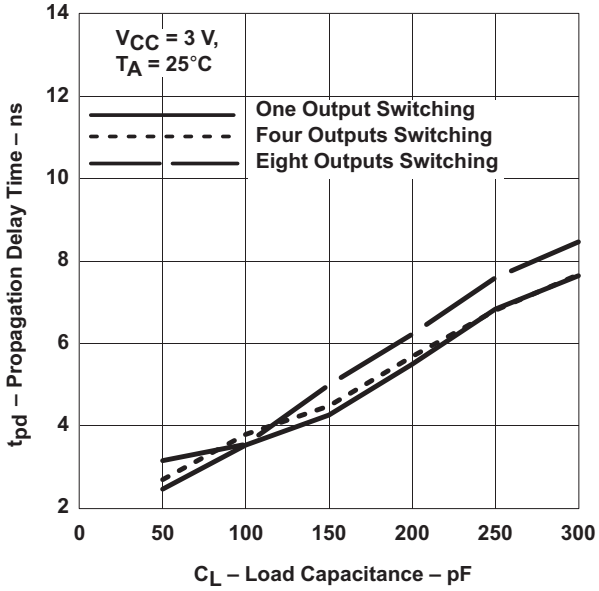


Figure 1. Propagation Delay (Low-to-High Transition) vs Load Capacitance

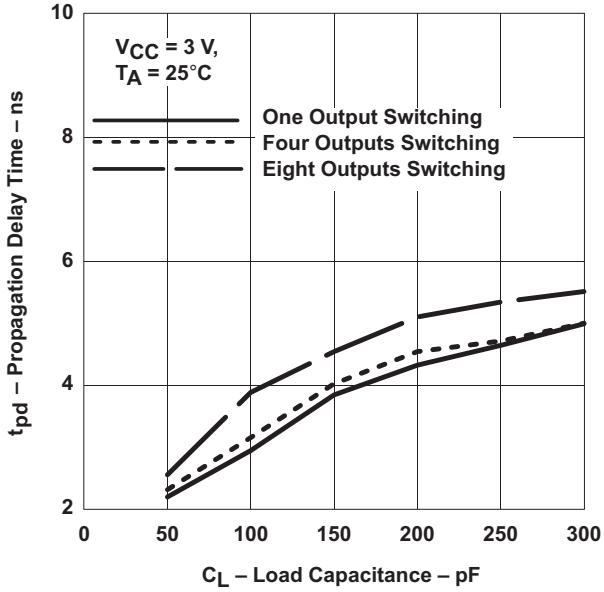
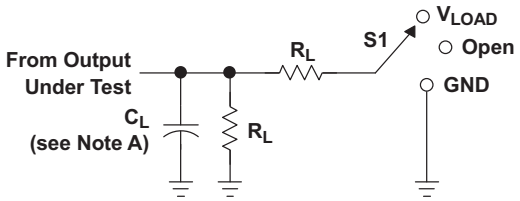


Figure 2. Figure 2. Propagation Delay (High-to-Low Transition) vs Load Capacitance

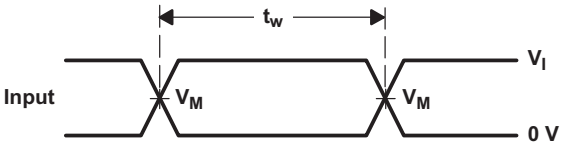
7 Parameter Measurement Information



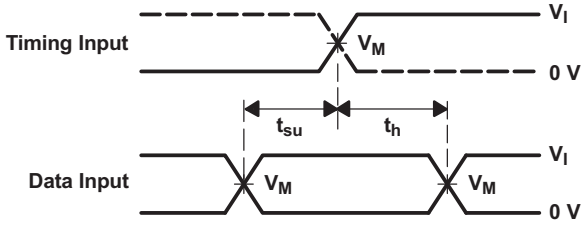
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

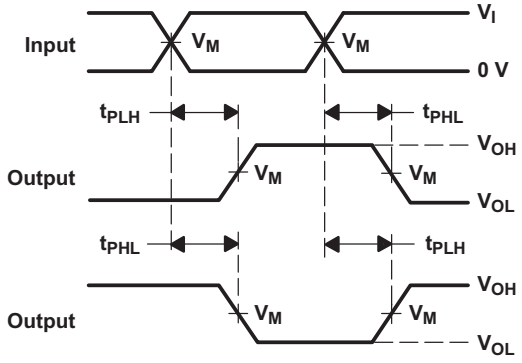
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



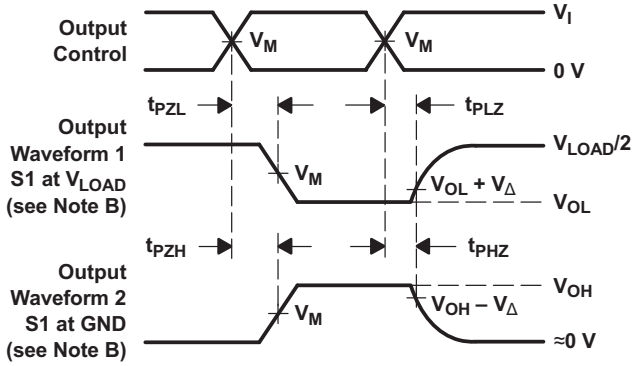
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

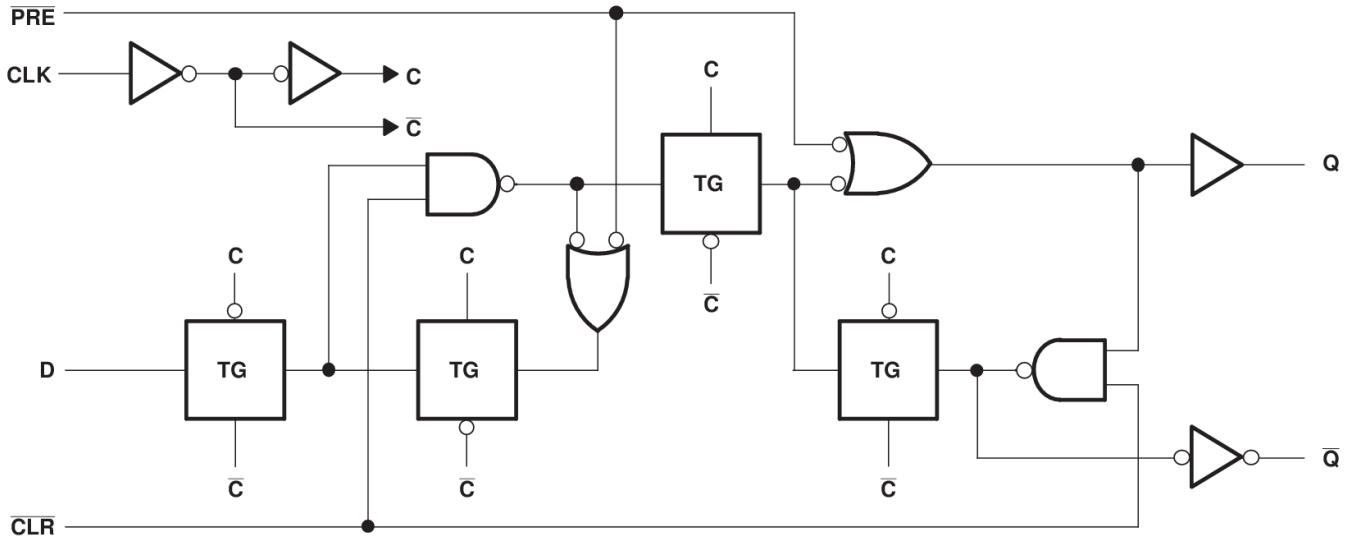
8 Detailed Description

8.1 Overview

The SNx4LVC74A devices feature two independent positive-edge triggered D flip-flops. Integrated preset ($\overline{PRE}$) and clear ($\overline{CLR}$) functions allow for easy setup and control during operation.

The SN54LVC74A device is specified from –55°C to 125°C, and the SN74LVC74A device is specified from –40°C to 125°C.

8.2 Functional Block Diagram



8.3 Feature Description

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

8.4 Device Functional Modes

Table 1 describes the SNx4LVC74A functionality and interactions between the $\overline{PRE}$, $\overline{CLR}$, CLK, and D inputs.

Table 1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A common application for the SN74LVC74A is a frequency divider. By connecting the $\overline{Q}$ output to the D input, the Q output toggles states on each positive edge of the incoming clock signal. Because it takes two positive edges, or two clock pulses, to complete one complete pulse on the output (one pulse to toggle from low to high, another to toggle from high to low), the incoming clock frequency is effectively divided by two.

9.2 Typical Application

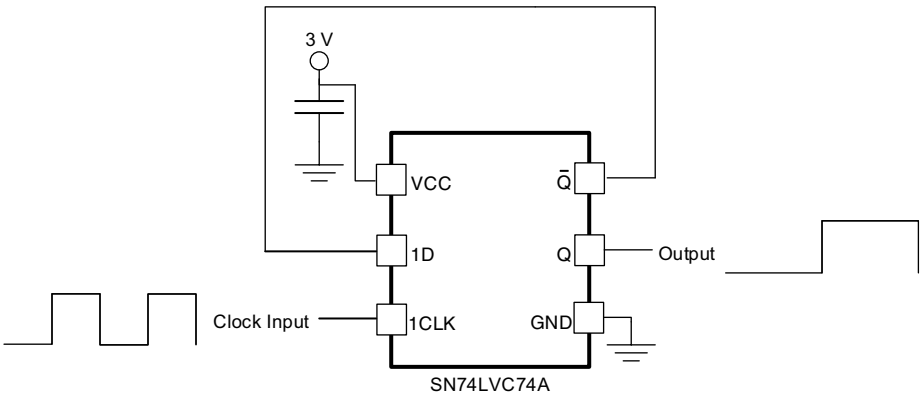


Figure 4. Frequency Divider

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specification, see ($\Delta t/\Delta V$) in *Recommended Operating Conditions*.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in *Recommended Operating Conditions* at any valid V_{CC}.
2. Recommended maximum output conditions:
   - Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
   - Outputs must not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curves

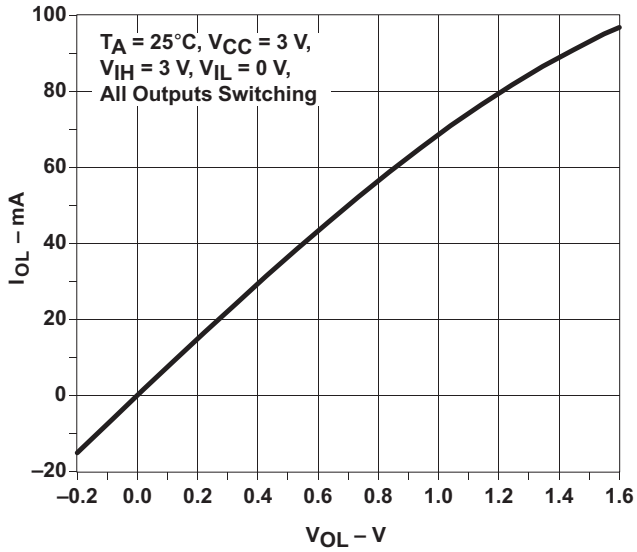


Figure 5. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

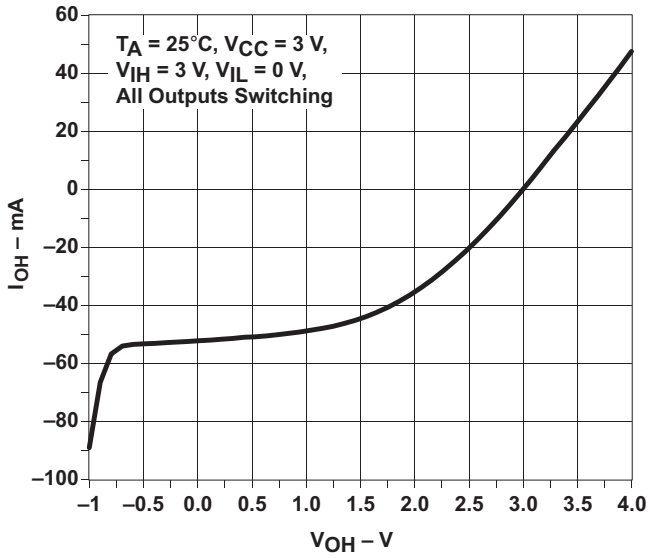


Figure 6. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

10 Power Supply Recommendations

The power supply may be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01-µF or 0.022-µF capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

Inputs must not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC}, whichever makes more sense or is more convenient.

11.2 Layout Example

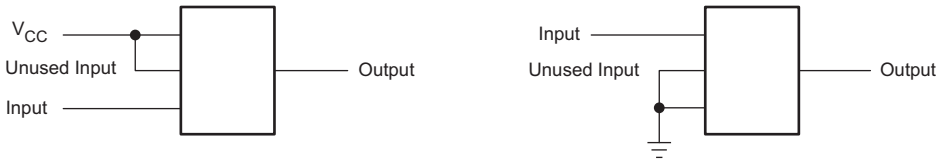


Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC74A	Click here	Click here	Click here	Click here	Click here
SN74LVC74A	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9761601Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9761601Q2A SNJ54LVC 74AFK	Samples
5962-9761601QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9761601QC A SNJ54LVC74AJ	Samples
5962-9761601QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9761601QD A SNJ54LVC74AW	Samples
5962-9761601VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9761601VD A SNV54LVC74AW	Samples
SN74LVC74AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 125		
SN74LVC74ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC74ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
SN74LVC74APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74ARGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A	Samples
SN74LVC74ARGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A	Samples
SNJ54LVC74AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9761601Q2A SNJ54LVC 74AFK	Samples
SNJ54LVC74AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9761601QC A SNJ54LVC74AJ	Samples
SNJ54LVC74AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9761601QD A SNJ54LVC74AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54LVC74A, SN54LVC74A-SP, SN74LVC74A :

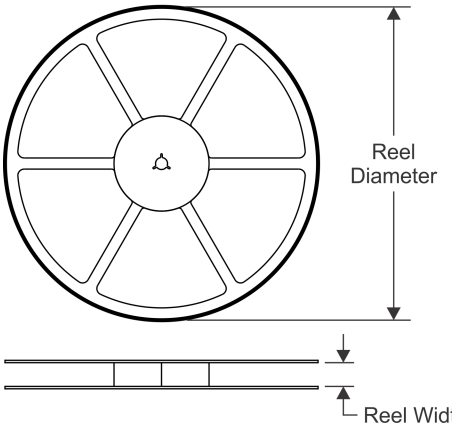
- Catalog: SN74LVC74A, SN54LVC74A
- Automotive: SN74LVC74A-Q1, SN74LVC74A-Q1
- Enhanced Product: SN74LVC74A-EP, SN74LVC74A-EP
- Military: SN54LVC74A
- Space: SN54LVC74A-SP

NOTE: Qualified Version Definitions:

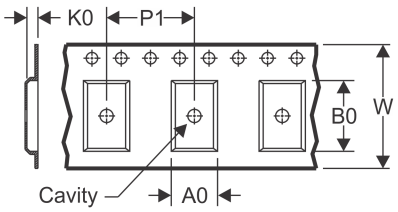
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

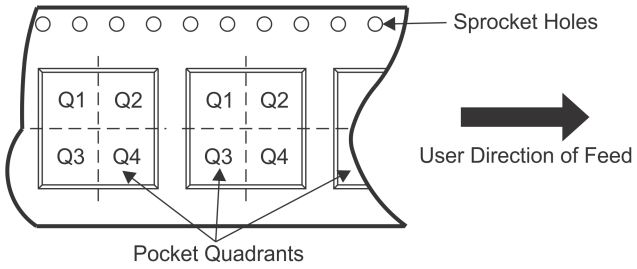


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

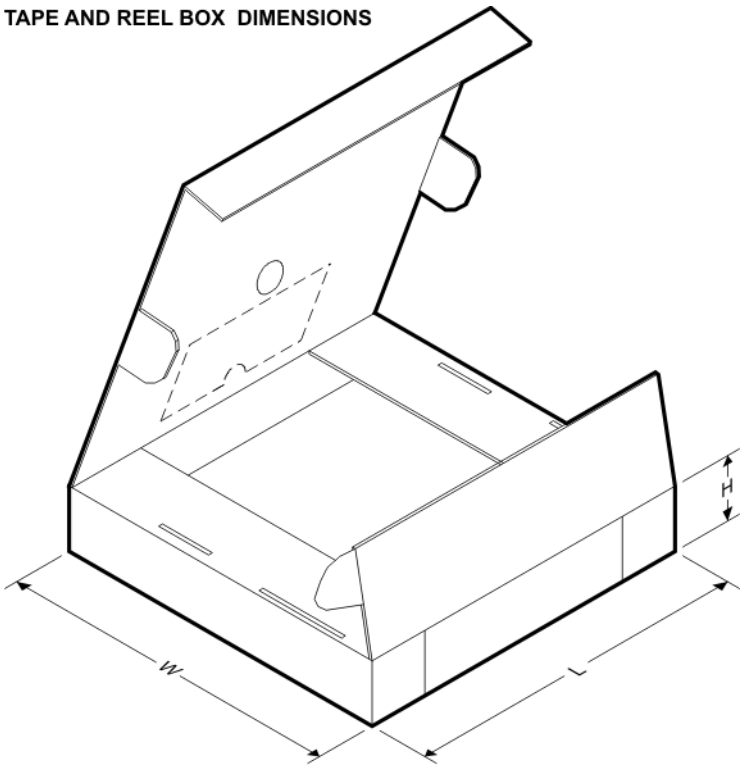
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC74ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC74ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC74ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC74APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

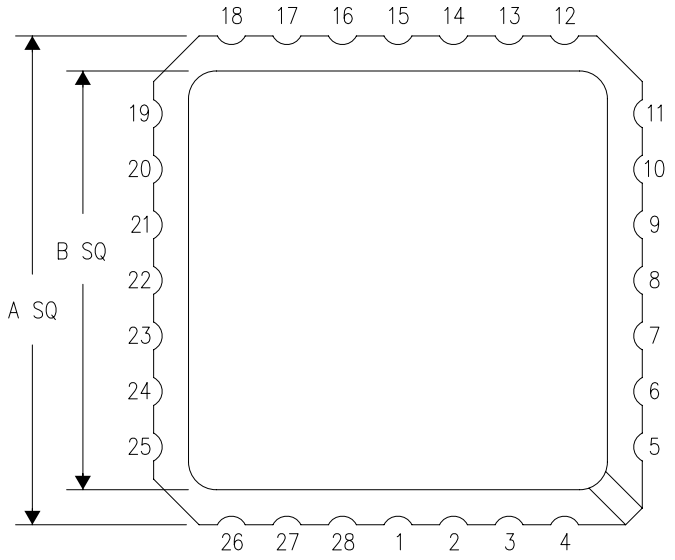


*All dimensions are nominal

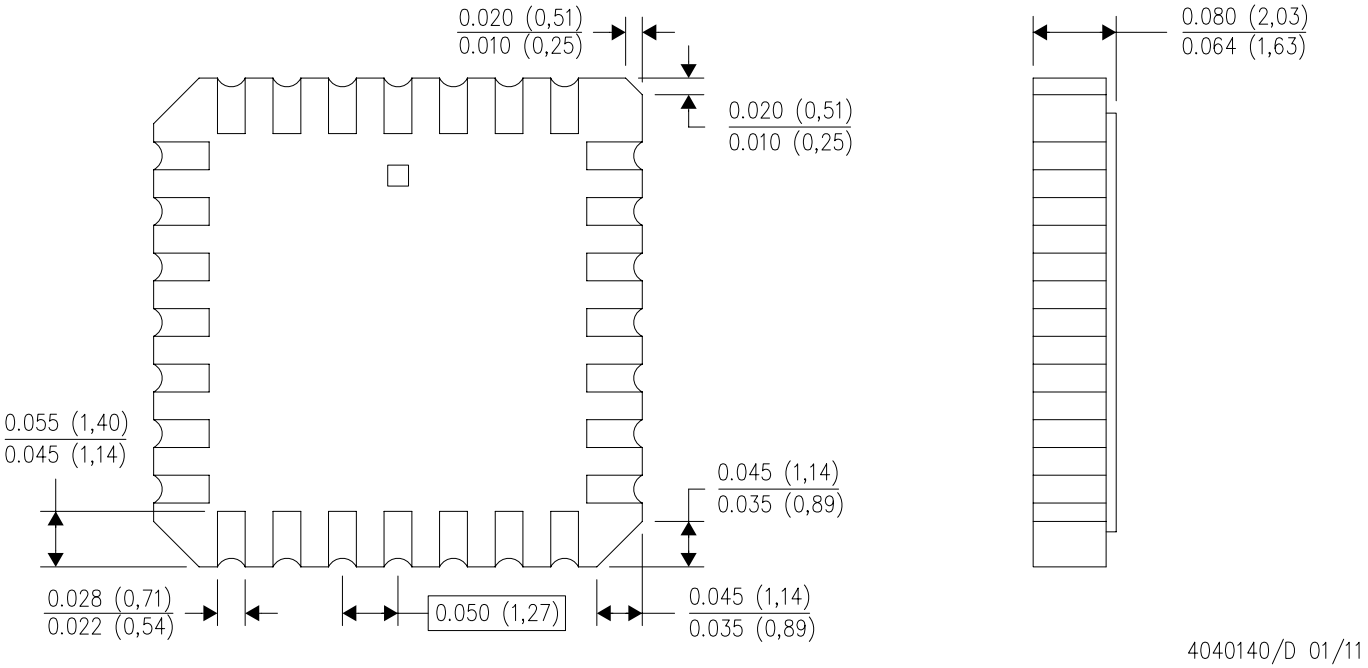
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC74ADBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74LVC74ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LVC74ADT	SOIC	D	14	250	367.0	367.0	38.0
SN74LVC74ANSR	SO	NS	14	2000	367.0	367.0	38.0
SN74LVC74APWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LVC74APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC74APWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LVC74APWT	TSSOP	PW	14	250	367.0	367.0	35.0
SN74LVC74ARGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



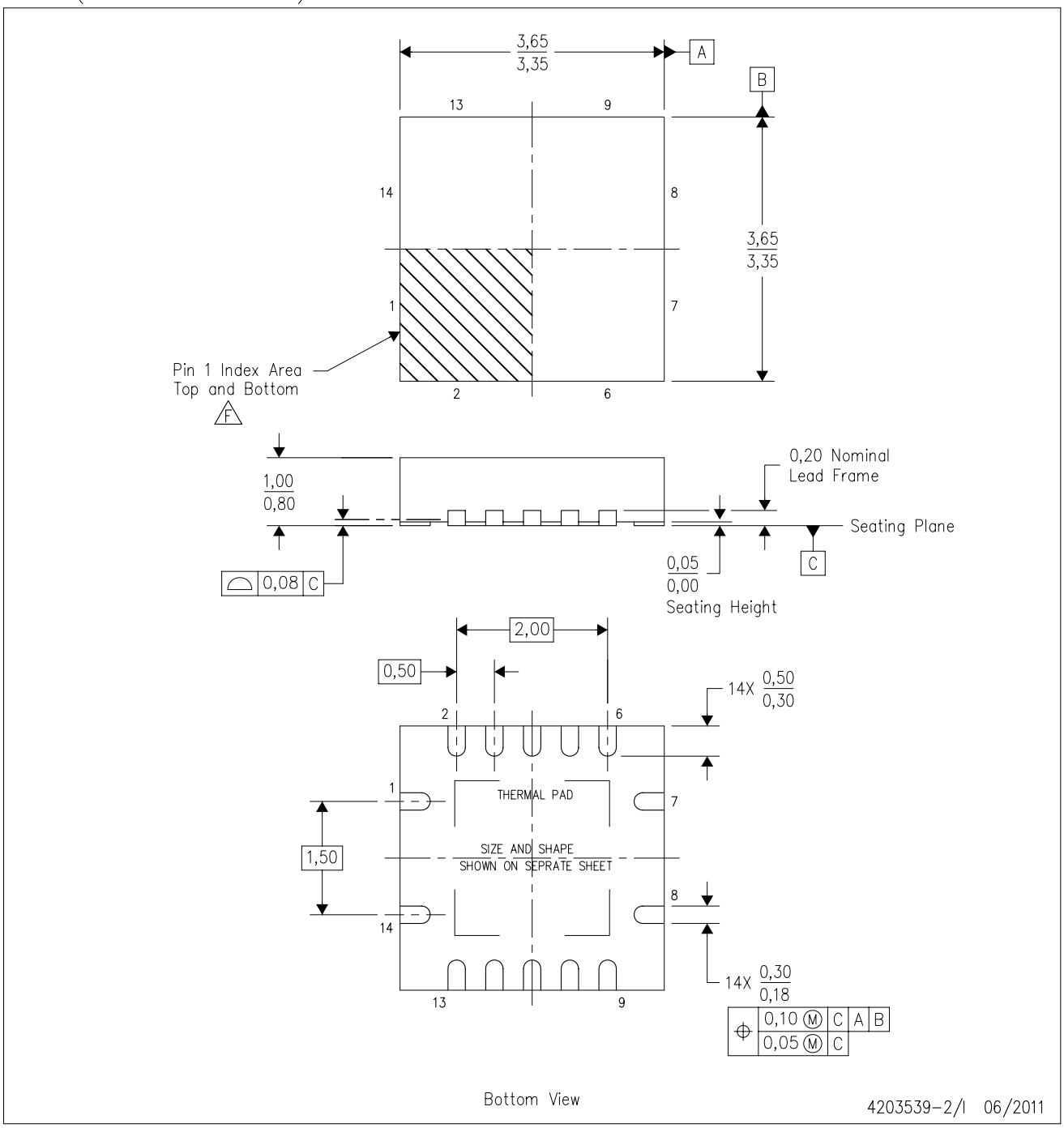
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

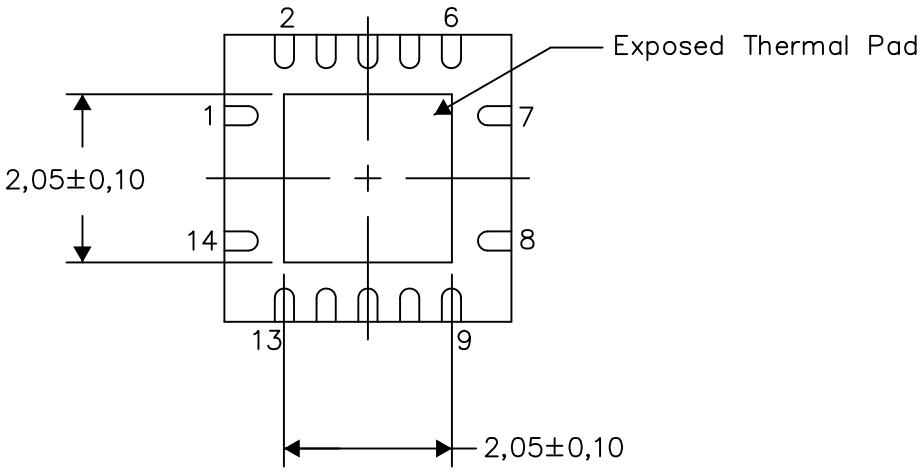
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

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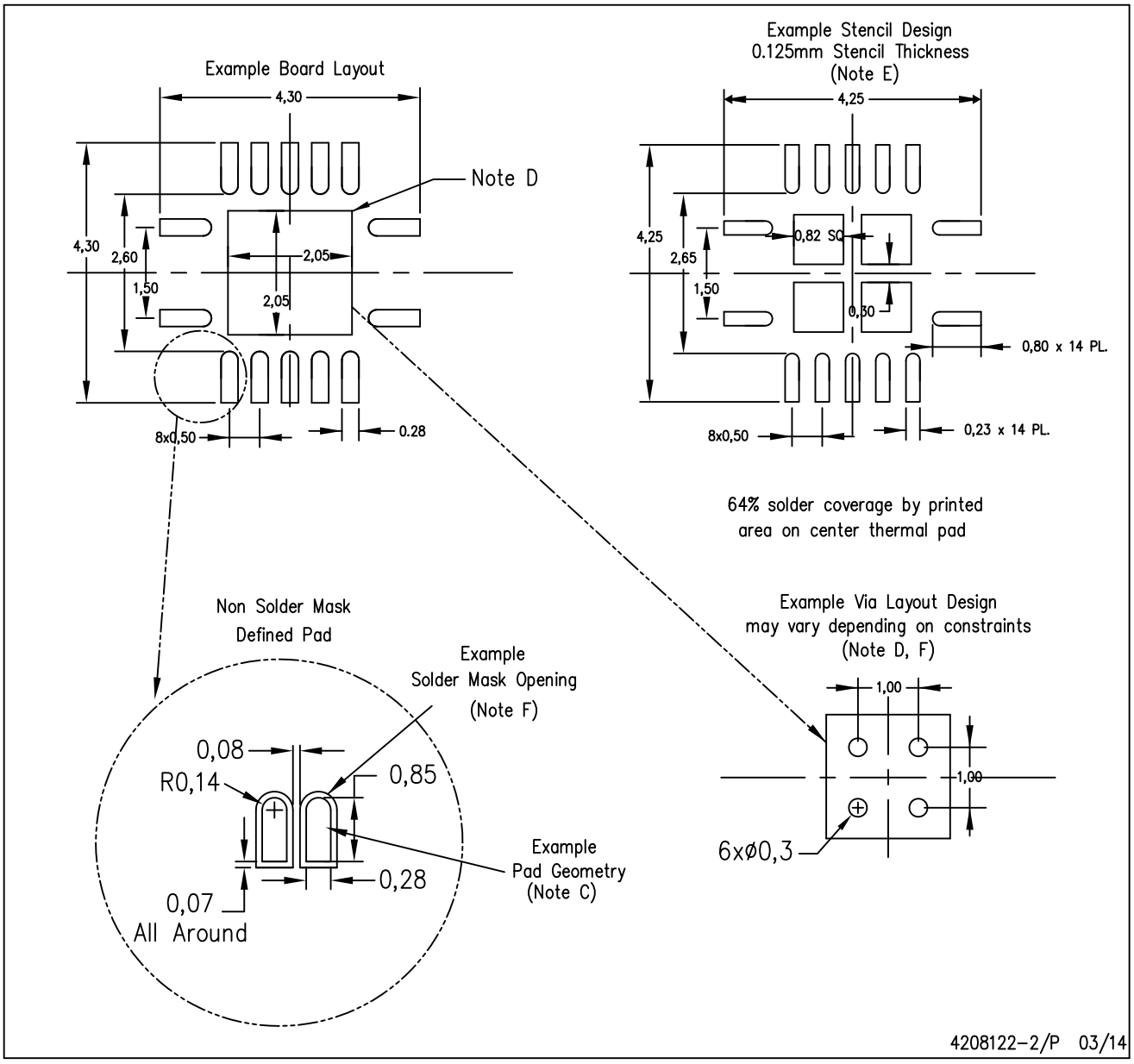
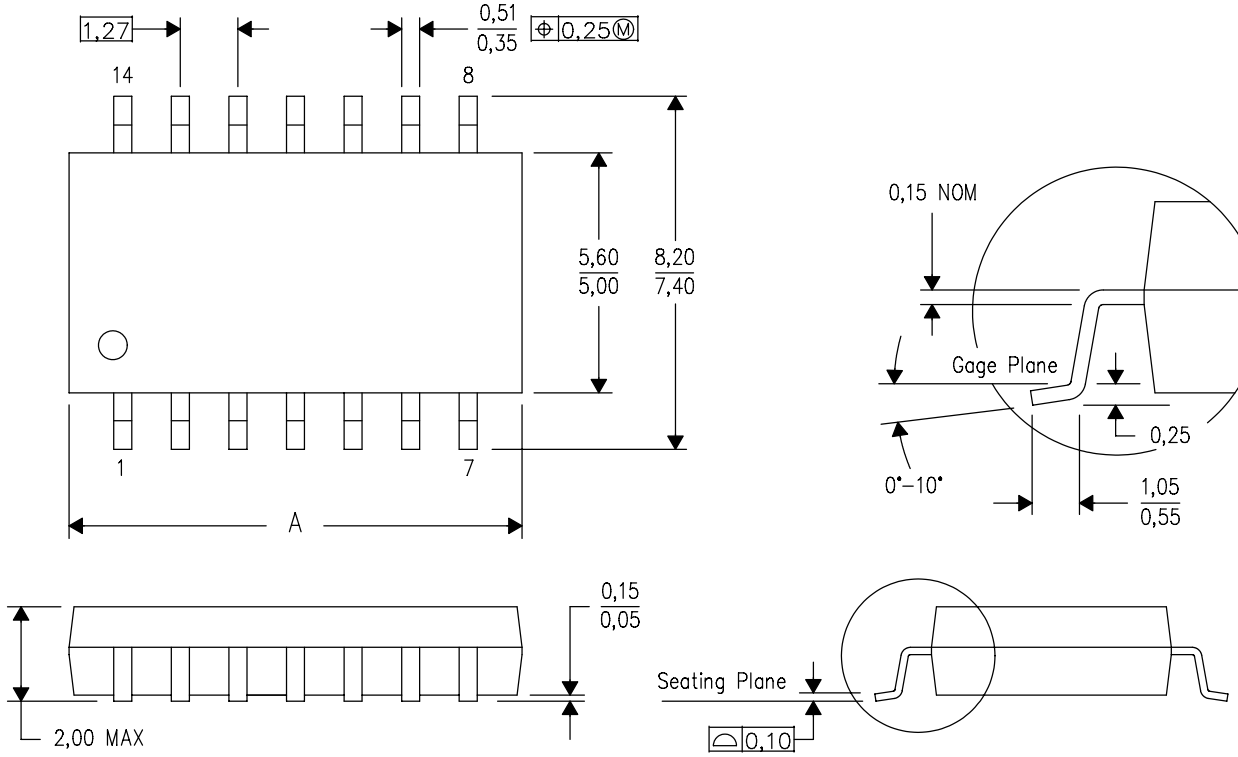


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

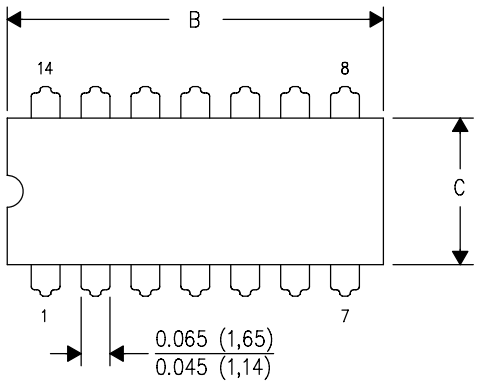
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

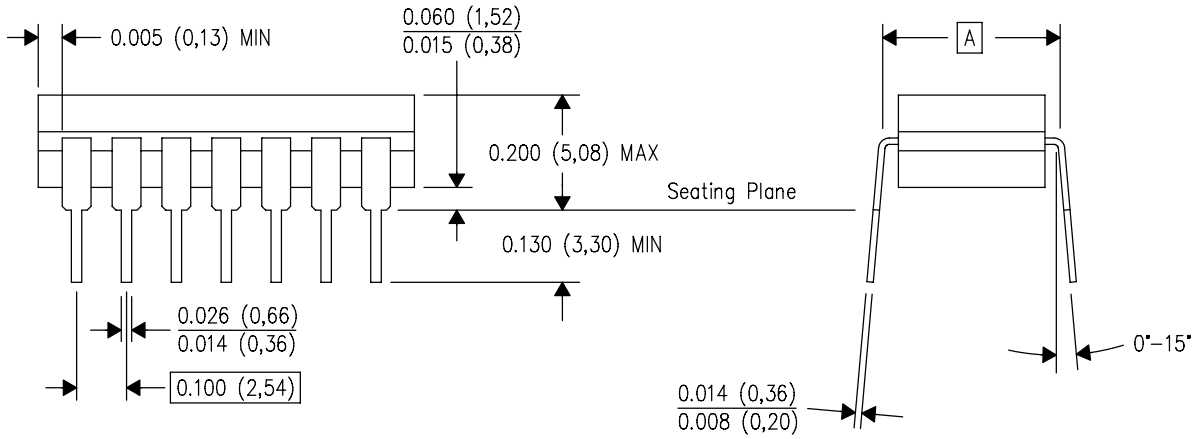
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



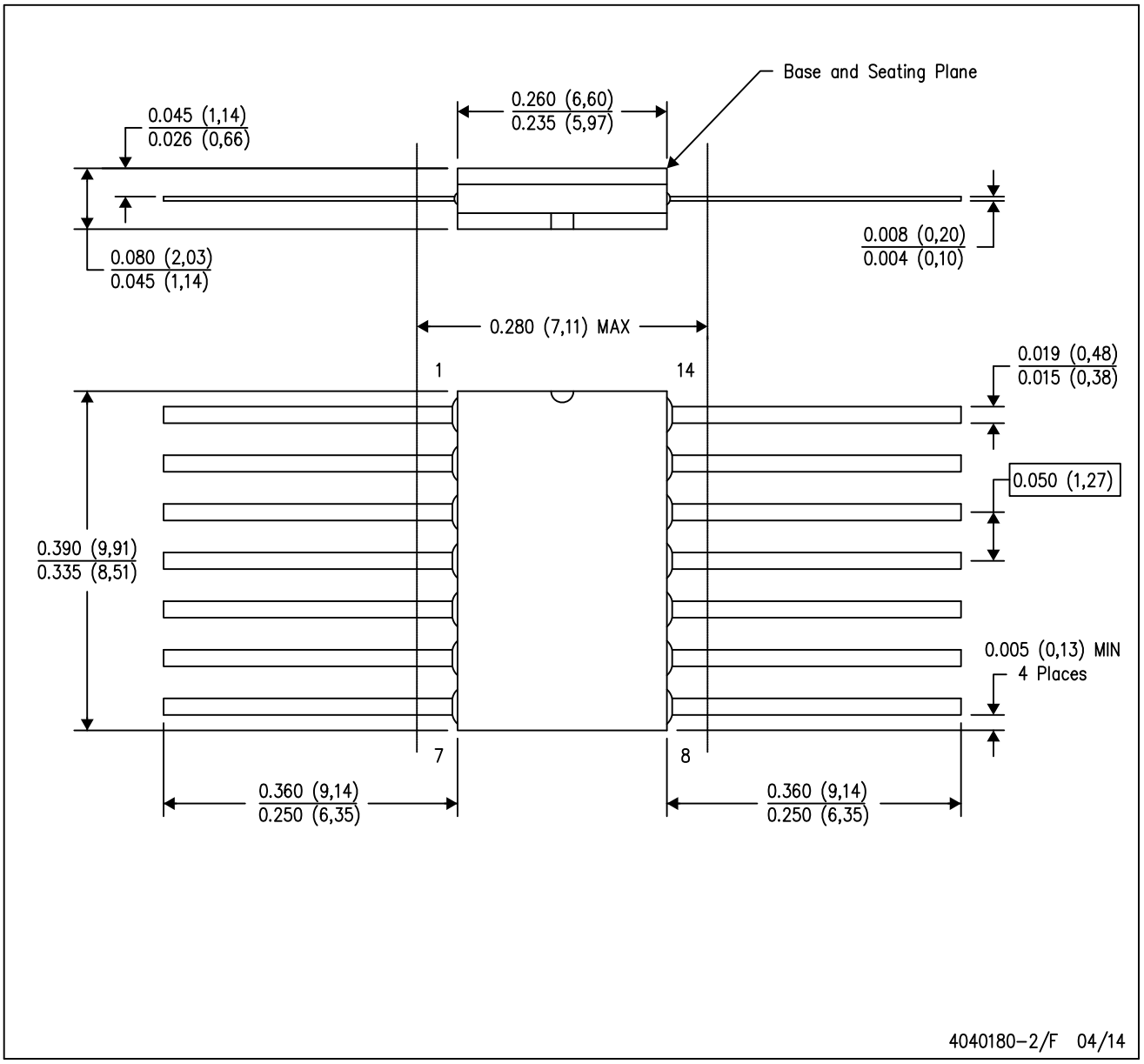
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

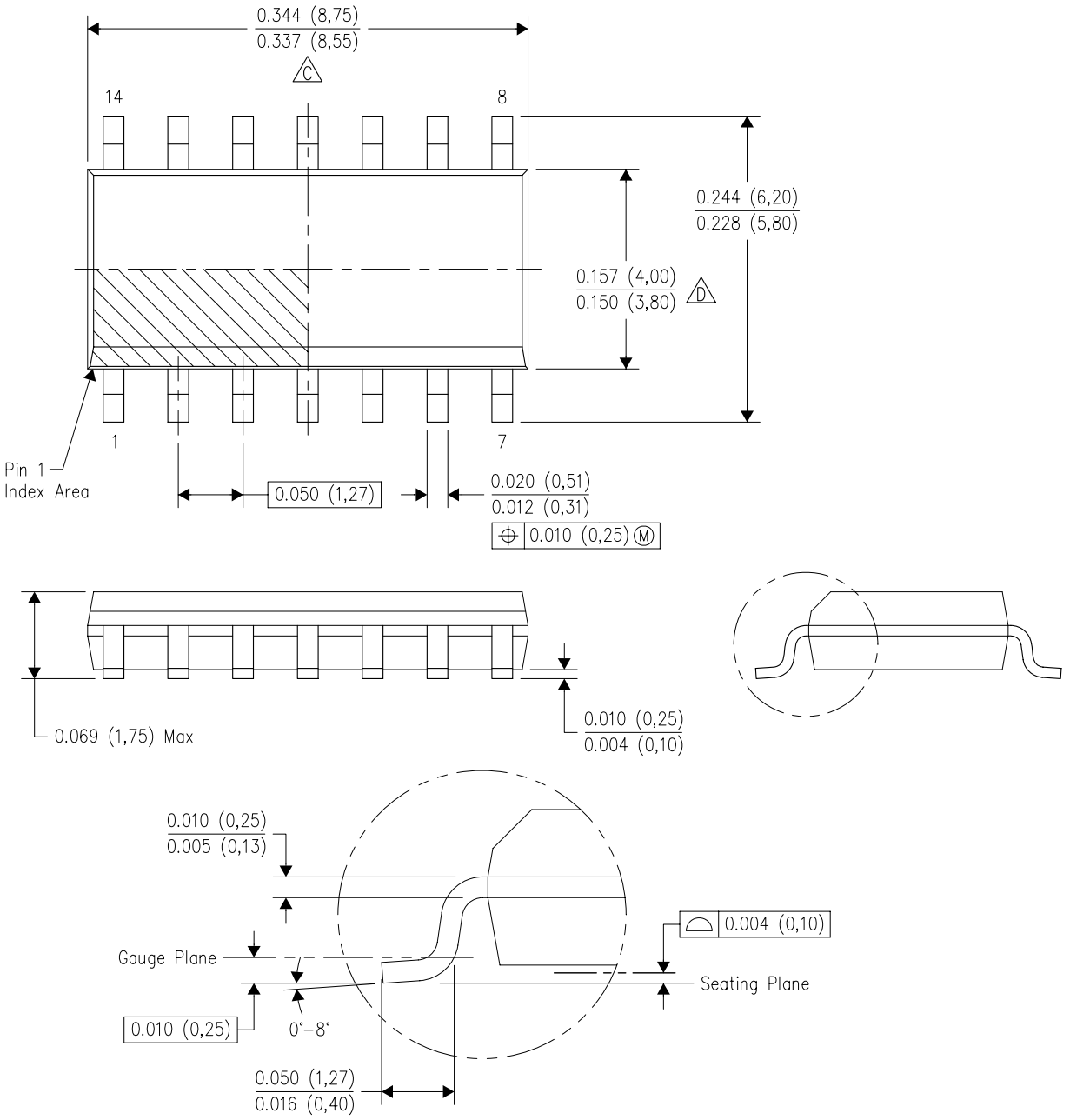
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

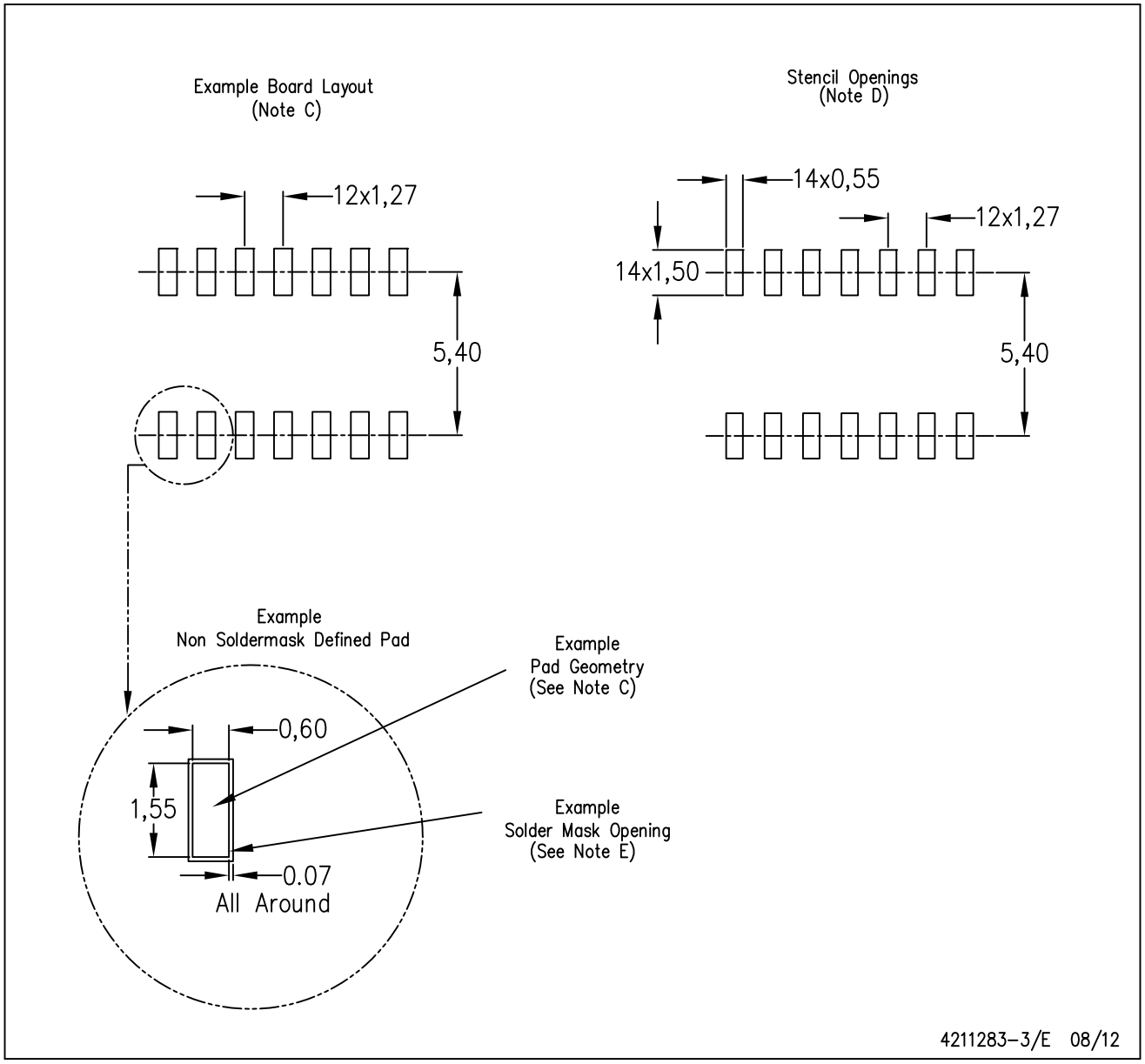
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

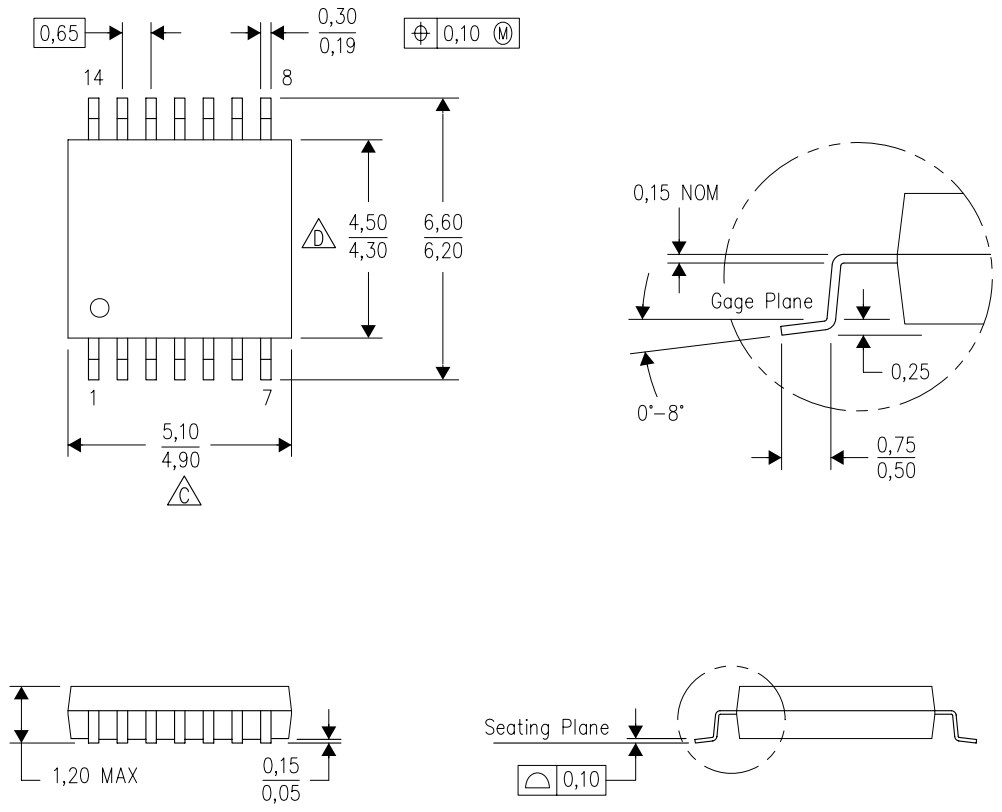
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

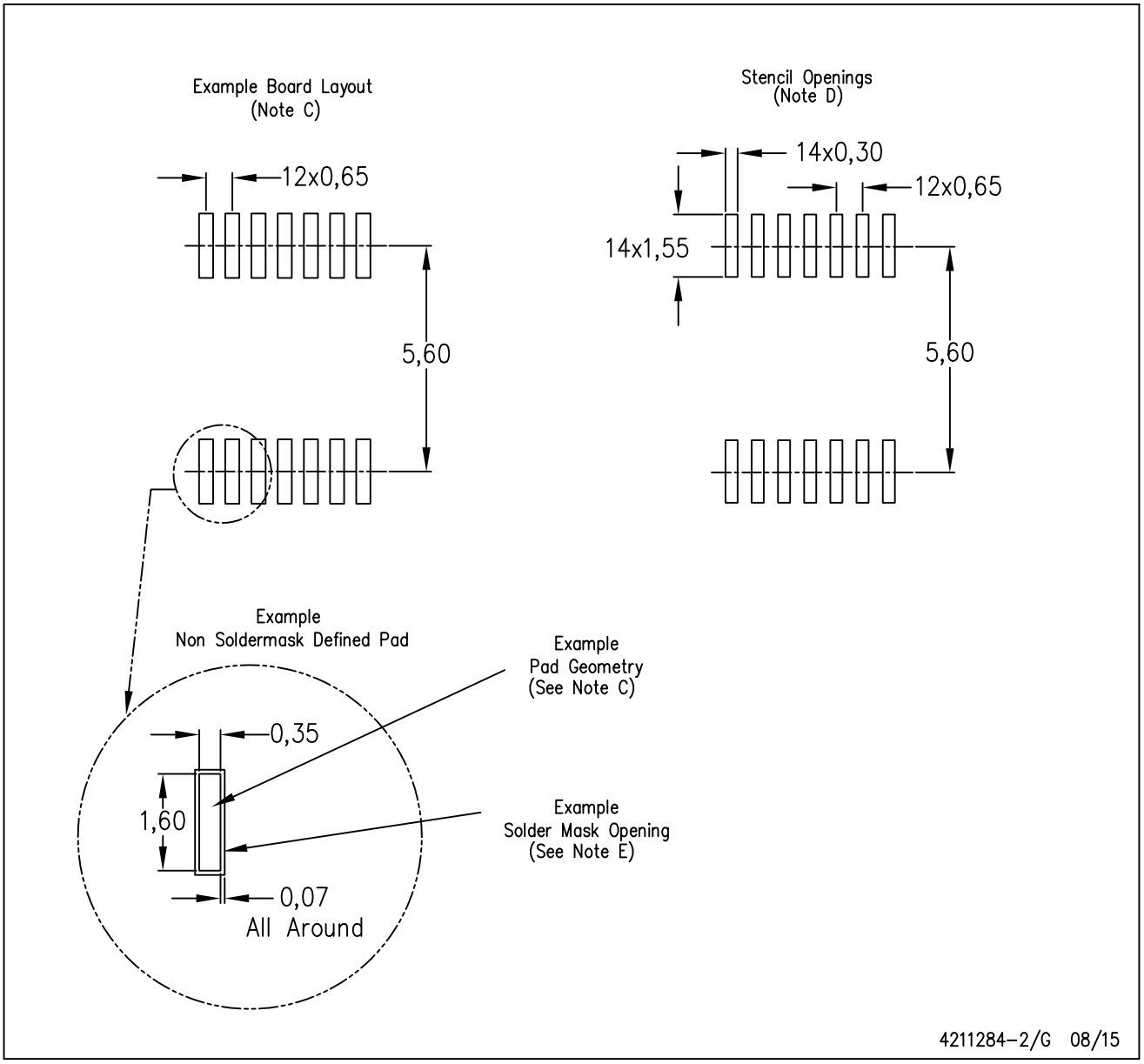
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

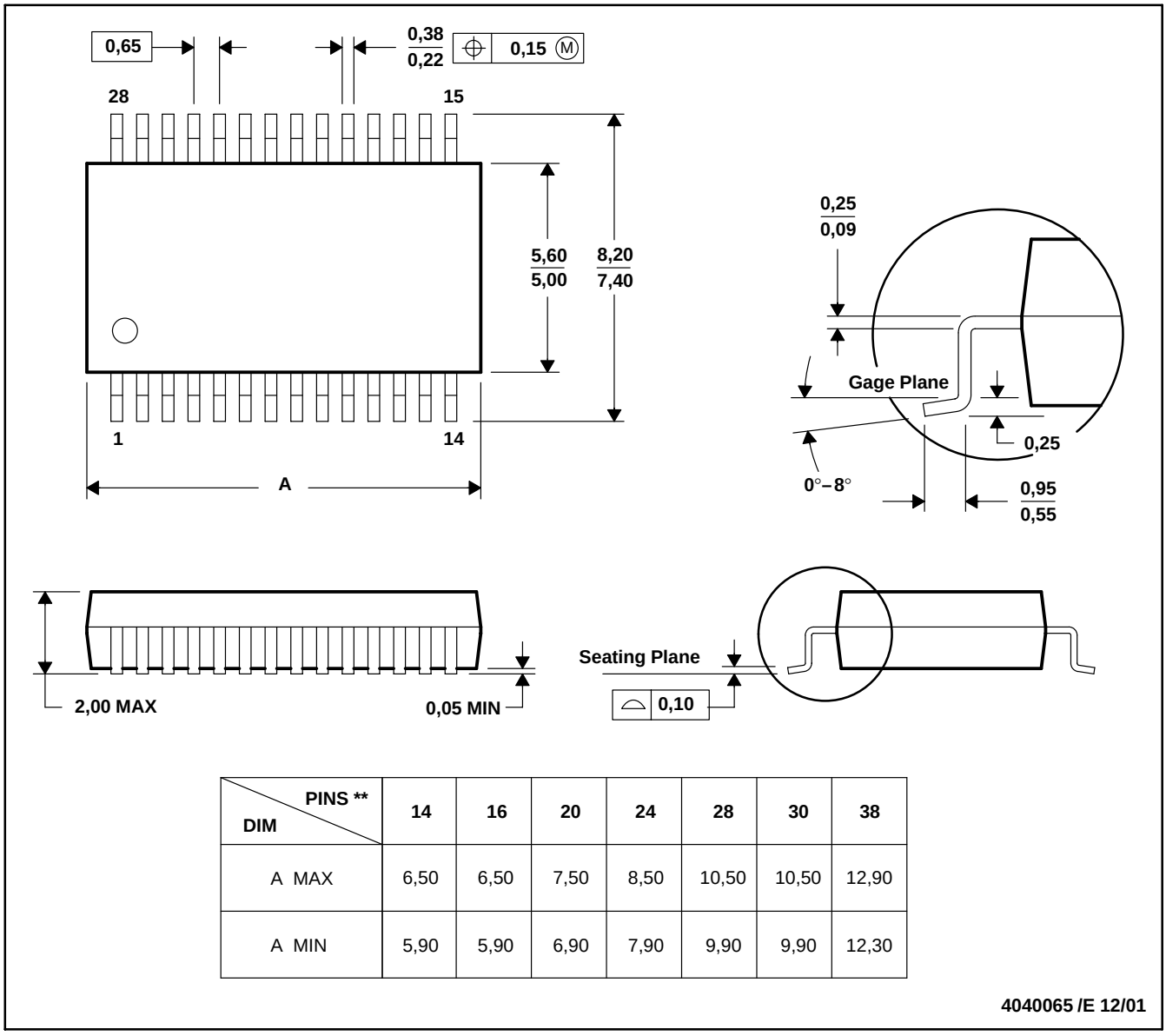


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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