

N-Channel 650V (D-S) Power MOSFET

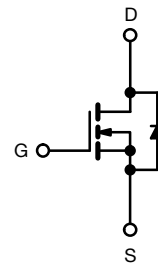
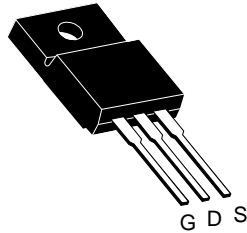
PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ max. (Ω) at 25 °C	$V_{GS} = 10$ V	0.50
Q_g max. (nC)	71	
Q_{gs} (nC)	14	
Q_{gd} (nC)	33	
Configuration	Single	

FEATURES

- Reduced t_{rr} , Q_{rr} , and I_{RRM}
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Low switching losses due to reduced Q_{rr}
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



TO-220 FULLPAK




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	18
		$T_C = 100$ °C	16
Pulsed Drain Current ^a	I_{DM}	53	A
Linear Derating Factor		1.7	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	367	mJ
Maximum Power Dissipation	P_D	68	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	37	V/ns
Reverse Diode dV/dt ^d			
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 5.1$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.5	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.67	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.5	-	4.5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}$	-	0.36	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}, I_D = 11\text{ A}$		-	7.0	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$		-	3322	-	pF
Output Capacitance	C_{oss}			-	205	-	
Reverse Transfer Capacitance	C_{rss}			-	120	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$		-	84	-	pF
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	293	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}, V_{DS} = 520\text{ V}$	-	71	-	nC
Gate-Source Charge	Q_{gs}			-	14	-	
Gate-Drain Charge	Q_{gd}			-	33	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	22	44	ns
Rise Time	t_r			-	34	68	
Turn-Off Delay Time	$t_{d(off)}$			-	68	102	
Fall Time	t_f			-	42	84	
Gate Input Resistance	R_g			$f = 1\text{ MHz}, \text{ open drain}$		-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	21	A
Pulsed Diode Forward Current	I_{SM}			-	-	53	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 11\text{ A}, V_{GS} = 0\text{ V}$		-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 11\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	160	-	ns
Reverse Recovery Charge	Q_{rr}			-	1.2	-	μC
Reverse Recovery Current	I_{RRM}			-	14	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

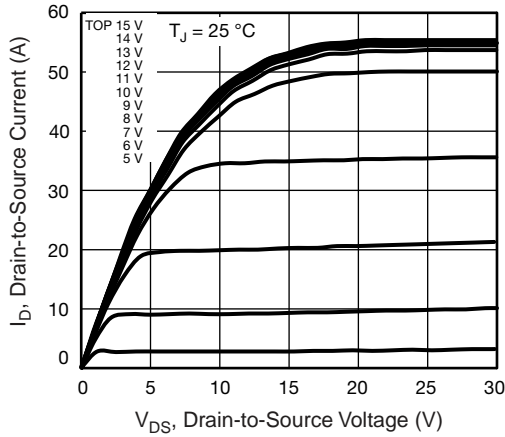


Fig. 1 - Typical Output Characteristics

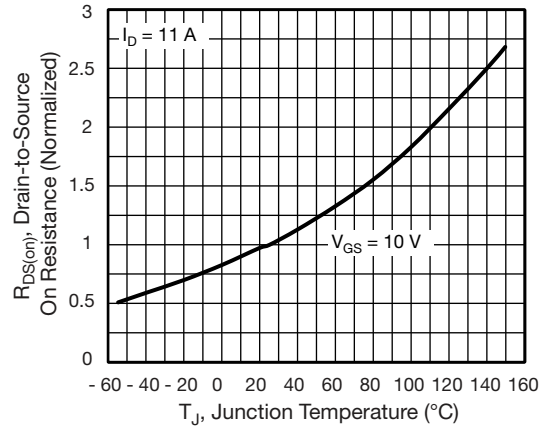


Fig. 4 - Normalized On-Resistance vs. Temperature



Fig. 2 - Typical Output Characteristics

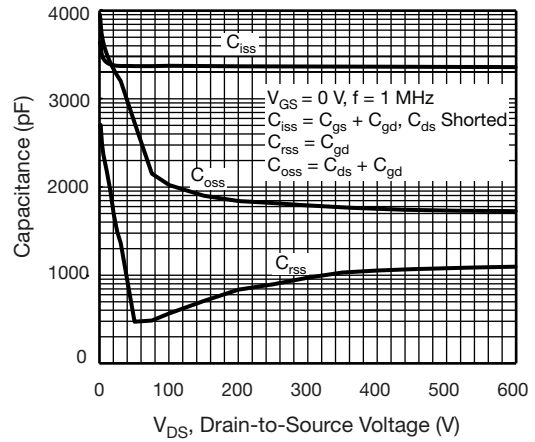


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 3 - Typical Transfer Characteristics

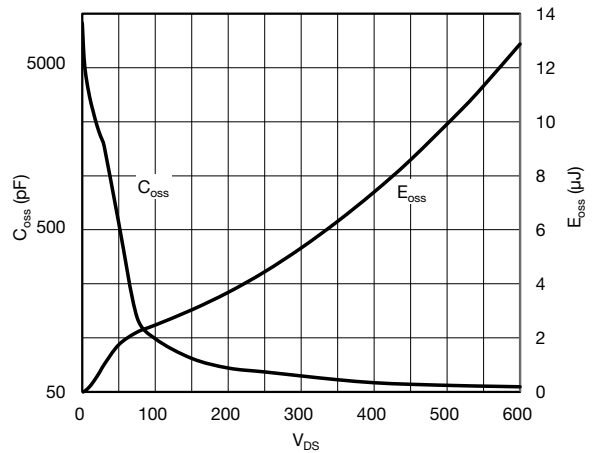


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}



Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 10 - Maximum Drain Current vs. Case Temperature

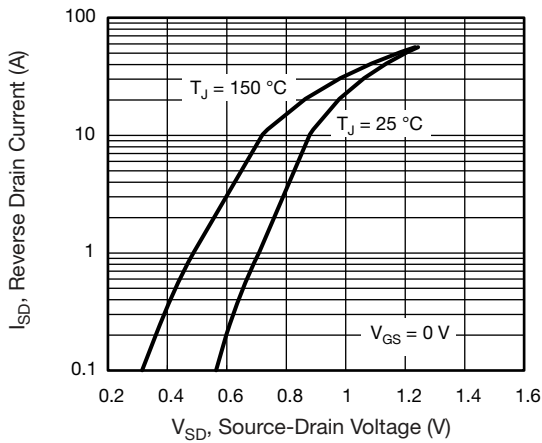


Fig. 8 - Typical Source-Drain Diode Forward Voltage

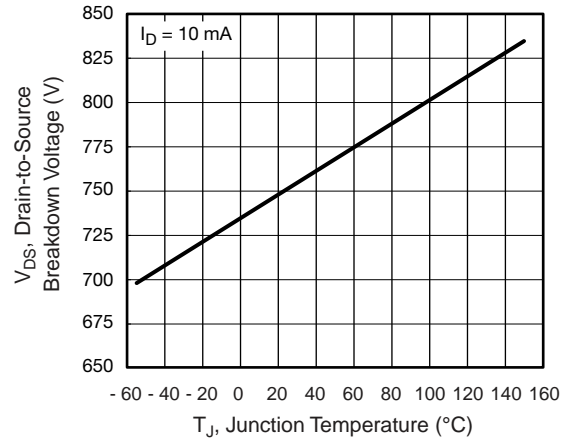


Fig. 11 - Temperature vs. Drain-to-Source Voltage

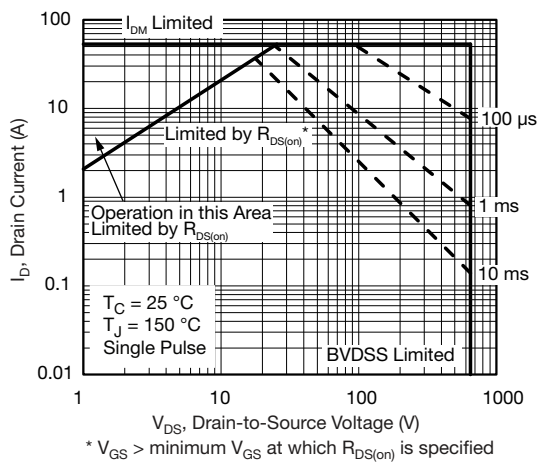


Fig. 9 - Maximum Safe Operating Area



Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 13 - Switching Time Test Circuit

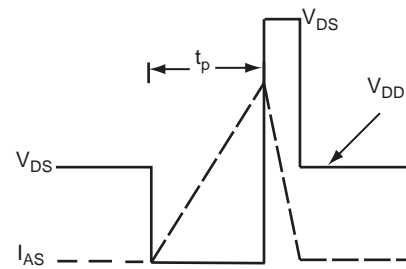


Fig. 16 - Unclamped Inductive Waveforms



Fig. 14 - Switching Time Waveforms



Fig. 17 - Basic Gate Charge Waveform

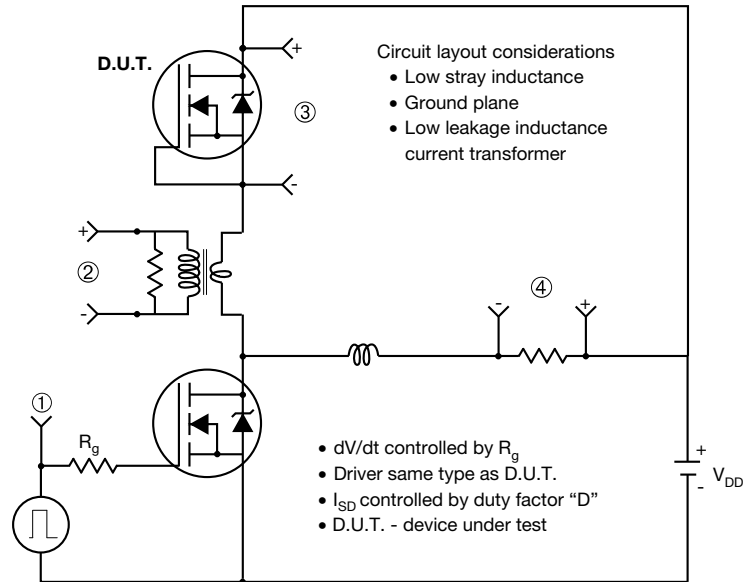


Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

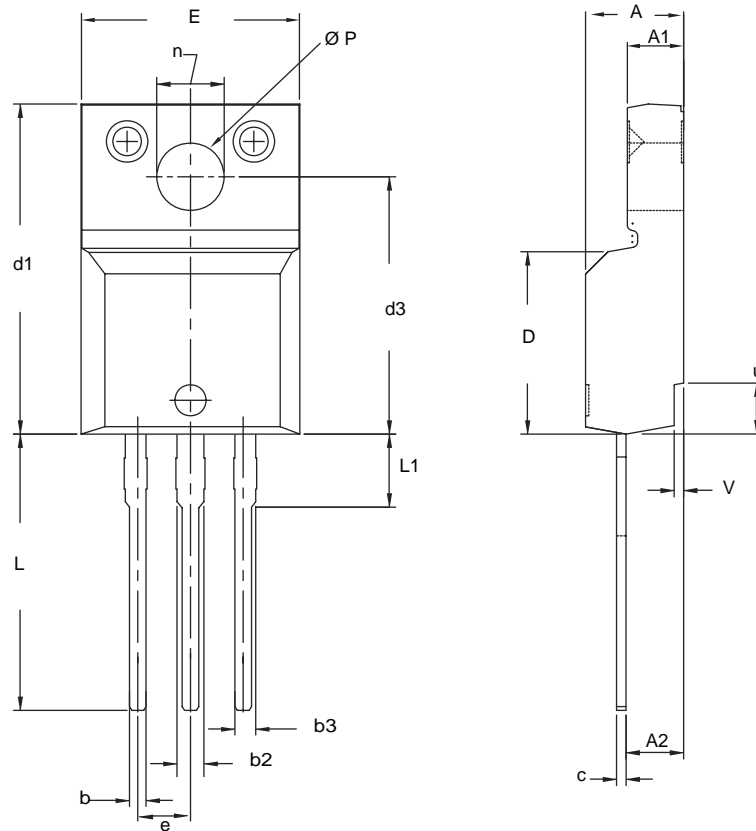


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

TO-220 FULLPAK (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09
DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

Disclaimer

All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

Taiwan VBsemi Electronics Co., Ltd., branches, agents, employees, and all persons acting on its or their representatives (collectively, the "Taiwan VBsemi"), assumes no responsibility for any errors, inaccuracies or incomplete data contained in the table or any other any disclosure of any information related to the product.(www.VBsemi.com)

Taiwan VBsemi makes no guarantee, representation or warranty on the product for any particular purpose of any goods or continuous production. To the maximum extent permitted by applicable law on Taiwan VBsemi relinquished: (1) any application and all liability arising out of or use of any products; (2) any and all liability, including but not limited to special, consequential damages or incidental ; (3) any and all implied warranties, including a particular purpose, non-infringement and merchantability guarantee.

Statement on certain types of applications are based on knowledge of the product is often used in a typical application of the general product VBsemi Taiwan demand that the Taiwan VBsemi of. Statement on whether the product is suitable for a particular application is non-binding. It is the customer's responsibility to verify specific product features in the products described in the specification is appropriate for use in a particular application. Parameter data sheets and technical specifications can be provided may vary depending on the application and performance over time. All operating parameters, including typical parameters must be made by customer's technical experts validated for each customer application. Product specifications do not expand or modify Taiwan VBsemi purchasing terms and conditions, including but not limited to warranty herein.

Unless expressly stated in writing, Taiwan VBsemi products are not intended for use in medical, life saving, or life sustaining applications or any other application. Wherein VBsemi product failure could lead to personal injury or death, use or sale of products used in Taiwan VBsemi such applications using client did not express their own risk. Contact your authorized Taiwan VBsemi people who are related to product design applications and other terms and conditions in writing.

The information provided in this document and the company's products without a license, express or implied, by estoppel or otherwise, to any intellectual property rights granted to the VBsemi act or document. Product names and trademarks referred to herein are trademarks of their respective representatives will be all.

Material Category Policy

Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be RoHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.com)

Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 / .

Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.