TEXAS INSTRUMENTS

SN54LVC257A, SN74LVC257A

SCAS294O –JANUARY 1993–REVISED JUNE 2015

SNx4LVC257A Quadruple 2-Line to 1-Line Data Selectors and Multiplexers With 3-State Outputs

1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Maximum t_{pd} of 4.6 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Cable Modem Termination Systems
- Tests and Measurements
- I/O Expanders
- Motor Drivers
- Network Switches
- Servers
- Telecom Infrastructure

3 Description

These quadruple 2-line to 1-line data selectors and multiplexers are designed for 1.65-V to 3.6-V V_{CC} operation.

The SNx4LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC257A	VQFN (16)	3.50 mm × 4.00 mm
	SOIC (16)	9.90 mm × 3.91 mm
	SO (16)	10.30 mm × 5.30 mm
	SSOP (16)	5.50 mm × 6.20 mm
	TSSOP (16)	4.40 mm × 5.00 mm
SN54LVC257A	CDIP (16)	6.92 mm × 21.34 mm
	CFP (16)	10.30 mm × 6.73 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)
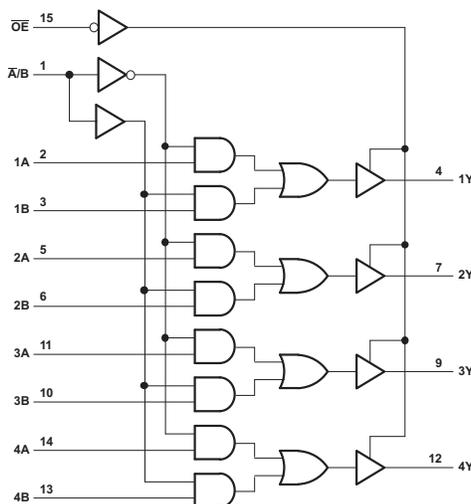
Pin numbers shown are for the D, DB, J, NS, PW , RGY , and W packages.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (June 2005) to Revision O   **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Product Folder Links: *SN54LVC257A SN74LVC257A*

5 Device Options

PART NUMBER	PACKAGE	BODY SIZE
SN74LVC257ARGYR	VQFN	3.50 mm × 4.00 mm
SN74LVC257AD	SOIC	3.90 mm × 9.90 mm
SN74LVC257ADT		
SN74LVC257ANSR	SO	5.30 mm × 10.10 mm
SN74LVC257ADBR	SSOP	5.50 mm × 6.20 mm
SN74LVC257APW	TSSOP	4.40 mm × 5.00 mm
SN74LVC257APWT		
SNJ54LVC257AJ	CDIP	6.92 mm × 21.34 mm
SNJ54LVC257AW	CFP	13.70 mm × 10.10 mm
SNJ54LVC257AFK	LCCC	8.89 mm × 8.89 mm

6 Pin Configuration and Functions

D, DB, NS, J, W, or PW Package
16-Pin SOIC, SSOP, SO, CDIP, CFP, or TSSOP
Top View

```
 A/B  [ 1      16 ]  VCC
 1A   [ 2      15 ]  OE
 1B   [ 3      14 ]  4A
 1Y   [ 4      13 ]  4B
 2A   [ 5      12 ]  4Y
 2B   [ 6      11 ]  3A
 2Y   [ 7      10 ]  3B
 GND  [ 8       9 ]  3Y
```
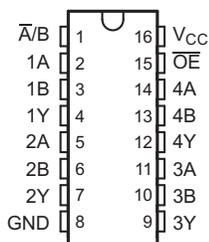
RGY Package
16-Pin VQFN with Exposed Thermal Pad
Top View

```
         A/B   VCC
          1     16
 1A   2              15   OE
 1B   3              14   4A
 1Y   4              13   4B
 2A   5              12   4Y
 2B   6              11   3A
 2Y   7              10   3B
          8     9
         GND   3Y
```
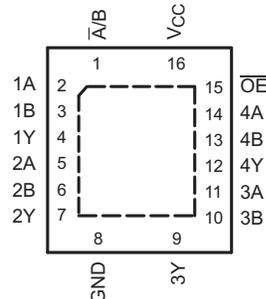
FK Package
20-Pin LCCC
Top View

```
        1A  A/B  NC  VCC  OE
         3   2   1   20   19
 1B  [ 4              18 ]  4A
 1Y  [ 5              17 ]  4B
 NC  [ 6              16 ]  NC
 2A  [ 7              15 ]  4Y
 2B  [ 8              14 ]  3A
         9  10  11  12  13
        2Y  GND  NC  3Y  3B
```
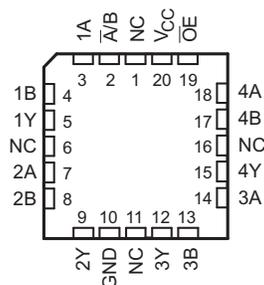
Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, SSOP, SO, CDIP, CFP, TSSOP, or VQFN	LCCC		
A/B	1	2	I	Select Pin, Low selects A, High selects B
1A	2	3	I/O	Multiplexer Signal Input
1B	3	4	I/O	Multiplexer Signal Input
1Y	4	5	I/O	Multiplexer Output
2A	5	7	I/O	Multiplexer Signal Input
2B	6	8	I/O	Multiplexer Signal Input
2Y	7	9	I/O	Multiplexer Output
3A	11	14	I/O	Multiplexer Signal Input
3B	10	13	I/O	Multiplexer Signal Input
3Y	9	12	I/O	Multiplexer Output
4A	14	18	I/O	Multiplexer Signal Input
4B	13	17	I/O	Multiplexer Signal Input
4Y	12	15	I/O	Multiplexer Output
GND	8	10	—	Ground
NC[(1)]	—	1, 6, 11, 16	—	No connect
OE	15	19	I/O	Active low Output enable
VCC	16	20	—	Power pin

(1) NC – no internal connection

Product Folder Links: *SN54LVC257A SN74LVC257A*

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	6.5	V
V_I	Input voltage[2]		−0.5	6.5	V
V_O	Output voltage[2] [3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

See [1]

			SN54LVC257A		SN74LVC257A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V				−4	mA
		V_{CC} = 2.3 V				−8	
		V_{CC} = 2.7 V		−12		−12	
		V_{CC} = 3 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
Δt/Δv	Input transition rise or fall rate			10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

7.4 Thermal Information: 16-Pin Packages

THERMAL METRIC[1]	SN54LVC257A, SN74LVC257A				UNIT
	D (SOIC)[2]	DB (SSOP)[2]	NS (SO)[2]	PW (TSSOP)[2]	
	16 PINS				
$R_{\theta JA}$ Junction-to-ambient thermal resistance	73	82	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Thermal Information: 20-Pin Package

THERMAL METRIC[1]	SN54LVC257A	UNIT
	RGY (LCCC)[2]	
	20 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	39	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-5.

Product Folder Links: *SN54LVC257A   SN74LVC257A*

7.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LVC257A MIN	SN54LVC257A TYP[1]	SN54LVC257A MAX	SN74LVC257A MIN	SN74LVC257A TYP[1]	SN74LVC257A MAX	UNIT
V_{OH}	I_{OH} = −100 μA	1.65 V to 3.6 V				V_{CC} − 0.2			V
	I_{OH} = −100 μA	2.7 V to 3.6 V	V_{CC} − 0.2						
	I_{OH} = −4 mA	1.65 V				1.2			
	I_{OH} = −8 mA	2.3 V				1.7			
	I_{OH} = −12 mA	2.7 V		2.2			2.2		
		3 V		2.4			2.4		
	I_{OH} = −24 mA	3 V		2.2			2.2		
V_{OL}	I_{OL} = 100 μA	1.65 V to 3.6 V						0.2	V
		2.7 V to 3.6 V			0.2				
	I_{OL} = 4 mA	1.65 V						0.45	
	I_{OL} = 8 mA	2.3 V						0.7	
	I_{OL} = 12 mA	2.7 V			0.4			0.4	
	I_{OL} = 24 mA	3 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	3.6 V			±5			±5	μA
I_{OZ}	V_O = V_{CC} or GND	3.6 V			±15			±10	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			10			10	μA
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND	3.3 V		5			5		pF
C_o	V_O = V_{CC} or GND	3.3 V		5			5		pF

(1)   All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

7.7 SN54LVC257A Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.7 V MIN	V_{CC} = 2.7 V MAX	V_{CC} = 3.3 V ± 0.3 V MIN	V_{CC} = 3.3 V ± 0.3 V MAX	UNIT
t_{pd}	A or B	Y		5.4	1	4.6	ns
	$\overline{A}$/B			7.5	1	6.4	
t_{en}	$\overline{OE}$	Y		6.7	1	5.6	ns
t_{dis}	$\overline{OE}$	Y		4.7	0.5	4.3	ns
$t_{sk(o)}$						1	ns

7.8 SN74LVC257A Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V MIN	V_{CC} = 1.8 V ± 0.15 V MAX	V_{CC} = 2.5 V ± 0.2 V MIN	V_{CC} = 2.5 V ± 0.2 V MAX	V_{CC} = 2.7 V MIN	V_{CC} = 2.7 V MAX	V_{CC} = 3.3 V ± 0.3 V MIN	V_{CC} = 3.3 V ± 0.3 V MAX	UNIT
t_{pd}	A or B	Y	1	13.5	1	7.4	1	5.4	1	4.6	ns
	$\overline{A}$/B		1	15.6	1	9.5	1	7.5	1	6.4	
t_{en}	$\overline{OE}$	Y	1	14.6	1	8.7	1	6.7	1	5.6	ns
t_{dis}	$\overline{OE}$	Y	1	15.4	1	6.7	1	4.7	1	4.3	ns
$t_{sk(o)}$										1	ns

7.9 Operating Characteristics

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V TYP	V_{CC} = 2.5 V TYP	V_{CC} = 3.3 V TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	13.5	14.5	15.5	pF

7.10 Typical Characteristics

Figure 1. Propagation Delay (Low to High Transition) vs Load Capacitance

Figure 2. Propagation Delay (High to Low Transition) vs Load Capacitance
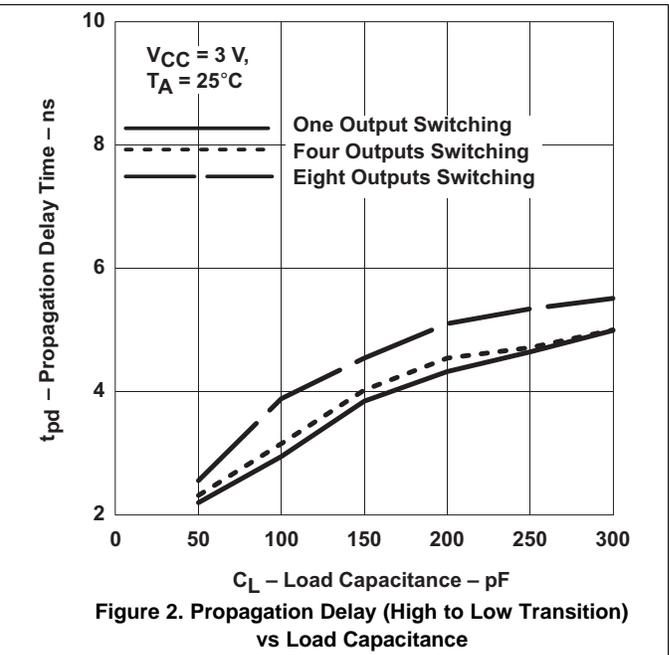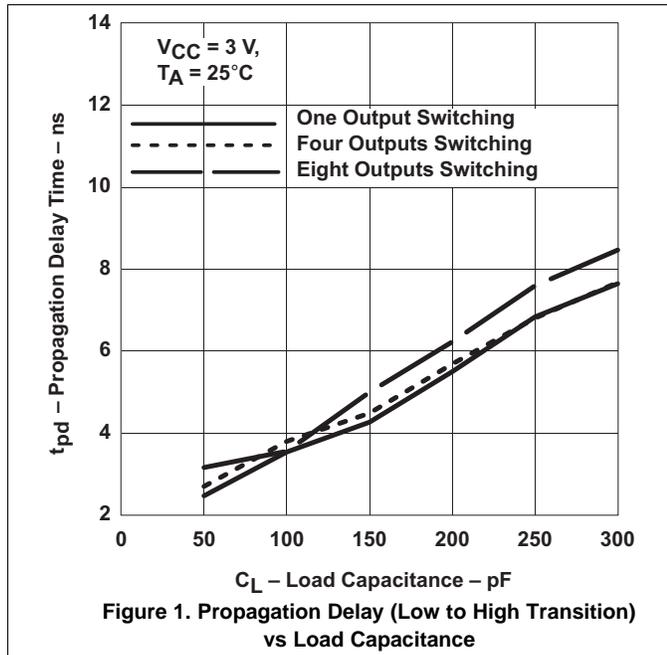
8 Parameter Measurement Information
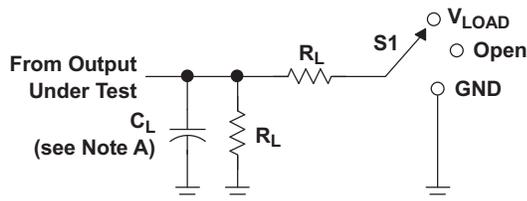
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V±0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V±0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
3.3 V±0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
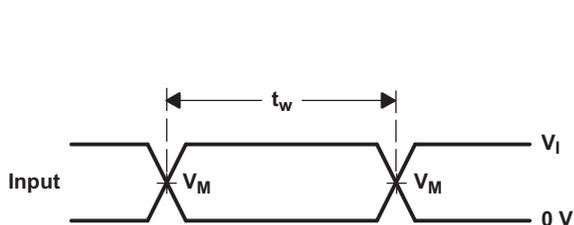
**VOLTAGE WAVEFORMS
PULSE DURATION**
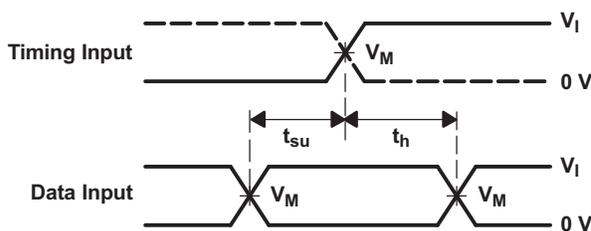
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
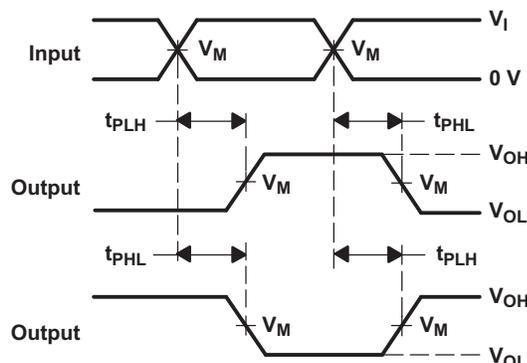
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**
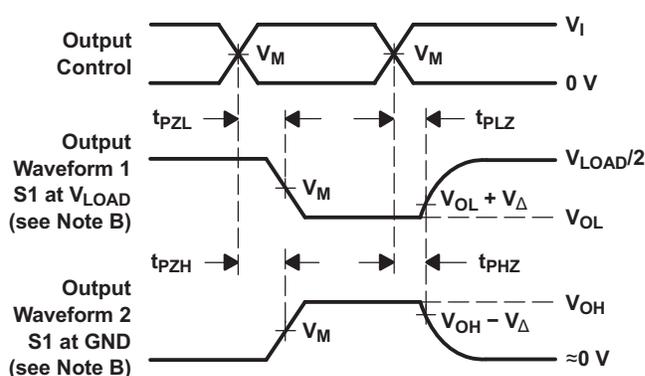
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
        B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
            Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
        C. All input pulses are supplied by generators having the following characteristcs: PRR ≤10 MHz, Z_O = 50 Ω.
        D. The outputs are measured one at a time, with one transition per measuremert.
        E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
        F. t_{PZL} and t_{PZH} are the same as t_{en}.
        G. t_{PLH} and t_{PHL} are the same as t_{pd}.
        H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

9 Detailed Description

9.1 Overview

These quadruple 2-line to 1-line data selectors and multiplexers are designed for 1.65-V to 3.6-V V_{CC} operation.

The SNx4LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

9.2 Functional Block Diagram
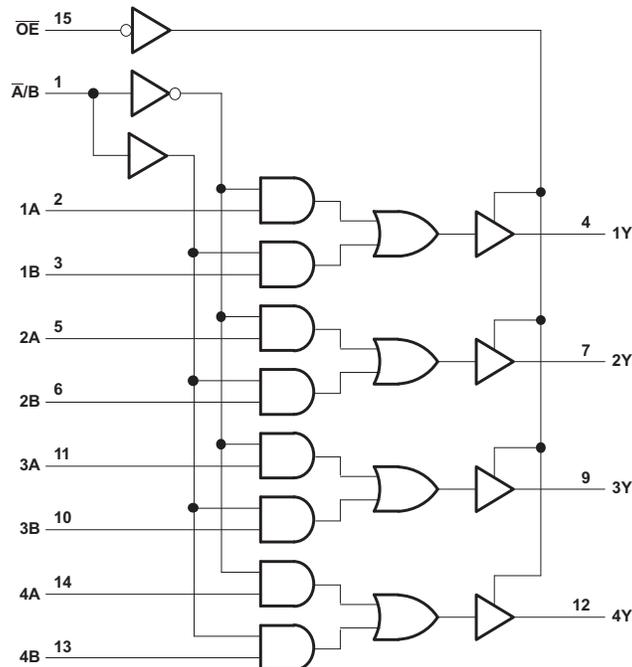
9.3 Feature Description

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V and 5-V system environment. Device features a maximum t_{pd} of 4.6 ns allowing the device to be used in high-speed applications as well.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

9.4 Device Functional Modes

Table 1 lists the functional modes for the SN54LVC257A and SN74LVC257A devices.

Table 1. Function Table

INPUTS				OUTPUT
$\overline{OE}$	$\overline{A}/B$	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SNx4LVC257A devices are useful for digital signal data selector or multiplexer applications.

10.2 Typical Application

The SNx4LVC257A devices use CMOS technology and have balanced output drive. These devices can be used for down level translation and multiplexer function as shown in Figure 4.
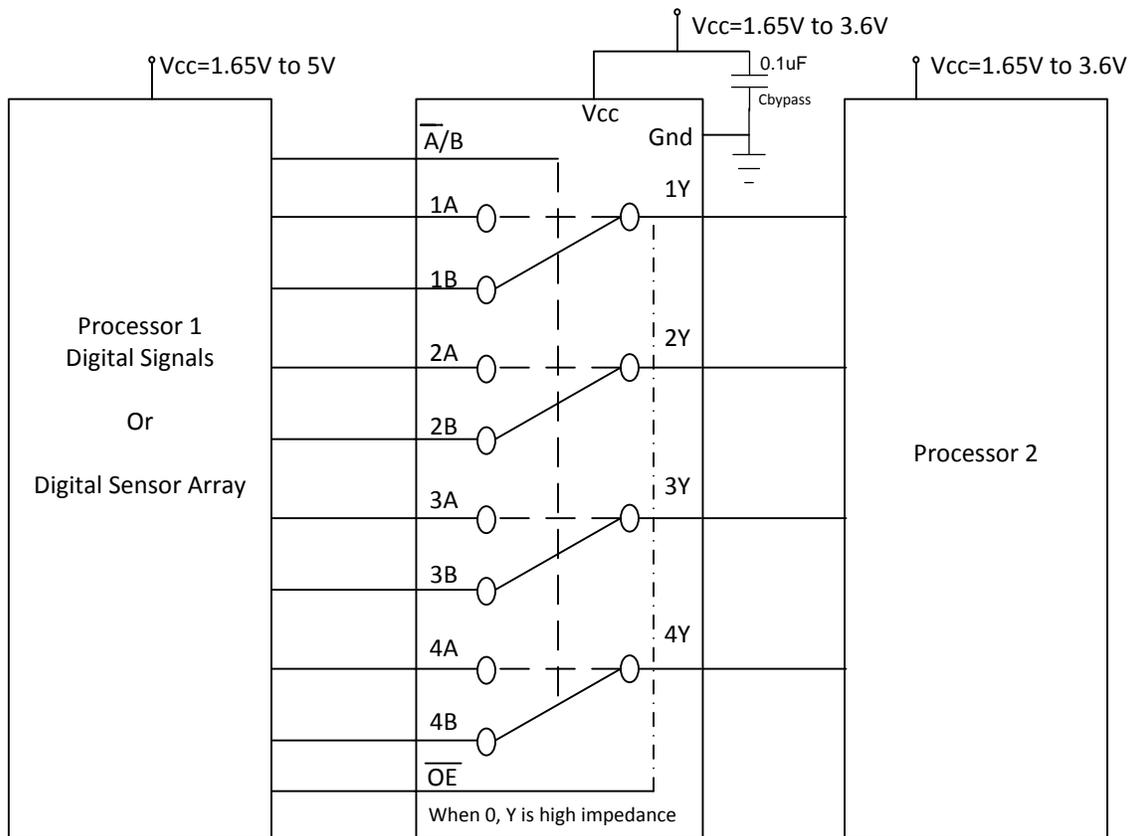

Figure 4. SNx4LVC257A Used as Level Translation and as a Multiplexer

10.2.1 Design Requirements

Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – For rise time and fall time specification, see ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   – For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   – Inputs are over voltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommend Output Conditions
   – Load currents must not exceed (I_O max) per output and must not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are in the *Recommended Operating Conditions* table.
   – Outputs must not be pulled above V_{CC}.

10.2.3 Application Curves

Figure 5. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

Figure 6. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

Product Folder Links: *SN54LVC257A SN74LVC257A*
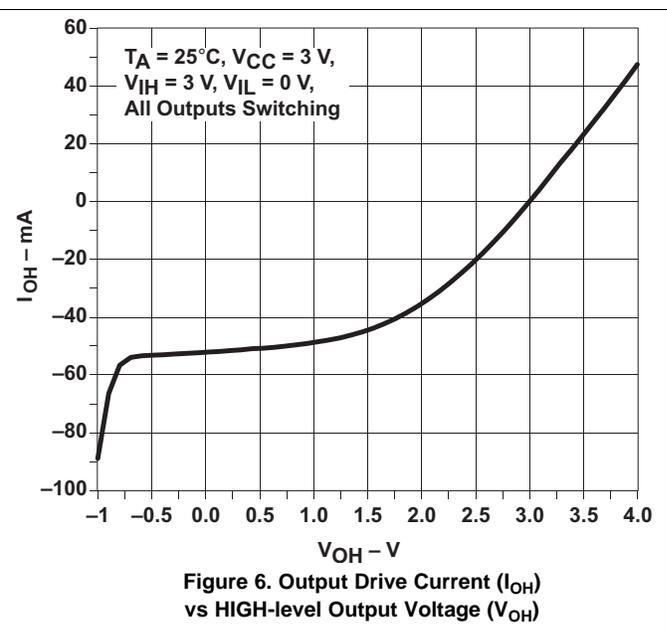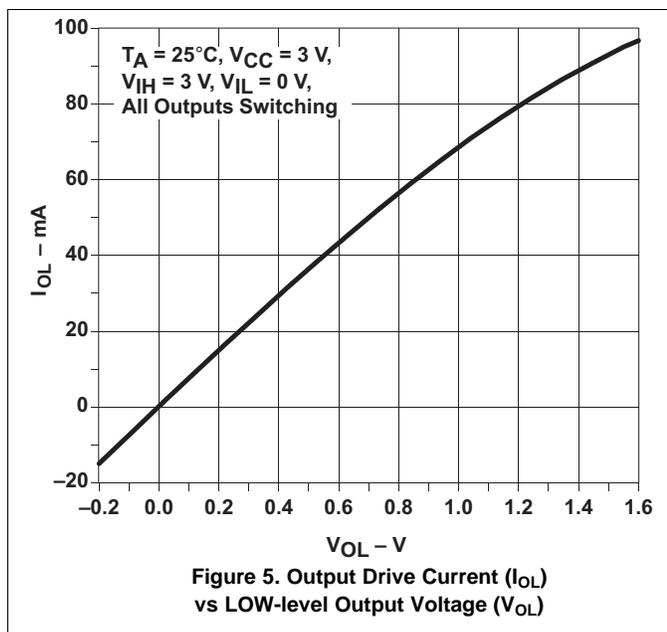
11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01-μF or 0.022-μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

12.2 Layout Example
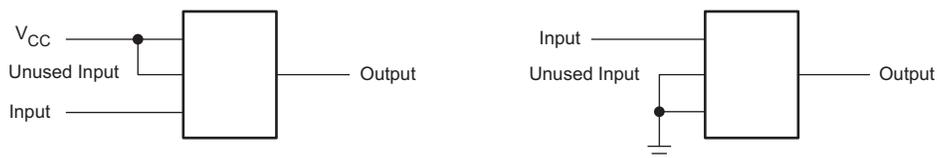
Figure 7. Layout Diagrams

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC257A	Click here	Click here	Click here	Click here	Click here
SN74LVC257A	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0050901QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-0050901QF A SNJ54LVC257AW	Samples
SN74LVC257AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	Samples
SN74LVC257ADBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	-40 to 85		
SN74LVC257ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	Samples
SN74LVC257ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	Samples
SN74LVC257ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	Samples
SN74LVC257ADT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	Samples
SN74LVC257ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC257A	Samples
SN74LVC257APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257APWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		
SN74LVC257APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC257APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC257A	Samples
SN74LVC257ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC257A	Samples
SNJ54LVC257AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-0050901QFA SNJ54LVC257AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

![Texas Instruments logo]

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC257A, SN74LVC257A :

- Catalog: SN74LVC257A

- Automotive: SN74LVC257A-Q1, SN74LVC257A-Q1

- Enhanced Product: SN74LVC257A-EP, SN74LVC257A-EP

- Military: SN54LVC257A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

K0 — P1

B0 — W

Cavity — A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
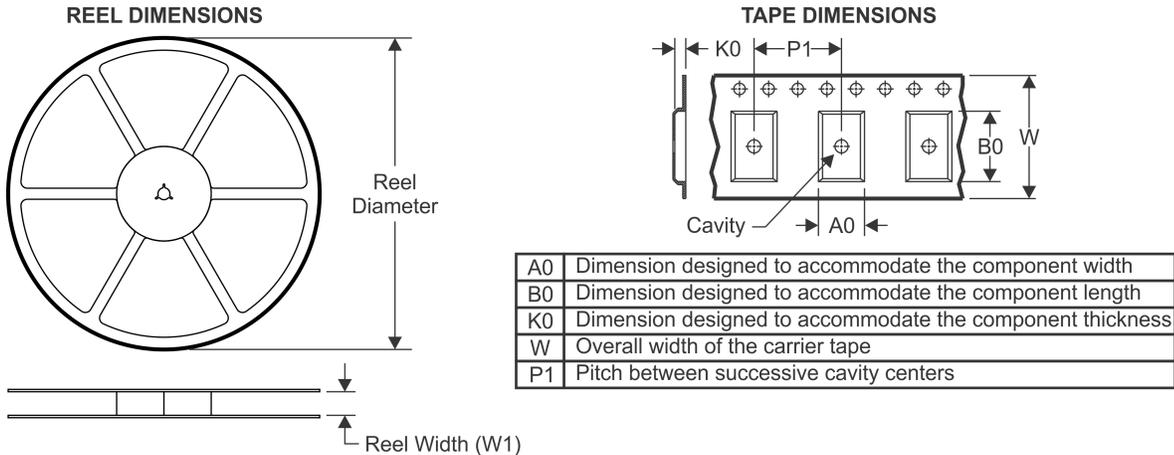
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1 | Q2   Q1 | Q2
Q3 | Q4   Q3 | Q4

User Direction of Feed

Pocket Quadrants
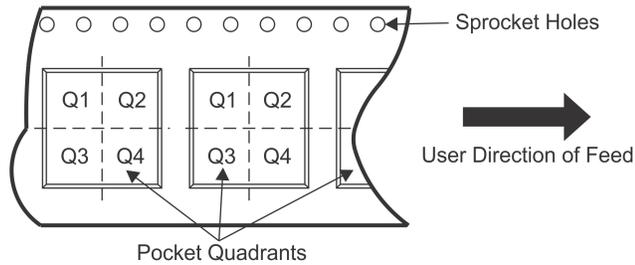
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC257ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC257ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC257ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC257ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC257ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LVC257ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LVC257ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LVC257APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LVC257APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LVC257APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LVC257APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LVC257ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

W (R−GDFP−F16)   CERAMIC DUAL FLATPACK
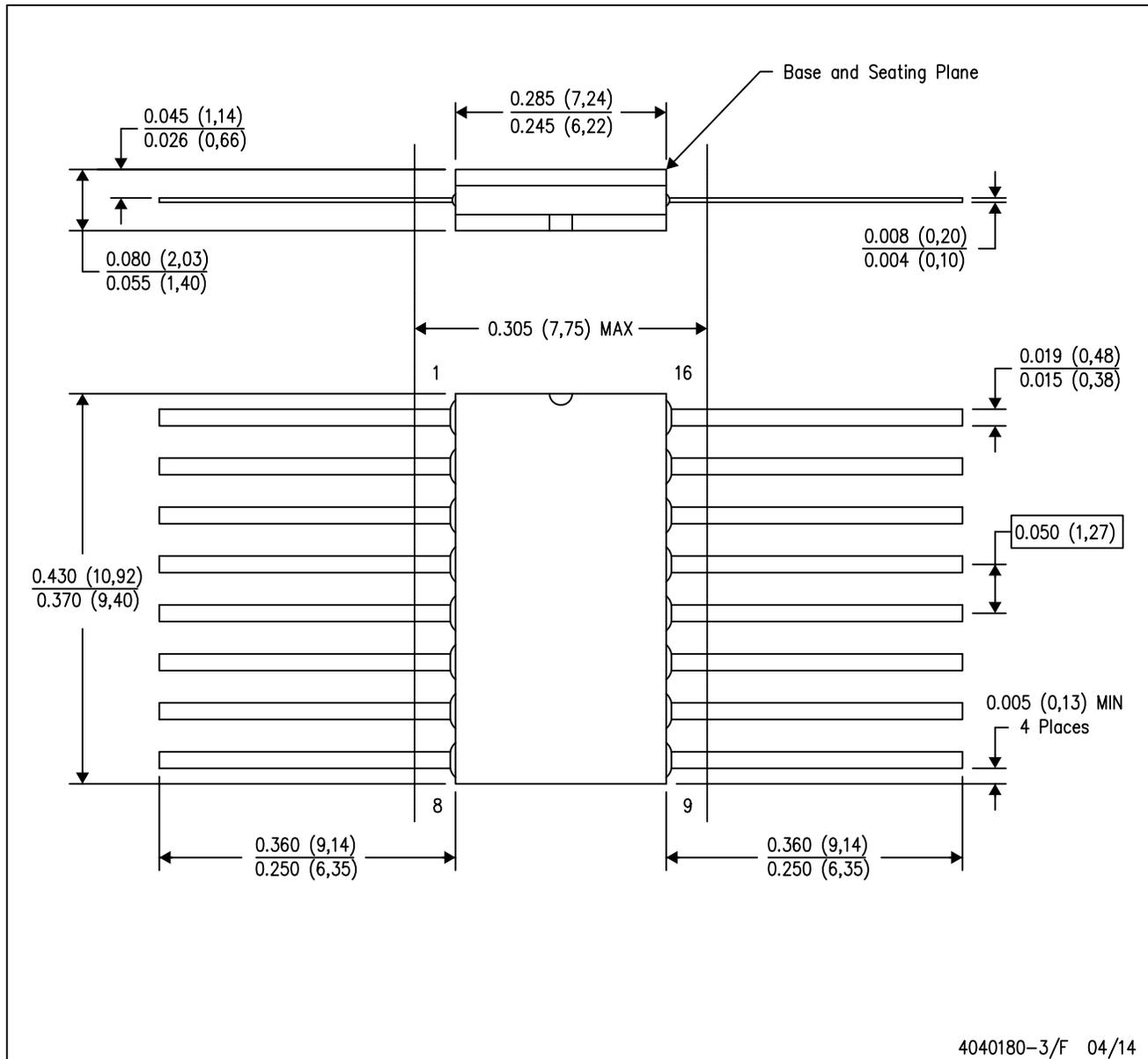
Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.285 (7,24)
0.245 (6,22)

0.080 (2,03)
0.055 (1,40)

0.008 (0,20)
0.004 (0,10)

0.305 (7,75) MAX

1   16

0.019 (0,48)
0.015 (0,38)

0.430 (10,92)
0.370 (9,40)

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8   9

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180−3/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within MIL STD 1835 GDFP2−F16

PW (R−PDSO−G16) PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

16   9

D 4,50
   4,30

6,60
6,20

1   8

5,10
4,90

C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ | 0,10
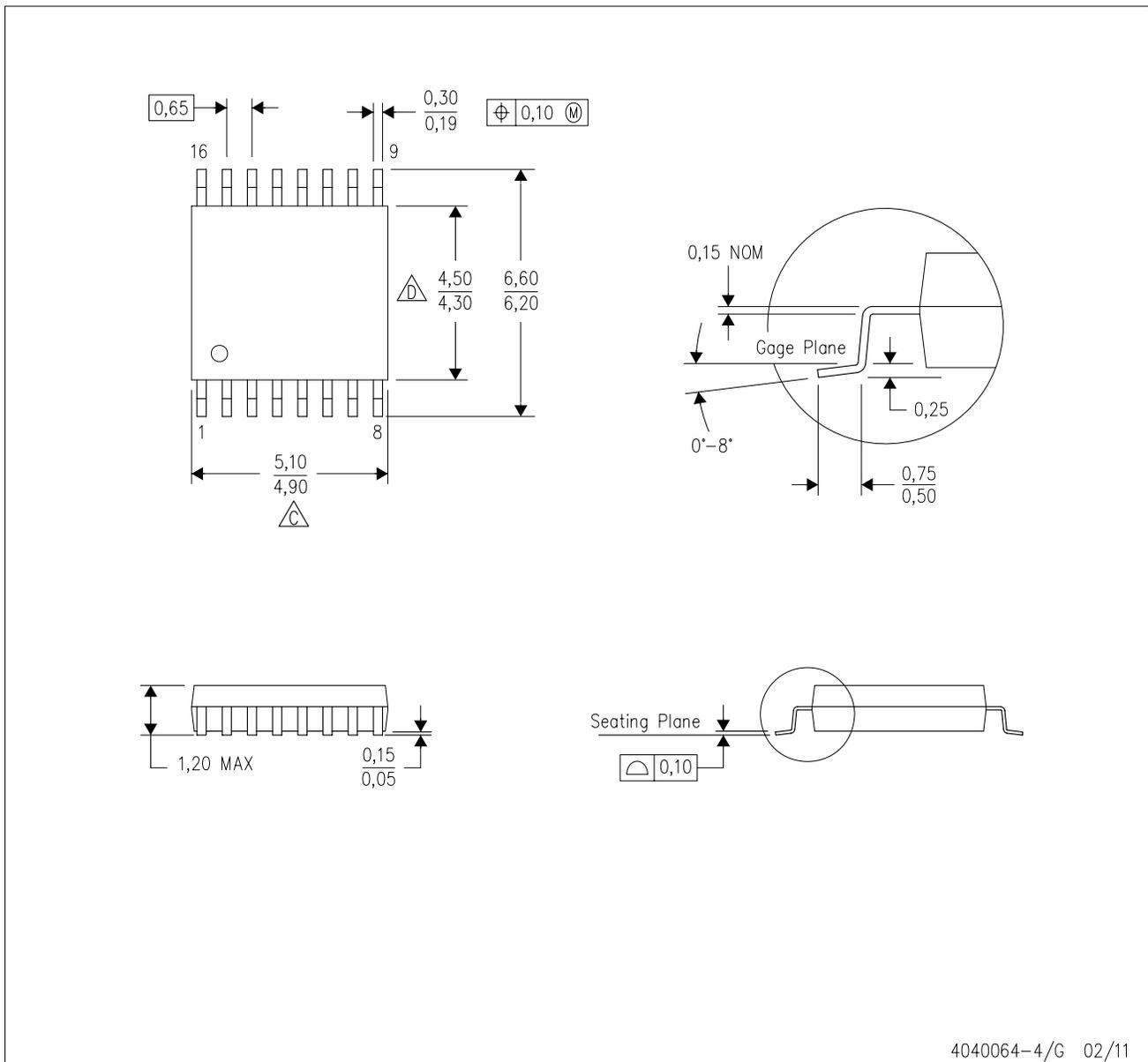
4040064−4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153
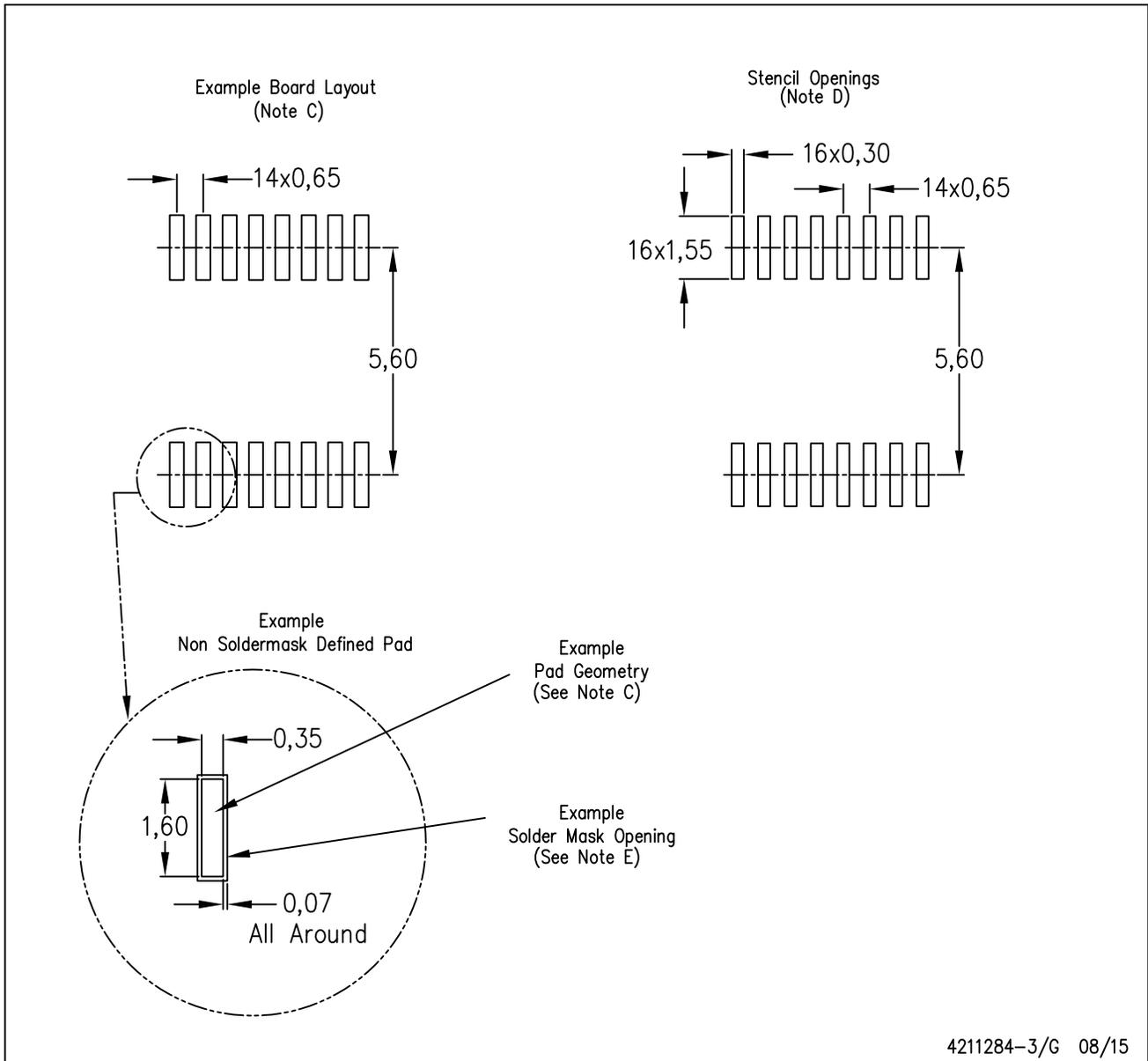
TEXAS
INSTRUMENTS
www.ti.com

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

14x0,65

5,60

Stencil Openings
(Note D)

16x0,30

14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

0,35

1,60

0,07
All Around

4211284−3/G 08/15

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
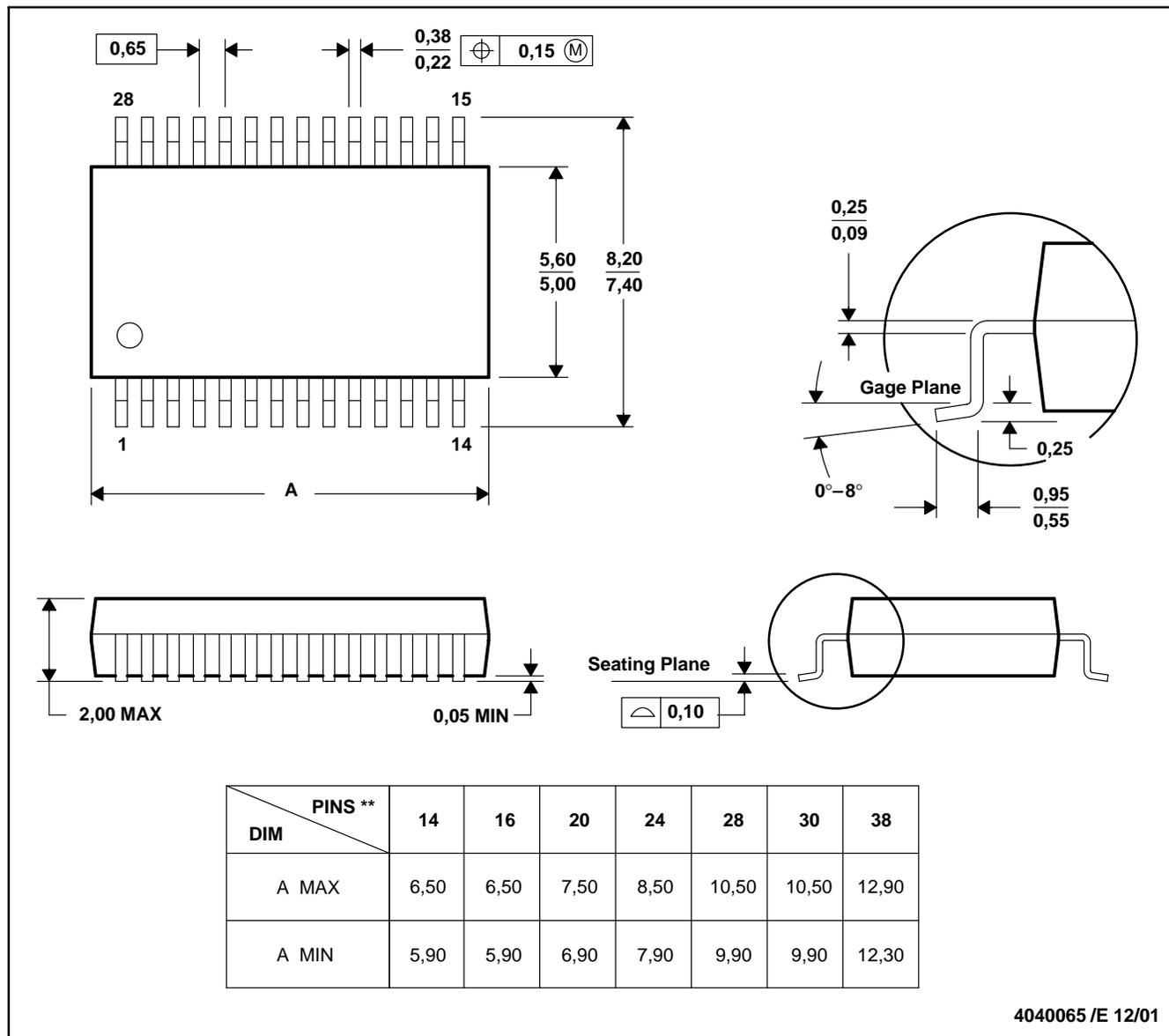
PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
               B. This drawing is subject to change without notice.
               C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
               D. Falls within JEDEC MO-150

RGY (R-PVQFN-N16)   PLASTIC QUAD FLATPACK NO-LEAD
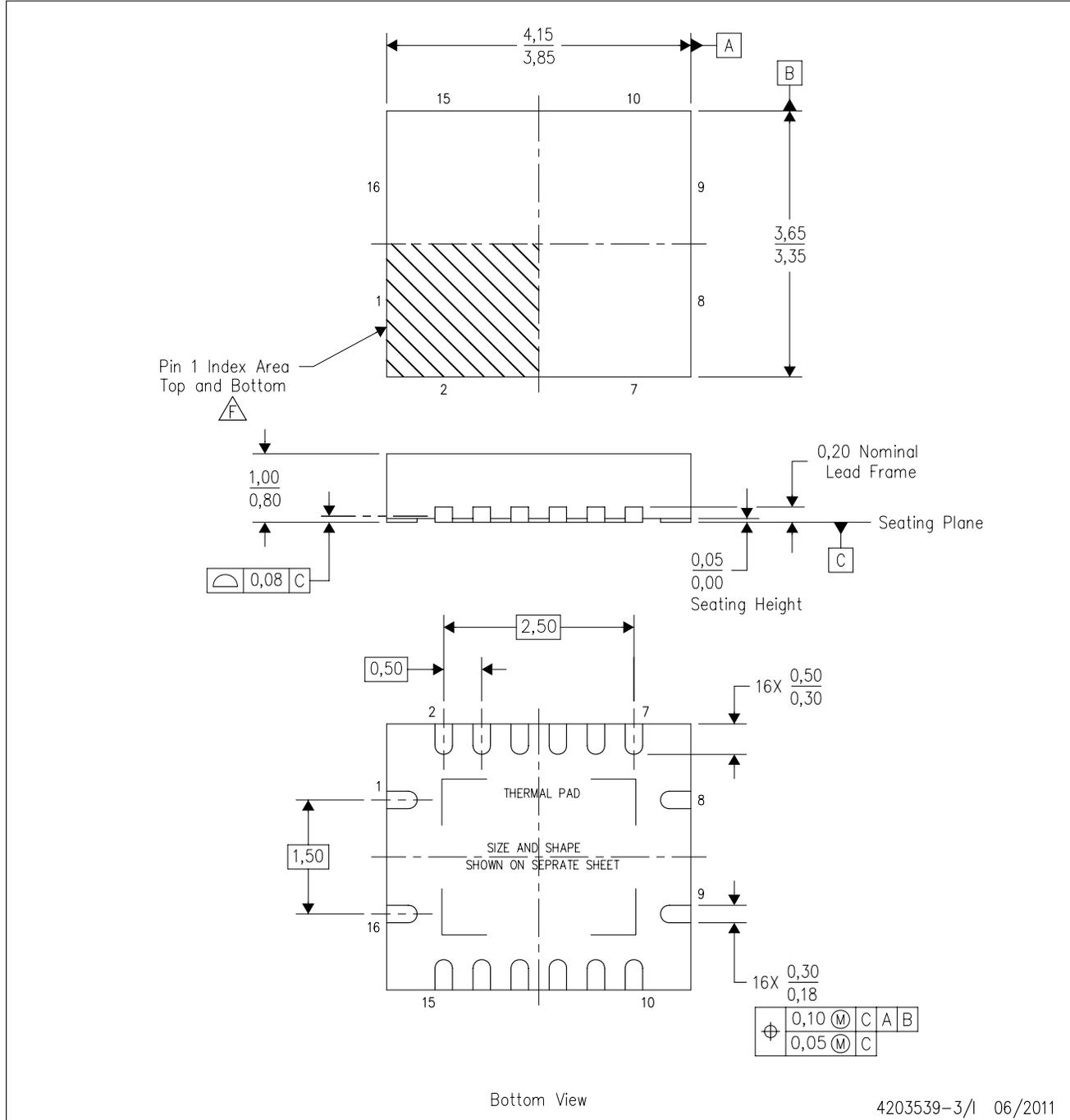
$\frac{4,15}{3,85}$ A

B

15   10

16   9

1   8

$\frac{3,65}{3,35}$

2   7

Pin 1 Index Area
Top and Bottom

F

$\frac{1,00}{0,80}$

0,20 Nominal
Lead Frame

Seating Plane

0,08   C

$\frac{0,05}{0,00}$
Seating Height

C

2,50

0,50

16X $\frac{0,50}{0,30}$

2   7

1   THERMAL PAD   8

1,50   SIZE AND SHAPE
         SHOWN ON SEPRATE SHEET

16   9

15   10

16X $\frac{0,30}{0,18}$

⊕ | 0,10 Ⓜ | C | A | B
  | 0,05 Ⓜ | C

Bottom View

4203539-3/I 06/2011

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No-Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
              The Pin 1 identifiers are either a molded, marked, or metal feature.
         G.   Package complies to JEDEC MO–241 variation BA.

RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad

2,05±0,10

2,55±0,10
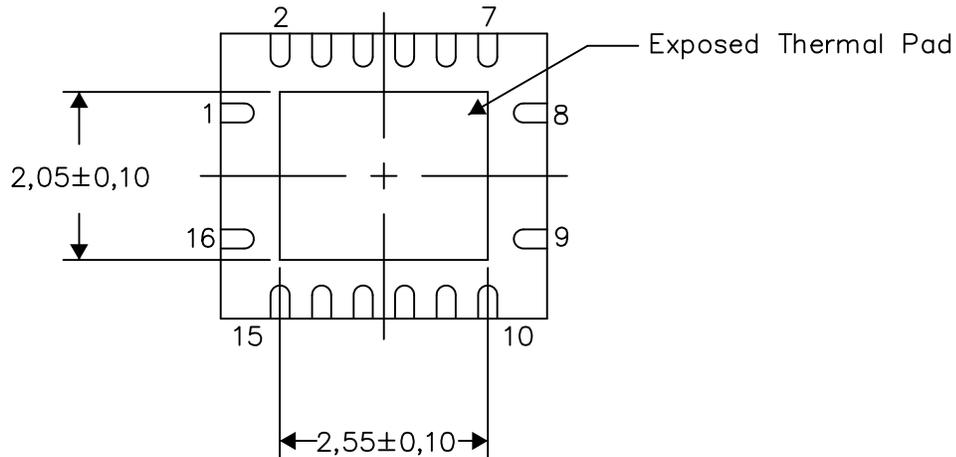
Bottom View

Exposed Thermal Pad Dimensions

4206353−3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R−PVQFN−N16)　　　PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

4,80
4,30
2,60
1,50
2,55
2,05
Note D
0,85 X 16 PL.
0,28 X 16 PL.
10x0,50

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,75
4,25
2,65
1,50
0,82
1,07
0,30 x 2 PL.
0,80 x 16 PL.
0,23 x 16 PL.
10x0,50

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

0,08
R0,14
0,85
0,28
0,07
All Around

Example
Solder Mask Opening
(Note F)

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00
1,00
6xØ0,3

4208122−3/P 03/14

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Publication IPC−7351 is recommended for alternate designs.
　　　　　D.　This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
　　　　　　　QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
　　　　　　　for specific thermal information, via requirements, and recommended board layout.
　　　　　　　These documents are available at www.ti.com <http://www.ti.com>.
　　　　　E.　Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
　　　　　　　contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
　　　　　F.　Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⟋C⟍

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟋D⟍

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
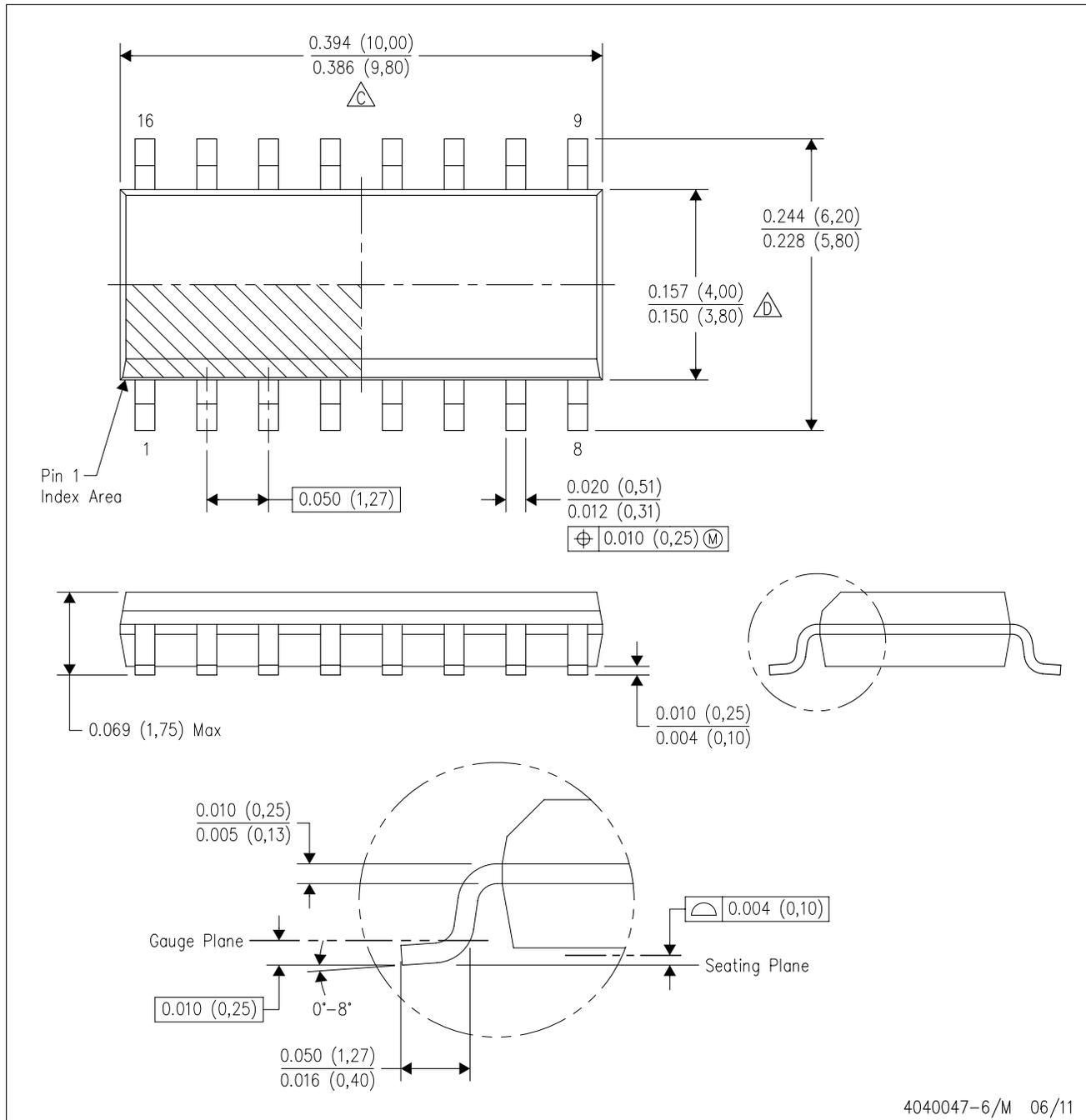
4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      ⟋C⟍ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
      ⟋D⟍ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.
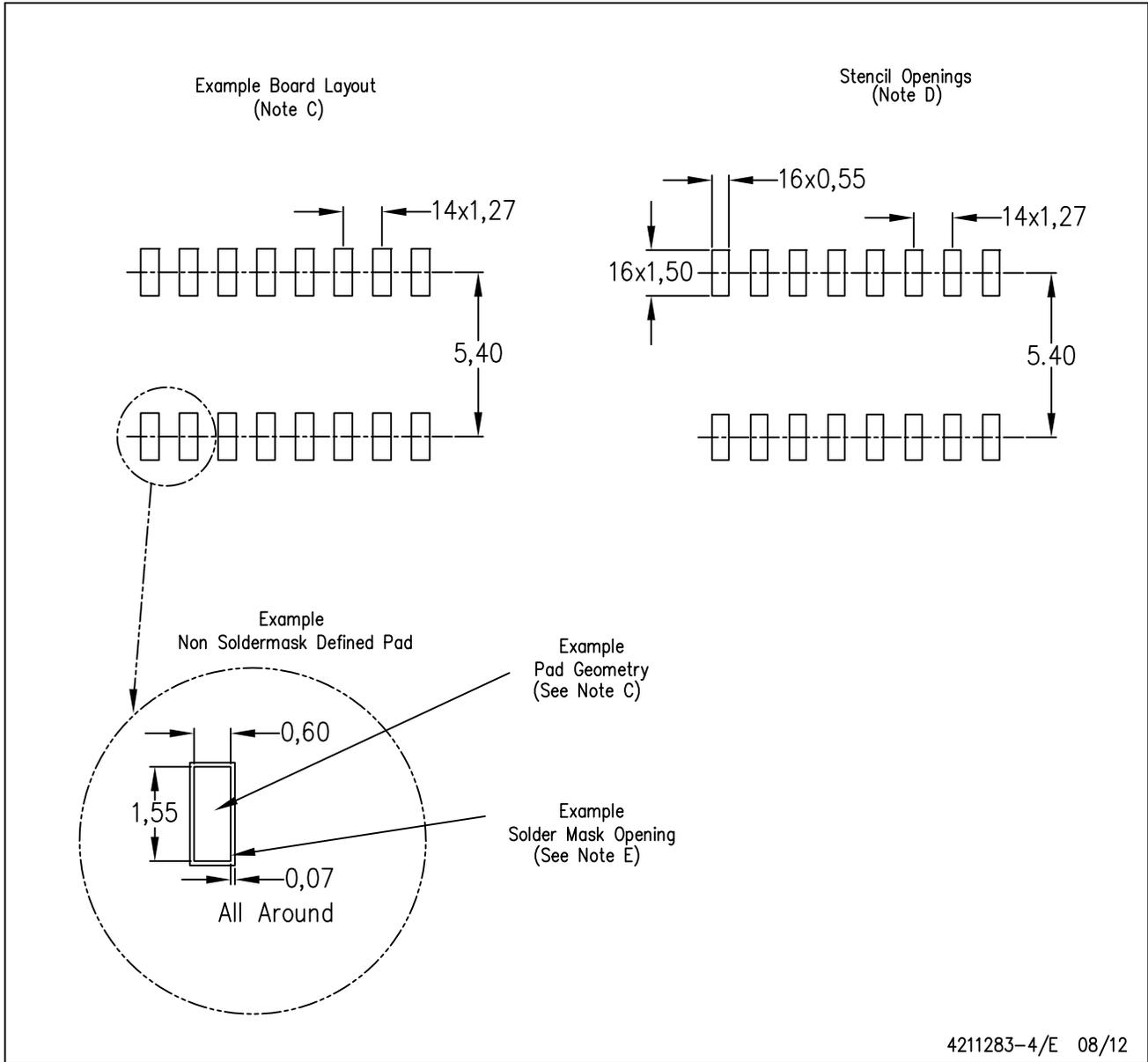
TEXAS INSTRUMENTS
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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

←―14x1,27

←―16x0,55

←――14x1,27

5,40

16x1,50―

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

―0,60

1,55

Example
Solder Mask Opening
(See Note E)

―0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA
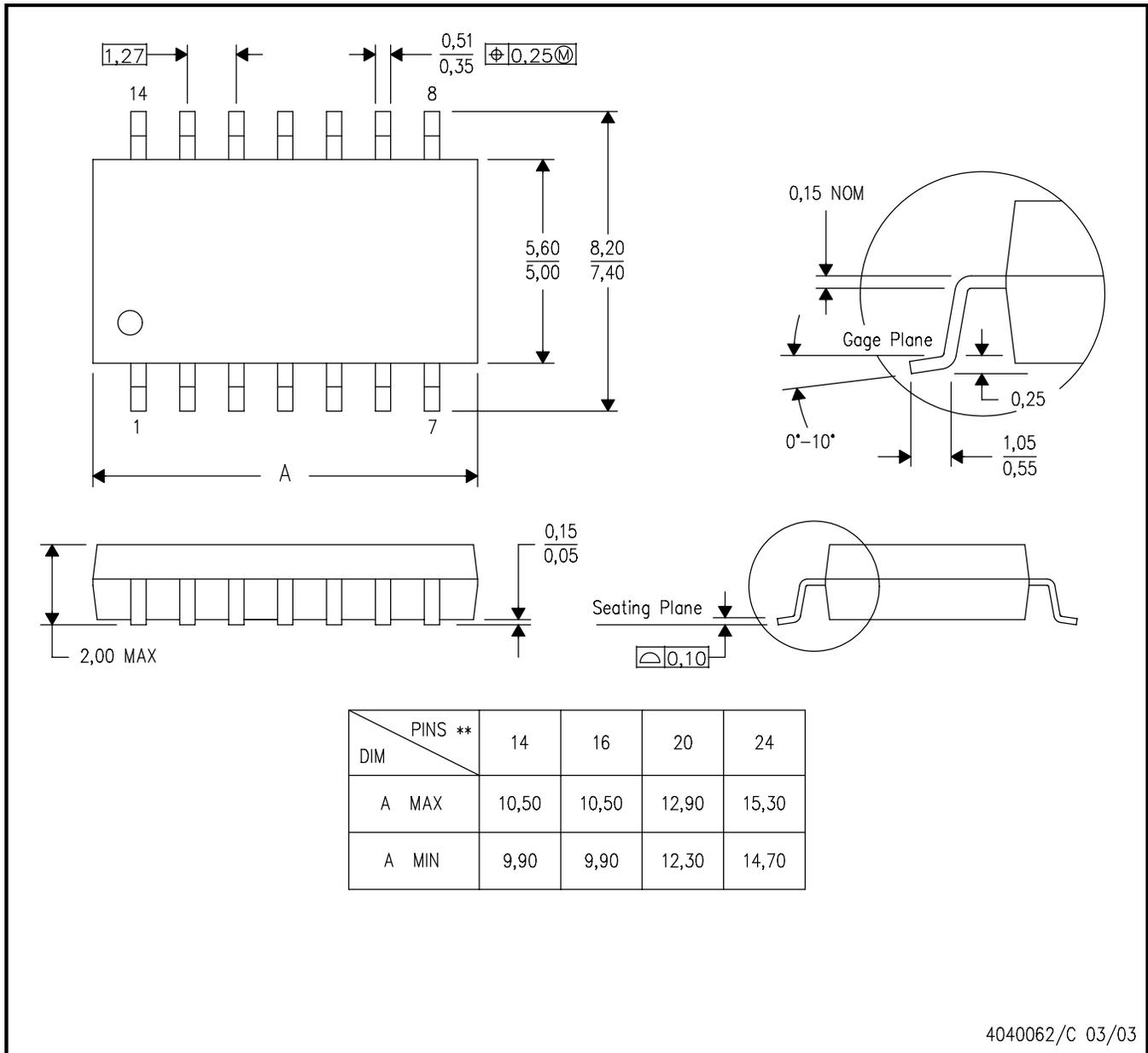
14-PINS SHOWN

2,00 MAX

Seating Plane

	PINS **	14	16	20	24
DIM					
A	MAX	10,50	10,50	12,90	15,30
A	MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		