3.8V TO 32V INPUT, 3.5A LOW IQ SYNCHRONOUS BUCK WITH ENHANCED EMI REDUCTION

Description

The AP63356/AP63357 is a 3.5A, synchronous buck converter with a wide input voltage range of 3.8V to 32V. The device fully integrates a 74mΩ high-side power MOSFET and a 40mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

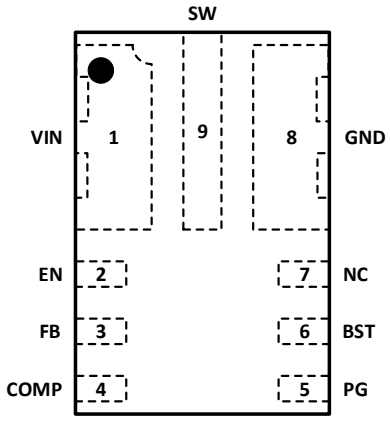
The AP63356/AP63357 device is easily used by minimizing the external component count due to its adoption of peak current mode control along with its integrated loop compensation network.

The AP63356/AP63357 design is optimized for Electromagnetic Interference (EMI) reduction. The device has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching. AP63356/AP63357 also features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The device is available in a 3mm × 2mm V-DFN3020-13 package.

Pin Assignments

Top View



V-DFN3020-13
(Type A)

Features

- VIN 3.8V to 32V
- 3.5A Continuous Output Current
- 0.8V ± 1% Reference Voltage
- 22μA Low Quiescent Current (Pulse Frequency Modulation)
- 450kHz Switching Frequency
- Pulse Width Modulation (PWM) Regardless of Output Load
  - AP63356
- Supports Pulse Frequency Modulation (PFM)
  - AP63357
  - Up to 86% Efficiency at 5mA Light Load
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Low-Dropout (LDO) Mode
- Power Good Indicator with 5MΩ Internal Pull-up
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Output Undervoltage Protection (UVP)
  - Cycle-by-Cycle Peak Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- 5V, 12V, and 24V Distributed Power Bus Supplies
- Flat Screen TV Sets and Monitors
- Power Tools and Laser Printers
- White Goods and Small Home Appliances
- FPGA, DSP, and ASIC Supplies
- Home Audio
- Network Systems
- Gaming Consoles
- Consumer Electronics
- General Purpose Point of Load

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

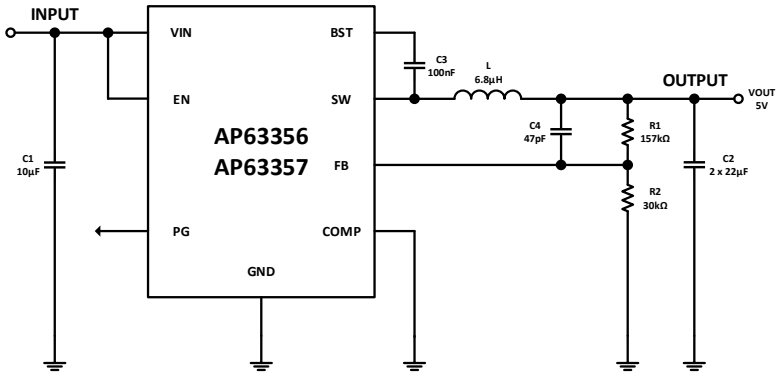


Figure 1. Typical Application Circuit

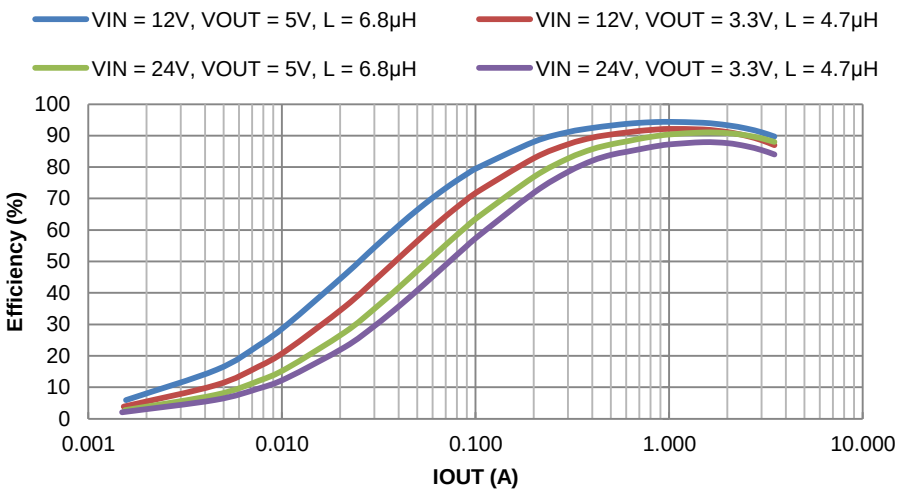


Figure 2. AP63356 Efficiency vs. Output Current

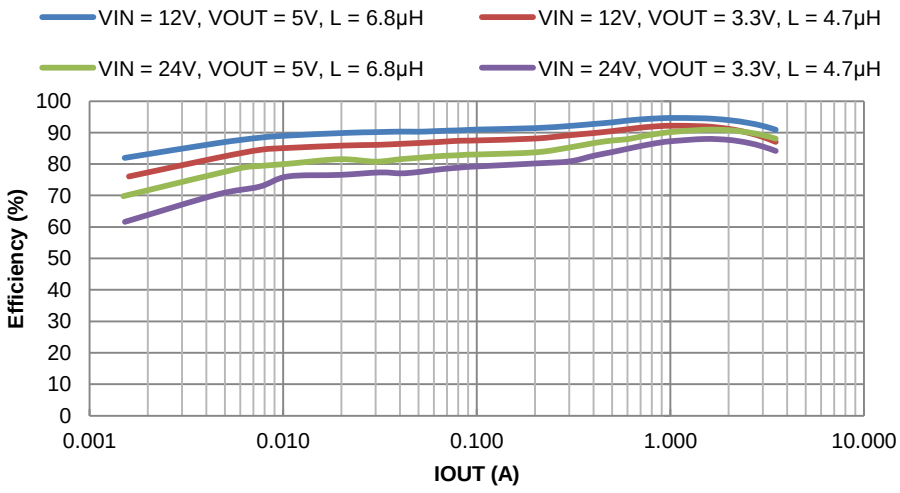


Figure 3. AP63357 Efficiency vs. Output Current

Pin Descriptions

Pin Name	Pin Number	Function
VIN	1	Power Input. VIN supplies the power to the IC as well as the step-down converter power MOSFETs. Drive VIN with a 3.8V to 32V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See **Input Capacitor** section for more details.
EN	2	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect to VIN or leave floating for automatic startup. The EN has a precision threshold of 1.18V for programing the UVLO. See **Enable** section for more details.
FB	3	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.
COMP	4	Compensation. Connect the COMP pin to GND to use internal loop compensation. Connect an external RC network to the COMP pin to adjust the loop response. See **External Loop Compensation Design** section for more details.
PG	5	Power-Good Pin. Open-drain power-good output with internal 5MΩ pull-up resistor that is pulled to GND when the output voltage is out of its regulation limits or during soft-start.
BST	6	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel power MOSFET. A 100nF capacitor is recommended from BST to SW to power the high-side driver.
NC	7	No Connect. There is no internal connection to this pin. The pin can be tied to any other pin or left floating.
GND	8	Power Ground.
SW	9	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.

Functional Block Diagram

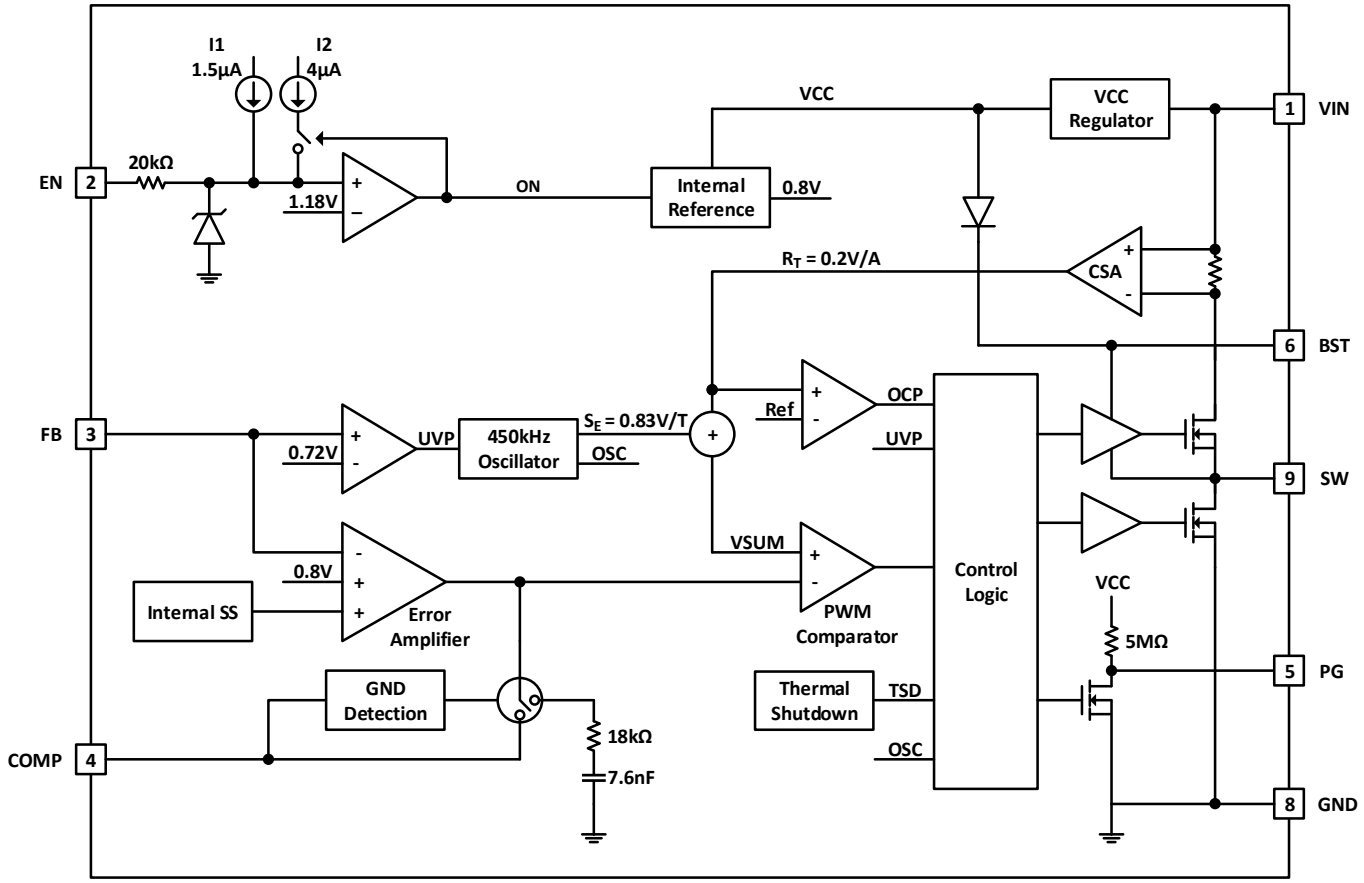


Figure 4. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (At T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +35.0 (DC)	V
		-0.3 to +40.0 (400ms)	
V_{EN}	Enable/UVLO Pin Voltage	-0.3 to +35.0	V
V_{FB}	Feedback Pin Voltage	-0.3 to +6.0	V
V_{COMP}	Compensation Pin Voltage	-0.3 to +6.0	V
V_{PG}	Power-Good Pin Voltage	-0.3 to +6.0	V
V_{BST}	Bootstrap Pin Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{SW}	Switch Pin Voltage	-0.3 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+170	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	2000	V
CDM	Charged Device Model	1000	V

Notes: 4. Stresses greater than the **Absolute Maximum Ratings** specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	V-DFN3020-13 (Type A)	25	°C/W
θ_{JC}	Junction to Case	V-DFN3020-13 (Type A)	5	°C/W

Note: 6. Test condition for V-DFN3020-13: Device mounted on FR-4 substrate, four-layer PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (At T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	3.8	32	V
VOUT	Output Voltage	0.8	31	V
T_A	Operating Ambient Temperature Range	-40	+85	°C
T_J	Operating Junction Temperature Range	-40	+125	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (At T_A = +25°C, VIN = 12V, unless otherwise specified. Min/Max limits apply across the recommended ambient temperature range, -40°C to +85°C, and input voltage range, 3.8V to 32V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V	—	1	3	μA
I_Q	Quiescent Supply Current	AP63356: V_{EN} = Floating, V_{FB} = 1.0V	—	258	—	μA
		AP63357: V_{EN} = Floating, V_{FB} = 1.0V	—	22	—	μA
UVLO	VIN Undervoltage Rising Threshold	—	3.3	3.5	3.6	V
	VIN Undervoltage Hysteresis	—	—	420	—	mV
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	74	—	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	40	—	mΩ
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 8)	—	4.0	5.0	6.0	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 8)	—	3.2	4.2	5.2	A
I_{PFMPK}	PFM Peak Current Limit	—	—	700	—	mA
I_{ZC}	Zero Cross Current Threshold	—	—	0	—	mA
f_{SW}	Oscillator Frequency	—	400	450	500	kHz
t_{ON_MIN}	Minimum On-Time	—	—	100	120	ns
V_{FB}	Feedback Voltage	CCM	0.792	0.800	0.808	V
V_{EN_H}	EN Logic High Threshold	—	1.15	1.18	1.21	V
V_{EN_L}	EN Logic Low Threshold	—	1.02	1.08	1.14	V
I_{EN}	EN Input Current	V_{EN} = 1.5V	—	5.5	—	μA
		V_{EN} = 1V	—	1.5	—	μA
t_{SS}	Soft-Start Time	—	—	4	—	ms
T_{SD}	Thermal Shutdown (Note 8)	—	—	170	—	°C
T_{Hys}	Thermal Shutdown Hysteresis (Note 8)	—	—	25	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP63356/AP63357 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.)

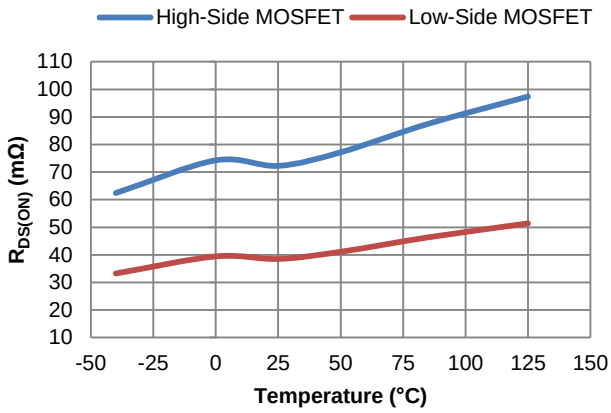


Figure 5. Power MOSFET $R_{DS(ON)}$ vs. Temperature

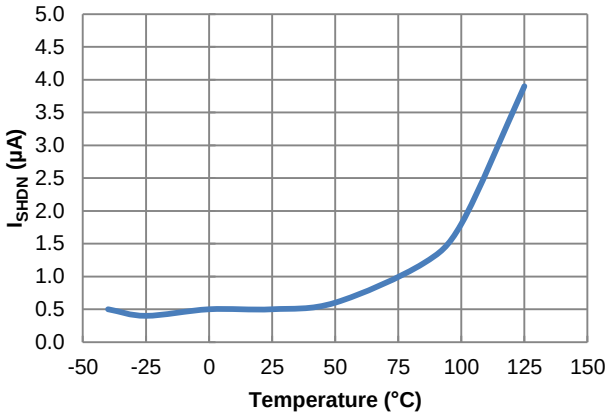


Figure 6. I_{SHDN} vs. Temperature

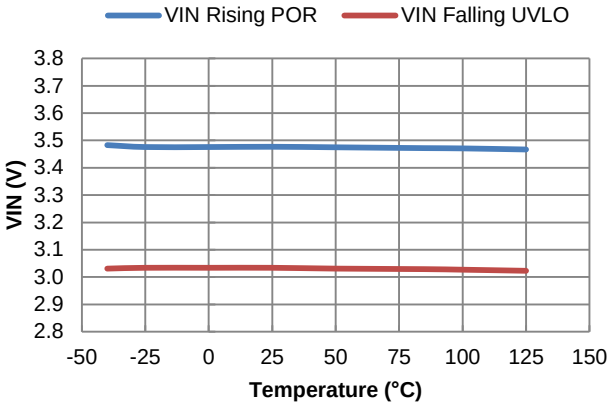


Figure 7. VIN Power-On Reset and UVLO vs. Temperature

Typical Performance Characteristics (AP63356/AP63357 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.) (continued)

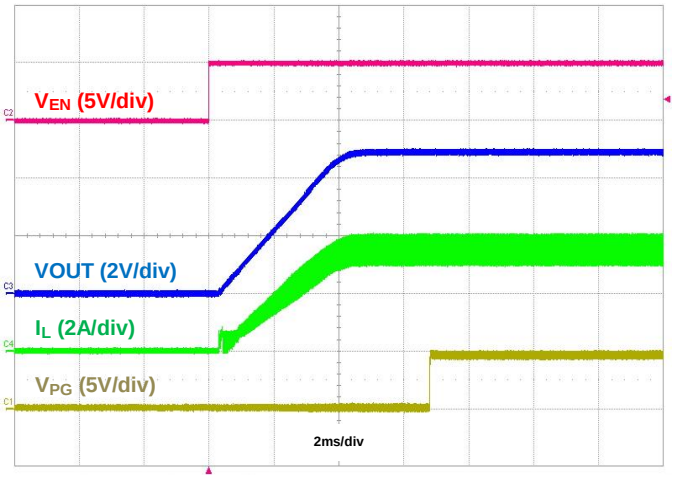


Figure 8. Startup Using EN, IOUT = 3.5A

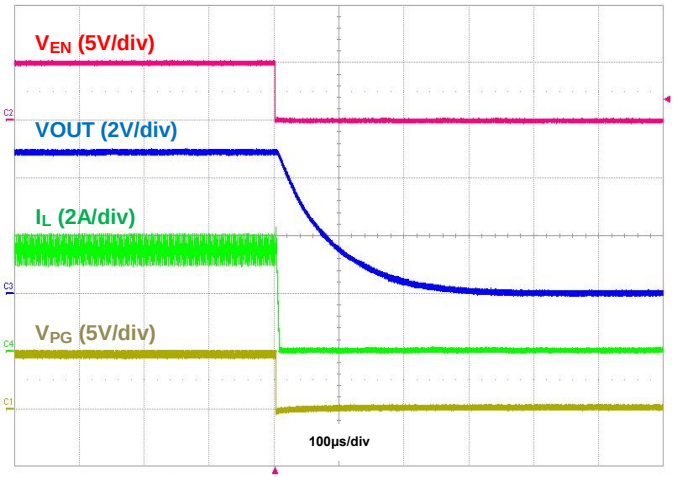


Figure 9. Shutdown Using EN, IOUT = 3.5A

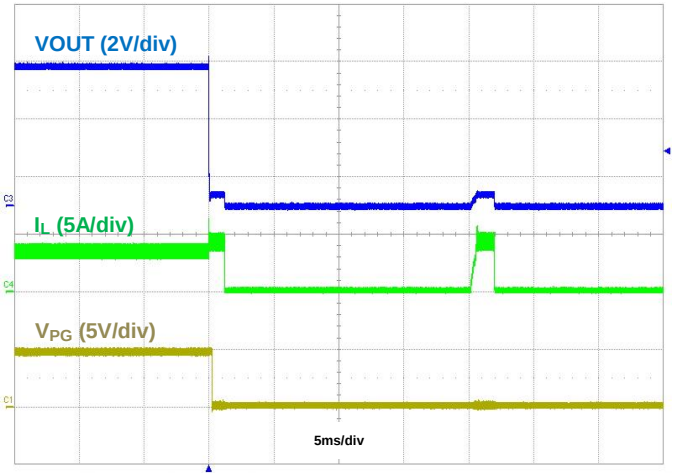


Figure 10. Output Short Protection, IOUT = 3.5A

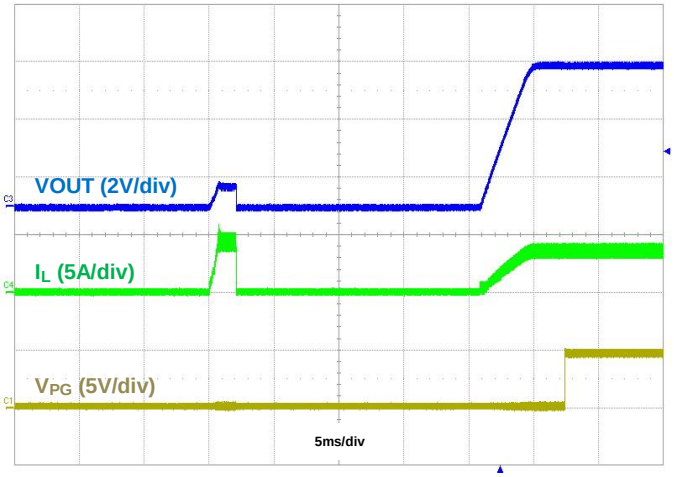


Figure 11. Output Short Recovery, IOUT = 3.5A

Typical Performance Characteristics (AP63356 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.)

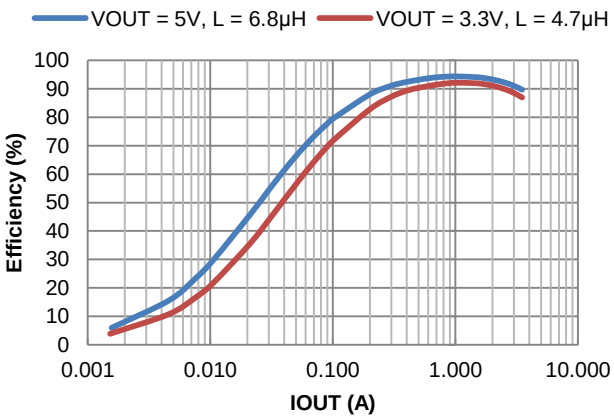


Figure 12. Efficiency vs. Output Current, VIN = 12V

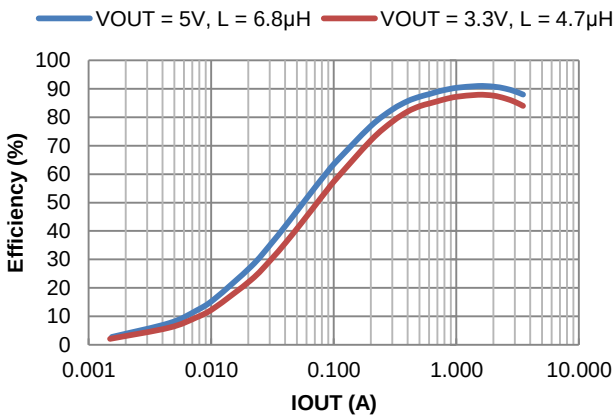


Figure 13. Efficiency vs. Output Current, VIN = 24V

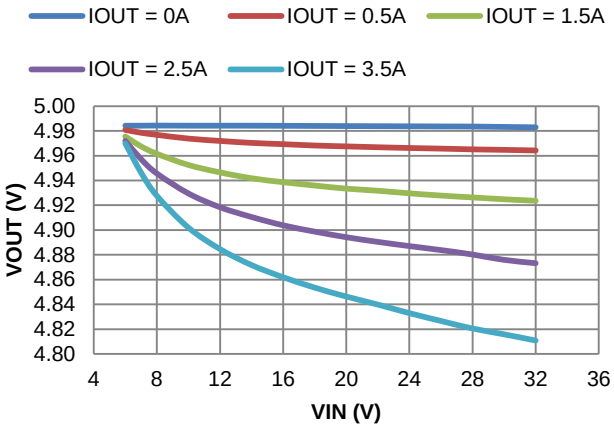


Figure 14. Line Regulation, VOUT = 5V

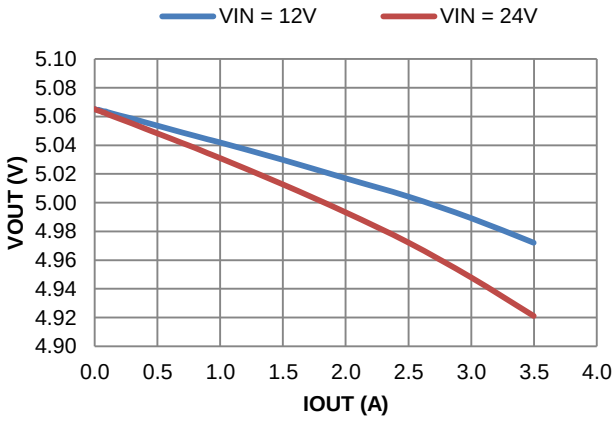


Figure 15. Load Regulation, VOUT = 5V

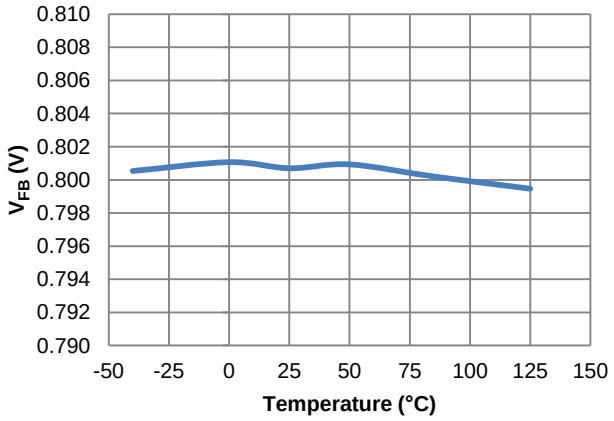


Figure 16. Feedback Voltage vs. Temperature

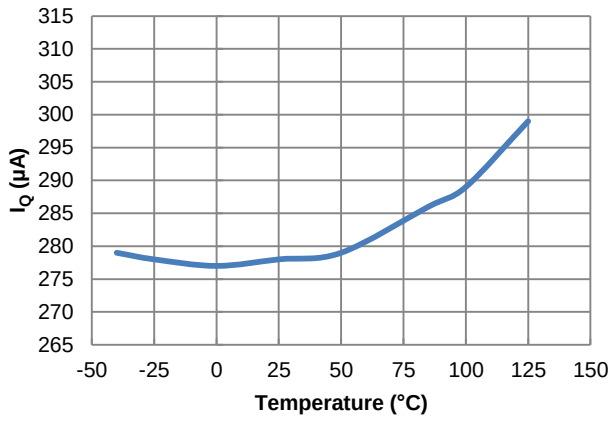


Figure 17. I_Q vs. Temperature

Typical Performance Characteristics (AP63356 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.) (continued)

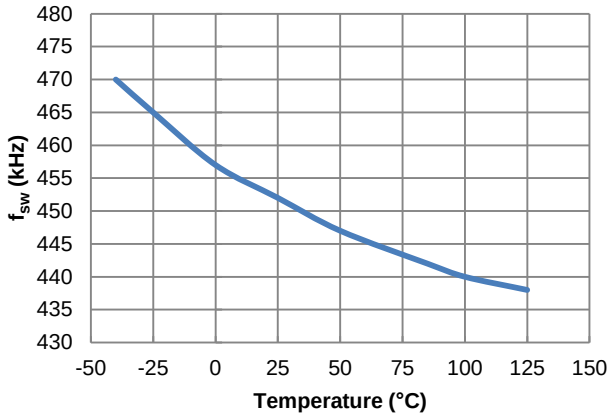


Figure 18. f_{sw} vs. Temperature, IOUT = 0A

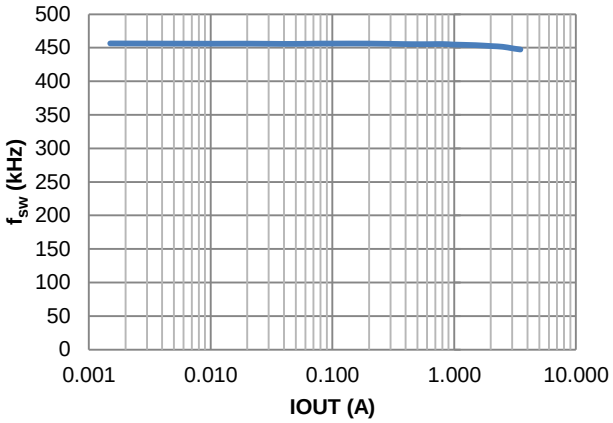


Figure 19. f_{sw} vs. Load

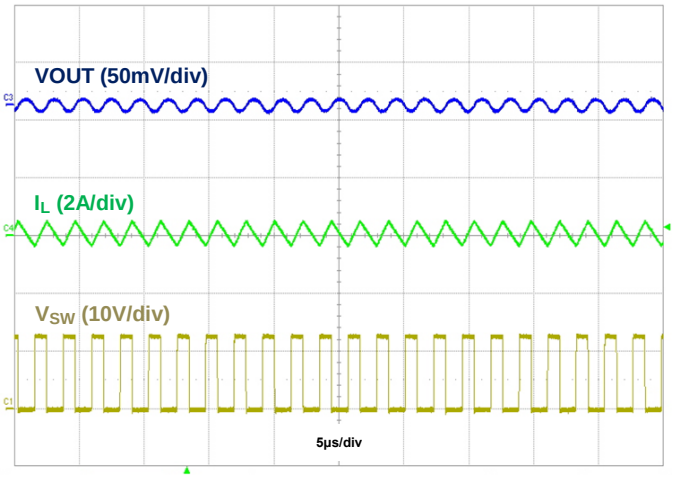


Figure 20. Output Voltage Ripple, IOUT = 50mA

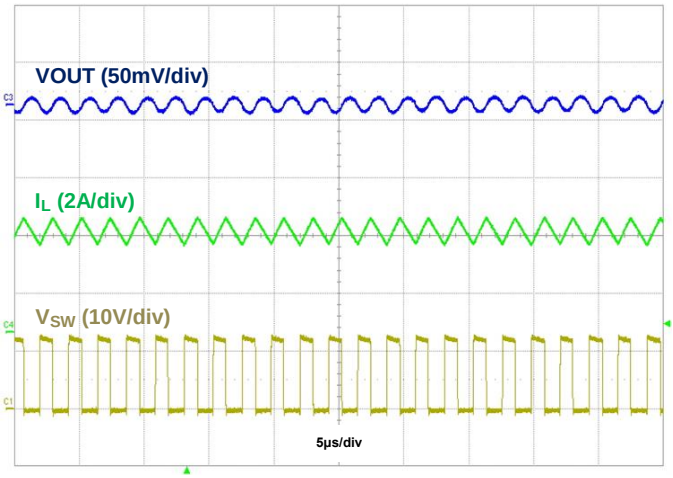


Figure 21. Output Voltage Ripple, IOUT = 3.5A

Typical Performance Characteristics (AP63356 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.) (cont.)

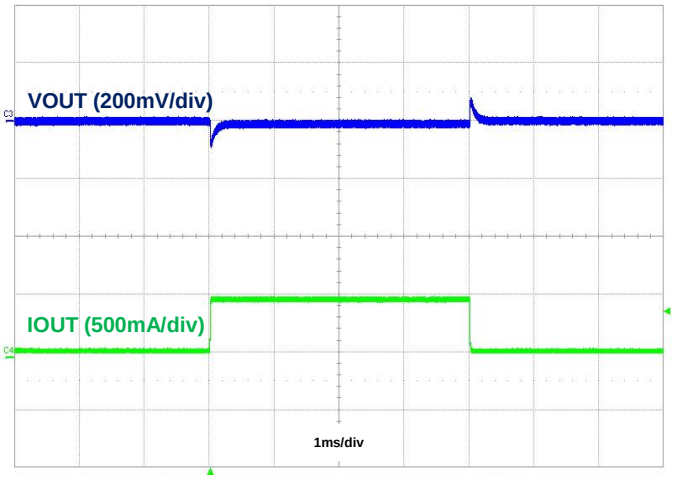


Figure 22. Load Transient, IOUT = 50mA to 500mA to 50mA

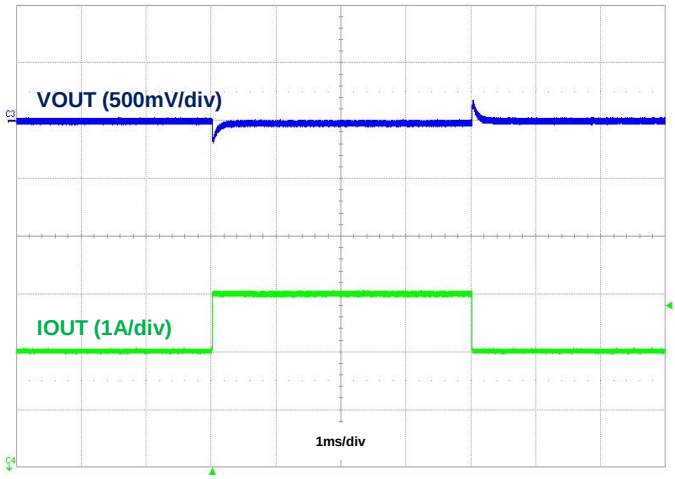


Figure 23. Load Transient, IOUT = 2.5A to 3.5A to 2.5A

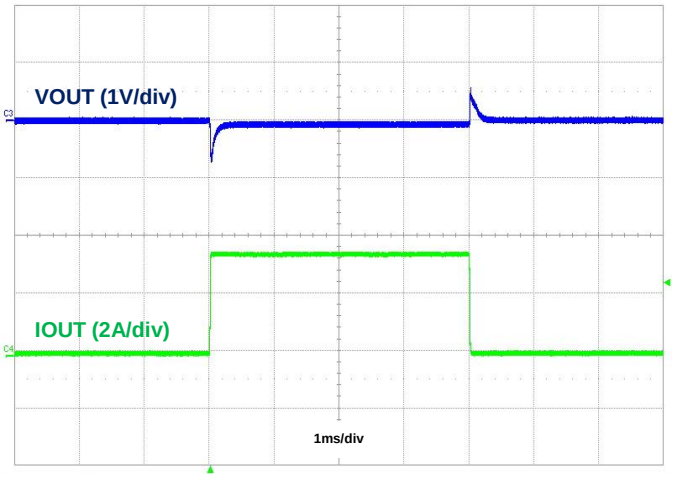


Figure 24. Load Transient, IOUT = 50mA to 3.5A to 50mA

Typical Performance Characteristics (AP63357 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.)

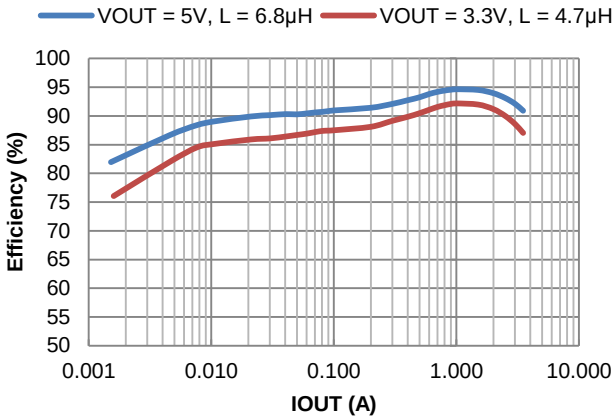


Figure 25. Efficiency vs. Output Current, VIN = 12V

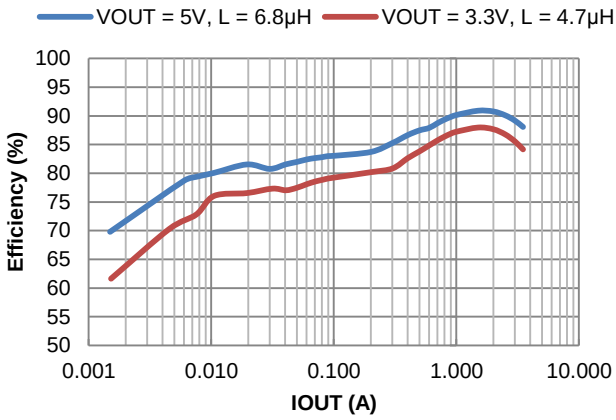


Figure 26. Efficiency vs. Output Current, VIN = 24V

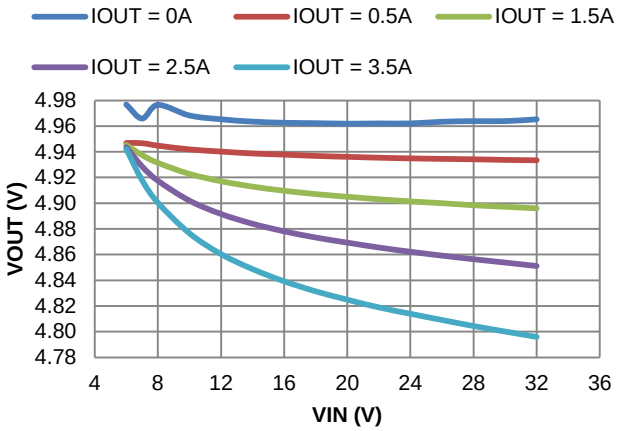


Figure 27. Line Regulation, VOUT = 5V

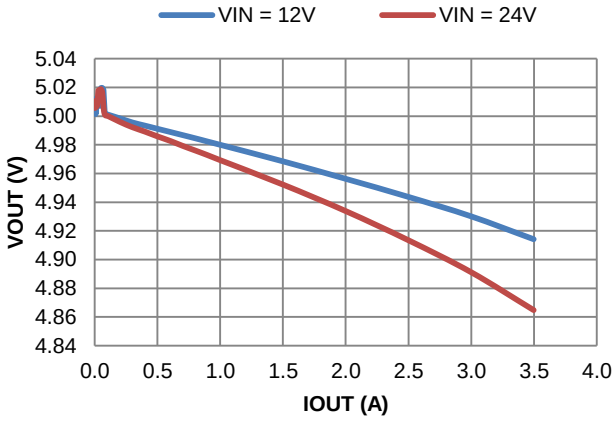


Figure 28. Load Regulation, VOUT = 5V

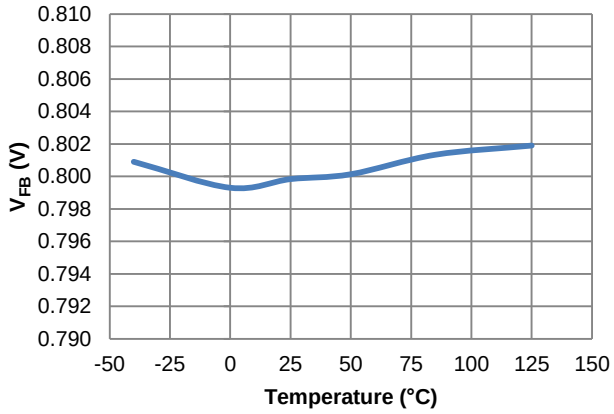


Figure 29. Feedback Voltage vs. Temperature

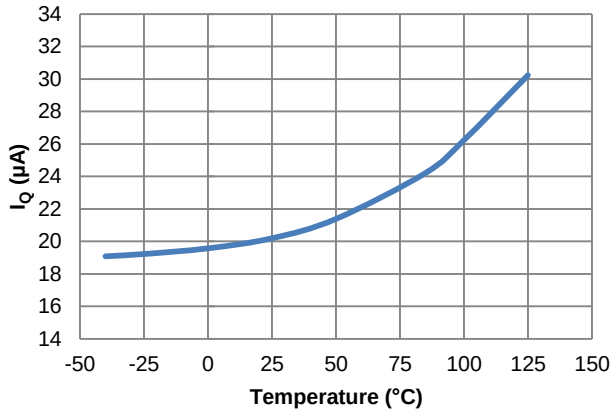


Figure 30. I_Q vs. Temperature

Typical Performance Characteristics (AP63357 at T_A = +25°C, VIN = 12V, VOUT = 5V, unless otherwise specified.) (continued)

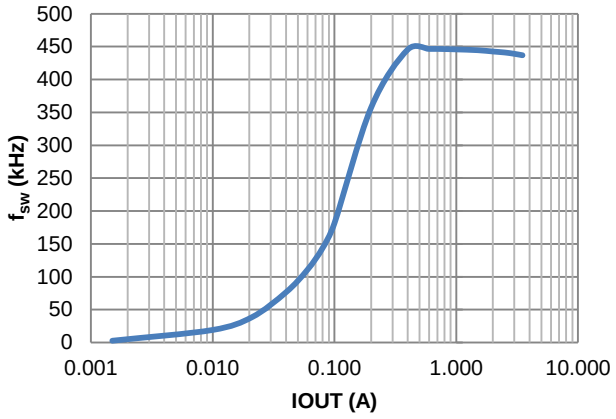


Figure 31. f_{sw} vs. Load

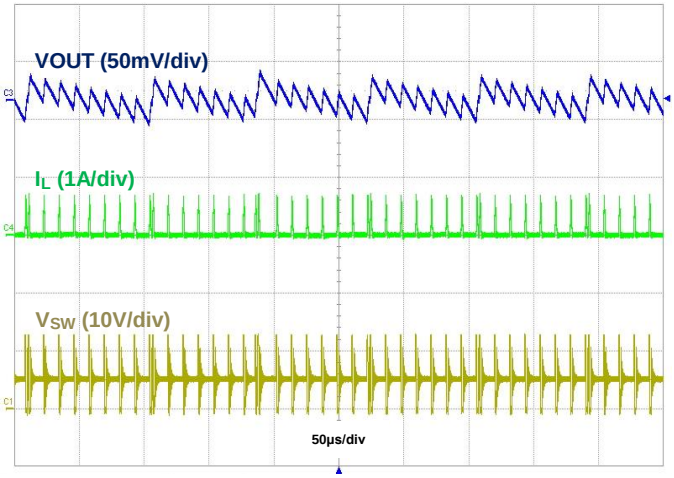


Figure 32. Output Voltage Ripple, IOUT = 50mA

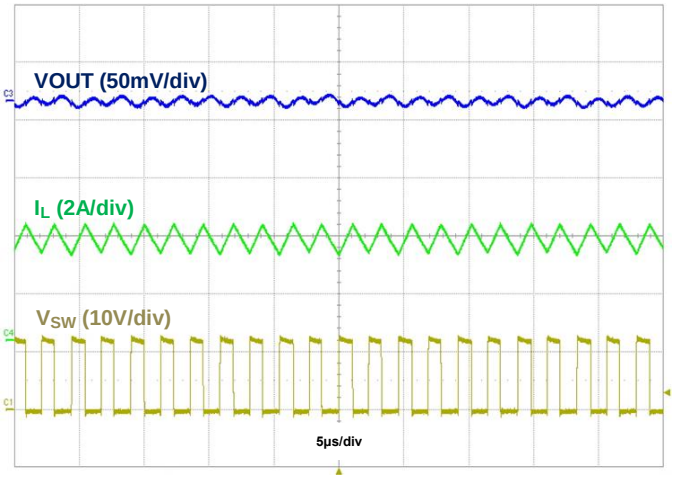


Figure 33. Output Voltage Ripple, IOUT = 3.5A

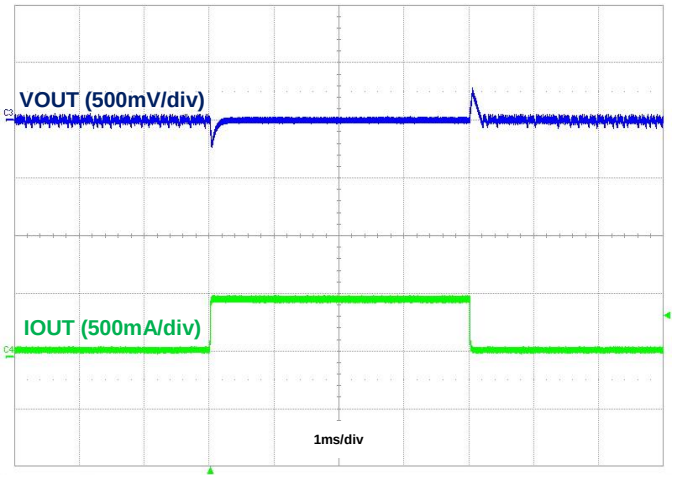


Figure 34. Load Transient, IOUT = 50mA to 500mA to 50mA

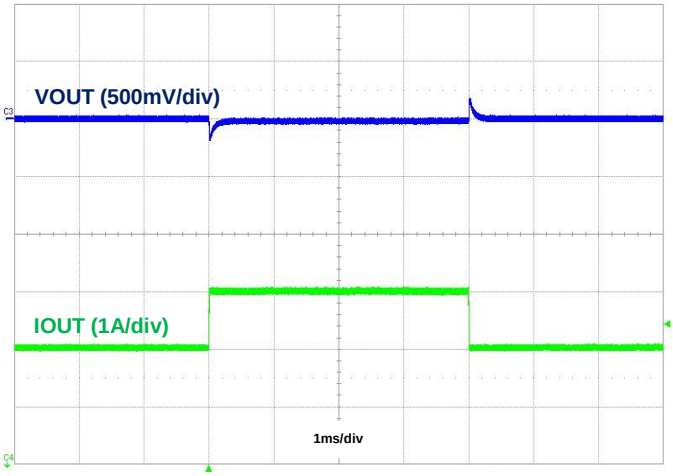


Figure 35. Load Transient, IOUT = 2.5A to 3.5A to 2.5A

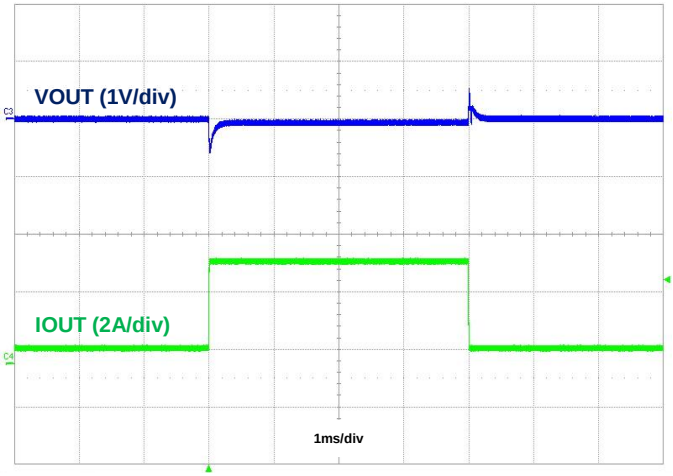


Figure 36. Load Transient, IOUT = 50mA to 3.5A to 50mA

Application Information

1 Pulse Width Modulation (PWM) Operation

The AP63356/AP63357 device is a 3.8V-to-32V input, 3.5A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 4. The device employs fixed-frequency peak current mode control. The internal 450kHz clock's rising edge initiates turning on the integrated high-side power MOSFET, Q1, for each cycle. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. The current across Q1 is sensed and converted to a voltage with a ratio of R_T via the CSA block. The CSA output is combined with an internal slope compensation, S_E, resulting in V_{SUM}. When V_{SUM} rises higher than the COMP node, the device turns off Q1 and turns on the low-side power MOSFET, Q2. The inductor current decreases when Q2 is on. On the rising edge of next clock cycle, Q2 turns off and Q1 turns on. This sequence repeats every clock cycle.

The error amplifier generates the COMP voltage by comparing the voltage on the FB pin with an internal 0.8V reference. An increase in load current causes the feedback voltage to drop. The error amplifier thus raises the COMP voltage until the average inductor current matches the increased load current. This feedback loop regulates the output voltage. The internal slope compensation circuitry prevents subharmonic oscillation when the duty cycle is greater than 50% for peak current mode control.

The peak current mode control, integrated loop compensation network, and built-in 4ms soft-start time simplify the AP63356/AP63357 footprint as well as minimizes the external component count.

In order to provide a small output ripple during light load conditions, the AP63356 operates in PWM regardless of output load.

2 Pulse Frequency Modulation (PFM) Operation

In heavy load conditions, the AP63357 operates in forced PWM mode. As the load current decreases, the internal COMP node voltage also decreases. At a certain limit, if the load current is low enough, the COMP node voltage is clamped and is prevented from decreasing any further. The voltage at which COMP is clamped corresponds to the 700mA PFM peak inductor current limit. As the load current approaches zero, the AP63357 enters PFM mode to increase the converter power efficiency at light load conditions. When the inductor current decreases to 0mA, zero cross detection circuitry on the low-side power MOSFET, Q2, forces it off. The buck converter does not sink current from the output when the output load is light and while the device is in PFM. Because the AP63357 works in PFM during light load conditions, it can achieve power efficiency of up to 86% at a 5mA load condition.

The quiescent current of AP63357 is 22μA typical under a no-load, non-switching condition.

3 Enable

When disabled, the device shutdown supply current is only 1μA. When applying a voltage greater than the EN logic high threshold (typical 1.18V, rising), the AP63356/AP63357 enables all functions and the device initiates the soft-start phase. The EN pin is a high-voltage pin and can be directly connected to VIN to automatically start up the device as VIN increases. An internal 1.5μA pull-up current source connected from the internal LDO-regulated VCC to the EN pin guarantees that if EN is left floating, the device still automatically enables once the voltage reaches the EN logic high threshold. The AP63356/AP63357 has a built-in 4ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic low threshold (typical 1.08V, falling), the internal SS voltage discharges to ground and device operation disables.

The EN pin can also be used to program the undervoltage lockout thresholds. See **Undervoltage Lockout (UVLO)** section for more details.

Alternatively, a small ceramic capacitor can be added from EN to GND. This delays the triggering of EN, which delays the startup of the output voltage. This is useful when sequencing multiple power rails to minimize input inrush current. The amount of capacitance is calculated by:

$$\mathbf{C_d[nF] = 1.27 \cdot t_d[ms]} \qquad \textbf{Eq. 1}$$

Where:

- C_d is the time delay capacitance in nF
- t_d is the delay time in ms

Application Information (continued)

4 Electromagnetic Interference (EMI) Reduction with Ringing-Free Switching Node and Frequency Spread Spectrum (FSS)

In some applications, the system must meet EMI standards. In relation to high frequency radiation EMI noise, the switching node's (SW's) ringing amplitude is especially critical. To dampen high frequency radiated EMI noise, the AP63356/AP63357 device implements a proprietary, multi-level gate driver scheme that achieves a ringing-free switching node without sacrificing the switching node's rise and fall slew rates as well as the converter's power efficiency.

To further improve EMI reduction, the AP663356/AP63357 device also implements FSS with a switching frequency jitter of ±6%. FSS reduces conducted and radiated interference at a particular frequency by spreading the switching noise over a wider frequency band and by not allowing emitted energy to stay in any one frequency for a significant period of time.

5 Adjusting Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP63356/AP63357 device has a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP63356/AP63357 disables if the input voltage falls below 3.08V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

Some applications may desire higher VIN UVLO threshold voltages than is provided by the default setup. A 4µA hysteresis pull-up current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO threshold voltages as shown in Figure 37.

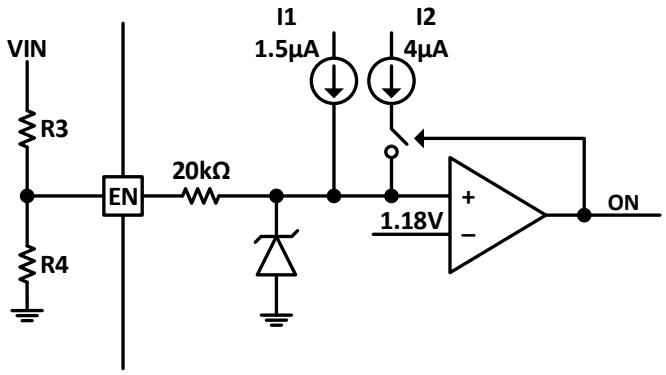


Figure 37. Programming UVLO

The resistive divider resistor values are calculated by:

$$R3 = \frac{0.915 \cdot V_{ON} - V_{OFF}}{4.127\mu A} \quad \text{Eq. 2}$$

$$R4 = \frac{1.08 \cdot R3}{V_{OFF} - 1.08V + 5.5\mu A \cdot R3} \quad \text{Eq. 3}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 3.6V
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 3.18V

6 Power-Good (PG) Indicator and Output Undervoltage Protection (UVP)

The PG pin of AP63356/AP63357 is an open-drain output that is actively held low during the soft-start period until the output voltage reaches 90% of its target value. If the output voltage decreases below its target value by 10%, UVP triggers and PG pulls low until the output returns to its set value. The PG rising edge transition is delayed by 3.5ms while the PG falling edge is delayed by 220µs to prevent false triggering.

Application Information (cont.)

7 Overcurrent Protection (OCP)

The AP63356/AP63357 has cycle-by-cycle peak current limit protection by sensing the current through the internal high-side power MOSFET, Q1. While Q1 is on, the internal sensing circuitry monitors its conduction current. Once the current through Q1 exceeds the peak current limit, Q1 immediately turns off. If Q1 consistently hits the peak current limit for 512 cycles, the buck converter enters hiccup mode and shuts down. After 8192 cycles of down time, the buck converter restarts powering up. Hiccup mode reduces the power dissipation in the overcurrent condition.

8 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of 170°C, the AP63356/AP63357 shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (145°C typical), the device initiates a normal power-up cycle with soft-start.

9 Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$T_{RISE} = PD \cdot (\theta_{JA}) \quad \text{Eq. 4}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE} \quad \text{Eq. 5}$$

Where:

- T_A is the ambient temperature of the environment

For the V-DFN3020-13 package, the θ_{JA} is 25°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of 125°C when considering the thermal design. Figure 38 shows a typical derating curve versus ambient temperature.

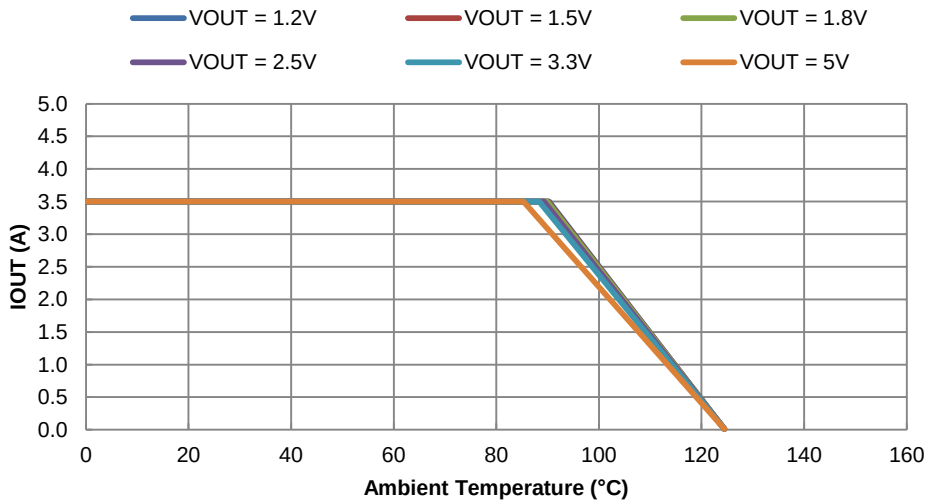


Figure 38. Output Current Derating Curve vs. Ambient Temperature, VIN = 12V

Application Information (cont.)

10 Setting the Output Voltage

The AP63356/AP63357 has adjustable output voltages starting from 0.8V using an external resistive divider. An optional external capacitor, C4 in Figure 1, of 10pF to 220pF improves the transient response. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R1 can be determined by the following equation:

$$\mathbf{R1 = R2 \cdot \left(\frac{VOUT}{0.8V} - 1\right)} \qquad \textbf{Eq. 6}$$

Table 1 shows a list of recommended component selections for common AP63356/AP63357 output voltages referencing Figure 39 using internal compensation.

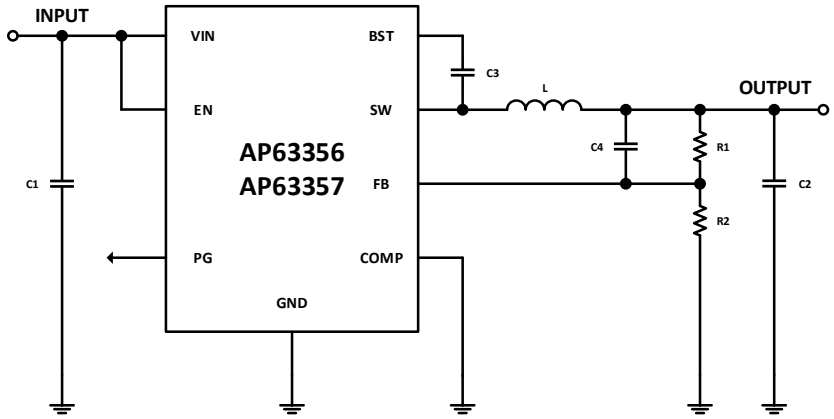


Figure 39. Typical Application Circuit Using Internal Compensation

Table 1. Recommended Components Selections Using Internal Compensation

AP63356/AP63357							
Output Voltage (V)	**R1 (kΩ)**	**R2 (kΩ)**	**L (μH)**	**C1 (μF)**	**C2 (μF)**	**C3 (nF)**	**C4 (pF)**
1.2	15	30	2.2	10	3 x 22	100	OPEN
1.5	27	30	2.2	10	2 x 22	100	OPEN
1.8	39	30	2.2	10	2 x 22	100	OPEN
2.5	62	30	3.3	10	2 x 22	100	27
3.3	91	30	4.7	10	2 x 22	100	33
5.0	157	30	6.8	10	2 x 22	100	47
12.0	422	30	10.0	10	4 x 22	100	OPEN

Application Information (cont.)

10 Setting the Output Voltage (continued)

Table 2 shows a list of recommended component selections for common AP63356/AP63357 output voltages referencing Figure 40 using external compensation.

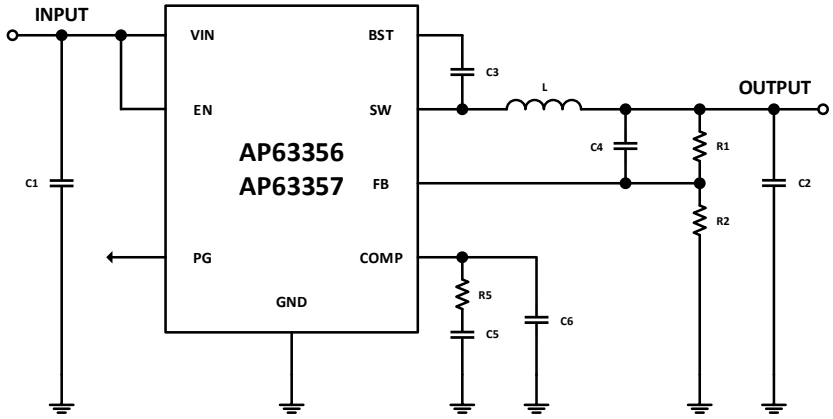


Figure 40. Typical Application Circuit Using External Compensation

Table 2. Recommended Components Selections Using External Compensation

AP63356/AP63357										
Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C1 (µF)	C2 (µF)	C3 (nF)	C4 (pF)	R5 (kΩ)	C5 (nF)	C6 (pF)
2.5	62	30	3.3	10	2 x 22	100	OPEN	27	3.9	OPEN
3.3	91	30	4.7	10	3 x 22	100	OPEN	27	3.3	OPEN
5.0	157	30	6.8	10	3 x 22	100	OPEN	38	3.3	OPEN
12.0	422	30	10.0	10	4 x 22	100	OPEN	47	6.8	OPEN

11 Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{sw}}} \quad \textbf{Eq. 7}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the buck converter switching frequency

For AP63356/AP63357, choose ΔI_L to be 30% to 50% of the maximum load current of 3.5A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}} = I_{LOAD} + \frac{\Delta I_L}{2}} \quad \textbf{Eq. 8}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 2.2µH to 10µH with a DC current rating of at least 35% higher than the maximum load current. For highest efficiency, the inductor's DC resistance should be less than 30mΩ. Use a larger inductance for improved efficiency under light load conditions.

Application Information (cont.)

12 Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large dI/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor greater than 10µF is sufficient for most applications.

13 Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and enters 100% duty cycle to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and sets the on-time to minimum to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{sw}} \cdot \mathbf{COUT}} \right) \quad \textbf{Eq. 9}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 22µF to 68µF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})} \right) \quad \textbf{Eq. 10}$$

Where:

- I_{Trans} is the load transient
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage

14 Bootstrap Capacitor and Low-Dropout (LDO) Operation

To ensure proper operation, a ceramic capacitor must be connected between the BST and SW pins. A 100nF ceramic capacitor is sufficient. If the bootstrap capacitor voltage falls below 2.3V, the boot undervoltage protection circuit turns Q2 on for 220ns to refresh the bootstrap capacitor and raise its voltage back above 2.85V. The bootstrap capacitor threshold voltage is always maintained to ensure enough driving capability for Q1. This operation may arise during long periods of no switching such as in PFM with light load conditions. Another event that requires the refreshing of the bootstrap capacitor is when the input voltage drops close to the output voltage. Under this condition, the regulator enters low-dropout mode by holding Q1 on for multiple clock cycles. To prevent the bootstrap capacitor from discharging, Q2 is forced to refresh. The effective duty cycle is approximately 100% so that it acts as an LDO to maintain the output voltage regulation.

Application Information (cont.)

15 External Loop Compensation Design

When the COMP pin is not connected to GND, the COMP pin is active for external loop compensation. The regulator uses a constant frequency, peak current mode control architecture to achieve a fast loop response. The inductor is not considered as a state variable since its peak current is constant. Thus, the system becomes a single-order system. For loop stabilization, it is simpler to design a Type II compensator for current mode control than it is to design a Type III compensator for voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 41 shows the small signal model of the synchronous buck regulator.

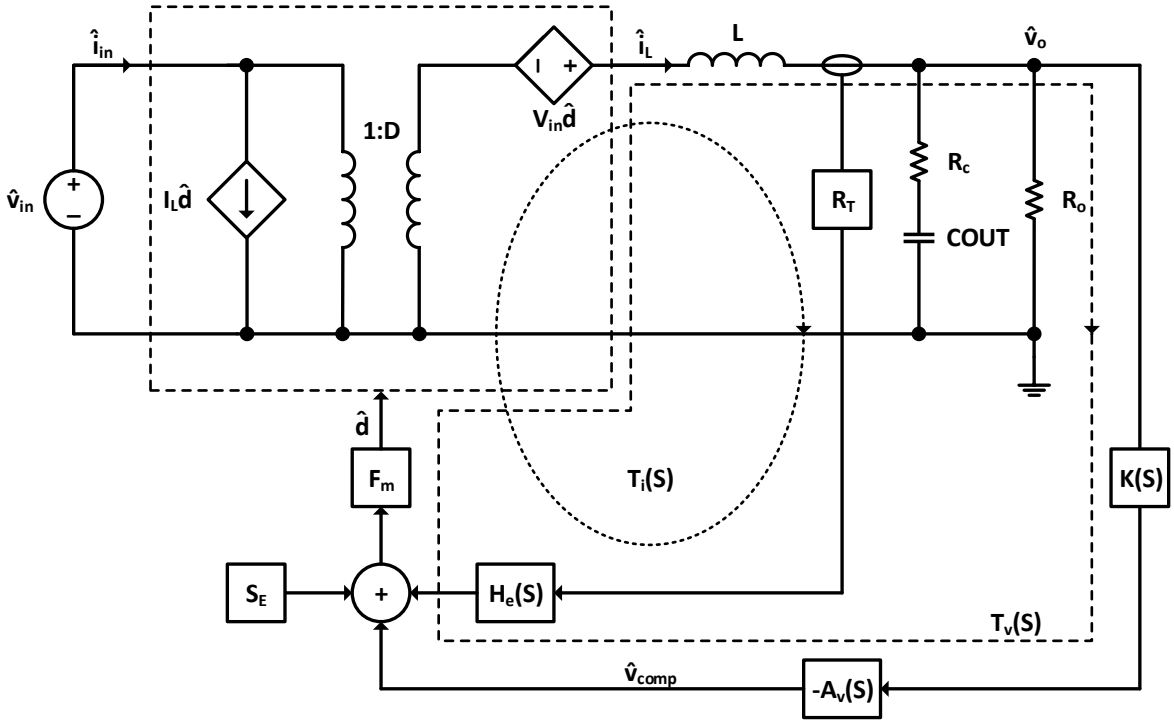


Figure 41. Small Signal Model of Buck Regulator

Where:

- $T_v(S)$ is the voltage loop
- $T_i(S)$ is the current loop
- K(S) is the voltage sense gain
- $-A_v(S)$ is the feedback compensation gain
- $H_e(S)$ is the current sampling function
- F_m is the PWM comparator gain
- V_{in} is the DC input voltage
- D is the duty cycle
- R_c is the ESR of the output capacitor, COUT
- R_o is the output load resistance
- $\hat{v}_{in}$ is the AC small-signal input voltage
- $\hat{i}_{in}$ is the AC small-signal input current
- $\hat{d}$ is the modulation of the duty cycle
- $\hat{i}_L$ is the AC small signal of the inductor current
- $\hat{v}_o$ is the AC small signal of output voltage
- $\hat{v}_{comp}$ is the AC small signal voltage of the compensation network

Application Information (cont.)

15 External Loop Compensation Design (continued)

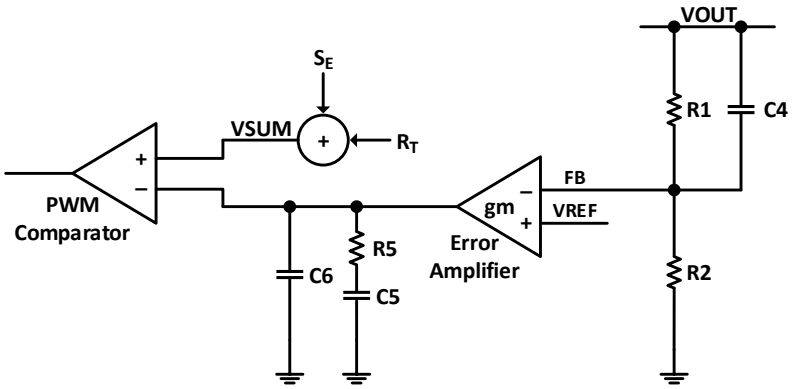


Figure 42. Type II Compensator

Figure 42 shows a Type II compensator. Its transfer function is expressed in the following equation:

$$\mathbf{A_v(S) \cdot K(S) = \frac{gm \cdot R5}{S \cdot (C5 + C6) \cdot (R1 + R2)} \frac{\left(1 + \frac{S}{\omega_{z1}}\right)\left(1 + \frac{S}{\omega_{z2}}\right)}{\left(1 + \frac{S}{\omega_{p1}}\right)\left(1 + \frac{S}{\omega_{p2}}\right)}} \quad \textbf{Eq. 11}$$

Where the poles and zeroes are:

$$\mathbf{\omega_{z1} = \frac{1}{R5 \cdot C5}} \quad \textbf{Eq. 12}$$

$$\mathbf{\omega_{z2} = \frac{1}{R1 \cdot C4}} \quad \textbf{Eq. 13}$$

$$\mathbf{\omega_{p1} = \frac{C5 + C6}{R5 \cdot C5 \cdot C6}} \quad \textbf{Eq. 14}$$

$$\mathbf{\omega_{p2} = \frac{R1 + R2}{R1 \cdot R2 \cdot C4}} \quad \textbf{Eq. 15}$$

The goal of loop compensation design is to achieve:

- High DC Gain
- Gain Margin less than -10dB
- Phase Margin greater than 45°
- Loop Bandwidth Crossover Frequency (f_c) less than 10% of f_{sw}

Application Information (cont.)

15 External Loop Compensation Design (cont.)

The loop gain at the crossover frequency has unity gain. Therefore, the compensator resistance, R5, is determined by:

$$R5 = \frac{2\pi \cdot f_c \cdot VOUT \cdot COUT \cdot R_T}{g_m \cdot V_{FB}} = 5.2x10^3[\frac{\Omega}{A}] \cdot f_c \cdot VOUT \cdot COUT \quad \text{Eq. 16}$$

Where:

- g_m is 0.3mS
- R_T is 0.2V/A
- V_{FB} is 0.8V
- f_c is the desired crossover frequency

Be aware that most ceramic capacitors will degrade with voltage stress or temperature extremes. Refer to its datasheet and use its worst case capacitance value for calculations.

The compensation capacitors C5 and C6 are then equal to:

$$C5 = \frac{VOUT \cdot COUT}{IOUT \cdot R5} \quad \text{Eq. 17}$$

$$C6 = \max\left(\frac{R_C \cdot COUT}{R5}, \frac{1}{\pi \cdot f_{sw} \cdot R5}\right) \quad \text{Eq. 18}$$

Where:

- IOUT is the output load current

The inclusion of C6 can increase gain margin and can decrease phase margin. In most cases, C6 is optional and may be omitted.

The zero, ω_{z2}, is optional as it can increase both the phase margin and gain bandwidth and can decrease gain margin. If used, place this zero at around two to five times f_C. Thus, C4 is in the approximate range of:

$$C4 = \left[\frac{1}{10\pi \cdot f_C \cdot R1}, \frac{1}{4\pi \cdot f_C \cdot R1}\right] \quad \text{Eq. 19}$$

Application Information (cont.)

15 External Loop Compensation Design (cont.)

The following is an example of how to choose component values for external loop compensation. Actual component values used in the application circuit may vary slightly from the calculated first-order approximation equations.

Let the following conditions be defined:

- VIN = 24V
- VOUT = 5V
- IOUT = 3.5A
- f_{sw} = 450kHz
- f_c = 45kHz
- R1 = 157kΩ
- R2 = 30kΩ
- L = 6.8µH
- COUT = 3 × 22µF (Effectively, COUT ≈ 36µF)
- R_C ≈ 1mΩ

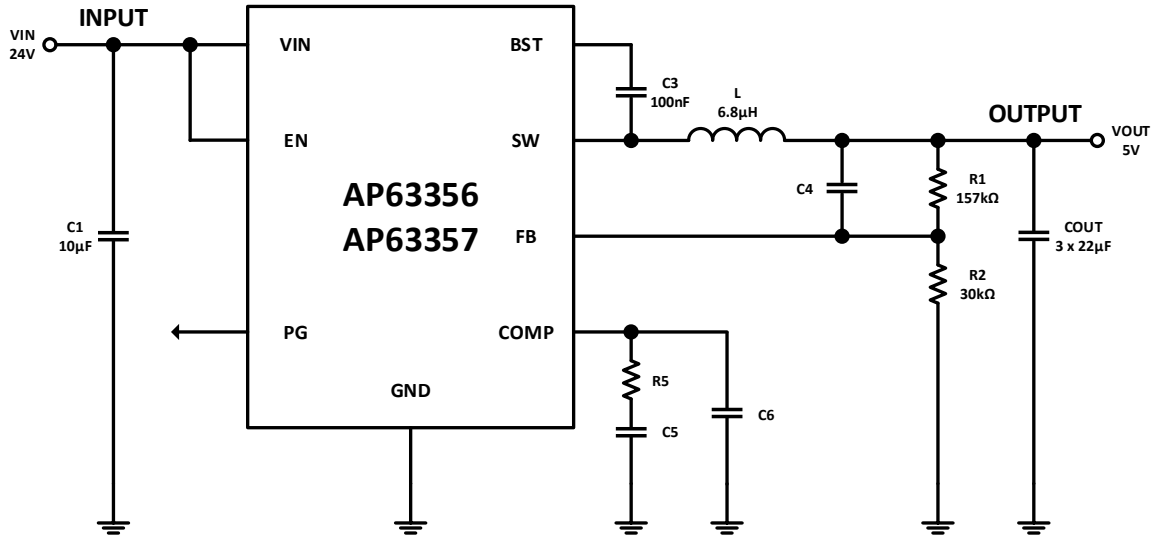


Figure 43. Example Circuit for External Loop Compensation Calculations

The calculations of the main component values involved in the external loop compensation, R5 and C5, are required. If the optional C4 and C6 capacitors are used, their calculations are also required.

Application Information (cont.)

15 External Loop Compensation Design (cont.)

From Eq. 16, the value of R5 is calculated as:

$$\begin{aligned} \mathbf{R5} &= \mathbf{5.2x10^3}[\frac{\mathbf{\Omega}}{\mathbf{A}}] \cdot \mathbf{f_c} \cdot \mathbf{VOUT} \cdot \mathbf{COUT} \\ &= \mathbf{5.2x10^3}[\frac{\mathbf{\Omega}}{\mathbf{A}}] \cdot \mathbf{45kHz} \cdot \mathbf{5V} \cdot \mathbf{36\mu F} \\ &\approx \mathbf{42.1k\Omega} \end{aligned}$$

Choose a standard resistor value for R5 close to its calculated value. For example, choose R5 to be 42.2kΩ.

From Eq. 17, C5 is calculated as:

$$\begin{aligned} \mathbf{C5} &= \frac{\mathbf{VOUT} \cdot \mathbf{COUT}}{\mathbf{IOUT} \cdot \mathbf{R5}} \\ &= \frac{\mathbf{5V} \cdot \mathbf{36\mu F}}{\mathbf{3.5A} \cdot \mathbf{42.1k\Omega}} \\ &\approx \mathbf{1.2nF} \end{aligned}$$

Choose 1.2nF for C5 since it already is a standard capacitor value.

From Eq. 18, C6 is calculated as:

$$\begin{aligned} \mathbf{C6} &= \mathbf{max}\left(\frac{\mathbf{R_C} \cdot \mathbf{COUT}}{\mathbf{R5}}, \frac{\mathbf{1}}{\mathbf{\pi} \cdot \mathbf{f_{sw}} \cdot \mathbf{R5}}\right) \\ &= \mathbf{max}\left(\frac{\mathbf{1m\Omega} \cdot \mathbf{36\mu F}}{\mathbf{42.1k\Omega}}, \frac{\mathbf{1}}{\mathbf{\pi} \cdot \mathbf{450kHz} \cdot \mathbf{42.1k\Omega}}\right) \\ &= \mathbf{max}(\mathbf{0.8pF}, \mathbf{16.8pF}) \\ &= \mathbf{16.8pF} \end{aligned}$$

C6 is optional. If used, choose a standard capacitor value for C6 close to its calculated value. For example, choose C6 to be 15pF.

From Eq. 19, the approximate range of C4 is calculated as:

$$\begin{aligned} \mathbf{C4} &= \left[\frac{\mathbf{1}}{\mathbf{10\pi} \cdot \mathbf{f_C} \cdot \mathbf{R1}}, \frac{\mathbf{1}}{\mathbf{4\pi} \cdot \mathbf{f_C} \cdot \mathbf{R1}}\right] \\ &= \left[\frac{\mathbf{1}}{\mathbf{10\pi} \cdot \mathbf{45kHz} \cdot \mathbf{157k\Omega}}, \frac{\mathbf{1}}{\mathbf{4\pi} \cdot \mathbf{45kHz} \cdot \mathbf{157k\Omega}}\right] \\ &= [\mathbf{4.5pF}, \mathbf{11.3pF}] \end{aligned}$$

C4 is optional. If used, choose a standard capacitor value for C4 that is close to its calculated range. For example, choose C4 to be 10pF.

Application Information (cont.)

15 External Loop Compensation Design (cont.)

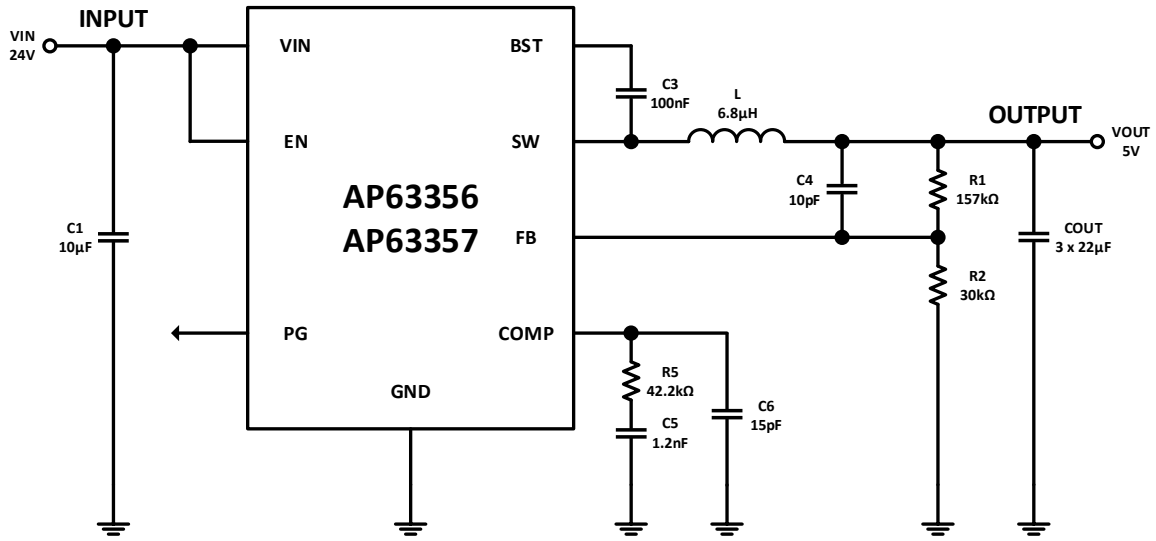


Figure 44. Example Circuit with Calculated Component Values for External Loop Compensation

The first-order calculated loop response has the following characteristics:

- Bandwidth is around 41.7kHz
- Phase Margin is around 65.6°
- Gain Margin is around -13.2dB

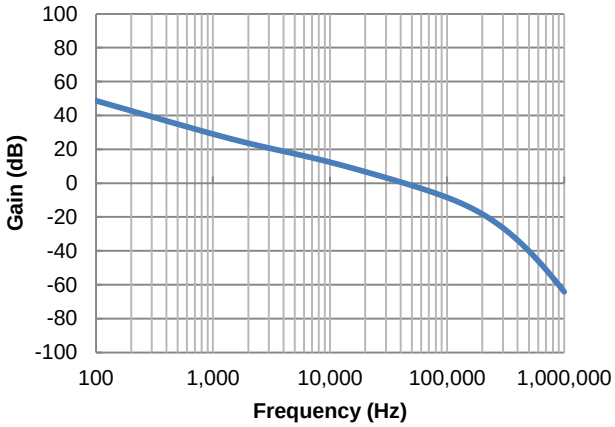


Figure 45. Closed-Loop Bandwidth

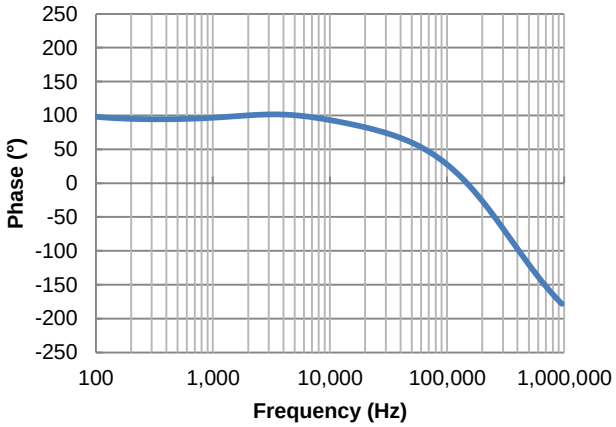


Figure 46. Closed-Loop Phase Margin

Layout

PCB Layout

1. The AP63356/AP63357 works at 3.5A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 47 for more details.

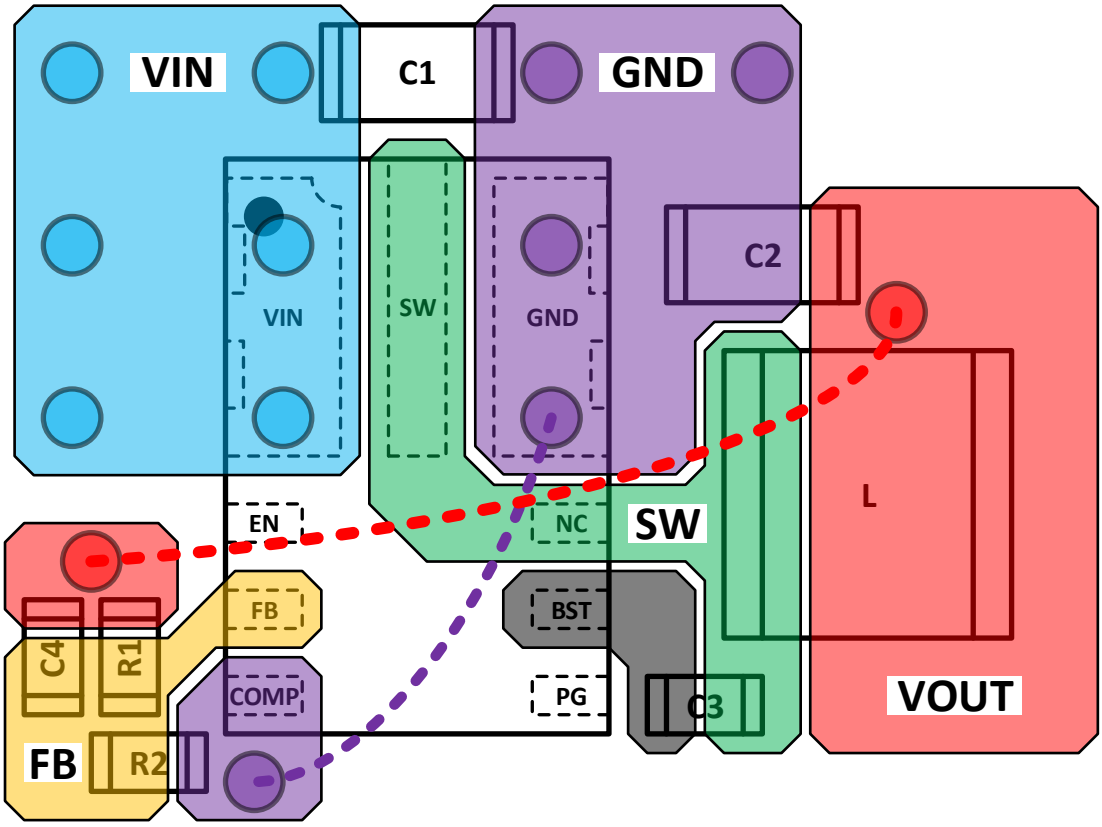
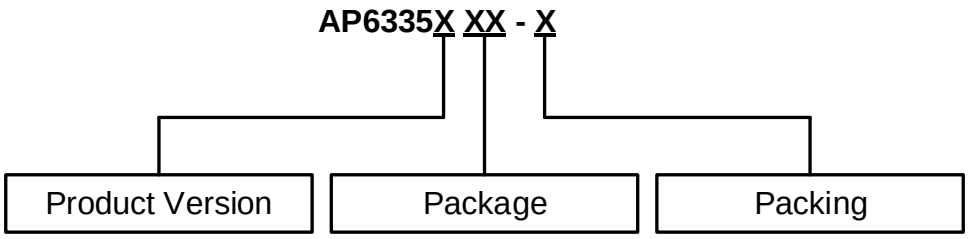


Figure 47. Recommended PCB Layout

Ordering Information

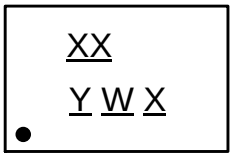


Orderable Device	Operation Mode	FSS Feature	Package Code	Tape and Reel	
				Quantity	Part Number Suffix
AP63356DV-7	PWM Only	Yes	DV	3000	-7
AP63357DV-7	PFM/PWM	Yes	DV	3000	-7

Marking Information

V-DFN3020-13 (Type A)

(Top View)



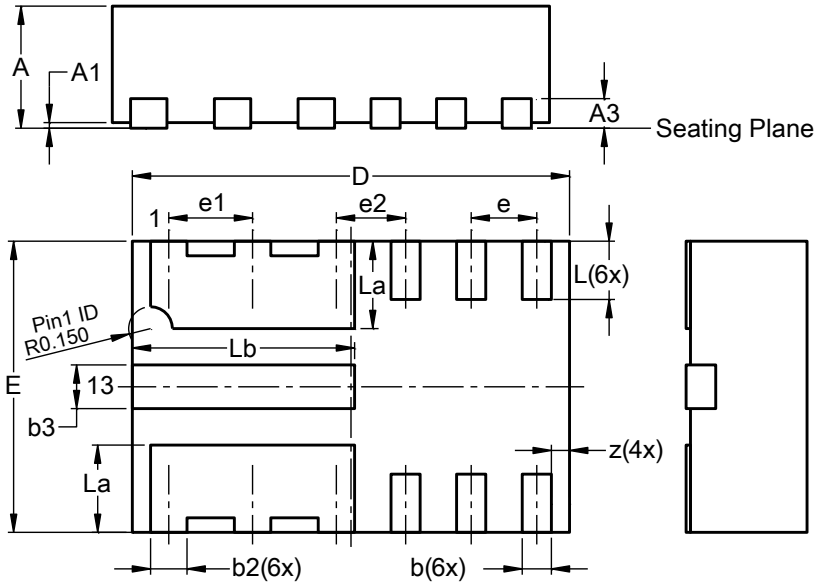
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : Internal Code

Orderable Device	Package	Identification Code
AP63356DV-7	V-DFN3020-13 (Type A)	J4
AP63357DV-7	V-DFN3020-13 (Type A)	J5

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3020-13 (Type A)

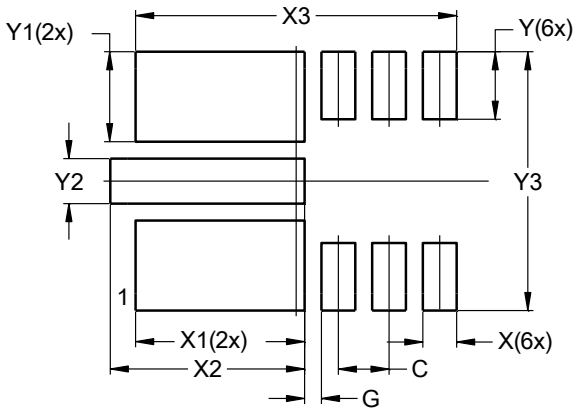


V-DFN3020-13			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.203
b	0.15	0.25	0.20
b2	0.20	0.30	0.25
b3	0.25	0.35	0.30
D	2.95	3.05	3.00
E	1.95	2.05	2.00
e	0.45 BSC		
e1	0.575 BSC		
e2	0.475 BSC		
L	0.35	0.45	0.40
La	0.55	0.65	0.60
Lb	1.475	1.575	1.525
z	-	-	0.125
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3020-13 (Type A)



Dimensions	Value (in mm)
C	0.45
G	0.15
X	0.30
X1	1.50
X2	1.73
X3	2.85
Y	0.60
Y1	0.80
Y2	0.40
Y3	2.30

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