TEXAS INSTRUMENTS

SN54AHC273, SN74AHC273

SCLS376I –JUNE 1997–REVISED MARCH 2015

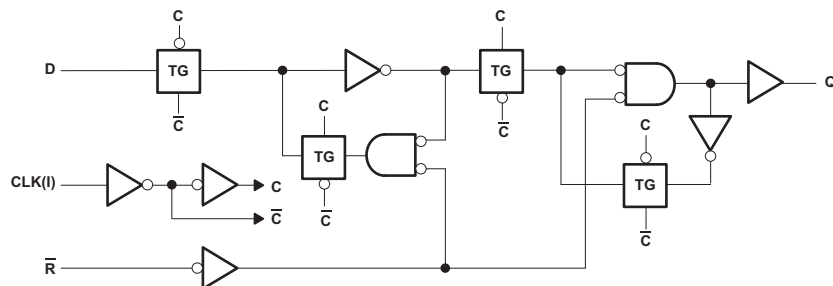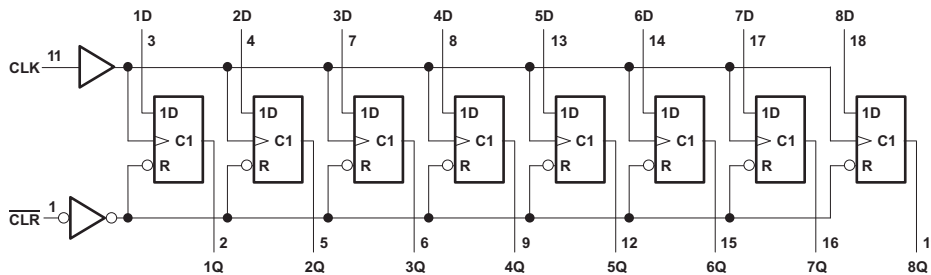# SNx4AHC273 Octal D-Type Flip-Flops With Clear

1 Features

- Operating Range 2-V to 5.5-V V_{CC}
- Contain Eight Flip-Flops With Single-Rail Outputs
- Direct Clear Input
- Individual Data Input to Each Flip-Flop
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Buffers and Storage Registers
- Shift Registers
- Pattern Generators
- Servers
- PCs and Notebooks
- Network Switches
- Memory Systems
- Databases

3 Description

These devices are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{CLR}$) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC273	PDIP (20)	24.33 mm × 6.35 mm
	SSOP (20)	7.20 mm × 5.30 mm
	TSSOP (20)	6.50 mm × 4.40 mm
	TVSOP (20)	5.00 mm × 4.40 mm
	SOIC (20)	12.80 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematics

Table of Contents

5 Revision History

Changes from Revision H (July 2014) to Revision I   **Page**

- Changed I_{OH} test conditions for V_{OH} from mA to µA to fix typographical error. 5

Changes from Revision G (June 1997) to Revision H   **Page**

- Updated document to new TI data sheet standards. 1
- Deleted Ordering Information table. 1
- Added Military Disclaimer to Features list. 1
- Added Applications. 1
- Added Handling Ratings table. 4
- Changed MAX operating temperature from 85°C to 125°C in Recommended Operating Conditions table. 4
- Added Thermal Information table. 5
- Added Typical Characteristics. 7
- Added Detailed Description section.. 9
- Added Application and Implementation section.. 11

6 Pin Configuration and Functions

SN54AHC273 . . . J OR W PACKAGE
SN74AHC273 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)
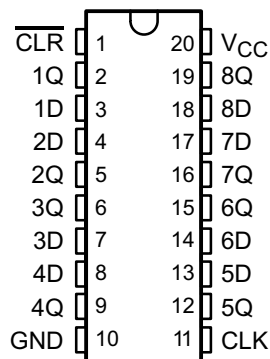
SN54AHC273 . . . FK PACKAGE
(TOP VIEW)
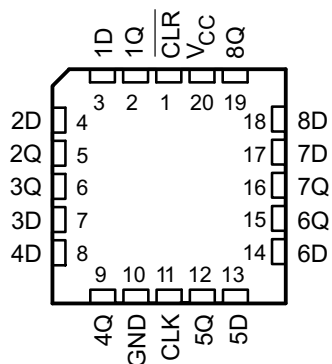
Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{CLR}}$	I	Clear Pin
2	1Q	O	1Q Output
3	1D	I	1D Input
4	2D	I	2D Input
5	2Q	O	2Q Output
6	3Q	O	3Q Output
7	3D	I	3D Input
8	4D	I	4D Input
9	4Q	O	4Q Output
10	GND	—	Ground Pin
11	CLK	I	Clock Pin
12	5Q	O	5Q Output
13	5D	I	5D Input
14	6D	I	6D Input
15	6Q	O	6Q Output
16	7Q	O	7Q Output
17	7D	I	7D Input
18	8D	I	8D Input
19	8Q	O	8Q Output
20	VCC	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Output voltage range[2]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			SN54AHC273		SN74AHC273		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5.5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 3 V ± 0.3 V		4		4	mA
		V_{CC} = 5.5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5.5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

Product Folder Links: *SN54AHC273 SN74AHC273*

7.4 Thermal Information

THERMAL METRIC[1]		SN74AHC273						UNIT
		N	DW	NS	DB	PW	DGV	
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.9	81.8	79.4	98.7	104.7	118.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.8	47.8	45.9	60.4	38.8	33.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.7	49.4	46.9	56.9	55.7	59.6	
ψ_{JT}	Junction-to-top characterization parameter	26.9	20.1	19.1	21.6	2.9	1.1	
ψ_{JB}	Junction-to-board characterization parameter	34.7	49.0	46.5	53.5	55.1	58.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the TI application report *IC Package Thermal Metrics* (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC273		SN74AHC273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	2 V	1.9			1.9		1.9		V
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1[1]		±1	μA
I_{CC}	V_I = V_{CC} or GND I_O = 0	5.5 V			4		40		40	μA
C_i	V_I = V_{CC} or GND	5 V		2.5	10				10	pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

7.6 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			SN54AHC273				SN74AHC273				UNIT
			T_A = 25°C		MIN	MAX	T_A = 25°C		MIN	MAX	
			MIN	MAX			MIN	MAX			
t_w	Pulse Duration	$\overline{CLR}$ low	5		6		5		6		ns
		CLK high or low	5		6.5		5		6.5		
t_{su}	Setup time	Data before CLK↑	5.5		6.5		5.5		6.5		ns
		CLR before CLK↑	2.5		2.5		2.5		2.5		
t_h	Hold time, data after CLK↑		1.5		2		1		1		ns

7.7 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			SN54AHC273				SN74AHC273				UNIT
			T_A = 25°C		MIN	MAX	T_A = 25°C		MIN	MAX	
			MIN	MAX			MIN	MAX			
t_w	Pulse Duration	$\overline{CLR}$ low	5		5		5		5		ns
		CLK high or low	5		5		5		5		
t_{su}	Setup time	Data before CLK↑	4.5		4.5		4.5		4.5		ns
		CLR before CLK↑	2		2		2		2		
t_h	Hold time, data after CLK↑		1.5		2		1		1		ns

7.8 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC273		SN74AHC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	75[1]	120[1]		65[1]		65		MHz
			C_L = 50 pF	50	75		45		45		
t_{PHL}	$\overline{CLR}$	Q	C_L = 15 pF		8.9[1]	13.6[1]	1[1]	16[1]	1	16	ns
t_{PLH}	CKL	Q	C_L = 15 pF		8.7[1]	13.6[1]	1[1]	16[1]	1	16	
t_{PHL}					8.7[1]	13.6[1]	1[1]	16[1]	1	16	ns
t_{PHL}	$\overline{CLR}$	Q	C_L = 50 pF		11.4	17.1	1	19.5	1	19.5	ns
t_{PLH}	CLK	Q	C_L = 50 pF		11.2	17.1	1	19.5	1	19.5	ns
t_{PHL}					11.2	17.1	1	19.5	1	19.5	ns
$t_{sk(o)}$			C_L = 50 pF			1.5[2]				1.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.9 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC273		SN74AHC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	120[1]	165[1]		100[1]		100		MHz
			C_L = 50 pF	80	110		70		70		
t_{PHL}	$\overline{CLR}$	Q	C_L = 15 pF		5.2[1]	8.5[1]	1[1]	10[1]	1	10	ns
t_{PLH}	CKL	Q	C_L = 15 pF		5.8[1]	9[1]	1[1]	10.5[1]	1	10.5	
t_{PHL}					5.8[1]	9[1]	1[1]	10.5[1]	1	10.5	ns
t_{PHL}	$\overline{CLR}$	Q	C_L = 50 pF		6.7	10.5	1	12	1	12	
t_{PLH}	CLK	Q	C_L = 50 pF		7.3	11	1	12.5	1	12.5	ns
t_{PHL}					7.3	11	1	12.5	1	12.5	ns
$t_{sk(o)}$			C_L = 50 pF			1[2]				1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

Product Folder Links: *SN54AHC273 SN74AHC273*

7.10 Noise Characteristics[1]

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER		SN74AHC273			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

(1)   Characteristics are for surface-mount packages only.

7.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	31	pF

7.12 Typical Characteristics
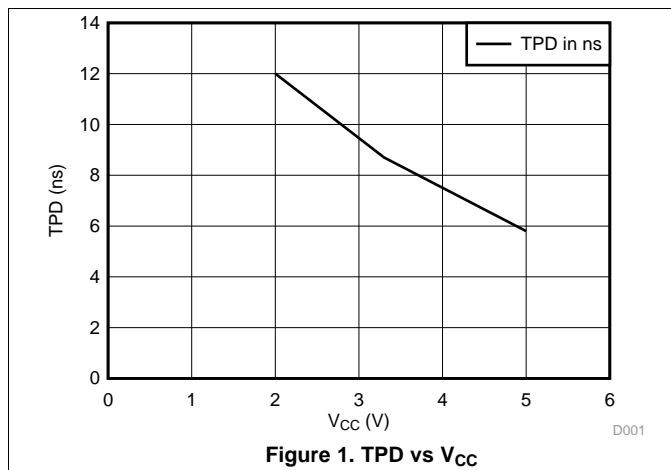
Figure 1. TPD vs V_{CC}
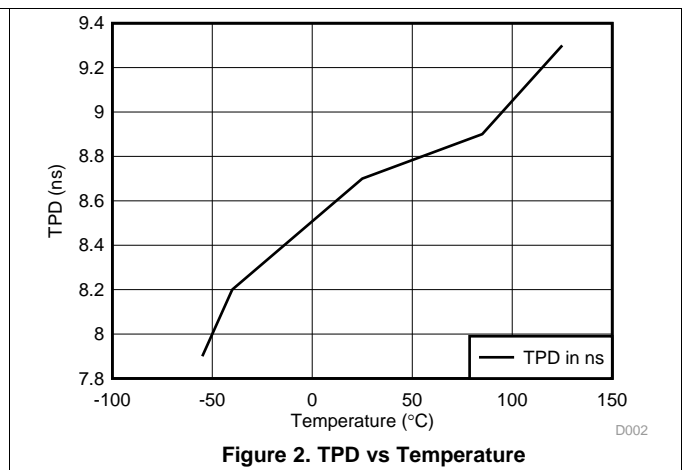
Figure 2. TPD vs Temperature

8 Parameter Measurement Information

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.
   E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

Product Folder Links: *SN54AHC273 SN74AHC273*

9 Detailed Description

9.1 Overview

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The inputs are 5 V tolerant and can be driven from 5-V devices. This feature allows the use of these devices as down translators in a mixed 5-V to 3.3-V system environment.

9.2 Functional Block Diagrams
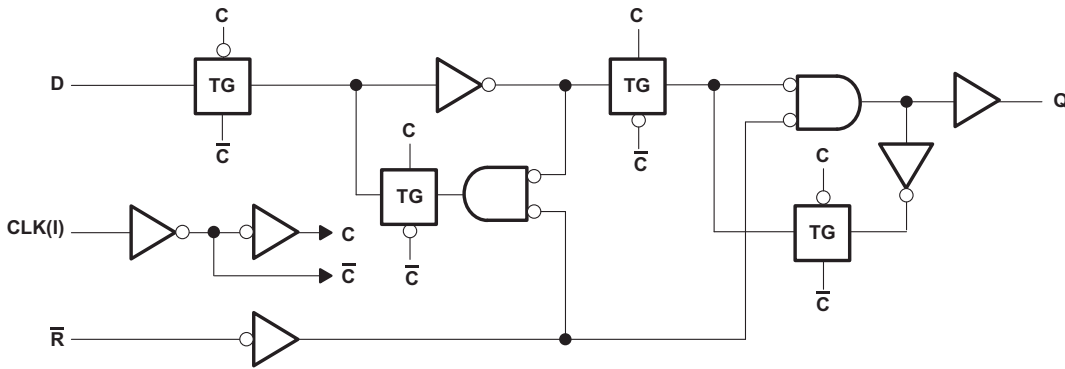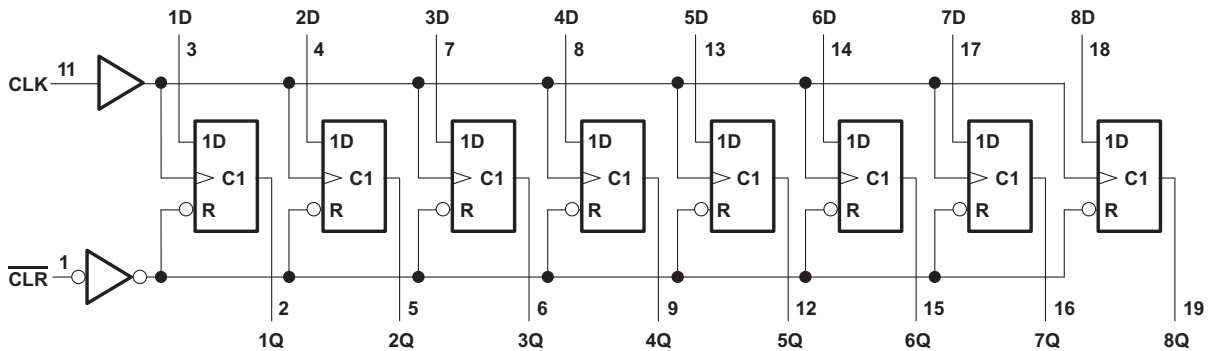
9.3 Feature Description

* Wide operating voltage range
    – Operates from 2 V to 5.5 V
* Allows down voltage translation
    – Inputs accept voltages to 5.5 V
* Slow edge rates minimize output ringing

9.4 Device Functional Modes

Table 1. Function Table

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Y
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

10 Application and Implementation

10.1 Application Information

The SNx4AHC273 is a low-drive CMOS device that can be used for a multitude of applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC}. This feature makes the device ideal for translating down to the V_{CC} level. Figure 5 shows the reduction in ringing compared to higher drive parts such as AC.

10.2 Typical Application
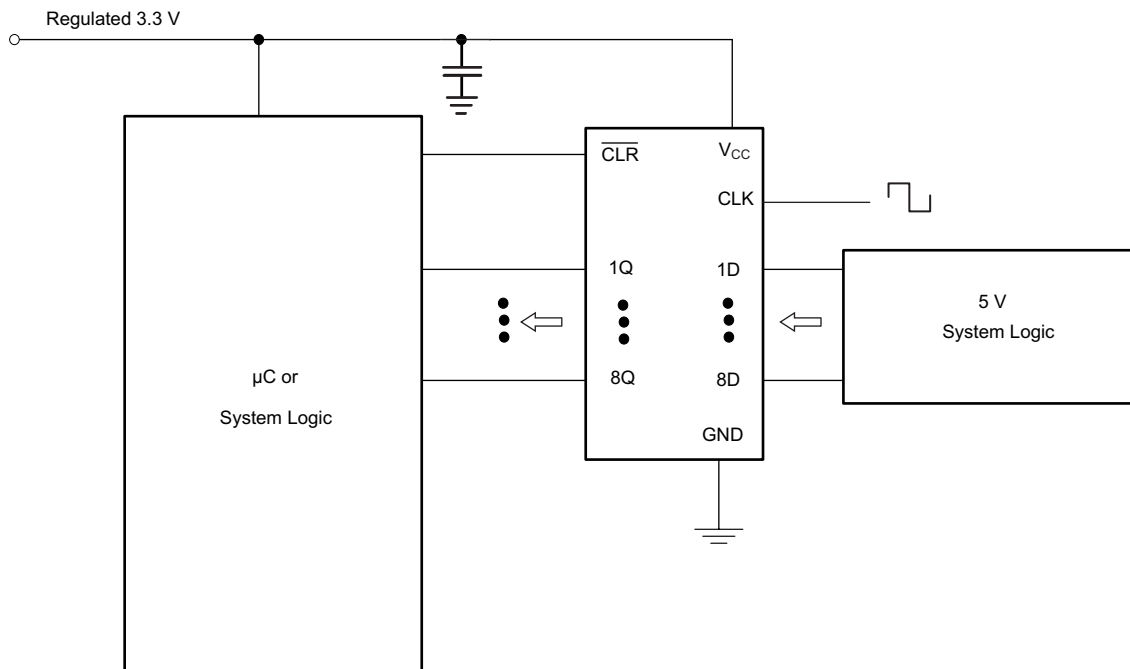
Figure 4. Specific Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended input conditions
   – Rise time and fall time specs: See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   – Specified High and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
   – Load currents should not exceed 25 mA per output and 75 mA total for the part
   – Outputs should not be pulled above V_{CC}

Typical Application (continued)

10.2.3 Application Curves

Figure 5. Switching Characteristics Comparison
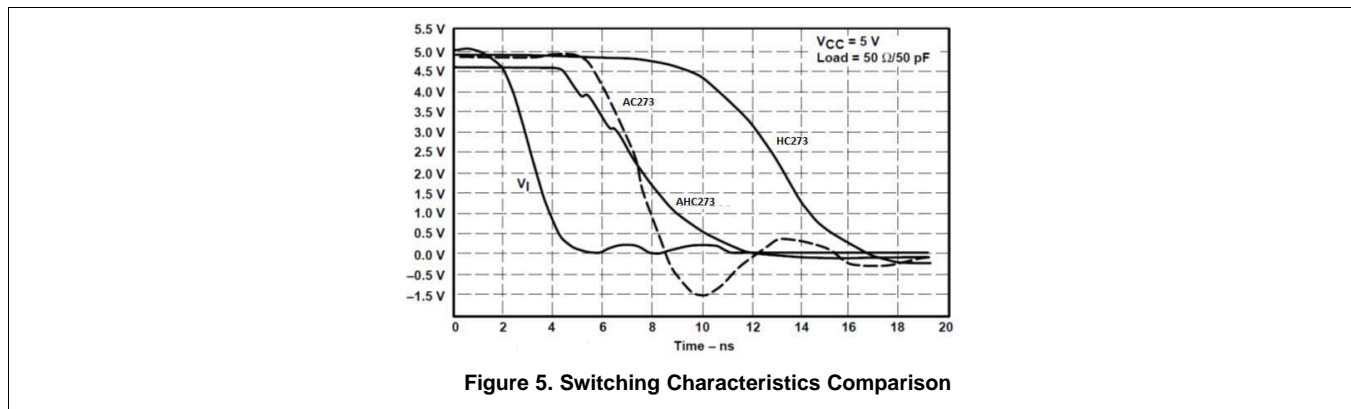
11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple VCC pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 6 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally inputs will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver.

12.2 Layout Example

Figure 6. Layout Diagram

Product Folder Links: *SN54AHC273 SN74AHC273*
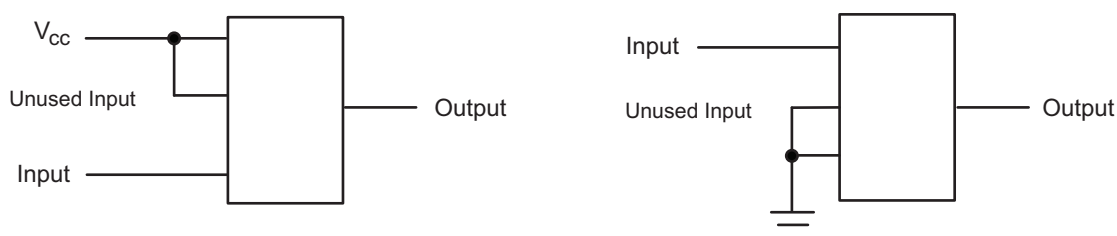
13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC273	Click here	Click here	Click here	Click here	Click here
SN74AHC273	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9853001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9853001Q2A SNJ54AHC 273FK	Samples
5962-9853001QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9853001QR A SNJ54AHC273J	Samples
5962-9853001QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9853001QS A SNJ54AHC273W	Samples
SN74AHC273DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74AHC273DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SN74AHC273DGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SN74AHC273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273	Samples
SN74AHC273DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273	Samples
SN74AHC273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273	Samples
SN74AHC273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC273N	Samples
SN74AHC273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273	Samples
SN74AHC273PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SN74AHC273PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SN74AHC273PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74AHC273PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SN74AHC273PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHC273FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9853001Q2A SNJ54AHC 273FK	Samples
SNJ54AHC273J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9853001QR A SNJ54AHC273J	Samples
SNJ54AHC273W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9853001QS A SNJ54AHC273W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHC273, SN74AHC273 :

- Catalog: SN74AHC273

- Military: SN54AHC273

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC273DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC273NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.5	12.0	24.0	Q1
SN74AHC273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC273DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AHC273DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74AHC273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC273NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHC273PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.300 (7,62)
0.245 (6,22)

0.100 (2,45)
0.045 (1,14)

0.009 (0,23)
0.004 (0,10)

0.320 (8,13) MAX

1   20

0.022 (0,56)
0.015 (0,38)

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

0.370 (9,40)
0.250 (6,35)

0.370 (9,40)
0.250 (6,35)

4040180−4/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only.
          E.   Falls within Mil−Std 1835 GDFP2−F20

FK (S−CQCC−N**) LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.080\ (2,03)}{0.064\ (1,63)}$

$\frac{0.055\ (1,40)}{0.045\ (1,14)}$

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

$\frac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS−004

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MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R—GDIP—T**)   CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package is hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
        E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

0,23
0,13

⊕ 0,07 Ⓜ

24   13

4,50   6,60
4,30   6,20

0,16 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1   12

A

1,20 MAX

0,15
0,05

Seating Plane

△ 0,08

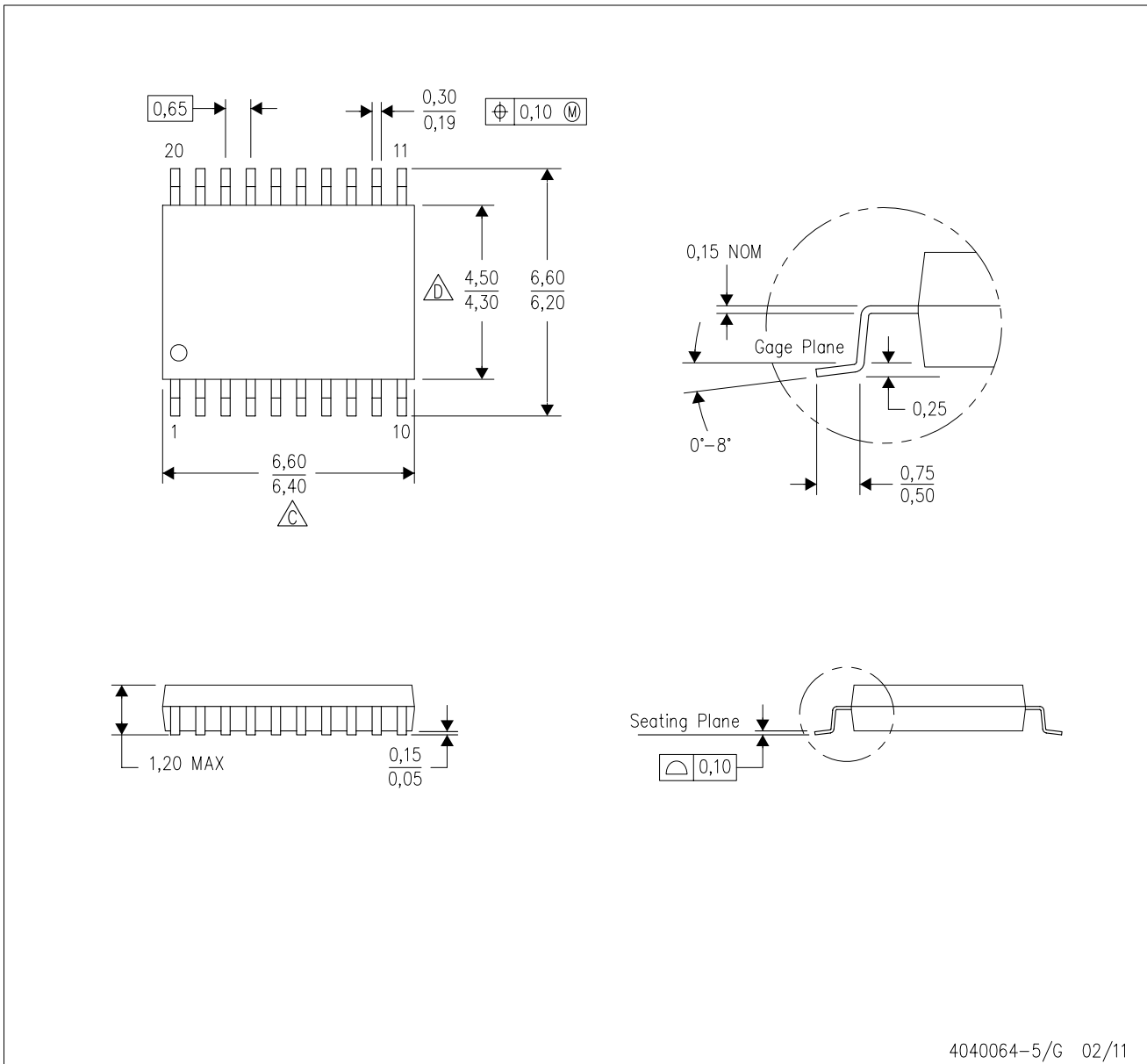| DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
           D. Falls within JEDEC: 24/48 Pins – MO-153
                                14/16/20/56 Pins – MO-194

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65   0,30 / 0,19   ⊕ 0,10 (M)

20   11

4,50 / 4,30   6,60 / 6,20

0,15 NOM

Gage Plane

1   10

0°−8°

0,25

6,60 / 6,40

0,75 / 0,50

1,20 MAX   0,15 / 0,05

Seating Plane

⌒ 0,10

4040064−5/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
          D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

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PW (R–PDSO–G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284–5/G 08/15

NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Publication IPC–7351 is recommended for alternate design.
            D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
                contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
            E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

0,65

0,38
0,22
⊕ | 0,15 Ⓜ

28   15

0,25
0,09

5,60
5,00

8,20
7,40

Gage Plane

0,25

0°–8°

0,95
0,55

1   14

A

2,00 MAX

0,05 MIN

Seating Plane

△ | 0,10

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-150

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) /D\

0.045 (1,14) / 0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
/C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
/D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

18X 1.27

20

13.0 / 12.6 NOTE 3

2X 11.43

10

11

B

7.6 / 7.4 NOTE 4

20X 0.51 / 0.31

⌖ | 0.25 Ⓜ | C | A | B

C

SEATING PLANE

◯ | 0.1 | C

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

0.25
GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM
℄

1

20X (0.6)

20

18X (1.27)

SYMM
℄

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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