AC33M4064T, AC33M3064T Datasheet

32-bit Cortex-M3 based Programmable Motor Controller

Datasheet Version 1.01

Features

Core

- Maximum operating frequency: 48MHz
- 32-bit ARM Cortex-M3

Memories

- 64KB code flash memory
- 8KB SRAM

Clock, reset and power management

- Two main operating clocks: HCLK, PCLK
- Two system reset: cold reset, warm reset
- Power management mode: Run mode, Sleep mode

Interrupt management

- Nested Vector Interrupt Controller (NVIC)

Timers

- Watchdog Timer
- Six general purpose timers
  - Periodic, one-shot, PWM, capture mode

Communication interfaces

- 2 UARTs, 1 I2C, 1 SPI

Motor Pulse-Width Modulation

- MPWM generators

1.5Msps ADC

- 2 units with 11 channel Inputs

Development support

- SWD debug interface
- JTAG Debugger (JTAG is only for LQFP-48)

Four types of package options

- LQFP48-0707 (0.5mm pitch)
- LQFP32-0707 (0.8mm pitch)

Operating voltage

- 3.0V to 5.5V

Operating temperature

- Commercial grade (-40℃ to +105℃)

Product selection table

Table 1. Device Summary

Device name	Flash	SRAM	UART	SPI	I2C	MPWM	ADC	I/O ports	Package
AC33M4064T	64KB	8KB	2	1	1	1	2-unit 11 ch	44	LQFP-48
AC33M3064T*	64KB	8KB	2	1	1	1	2-unit 7 ch	28	LQFP-32

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

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1 Description

AC33Mx064T CPU core is supported by ARM Cortex-M3 processor which provides a high-performance and low-cost platform.

1.1 Device overview

In this section, features of AC33Mx064T series and peripheral counts are introduced.

Table 2. AC33Mx064T Series Features and Peripheral Counts

Peripherals		Description
Core	CPU	• Maximum operating frequency: 48MHz • 32-bit ARM Cortex-M3 CPU
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller)
Memory	Code flash	Capacity : 64Kbytes code flash memory
	BOOT ROM	• UART, SPI boot modes • In-system programming
	SRM	8 KB
System Control Unit (SCU)	Operating frequency	48MHz
	Clock	• MainOSC : X-TAL(4MHz~8MHz) • PLL Clock : 4MHz ~ 48MHz • Internal RING OSC : 1MHz
	Clock monitoring	System Fail-Safe function by Clock Monitoring
	Operating mode	• RUN mode • SLEEP mode
	Reset	• nRESET pin reset • Core reset • Software reset
	LDO	Low-dropout (LDO) regulator built in for low-voltage operation
	POR	Power On Reset
	LVD	Programmable Low Voltage Detector (Brown-Out Detector)
General Purpose I/O (GPIO)		• General Purpose I/O (GPIO) — 44Ports : 48-Pin — 28rts: 32-Pin

Table 2. AC33Mx064T Series Features and Peripheral Counts (continued)

Peripherals		Description
TIMER	16-bit Timer	• 6channels • Periodic, One-shot, PWM, Capture mode • Multi-Timer Synchronization Option
	WDT	1 channels
Serial interface	UART	2 channels supported
	SPI	1 channels supported
	I2C	1 channels supported
Motor Pulse-Width Modulation	MPWM	• 3-Phase Motor PWM with ADC triggering function • 1 channel
12-bit A/D Converter	ADC	• 1.5Msps high-speed ADC with sequential conversion function • 2 units with 11 channel Inputs
Operating voltage		3.0V to 5.5V
Operating temperature		Commercial grade (-40℃ to +105℃)
Package		• Three types of package options — 48-pin LQFP — 32-pin LQFP

1.2 Block diagram

In this section, the AC33Mx064T series with peripherals is described in block diagram.

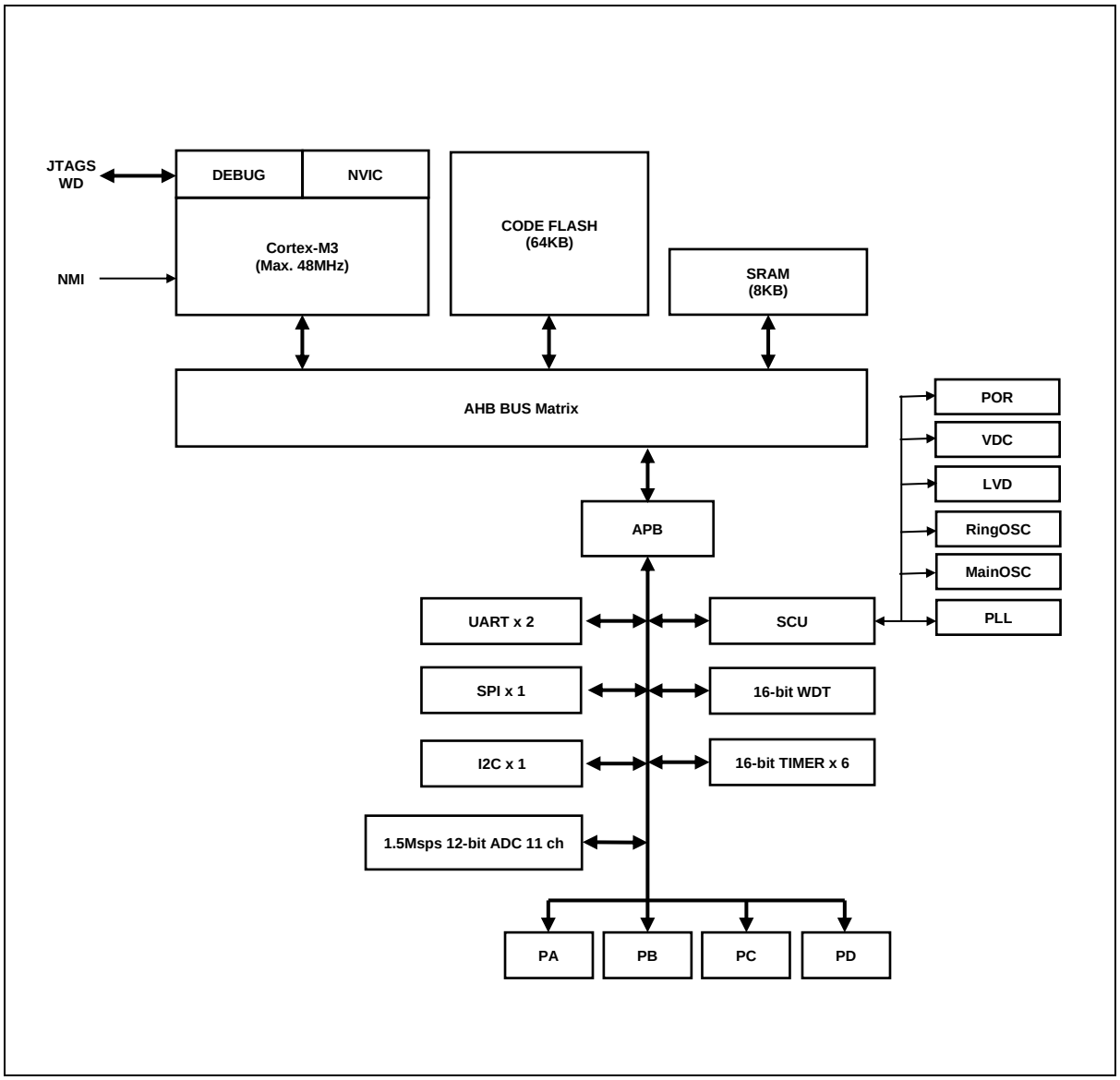


Figure 1. AC33Mx064T Block Diagram

2 Pinouts and pin descriptions

In this chapter, pinouts and pin descriptions of the AC33Mx064T series are introduced.

2.1 Pinouts

2.1.1 AC33M4064T (LQFP-48)

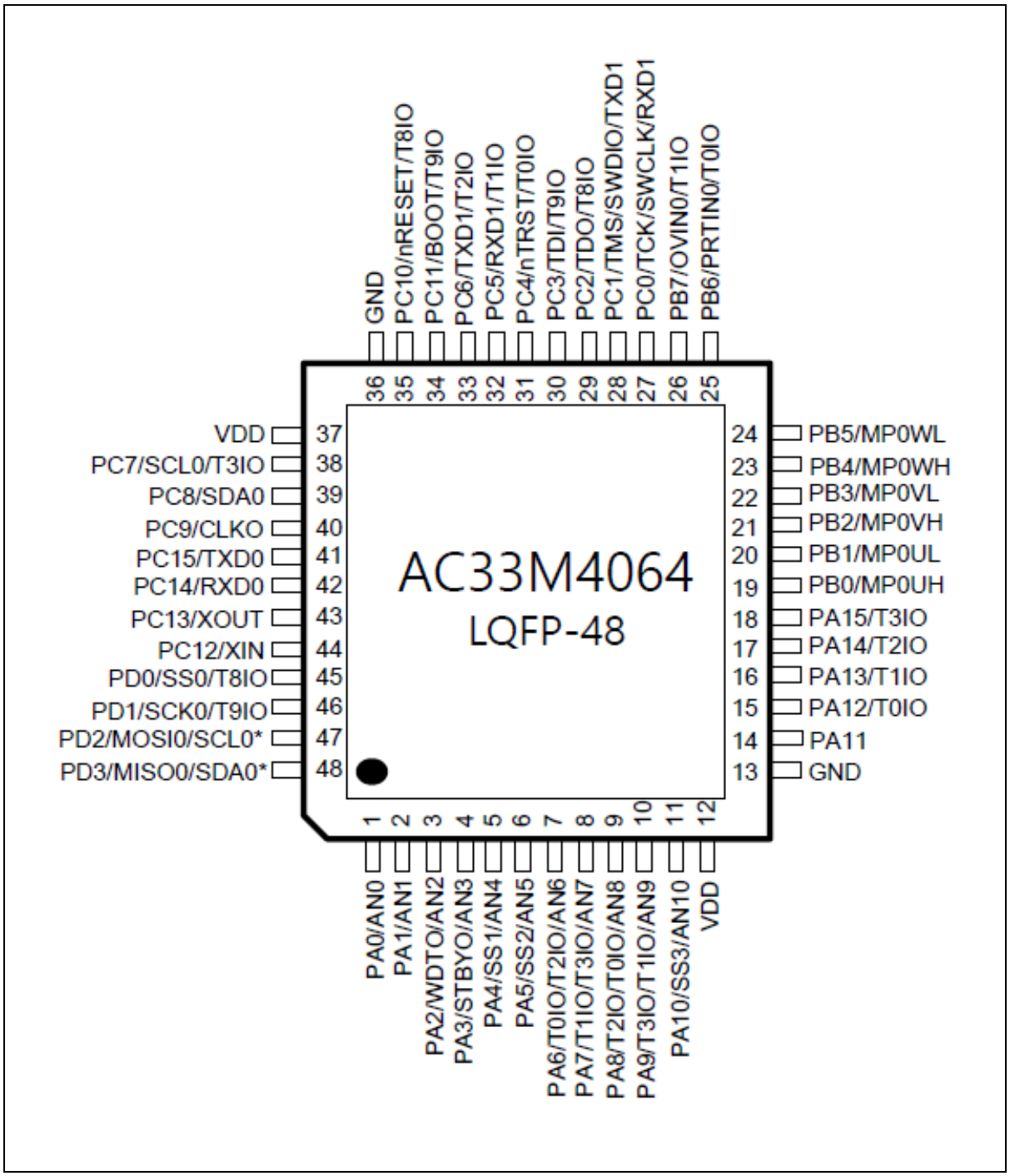


Figure 2. LQFP 48 Pinouts

2.1.2 AC33M3064T (LQFP-32)

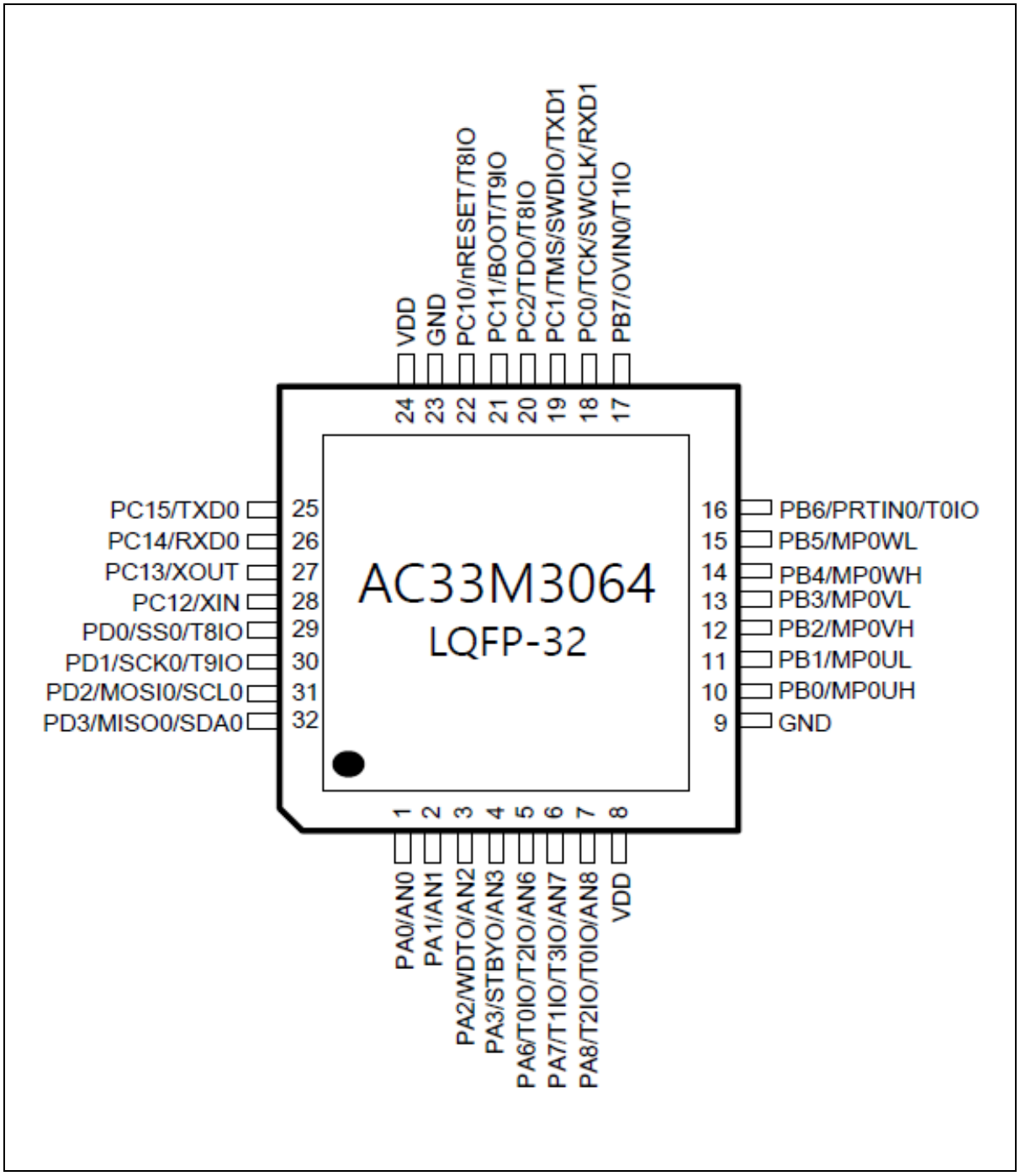


Figure 3. LQFP 32 Pinouts

2.2 Pin description

Pin configuration information in Table 3 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to five selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 3. Pin Description

Pin No		Pin Name	Type	Description	Remark
LQFP48	LQFP32				
1	1	PA0*	IOUS	PORT A Bit 0 Input/Output	
		AN0	IA	Analog Input 0	
2	2	PA1*	IOUS	PORT A Bit 1 Input/Output	
		AN1	IA	Analog Input1	
3	3	PA2*	IOUS	PORT A Bit 2 Input/Output	
		WDTO	O	Watchdog timer overflow output	
		AN2	IA	Analog Input2	
4	4	PA3*	IOUS	PORT A Bit 3 Input/Output	
		STBO	O	Stop mode output	
		AN3	IA	Analog Input 3	
5	-	PA4*	IOUS	PORT A Bit 4 Input/Output	
		SS1	I/O	Slave Select 1 for SPI0	
		AN4	IA	Analog Input 4	
6	-	PA5*	IOUS	PORT A Bit 5 Input/Output	
		SS2	I/O	Slave Select 2 for SPI0	
		AN5	IA	Analog Input 5	
7	5	PA6*	IOUS	PORT A Bit 6 Input/Output	
		T0IO	I/O	Timer 0 Input/Output	
		T2IO	I/O	Timer 2 Input/Output	
		AN6	IA	Analog Input 6	
8	6	PA7*	IOUS	PORT A Bit 7 Input/Output	
		T1IO	I/O	Timer 1 Input/Output	
		T3IO	I/O	Timer 3 Input/Output	
		AN7	IA	Analog Input 7	
9	7	PA8*	IOUS	PORT A Bit 8 Input/Output	
		T2IO	I/O	Timer 2 Input/Output	
		T0IO	I/O	Timer 0 Input/Output	
		AN8	IA	Analog Input 8	

Table 3. Pin Description (continued)

Pin No		Pin Name	Type	Description	Remark
LQFP48	LQFP32				
10	-	PA9*	IOUS	PORT A Bit 9 Input/Output	
		T3IO	I/O	Timer 3 Input/Output	
		T1IO	I/O	Timer 1 Input/Output	
		AN9	IA	Analog Input 9	
11	-	PA10*	IOUS	PORT A Bit 10 Input/Output	
		SS3	Output	Slave Select 3 for SPI0	
		AN10	IA	Analog Input 10	
12	8	VDD	P	VDD	
13	9	GND	P	Ground	
14	-	PA11*	IOUS	PORT A Bit 11 Input/Output	
15	-	PA12*	IOUS	PORT A Bit 12 Input/Output	
		T0IO	I/O	Timer 0 Input/Output	
16	-	PA13*	IOUS	PORT A Bit 13 Input/Output	
		T1IO	I/O	Timer 1 Input/Output	
17	-	PA14*	IOUS	PORT A Bit 14 Input/Output	
		T2IO	I/O	Timer 2 Input/Output	
18	-	PA15*	IOUS	PORT A Bit 15 Input/Output	
		T3IO	I/O	Timer 3 Input/Output	
19	10	PB0	IOUS	PORT B Bit 0 Input/Output	
		PWM0UH	Output	PWM0 UH Output	
20	11	PB1	IOUS	PORT B Bit 1 Input/Output	
		PWM0UL	Output	PWM0 UL Output	
21	12	PB2	IOUS	PORT B Bit 2 Input/Output	
		PWM0VH	Output	PWM0 VH Output	
22	13	PB3	IOUS	PORT B Bit 3 Input/Output	
		PWM0VL	Output	PWM0 VL Output	
23	14	PB4	IOUS	PORT B Bit 4 Input/Output	
		PWM0WH	Output	PWM0 WH Output	
24	15	PB5	IOUS	PORT B Bit 5 Input/Output	
		PWM0WL	Output	PWM0 WL Output	
25	16	PB6	IOUS	PORT B Bit 6 Input/Output	
		PRTIN0	Input	PWM0 Protection Input signal 0	
		T0IO	I/O	Timer 0 Input/Output	
26	17	PB7	IOUS	PORT B Bit 7 Input/Output	
		OVIN0	Input	PWM0 Over-voltage input signal 0	

Table 3. Pin Description (continued)

Pin No		Pin Name	Type	Description	Remark
LQFP48	LQFP32				
		T1IO	I/O	Timer 1 Input/Output	
27	18	PC0	IOUS	PORT C Bit 0 Input/Output	
		TCK/SWCK	Input	JTAG TCK, SWD Clock Input	
		RXD1	Input	UART0 Rx Data Input	
28	19	PC1	IOUS	PORT C Bit 1 Input/Output	
		TMS/SWDIO	I/O	JTAG TMS, SWD Data Input/Output	
		TXD1	Input	UART0 Tx Data Output	
29	20	PC2	IOUS	PORT C Bit 2 Input/Output	
		TDO/SWO	Output	JTAG TDO, SWO Output	
		T8IO	I/O	Timer 8 Input/Output	
30	-	PC3	IOUS	PORT C Bit 3 Input/Output	
		TDI	Input	JTAG TDI Input	
		T9IO	I/O	Timer 9 Input/Output	
31	-	PC4	IOUS	PORT C Bit 4 Input/Output	
		nTRST	Input	JTAG nTRST Input	
		T0IO	Input	Timer 0 Input/Output	
32	-	PC5	IOUS	PORT C Bit 5 Input/Output	
		RXD1	Input	UART1 RXD Input	
		T1IO	I/O	Timer 1 Input/Output	
33	-	PC6	IOUS	PORT C Bit 6 Input/Output	
		TXD1	Output	UART1 TXD Output	
		T2IO	I/O	Timer 2 Input/Output	
34	21	PC11	IOUS	PORT C Bit 11 Input/Output	
		BOOT	Input	Boot mode Selection Input	
		T9IO	I/O	Timer 9 Input/Output	
35	22	PC10	IOUS	PORT C Bit 10 Input/Output	
		nRESET	Input	External Reset Input	Pull-up
		T8IO	I/O	Timer 8 Input/Output	
36	23	GND	P	Ground	
37	24	VDD	P	VDD	
38	-	PC7	IOUS	PORT C Bit 7 Input/Output	
		SCL0	Output	I²C Channel 0 SCL In/Out	
		T3IO	I/O	Timer 3 Input/Output	
39	-	PC8	IOUS	PORT C Bit 8 Input/Output	
		SDA0	Output	I²C Channel 0 SDA In/Out	

Table 3. Pin Description (continued)

Pin No		Pin Name	Type	Description	Remark
LQFP48	LQFP32				
40	-	PC9	IOUS	PORT C Bit 9 Input/Output	
		CLKO	Output	System Clock Output	
41	25	PC15	IOUS	PORT C Bit 15 Input/Output	
		TXD0	Output	UART0 TXD Output	
		MISO0	I/O	SPI0 Master-Input/Slave-Output	
42	26	PC14	IOUS	PORT C Bit 14 Input/Output	
		RXD0	Input	UART0 RXD Input	
		MOSI0	I/O	SPI0 Master-Output/Slave-Input	
43	27	PC13	IOUS	PORT C Bit 13 Input/Output	
		XOUT	OA	External Crystal Oscillator Output	
44	28	PC12	IOUS	PORT C Bit 12 Input/Output	
		XIN	IA	External Crystal Oscillator Input	
45	29	PD0	IOUS	PORT D Bit 0 Input/Output	
		SS0	I/O	SPI1 Slave Select	
		T8IO	I/O	Timer 8 Input/Output	
46	30	PD1	IOUS	PORT D Bit 1 Input/Output	
		SCK0	I/O	SPI0 Clock Input/Output	
		T9IO	I/O	Timer 9 Input/Output	
47	31	PD2	IOUS	PORT D Bit 2 Input/Output	
		MOSI0	I/O	SPI Channel 0 Master Out / Slave In	
		SCL0	Output	I²C Channel 0 SCL In/Out	
48	32	PD3*	IOUS	PORT D Bit 3 Input/Output	
		MISO0	I/O	SPI Channel 0 Master In / Slave Out	
		SDA0	Output	I²C Channel 0 SDA In/Out	

NOTES:

1. * Notation: I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. (*) Selected pin function after reset condition
3. Pin order may be changed with revision notice

3 System and memory overview

3.1 System architecture

Main system of AC33Mx064T series consists of the followings:

- ARM® Cortex® -M3 core
- Internal SRAM, Flash memory

3.1.1 Cortex-M0 core

ARM powered Cortex-M3 Core based on ARMv7M architecture which is optimized for small size and low power system. On core system timer (SYSTICK) provides a simple 24 bit timer easy to manage the system operation Thumb-compatible Thumb-2 only instruction set processor core makes code high-density. Hardware division and single-cycle multiplication is present Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling. JTAG and SWD debugging features are provided. Max 48MHz operating frequency with zero wait execution

3.1.2 Interrupt controller

Table 3. Interrupt Vector Map

Priority	Vector address	Interrupt source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MPU Fault Handler
-11	0x0000_0014	BUS Fault Handler
-10	0x0000_0018	Usage Fault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler

Table 3. Interrupt Vector Map (continued)

Priority	Vector address	Interrupt source
0	0x0000_0040	LVDFAIL
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	XOSCFAIL
3	0x0000_004C	WDT
4	0x0000_0050	Reserved
5	0x0000_0054	TIMER0
6	0x0000_0058	TIMER1
7	0x0000_005C	TIMER2
8	0x0000_0060	TIMER3
9	0x0000_0064	Reserved
10	0x0000_0068	
11	0x0000_006C	
12	0x0000_0070	
13	0x0000_0074	TIMER8
14	0x0000_0078	TIMER9
15	0x0000_007C	Reserved
16	0x0000_0080	GPIOAE
17	0x0000_0084	GPIOAO
18	0x0000_0088	GPIOBE
19	0x0000_008C	GPIOBO
20	0x0000_0090	GPIOCE
21	0x0000_0094	GPIOCO
22	0x0000_0098	GPIODE
23	0x0000_009C	GPIODO
24	0x0000_00A0	MPWM0
25	0x0000_00A4	MPWM0PROT
26	0x0000_00A8	MPWM0OVV
27	0x0000_00AC	Reserved
28	0x0000_00B0	
29	0x0000_00B4	
30	0x0000_00B8	
31	0x0000_00BC	
32	0x0000_00C0	SPI0
33	0x0000_00C4	Reserved
34	0x0000_00C8	
35	0x0000_00CC	

Table 3. Interrupt Vector Map (continued)

Priority	Vector address	Interrupt source
36	0x0000_00D0	I2C0
37	0x0000_00D4	Reserved
38	0x0000_00D8	UART0
39	0x0000_00DC	UART1
40	0x0000_00E0	Reserved
41	0x0000_00E4	
42	0x0000_00E8	
43	0x0000_00EC	ADC0
44	0x0000_00F0	ADC1
45	0x0000_00F4	Reserved
46	0x0000_00F8	
47	0x0000_00FC	
48	0x0000_0100	
49	0x0000_0104	
50	0x0000_0108	
51	0x0000_010C	
52	0x0000_0110	
53	0x0000_0114	
54	0x0000_0118	
55	0x0000_011C	
56	0x0000_0120	
57	0x0000_0124	
58	0x0000_0128	
59	0x0000_012C	
60	0x0000_0130	
61	0x0000_0134	
62	0x0000_0138	
63	0x0000_013C	

NOTE: Each external interrupt has an associated priority-level register. Each of them is 3 bits wide, occupying the three MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits). NVIC registers in the Cortex-M3 processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

```
**  __NVIC_PRIO_BITS = 3
```

3.2 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

3.2.1 Memory map

Figure 4 shows addressable memory space in memory map.

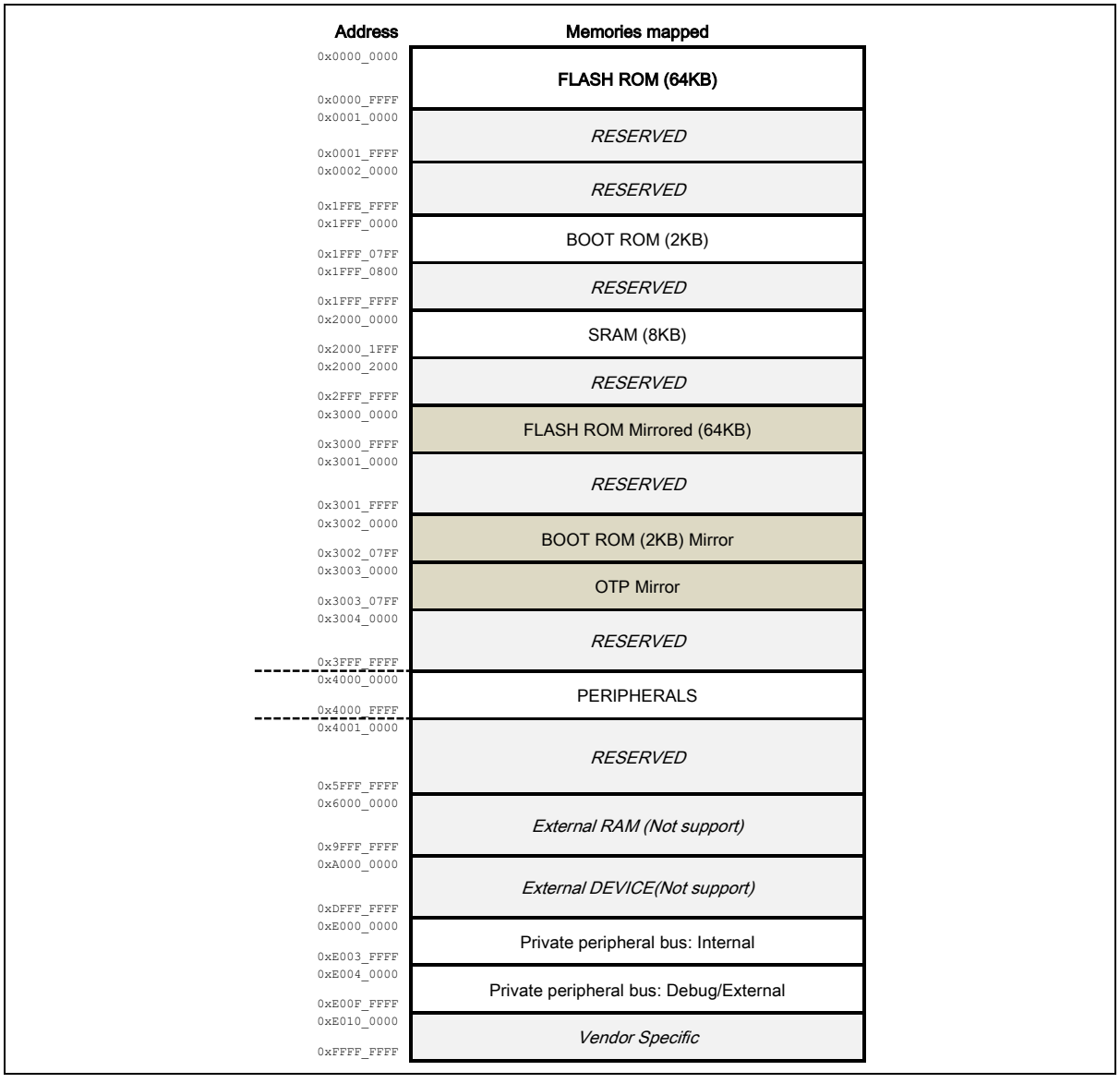


Figure 4. Main Memory Map

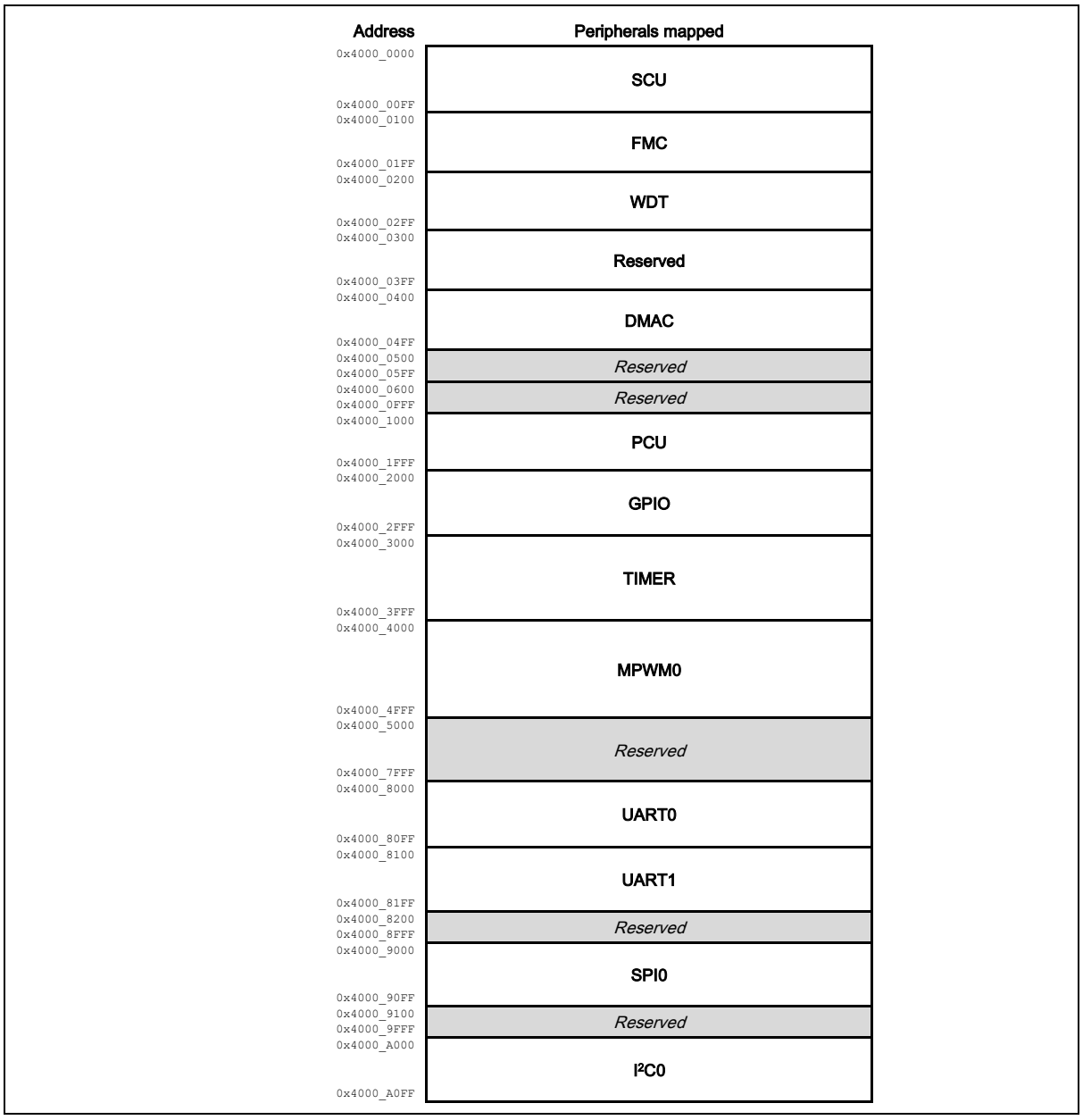


Figure 5. Peripheral Memory Map

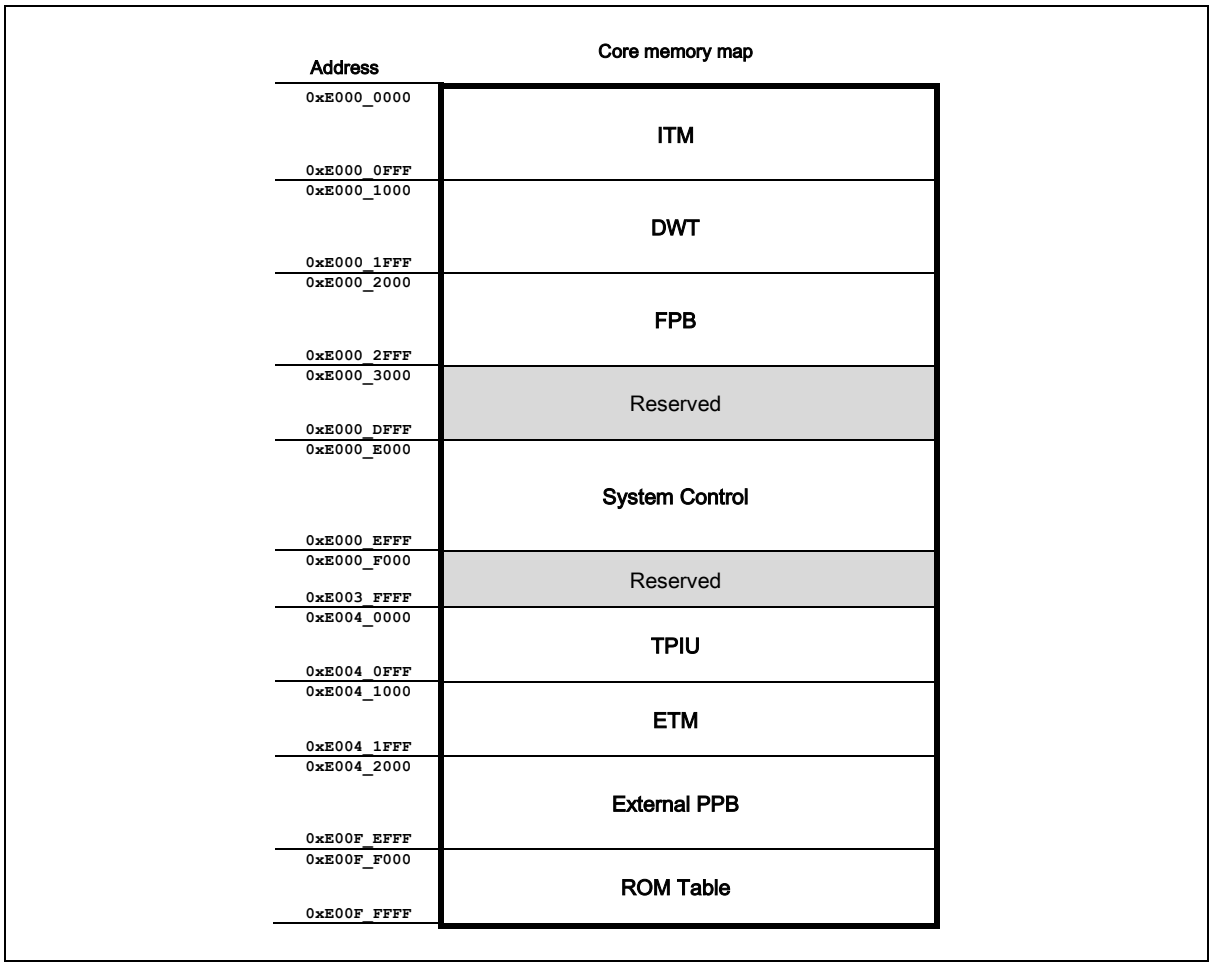


Figure 6. Cortex-M3 Private Memory Map

3.2.2 Embedded SRAM

On chip 8KB 0-wait SRAM can be used for working memory space and program code can be loaded on this SRAM.

3.2.3 Flash memory overview

The AC33Mx064T provides internal 64KB code flash memory and its controller. This is enough to program motor algorithm and general control the system. Self-programming is available and ISP and JTAG programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory.

3.3 Boot mode

3.3.1 Boot mode pins

AC33Mx064T series has a boot mode option to program internal flash memory. Boot mode can be entered by setting BOOT pin to ‘L’ at reset timing (Normal state is ‘H’).

Boot mode supports both of UART/SPI boot:

- UART boot and SPI boot uses TXD0/RXT0 ports.

Pins for the boot mode are listed in Table 4.

Table 4. Boot Mode Pin List

Block	Pin name	Dir	Description
SYSTEM	nRESET/PC10	I	Reset Input signal
	BOOT/PC11	I	‘0’ to enter Boot mode
UART0	RXD0/PC14	I	UART Boot Receive Data
	TXD0/PC15	O	UART Boot Transmit Data
SPI	SS0/PD0	I	SPI Boot Slave Select
	SCK0/PD1	I	SPI Boot Clock Input
	MOSI0/PD2	I	SPI Boot Data Input
	MISO0/PD3	O	SPI Boot Data Output

3.3.2 Boot mode connections

Users can design a target board using any of boot mode ports such as UART mode of UART0. Sample connection diagrams of boot mode are introduced in the following figures:

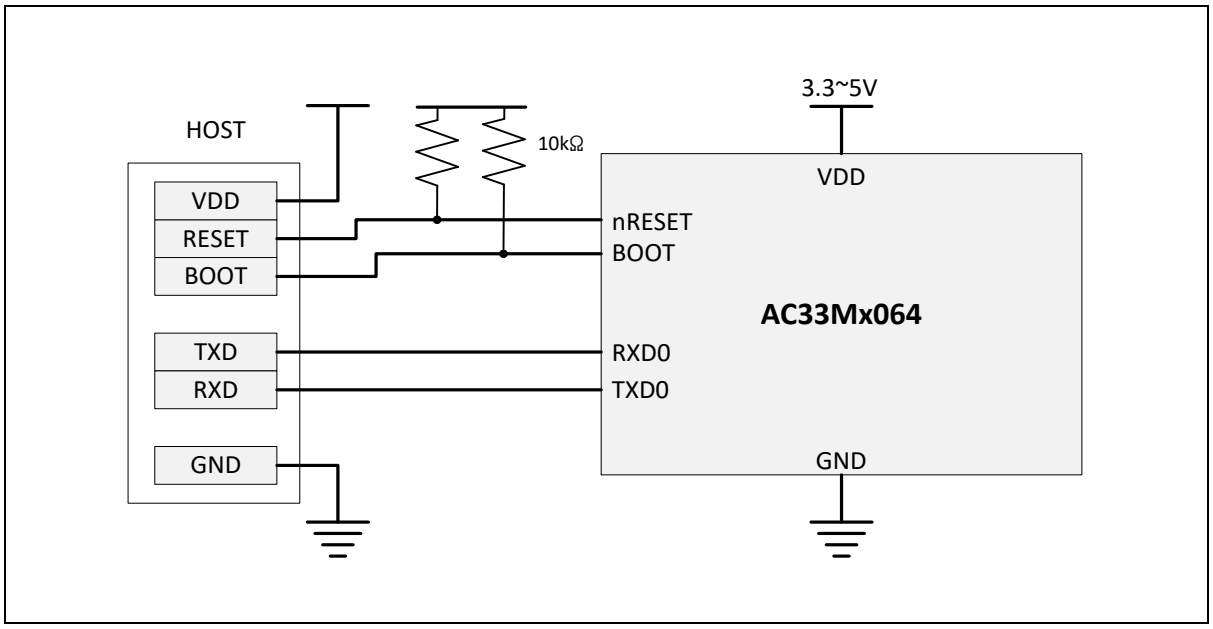


Figure 7. Connection Diagram of UART0 Boot

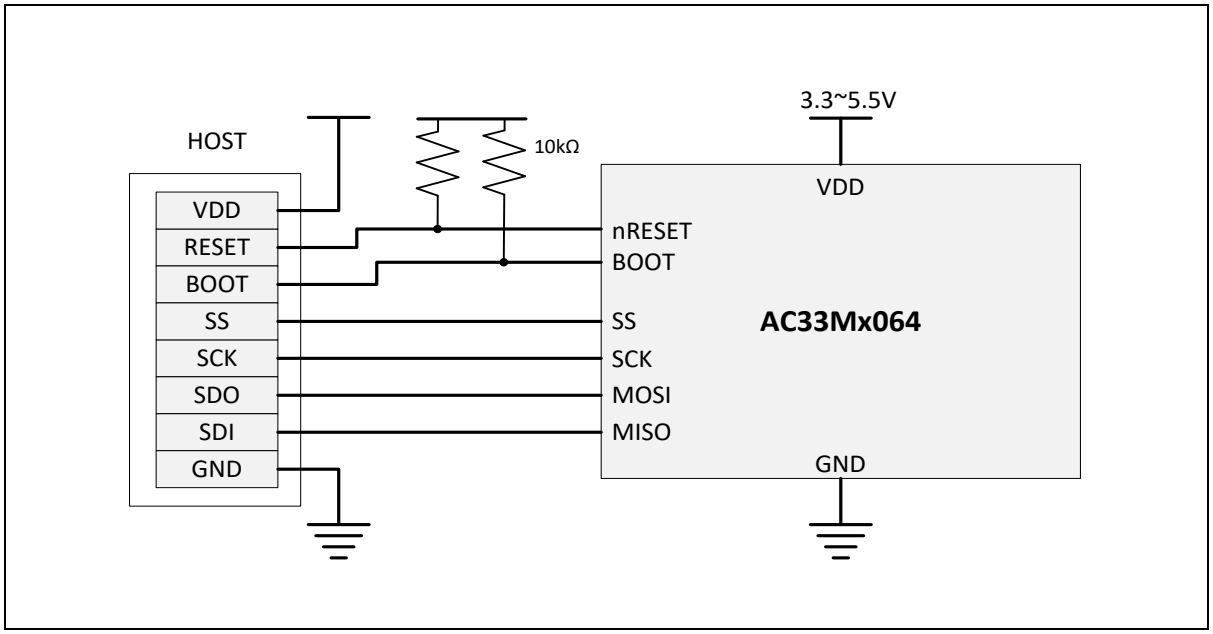


Figure 8. Connection Diagram of SPI Boot

4 System Control Unit (SCU)

AC33Mx064T series has a built-in intelligent power control block which manages system analog blocks and operating modes. System control unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

Table 5 are assigned for SCU block

Table 5. SCU Pins

Pin name	Type	Description
nRESET	I	External reset input
XIN/XOUT	OSC	External crystal oscillator
CLKO	O	Clock output monitoring signal

4.1 SCU block diagram

In this subsection, SCU block diagram is introduced in Figure 9.

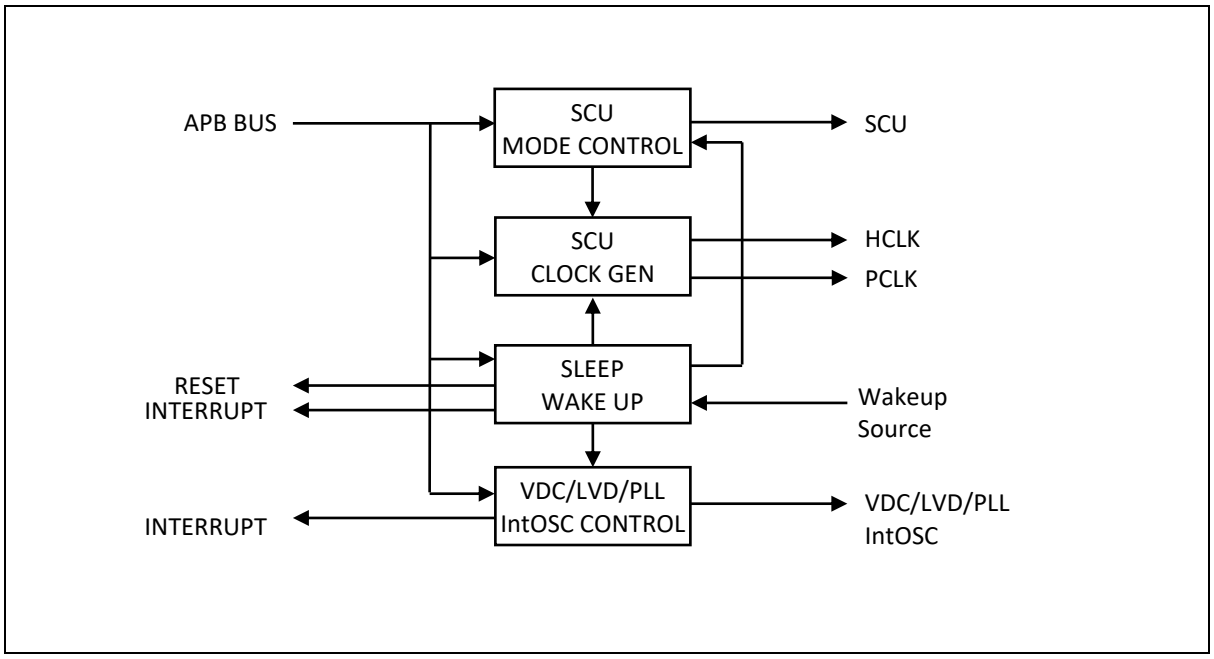
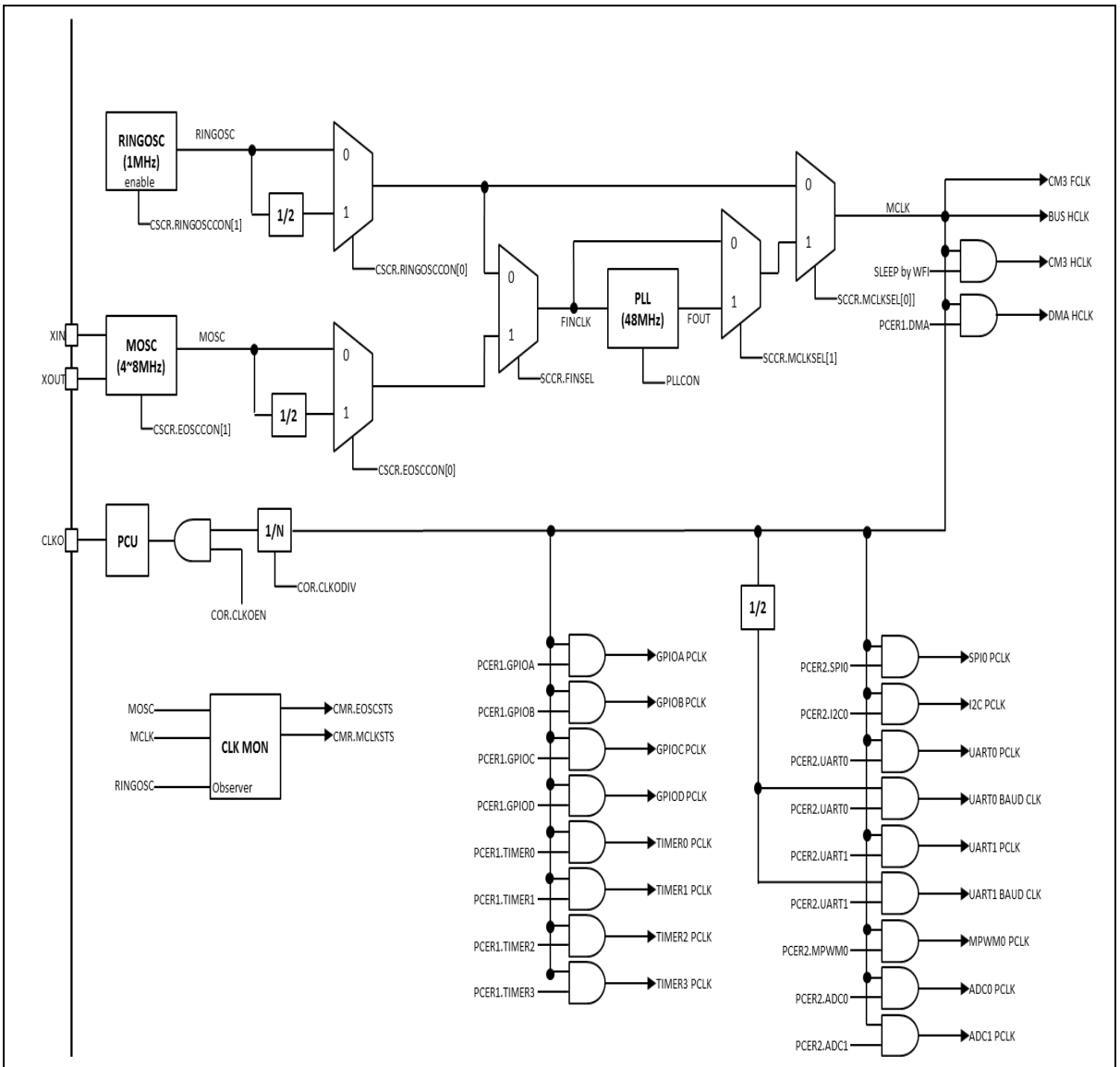


Figure 9. SCU Block Diagram

4.2 Clock system

AC33Mx064T series has two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 10 and Table 6, users can learn about the clock system of AC33Mx064T devices and clock sources.



NOTE : The PLL clock cannot be used as a RINGOSC (1MHz), because the PLL input Frequency ranges from 4MHz to 8MHz.

Figure 10. Clock Tree Configuration

A clock monitoring block is provided for security purpose. The RING OSC clock is a source clock for monitoring other clock sources. The clock monitoring block observes the status of MCLK clock and MOSC clock.

All muxes switching clock sources have glitch-free circuits internally. So clock can be switched without glitch risks. When you try to change the clock mux control, both of clock sources should be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 6. Clock Sources

Clock name	Frequency	Description
MainOSC	X-TAL(4MHz~8MHz)	External Crystal IOSC
PLL Clock	8MHz ~ 48MHz	On Chip PLL
ROSC	1MHz	Internal RING OSC

The PLL can synthesize PLLCLK clock up to 48MHz with FIN reference clock. It also has internal pre-divider and post-divider.

4.2.1 Configuration of miscellaneous clocks

4.2.2 HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M3 CPU requires 2 clocks related with HCLK clock. FCLK and HCLK. FCLK is free running clock and it is always running except power down mode. HCLK can be stopped in the sleep mode.

BUS system and memory systems operated by HCLK clock. Max bus operating clock speed is 48MHz. HCLK frequency should be controlled under 48MHz frequency.

4.2.3 Miscellaneous clock domain

Various clock sources are required for each functional blocks. The SCU provide clock source selection function with its dedicated pre-scaler for each functional blocks. The clock selection mux cannot provide glitch-free function, so the clock is unpredictable at clock selection changing time. Figure 11 shows miscellaneous clock configurations.

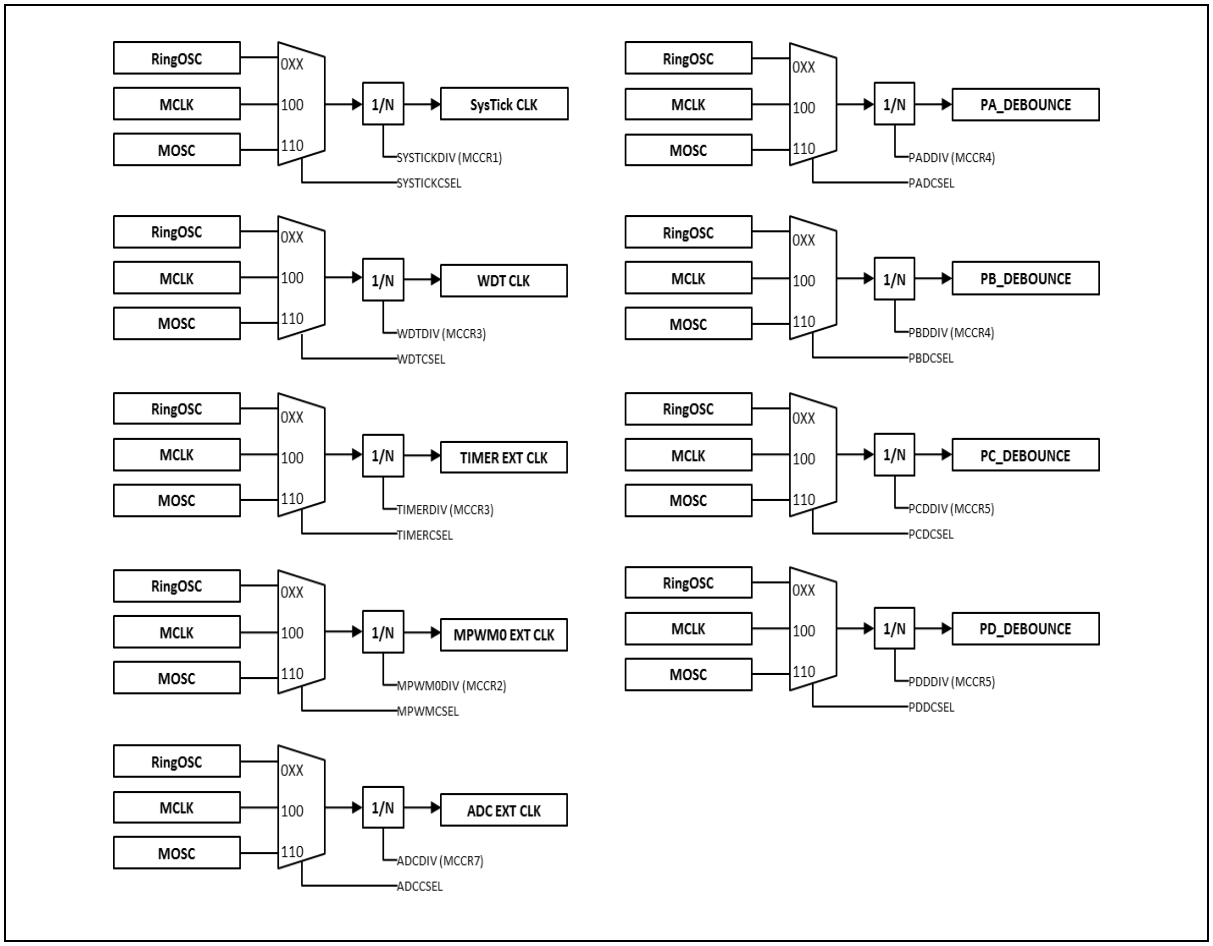


Figure 11. Miscellaneous Clock Configuration

4.2.4 PCLK clock domain

PCLK is a master clock of all peripherals. It can be stopped in power down modes. Each peripheral clock is generated by the PCER1 and PCER2 register set. PCLK clock distributions are showed in Figure 11. Before enabling the PCLK clock of each block, it can't be accessible even when reading its registers.

4.2.5 Clock configuration procedure

After power up, the default system clock is feed by RING OSC (1MHz) clock. RING OSC is default enabled at power up sequence. The other clock sources will be enabled by user controls with the RING OSC system clock.

MOSC clock can be enabled by CSCR register. Before enable MOSC block, the pin mux configuration should be set for XIN, XOUT function. PC12 and PC13 pins are shared with MOSC's XIN and XOUT function - PCCMR and PCCCR registers should be configured properly. After enabling the MOSC block, you must wait for more than 1msec time to ensure stable operation of crystal oscillation.

PLL clock can be enabled by PLLCON register. After enabling the PLL block, you must wait for PLL lock flag. PLL output clock is stable, you can select MCLK for your system requirement. Before changing the system clock, flash access wait should be set to the maximum value. After the system clock is changed, you will need to set flash access wait that you want if necessary.

You can find an example flow chart configuring the system clock in Figure 12.

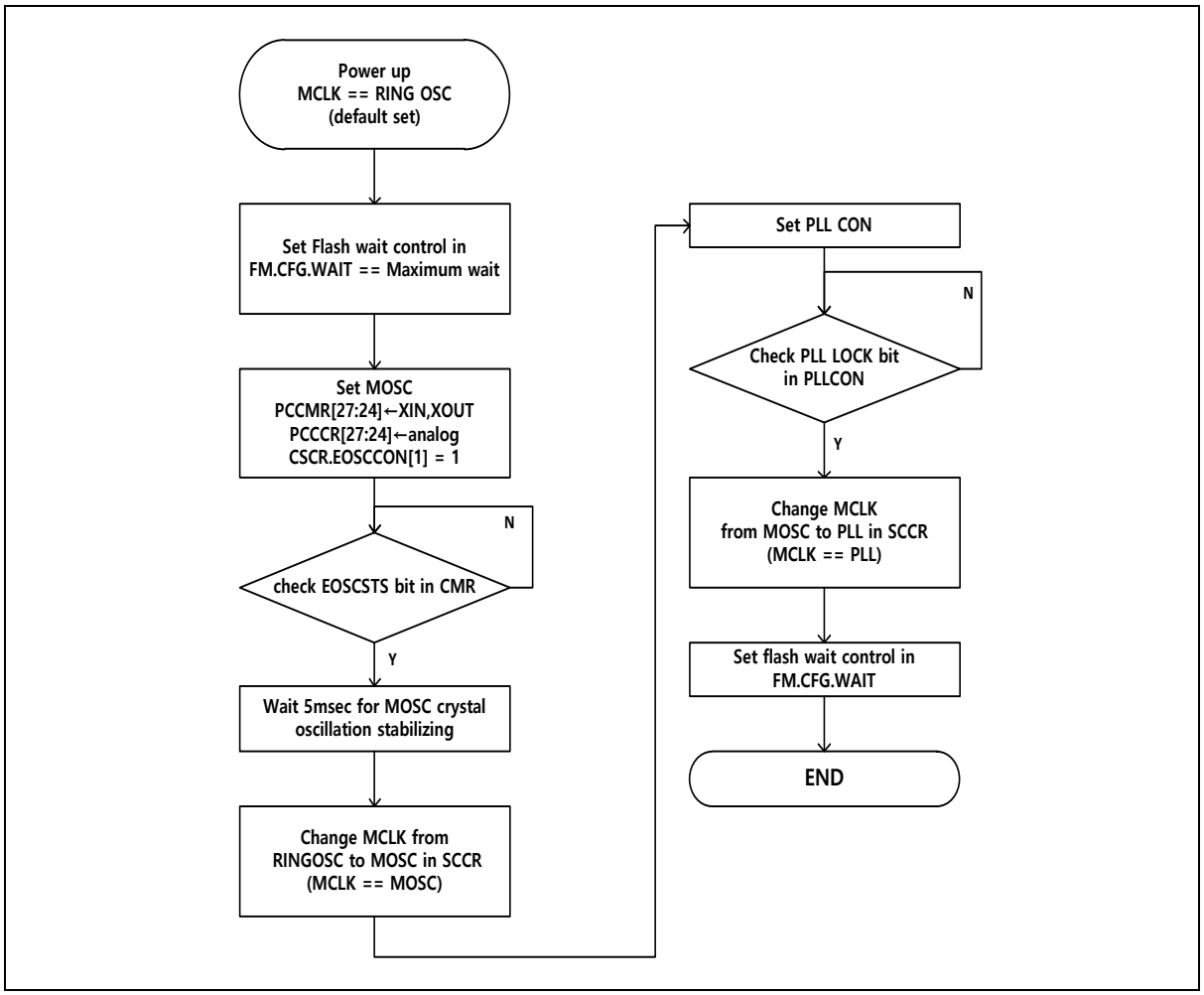


Figure 12. Clock Change Procedure

When you speed up the system clock until max operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for the performance. The wait control recommendation is provided in Table 7.

Table 7. Flash Wait Control Recommendation

FM.CFG.WAIT	FLASH Access Wait	Available Max System clock frequency
000	0 clock wait	Up to 16MHz
001	1 clock wait	Up to 32MHz
010	2 clock wait	Up to 48MHz
011	3 clock wait	Up to 48MHz

4.3 Reset

AC33Mx064T series has two system reset options. One is a cold reset that is effective during power up or down sequence. The other is a warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 8.

Table 8. Reset Sources

	Reset
Reset sources	• nRESET pin • WDT reset • LVD reset • MCLK Fail reset • MOSC Fail reset • S/W reset • CPU request reset

4.3.1 Cold reset

The cold reset is important feature of the chip when power is up. This characteristic will globally affect the system boot. Internal VDC is enabled when VDD power is turn on. Internal VDD level slope will follow by External VDD power slope. Internal PoR trigger level is 1.4V of internal VDC voltage out level. At this time, boot operation is started. The RING OSC clock is enabled and counts 4msec time for internal VDC level stabilizing. In this time, external VDD voltage level should be over than initial LVD level (2.3V). After 4msec counting, the CPU reset is released and start the operation.

Figure 13 shows the power-up process and the initial reset waveforms.

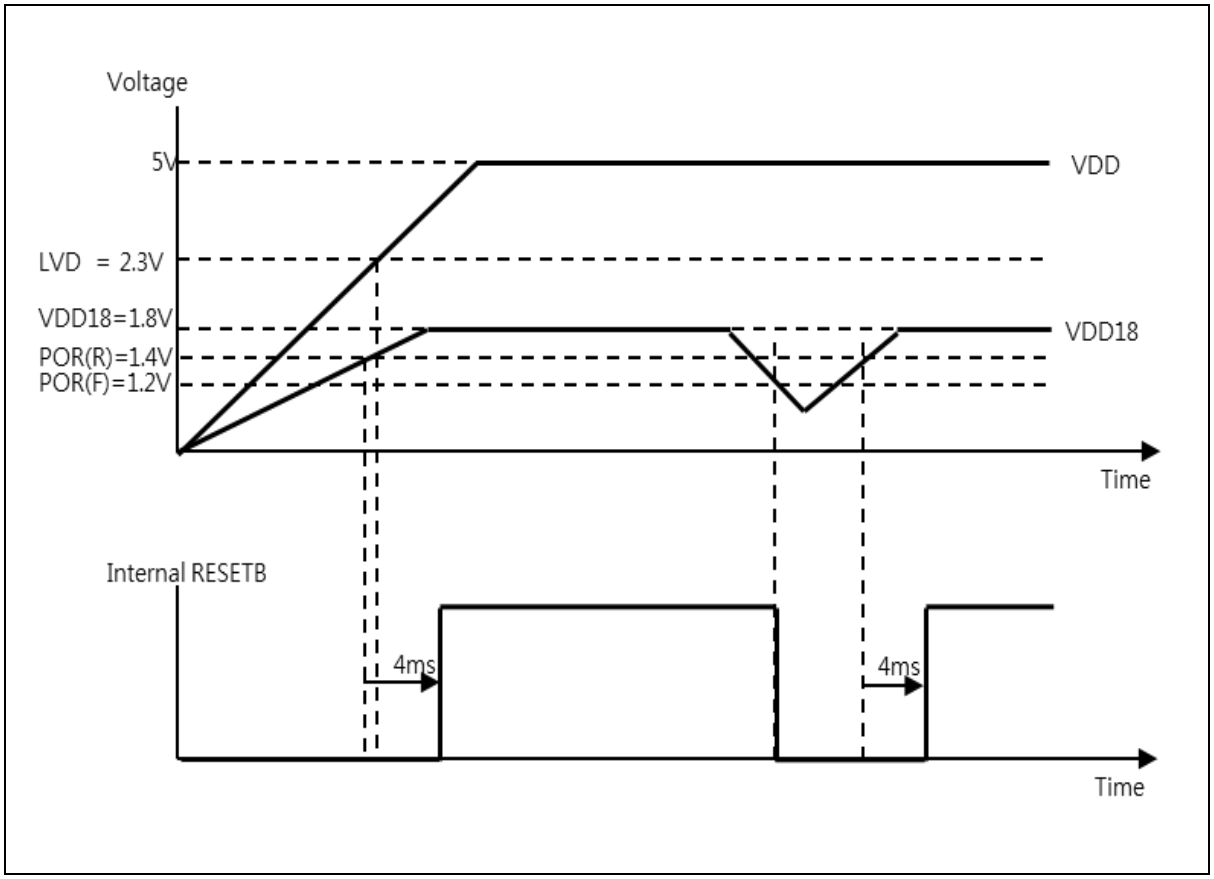


Figure 13. Power-Up POR Sequence

RSSR register shows the POR reset status. The last reset is come from POR, RSSR.PORST is set to “1”. After power up, this bit is always “1”. If abnormal internal voltage drop is occurred during normal operation, the system will be reset and this bit also set to “1”.

When the cold reset applied, all the chip returns to initial state.

4.3.2 Warm reset

The warm reset event has several reset sources and some parts of chip returns to initial state when warm reset condition is occurred. The warm reset source is controlled by RSER register and the status is appeared in RSSR register. The reset for each peripheral blocks is controlled by PRER register. The reset can be masked independently.

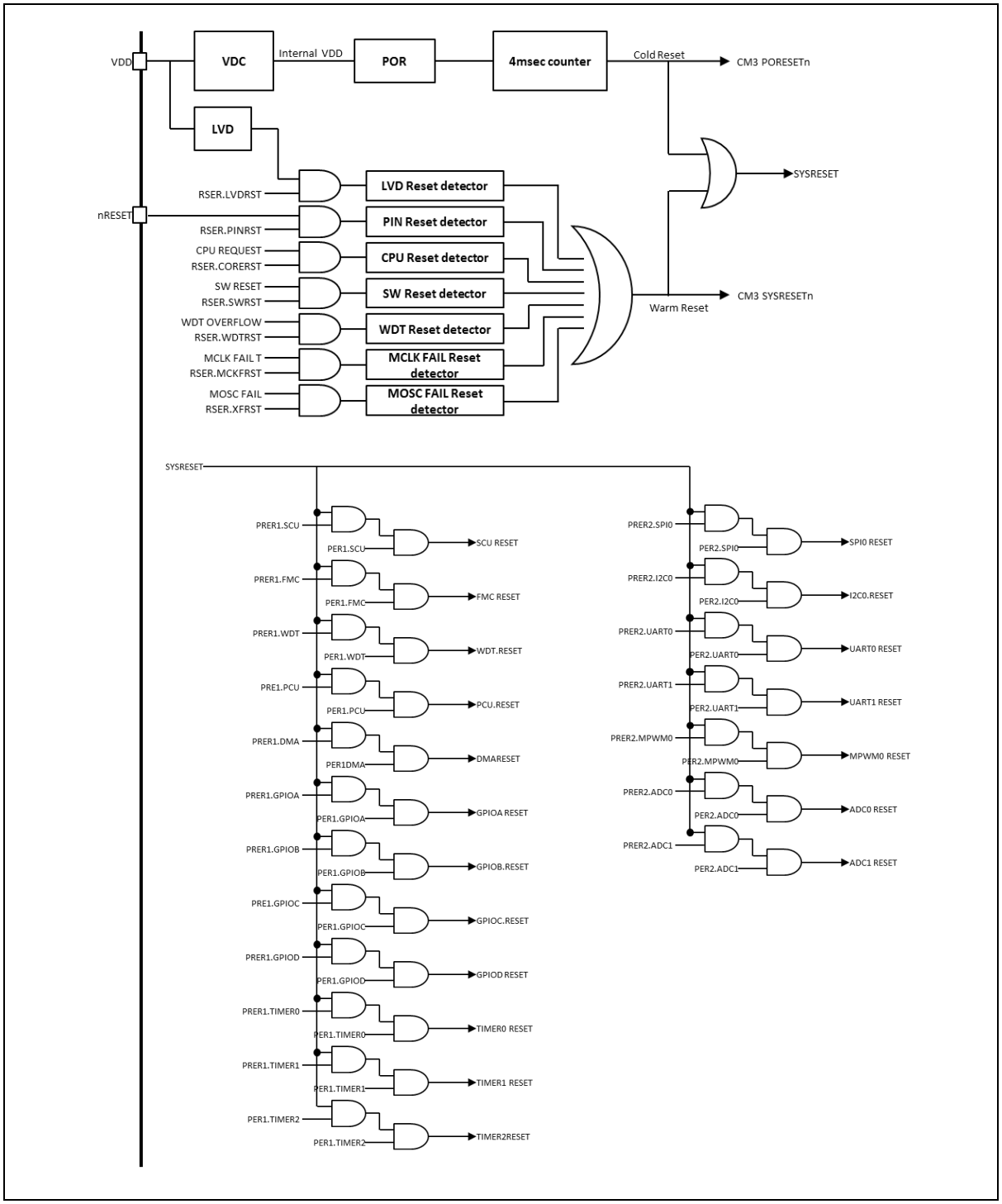


Figure 14. Reset Configuration

4.4 Operation mode

The INIT mode is initial state of the chip when reset is asserted. The RUN mode is max performance of the CPU with high-speed clock system. And the SLEEP mode can be used as the low power consumption mode. The low power consumption is achieved by halting processor core and unused peripherals.

Figure 15 shows the operation mode transition diagram.

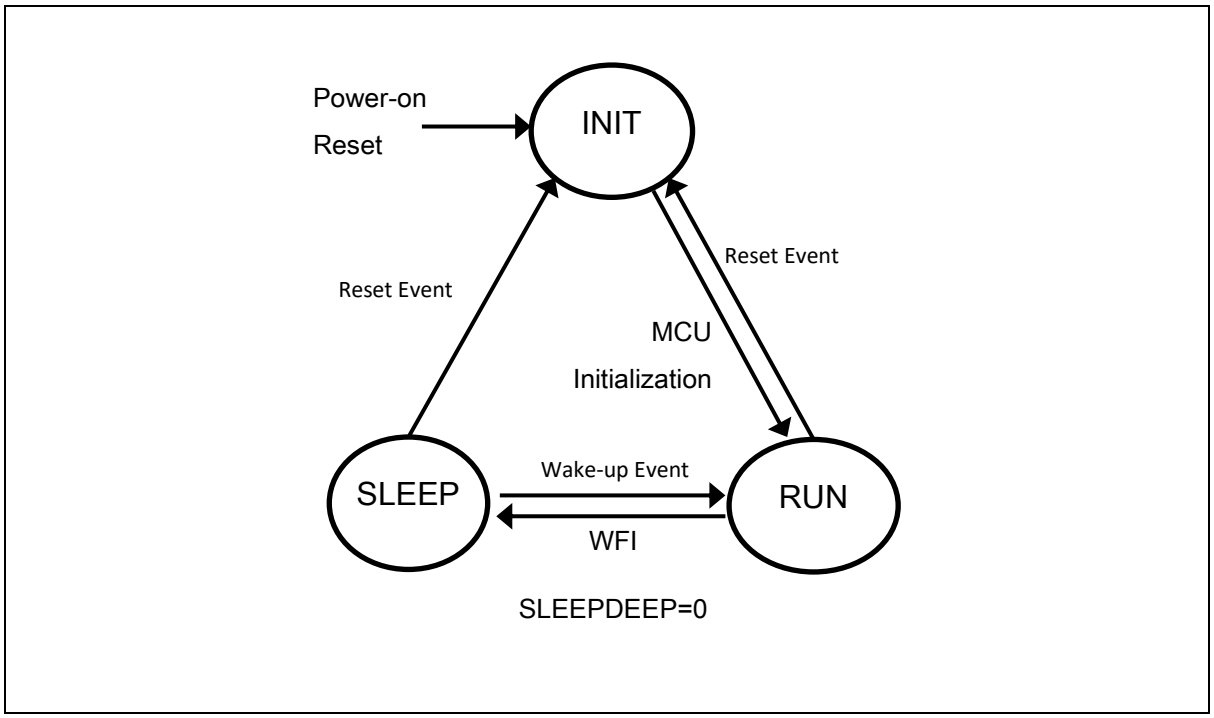


Figure 15. Operation Modes

4.4.1 RUN mode

This mode is to operate the CPU core and the peripheral hardware by using the high-speed clock. After reset followed by INIT state, it is entered into RUN mode.

4.4.2 SLEEP mode

Only the CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the PER and PCER register.

5 Port Control Unit (PCU)

AC33Mx064T MCU's Port Control Unit (PCU) block controls the external input and output (I/O) ports.

The PCU configures and controls external I/Os as listed in the following ways:

- Set external signal directions of each pins
- Set interrupt trigger mode for each pins
- Set internal pull-up register control and open drain control

Table 9 are assigned for PCU blocks.

Table 9. PCU Pins

Pin name	Type	Description
PA	IO	PA0 to PA15
PB	IO	PB0 to PB7
PC	IO	PC0 to PC15
PD	IO	PD0 to PD3

5.1 PCU block diagram

Figure 16 describes PCU in block diagram.

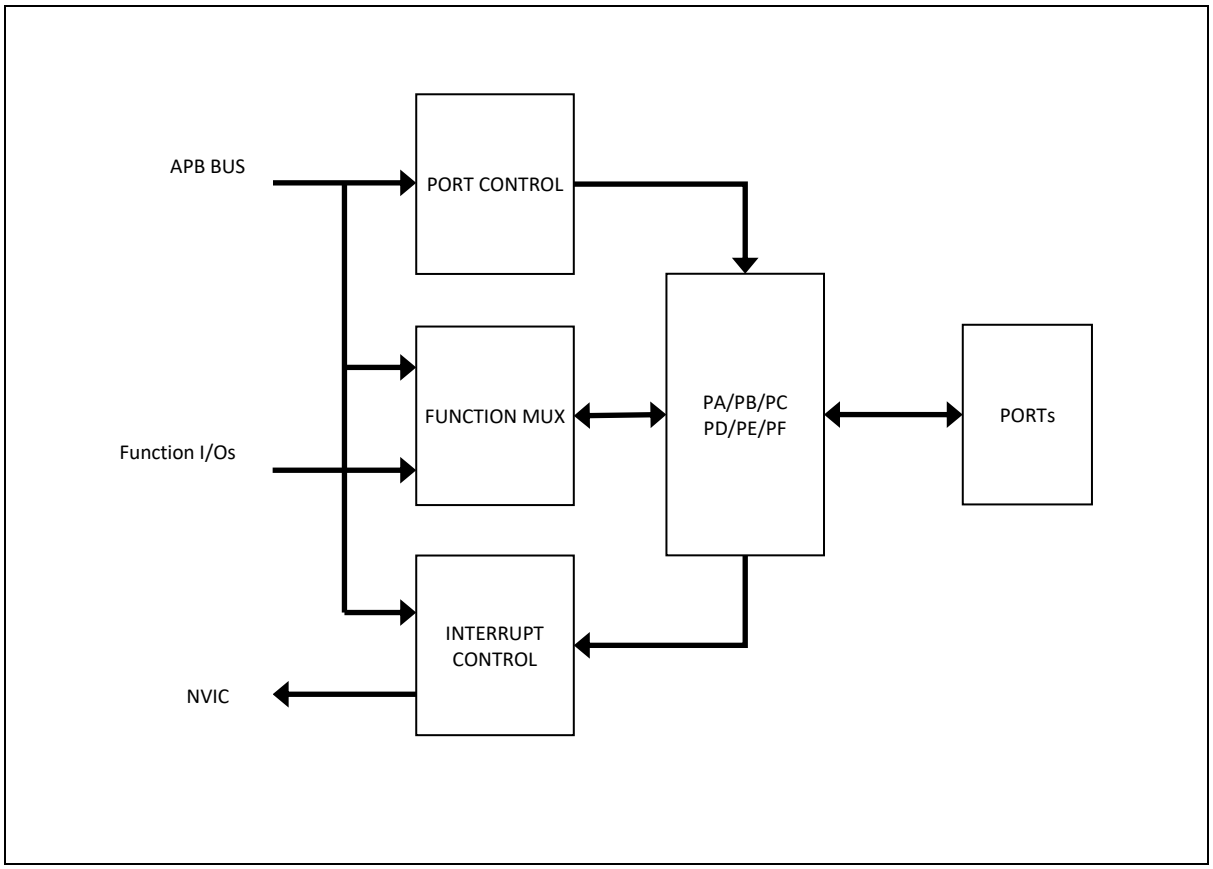


Figure 16. PCU Block Diagram

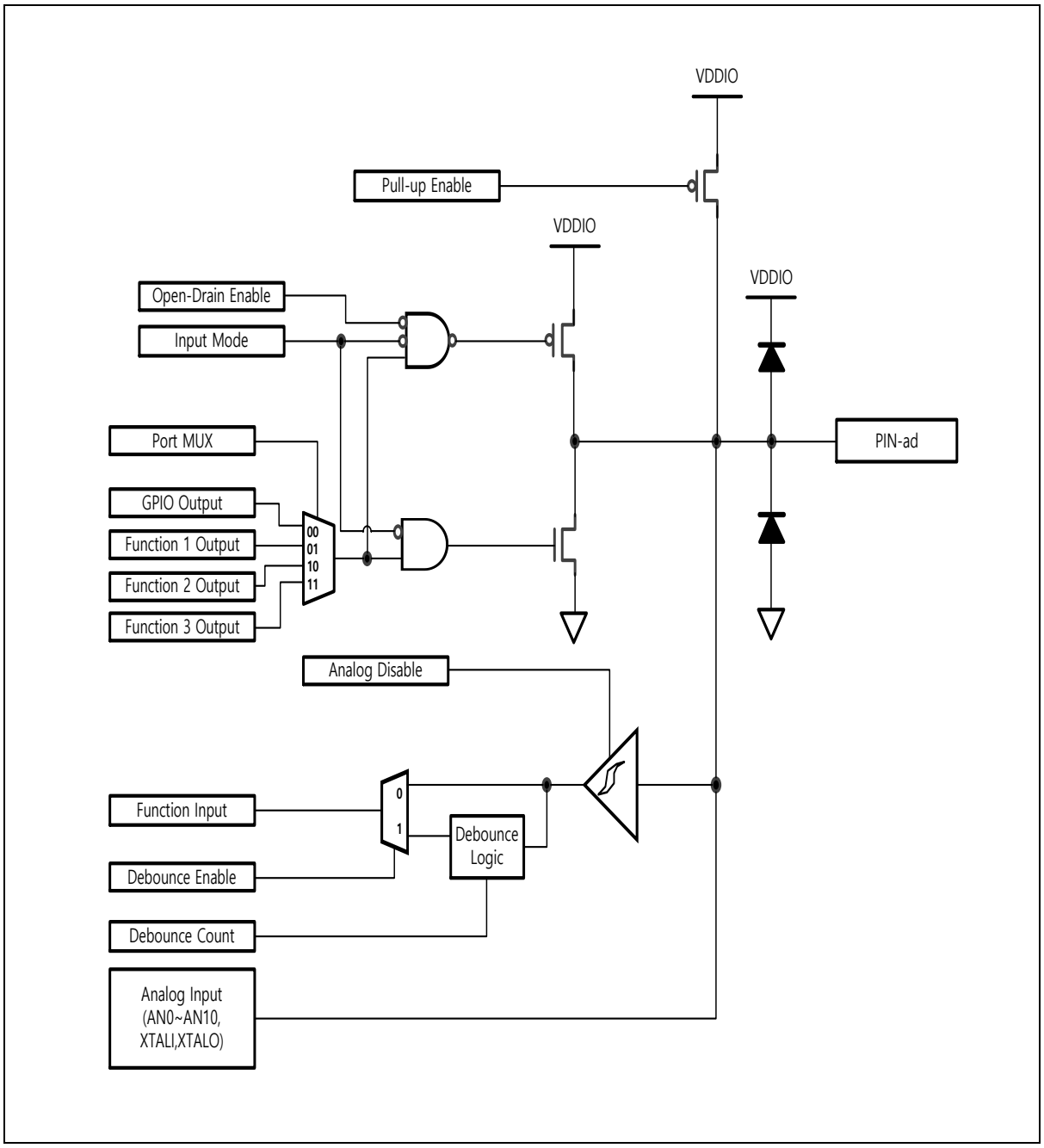


Figure 17. I/O Port Block Diagram (ADC and External Oscillator Pins)

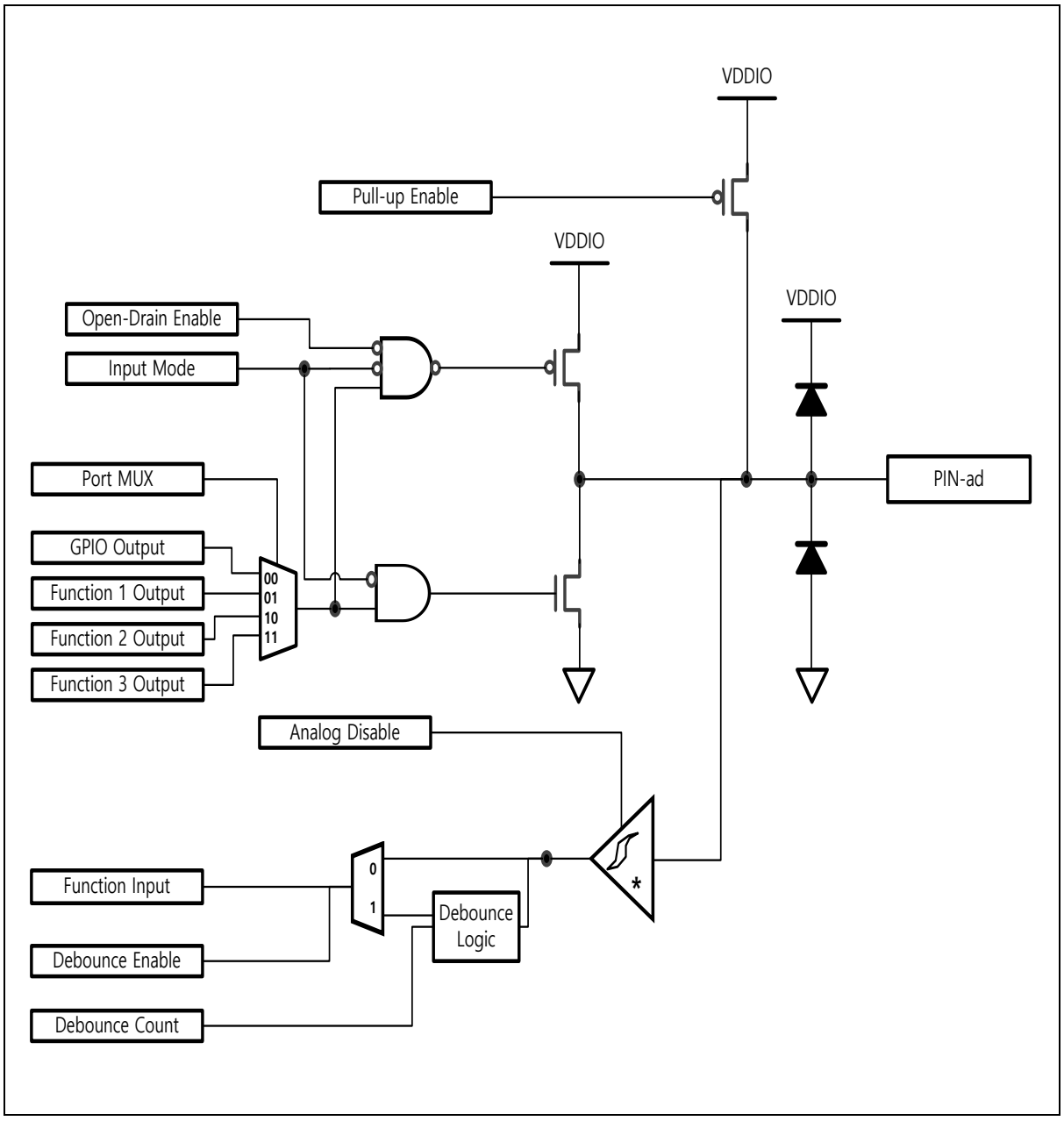


Figure 18. I/O Port Block Diagram (General I/O Pins)

5.2 Pin multiplexing

GPIO pins have alternative function pins. Table 10 shows pin multiplexing information.

Table 10. GPIO Alternative Function

Pin name	Alternative function			
	00	01	10	11
PA0	PA0*			AN0
PA1	PA1*			AN1
PA2	PA2*		WDTO	AN2
PA3	PA3*		STBO	AN3
PA4	PA4*	SS1		AN4
PA5	PA5*	SS2		AN5
PA6	PA6*	T0IO	T2IO	AN6
PA7	PA7*	T1IO	T3IO	AN7
PA8	PA8*	T2IO	T0IO	AN8
PA9	PA9*	T3IO	T1IO	AN9
PA10	PA10*	SS3		AN10
PA11	PA11*			
PA12	PA12*	T0IO		
PA13	PA13*	T1IO		
PA14	PA14*	T2IO		
PA15	PA15*	T3IO		
PB0	PB0*	MP0UH		
PB1	PB1*	MP0UL		
PB2	PB2*	MP0VH		
PB3	PB3*	MP0VL		
PB4	PB4*	MP0WH		
PB5	PB5*	MP0WL		
PB6	PB6*	PRTIN0	T0IO	
PB7	PB7*	OVIN0	T1IO	
PB8				
PB9				
PB10				
PB11				
PB12				
PB13				
PB14				

Table 10. GPIO Alternative Function (continued)

Pin name	Alternative function			
	00	01	10	11
PB15				
PC0	TCK/SWCLK*	RXD1		
PC1	TMS/SWDIO*	TXD1		
PC2	TDO/SWO*	T8IO		
PC3	TDI*	T9IO		
PC4	nTRST*	T0IO		
PC5*	RXD1	T1IO		
PC6*	TXD1	T2IO		
PC7*	SCL0	T3IO		
PC8*	SDA0			
PC9*	CLKO			
PC10	nRESET*	T8IO		
PC11/BOOT*		T9IO		
PC12*			XIN	
PC13*			XOUT	
PC14*	RXD0	MOSI0(2)		
PC15*	TXD0	MISO0(2)		
PD0*	SS0	T8IO		
PD1*	SCK0	T9IO		
PD2*	MOSI0	SCL0		
PD3*	MISO0	SDA0		

NOTES:

1. (*) mark indicates default pin setting.
2. (2) mark indicates secondary port

6 General Purpose I/O (GPIO)

Most of pins except dedicated function pins can be used general I/O ports. General input/output ports are controlled by GPIO block.

GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) select
- External interrupt interface
- Pull up enable or disable

Table 11 are assigned for GPIO blocks.

Table 11. GPIO Pins

Pin name	Type	Description
PA	IO	PA0 to PA15
PB	IO	PB0 to PB7
PC	IO	PC0 to PC15
PD	IO	PD0 to PD3

6.1 GPIO block diagram

Figure 19 describes GPIO in block diagram.

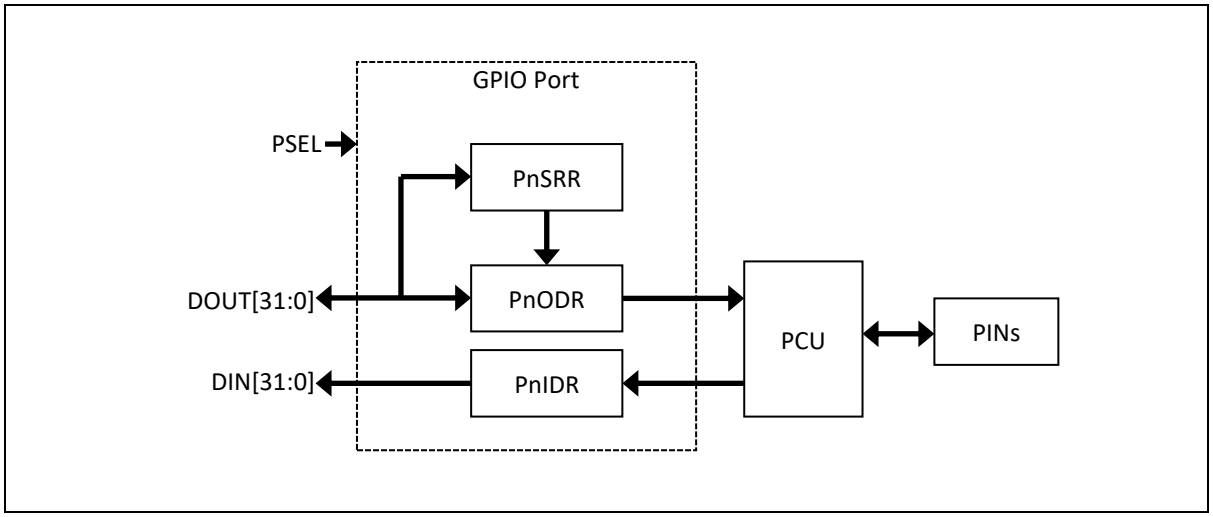


Figure 19. GPIO Block Diagram

7 Flash Memory Controller (FMC)

The Flash Memory Controller (FMC) is an interface controller of internal flash memories:

- 64KB Flash code memory
- 32-bit read data bus width
- Code cache block for fast access mode
- 128-byte page size
- Support page erase and macro erase
- 128-byte unit program

Table 12. Internal flash specification

Item	Description
Size	64KB
Start Address	0x0000_0000
End Address	0x0000_FFFF
Page Size	128-byte
Total Page Count	512 pages
PGM Unit	128-byte
Erase Unit	128-byte

7.1 Flash memory map

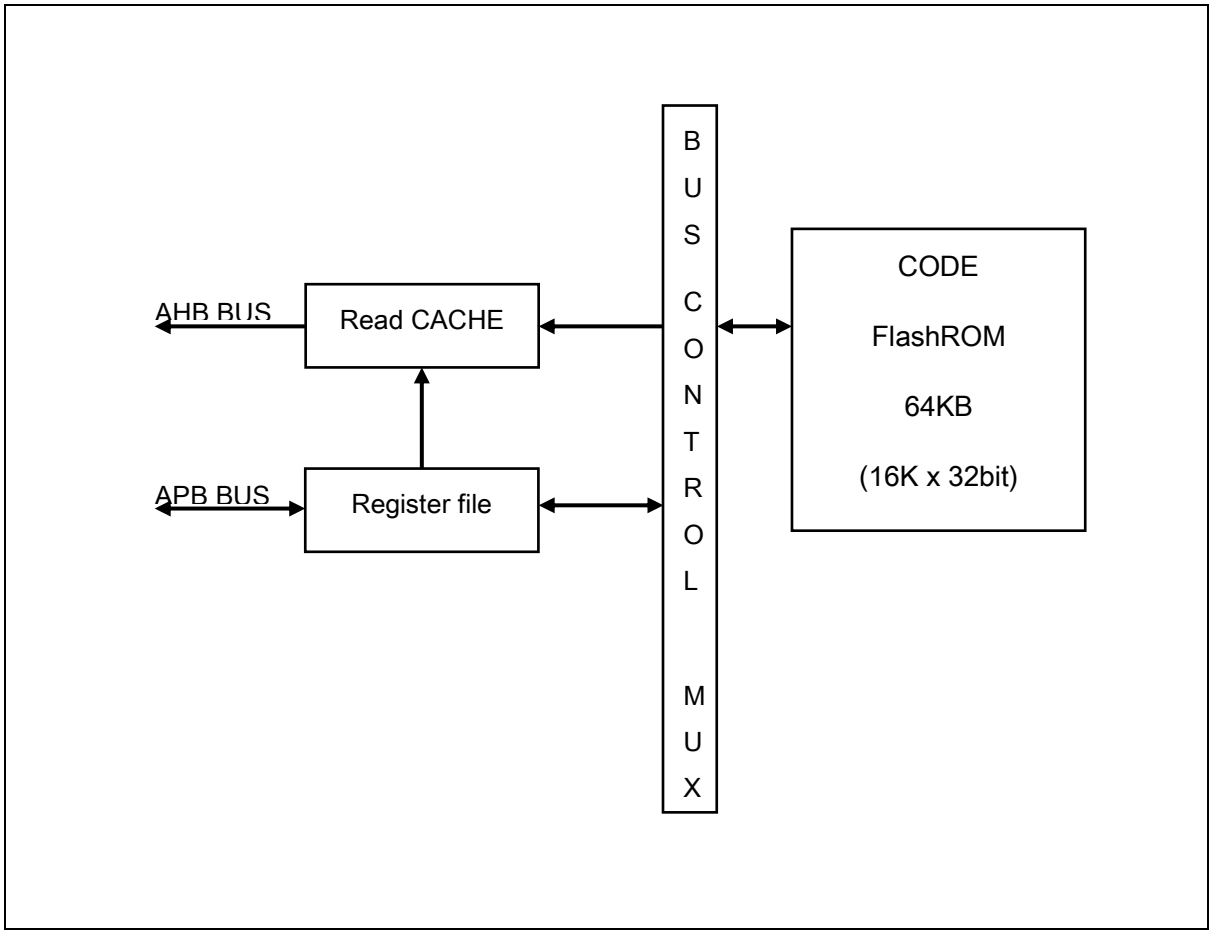


Figure 20. Block Diagram

8 Direct Memory Access Controller (DMAC)

The DMAC is direct memory access controller who can establish the data transfer between memory and peripherals without CPU operation.

DMAC of AC33Mx064T series features followings:

- 4 Channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through peripheral interrupt

8.1 DMAC block diagram

The DMAC block diagram is introduced in Figure 21.

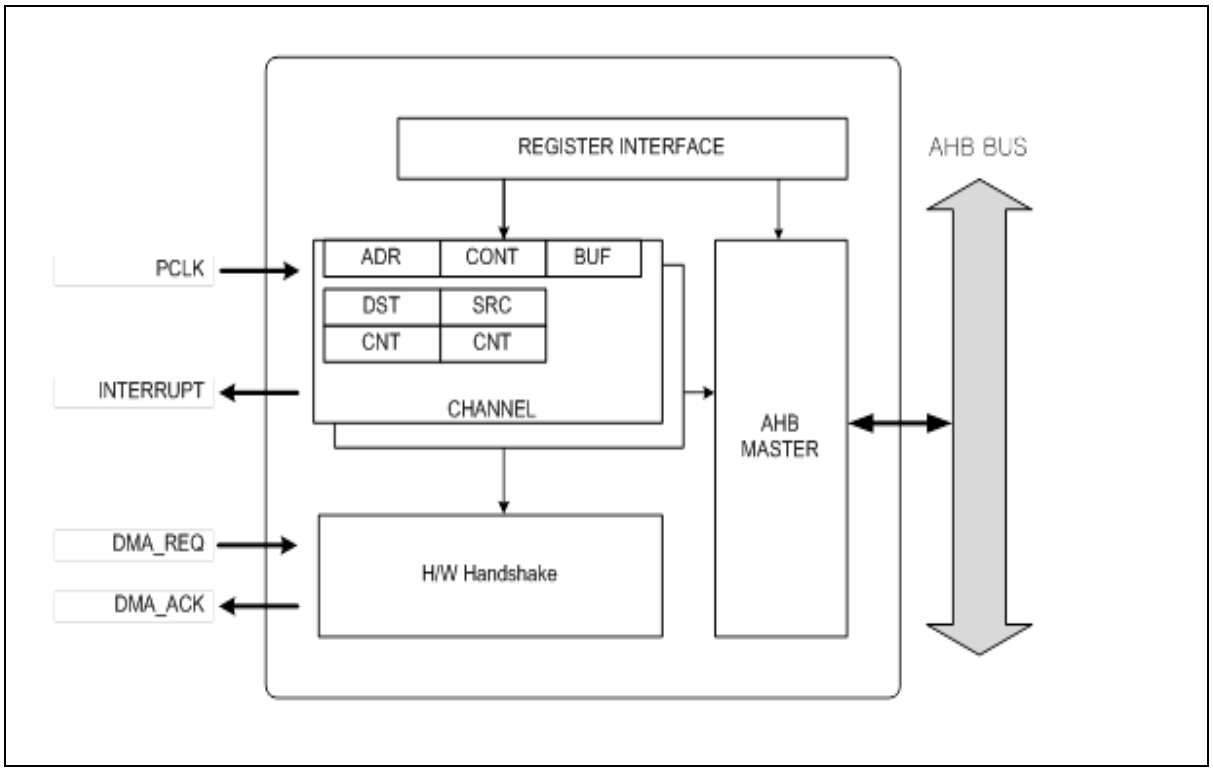


Figure 21. DMAC Block Diagram

9 Watchdog Timer (WDT)

Watchdog timer (WDT) monitors the operation of the MCU and is typically used to detect software errors. When the MCU becomes uncontrollable due to a malfunction, the WDT resets the MCU to recover it.

The AC33Mx064T series has one WDT module built in, which functions as a 32-bit down-counter. Once the WDT counts down to zero while set as a reset source, the MCU gets reset. When it is not used to monitor the MCU, it can be used as a cycle timer along with an interrupt.

WDT of AC33Mx064T series features followings:

- 32-bit down counter
- Select reset or periodic interrupt
- Count clock selection
- Dedicated pre-scaler
- Watchdog underflow output signal

9.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 22.

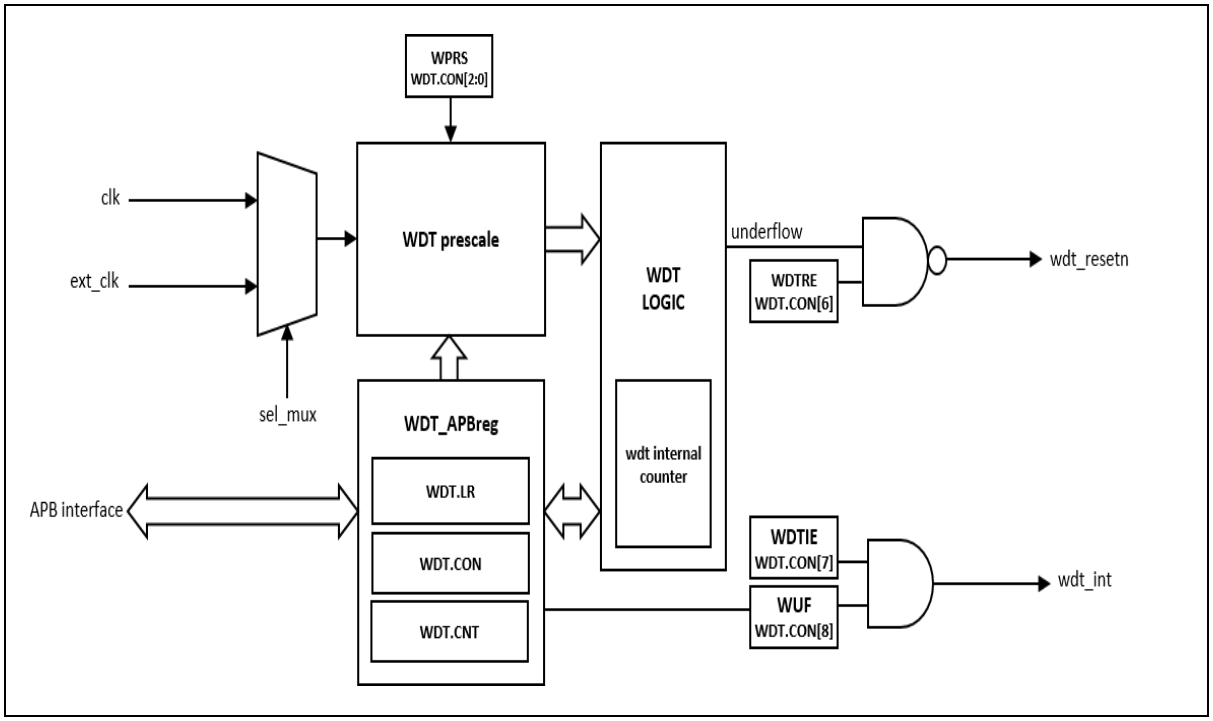


Figure 22. WDT Block Diagram

10 16-bit timer

A timer block of AC33Mx064T consists of 4 channels of 16 bit General purpose timers. They have independent 16 bit counter and dedicated prescaler feeds counting clock. They can support periodic timer, PWM pulse, one-shot timer and capture mode. They can be synchronized together.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source.

16-bit timer of A33M1x series features the followings:

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 10-bit prescaler
- Synchronous start and clear function

Table 13 introduces pins assigned for 16-bit timer.

Table 13. Pin Assignment of 16-bit Timer: External Pins

Pin name	Type	Description
TnIO	I/O	External clock/ capture input and PWM/ one-shot output

10.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 23.

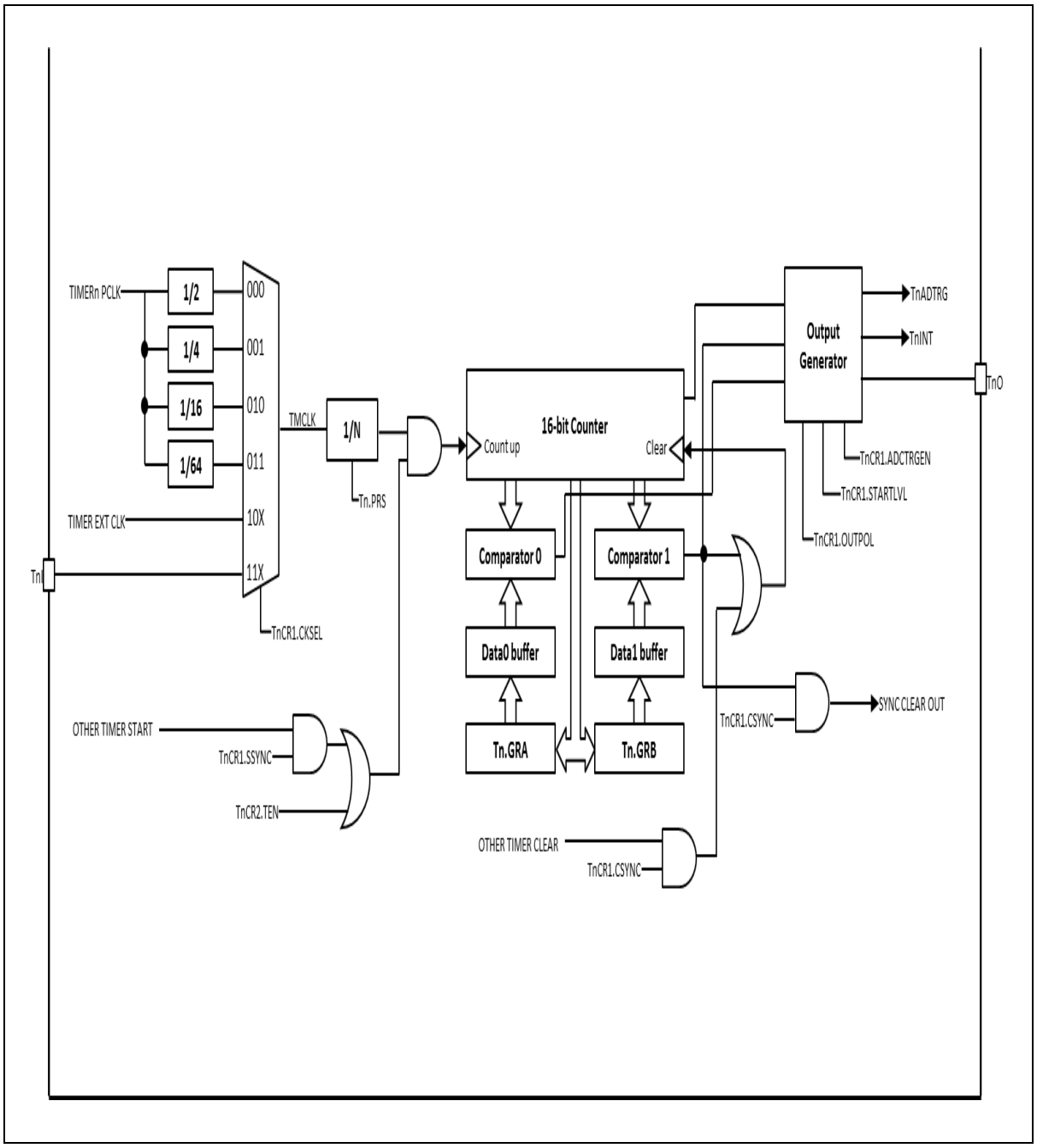


Figure 23. 16-bit Timer Block Diagram

11 Universal Asynchronous Receiver/Transmitter (UART)

2-channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

Programmable interrupt generation function will help to control the communication via UART channel. The UART of AC33Mx064T series features the followings:

- Compatible with 16450
- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable 16-bit fractional baud generator
- Programmable serial communication

  5-, 6-, 7- or 8- bit data transfer

  Even, odd, or no-parity bit insertion and detection

  1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register
- Loop-back control

Table 14 introduces pins assigned for the UART.

Table 14. Pin Assignment of UART: External Pins

Pin name	Type	Description
TXD0	O	UART Channel 0 transmit output
RXD0	I	UART Channel 0 receive input
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input

11.1 UART block diagram

In this section, UART is introduced in block diagrams.

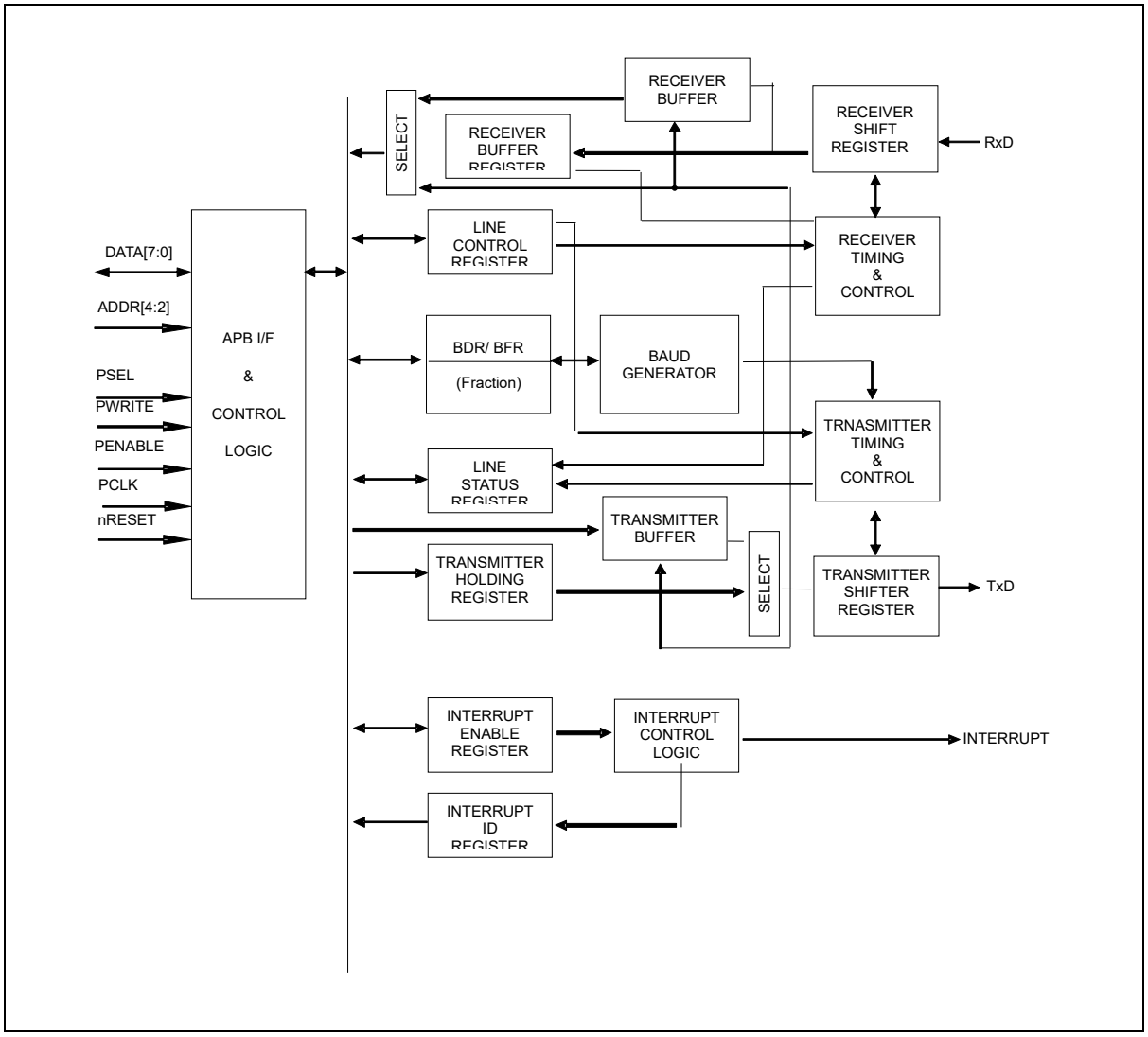


Figure 24. UART Block Diagram

12 Serial Peripheral Interface (SPI)

One Channel serial Interface is provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. 4 signals will be used for SPI communication – SS, SCK, MOSI, and MISO.

- Master or Slave operation.
- Programmable clock polarity and phase
- 8, 9, 16, 17-bit wide transmit/receive register.
- 8, 9, 16, 17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

Table 15. Pin Assignment of SPI: External Pins

Pin name	Type	Description
SS	I/O	SPI Slave select input / output
SCK	I/O	SPI Serial clock input / output
MOSI	I/O	SPI Serial data (Master output, Slave input)
MISO	I/O	SPI Serial data (Master input, Slave output)

12.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 25.

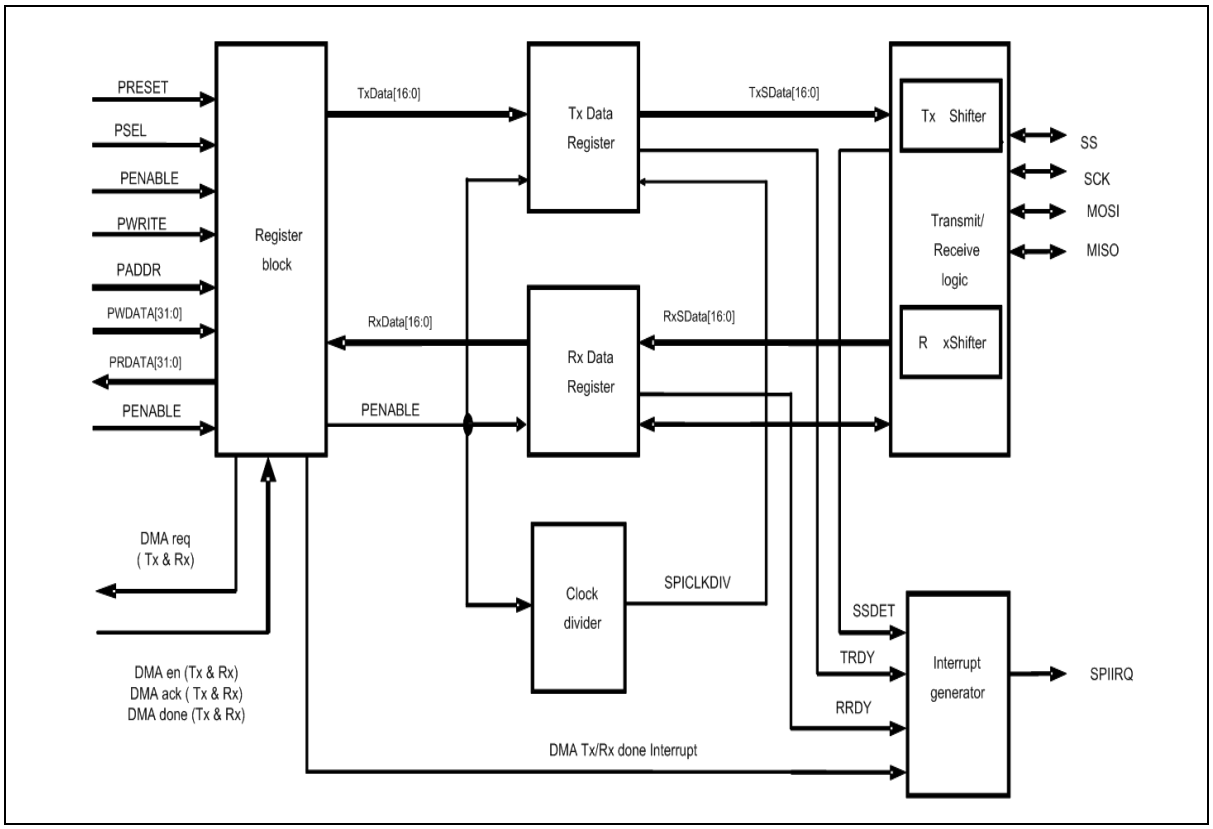


Figure 25. SPI Block Diagram

13 Inter Integrated Circuit (I2C)

Inter-Integrated Circuit (I2C) bus serves as an interface between the microcontroller and the serial I2C bus. It provides two wires, serial bus interface to a large number of popular devices and allows parallel-bus systems to communicate bidirectional with the I2C-bus.

I2C of AC33Mx064T features the followings:

- Master and slave operation
- Programmable communication speed
- Multi-master bus configuration
- 7-bit addressing mode
- Standard data rate of 100/400Kbps
- STOP signal generation and detection
- START signal generation

- ACK bit generation and detection

Table 16. Pin Assignment of I2C: External Pins

Pin name	Type	Description
SCL	I/O	I^2C channel Serial clock bus line (open-drain)
SDA	I/O	I^2C channel Serial data bus line (open-drain)

13.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.

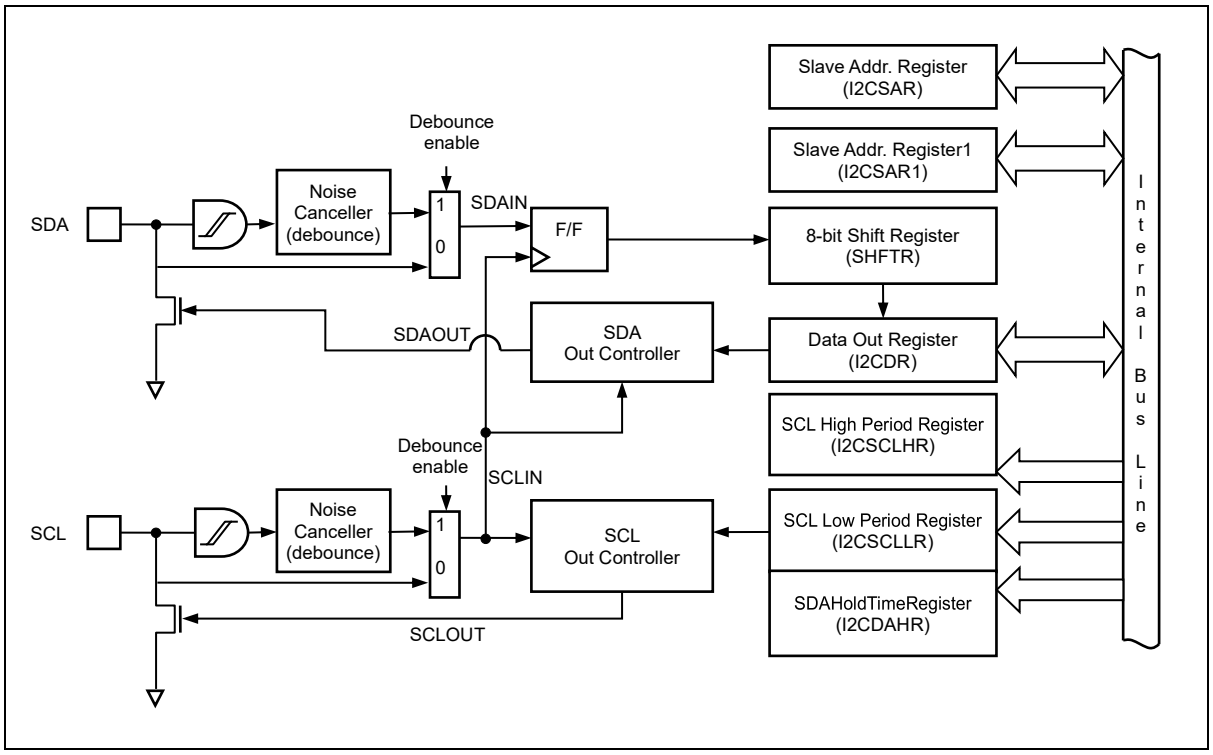


Figure 26. I2C Block Diagram

14 Motor Pulse Width Modulation (MPWM)

The MPWM is Programmable Motor controller which is optimized for 3-phase AC and DC motor control application. It can be used in many other application that need timing, counting and comparison.

The MPWM includes 3 channels, each of which controls a pair of outputs that is turn can control a motor.

MPWM normal mode of AC33Mx064T series features the followings:

- 16-bit Counter
- 6-channel outputs for motor control
- Dead-time supports
- Protection event and over voltage event handling
- 6 ADC trigger outputs
- Interval interrupt mode (period interrupt only)
- Up-down count mode

The MPWM clock source which is MPWM counter clock source will be provided from SCU block. The

MPWM resolution and period will be defined by this MPWM clock configuration. The default MPWM clock is same as RING OSC clock. Before enable MPWM module, the proper MPWM clock selection should be required.

Table 17 introduces pins assigned for MPWM.

Table 17. Pin Assignment of MPWM: External Pins

Pin name	Type	Description
MP0UH	O	MPWM 0 Phase-U H-side output
MP0UL	O	MPWM 0 Phase-U L-side output
MP0VH	O	MPWM 0 Phase-V H-side output
MP0VL	O	MPWM 0 Phase-V L-side output
MP0WH	O	MPWM 0 Phase-W H-side output
MP0WL	O	MPWM 0 Phase-W L-side output
PRTIN0	I	MPWM 0 Protection Input
OVIN0	I	MPWM 0 Over-voltage Input

14.1 MPWM block diagram

Figure 27 describes normal mode of MPWM in block diagram.

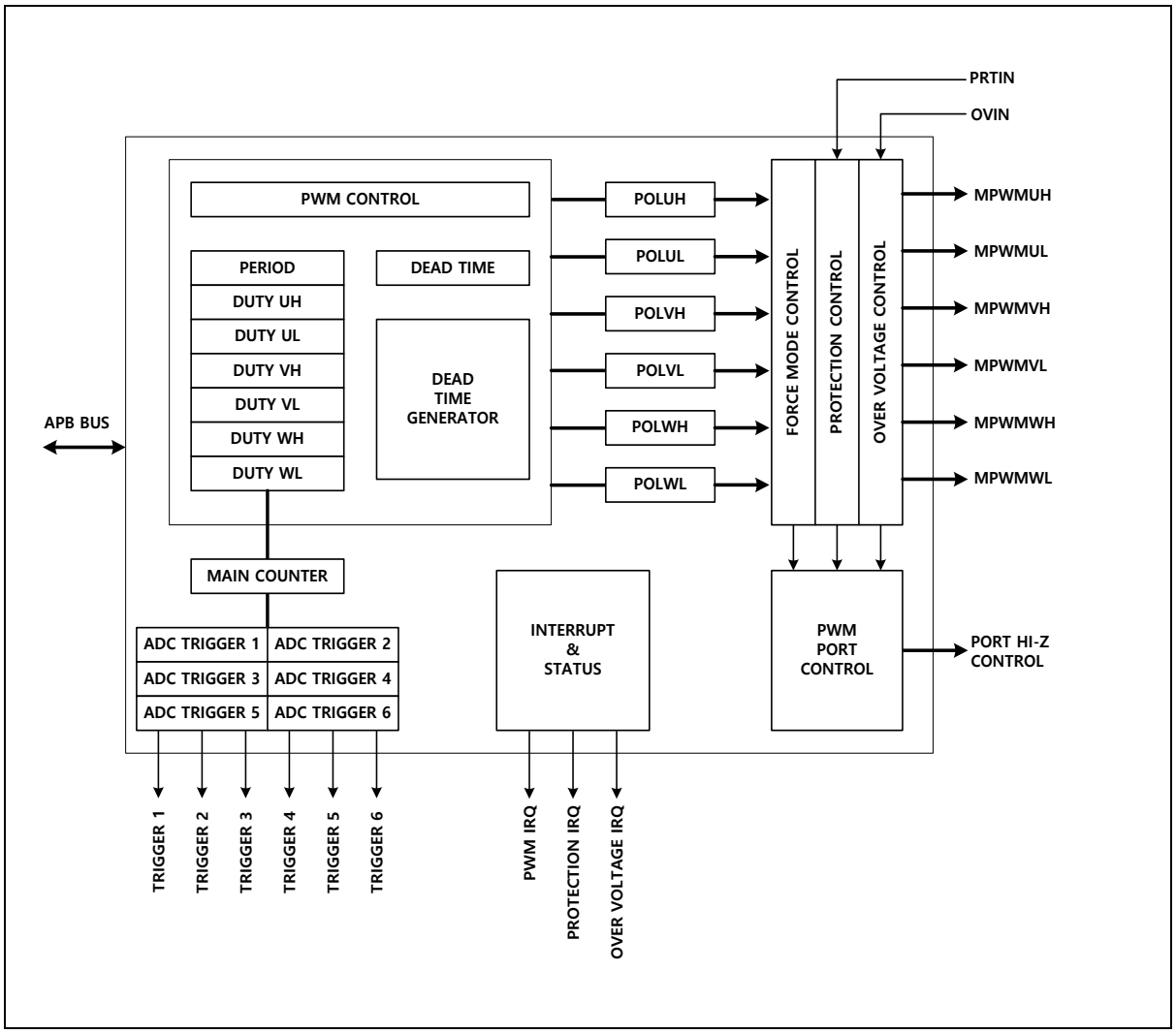


Figure 27. MPWM Block Diagram

15 12-bit Analog-to-Digital Converter (ADC)

ADC block of AC33Mx064T series consists of an independent ADC unit featuring the followings:

- 11 channels of analog inputs (each ADC has 8 input channels)
- Single and Continuous conversion mode
- Up to 8 times sequential conversion supports
- Software trigger supports
- 8 internal trigger sources supports (PWMs, timers)
- Adjustable sample and hold time

Table 18 introduces pins assigned for ADC.

Table 18. Pin Assignment of ADC: External Pins

Pin name	Type	Description
VDD	P	Analog Power(3.0V~5V)
VSS	P	Analog GND
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10

15.1 12-bit ADC block diagram

In this section, 12-bit ADC is described in a block diagram in Figure 28.

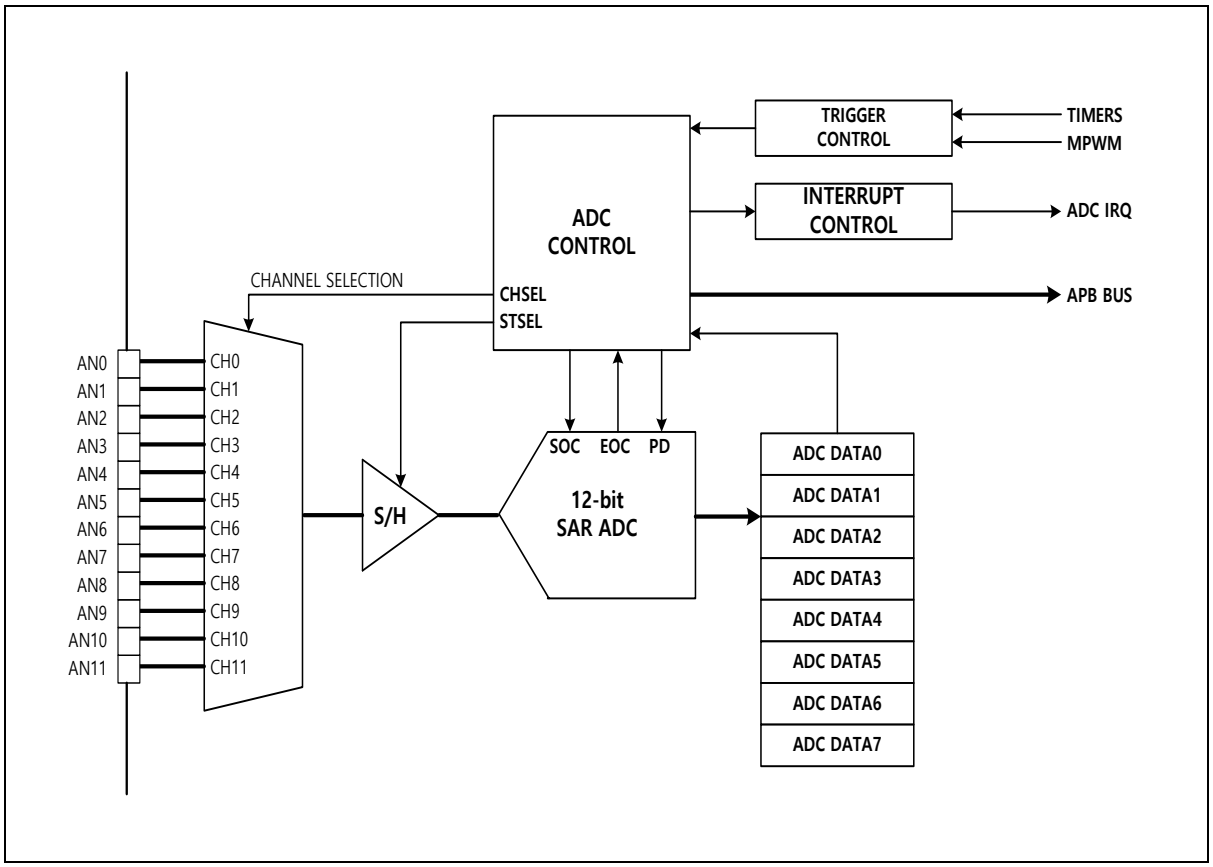


Figure 28. 12-bit ADC Block Diagram

16 Electrical characteristics

16.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 19. Absolute Maximum Rating

Parameter	Symbol	min	max	unit
Power supply (V_{DD})	V_{DD}	-0.5	+6	V
Analog power supply (AV_{DD})	AV_{DD}	-0.5	+6	V
VDC output voltage	V_{DD18}			V
Input high voltage		-	V_{DD}+0.5	V
Input low voltage		V_{SS} – 0.5	-	V
Output low current per pin	I_{OL}		2.5	mA
Output low current total	$\sum I_{OL}$		25	mA
Output high current per pin	I_{OH}		-2.5	mA
Output high current total	$\sum I_{OH}$		25	mA
Input main clock range		0.4	8	MHz
Operating frequency		-	48	MHz
Storage temperature	T_{ST}	-55	+125	℃
Operating temperature	T_{OP}	-40	+105	℃
Power supply (V_{DD})	V_{DD}	-0.5	+6	V

16.2 DC characteristics

Table 20. Recommended Operating Condition

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Supply voltage	V_{DD}		3.0		5.5	V
Supply voltage	AV_{DD}		3.0	5.0	5.5	V
Operating frequency	f	OSC_{MAIN}	4		8	MHz
		OSC_{INT}		1		MHz
		PLL	4		48	MHz
Operating temperature	T_{OP}	T_{OP}	-40		+105	℃

Table 21. DC Electrical Characteristics

(VDD = +5V, Ta = 25 ℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Input low voltage	V_{IL}	Schmitt input	-	-	$0.2V_{DD}$	V
Input high voltage	V_{IH}	Schmitt input	$0.8V_{DD}$	-	-	V
Output low voltage	V_{OL}	I_{OL} = 3mA	-	-	V_{SS}+1.0	V
Output high voltage	V_{OH}	I_{OH} = -3mA	V_{DD}–1.0	-	-	V
Input high leakage	I_{IH}				4	μA
Input low leakage	I_{IL}		-4			μA
Pull-up resister	R_{PU}	R_{MAX}:V_{DD}=3.0V R_{MIN}:V_{DD}=5V	30	-	70	kΩ

16.3 Current consumption

Table 22. Current Consumption in Each Mode

(Temperature: +25℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Normal operation	$I_{DD\ NORM}$	OSC_{RING}=RUN OSC_{MAIN}=8MHz HCLK=48MHz	-	20	-	mA
Sleep mode	$I_{DD\ SLEEP}$	OSC_{RING} =RUN OSC_{MAIN} =8MHz HCLK =48MHz	-	8.3	-	mA

NOTE: uart en, 1 port toggle @5V

16.4 POR electrical characteristics

Table 23. POR Electrical Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	V_{DD18}		1.6	1.8	2.0	V
Operating current	I_{DD}	Typ. <6μA If always on	-	60	-	nA
POR set level	V_{RISING}	V_{DD} rising (slow)	1.3	1.4	1.55	V
POR reset level	$V_{FALLING}$	V_{DD} falling (slow)	1.1	1.2	1.4	V

16.5 LVD electrical characteristics

Table 24. LVD Electrical Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	V_{DD}		1.7		5	V
Operating current	I_{DD}	Typ. <6μA when always on	-	1	-	mA
LVD set level 0	V_{LVD0}	V_{DD} falling (slow)	1.6	1.8	2.0	V
LVD set level 1	V_{LVD1}	V_{DD} falling (slow)	2.0	2.2	2.5	V
LVD set level 2	V_{LVD2}	V_{DD} falling (slow)	2.5	2.7	3.0	V
LVD set level 3	V_{LVD3}	V_{DD} falling (slow)	3.9	4.3	4.6	V

16.6 VDC electrical characteristics

Table 25. VDC Electrical Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	V_{DD}		3.0	-	5.5	V
VDC output voltage	V_{OUT}	@RUN	1.62	1.8	1.98	V
		@STOP	1.4	1.8	2.0	V
Regulation current	I_{OUT}				100	mA
Drop-out voltage	V_{DROP}	V_{DD}=3.0V I_{OUT}=100mA	-	-	200	mV
Current consumption	$I_{DD\ NORM}$	@RUN	-	100	150	μA
	$I_{DD\ STOP}$	@STOP	-	1	2	μA

16.7 External OSC characteristics

Table 26. External OSC Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Condition	Min	Typ	Max	unit
Operating voltage	V_{DD}		3.0	-	5.5	V
IDD	I_{DD}	@4MHz/5V	-	240		μA
Frequency	f_{osc}		4	8	10	MHz
Output voltage	V_{OUT}		1.2	2.4	-	V
Load capacitance	C_L		5	22	35	pF

16.8 PLL electrical characteristics

Table 27. PLL Electrical Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	V_{DD}		3.0		5.5	V
Output frequency	f_{OUT}		4		48	MHz
Operating current	I_{DD}	@50MHz		1.3		mA
Duty	f_{DUTY}		40	-	60	%
P-P jitter	JITTER	@Lock			500	Ps
VCO	VCO		20		80	MHz
Input frequency	f_{IN}		4		8	MHz
Locking time	t_{LOCK}				1	ms

16.9 ADC electrical characteristics

Table 28. ADC Electrical Characteristics

(Temperature: -40℃ ~to +105℃)

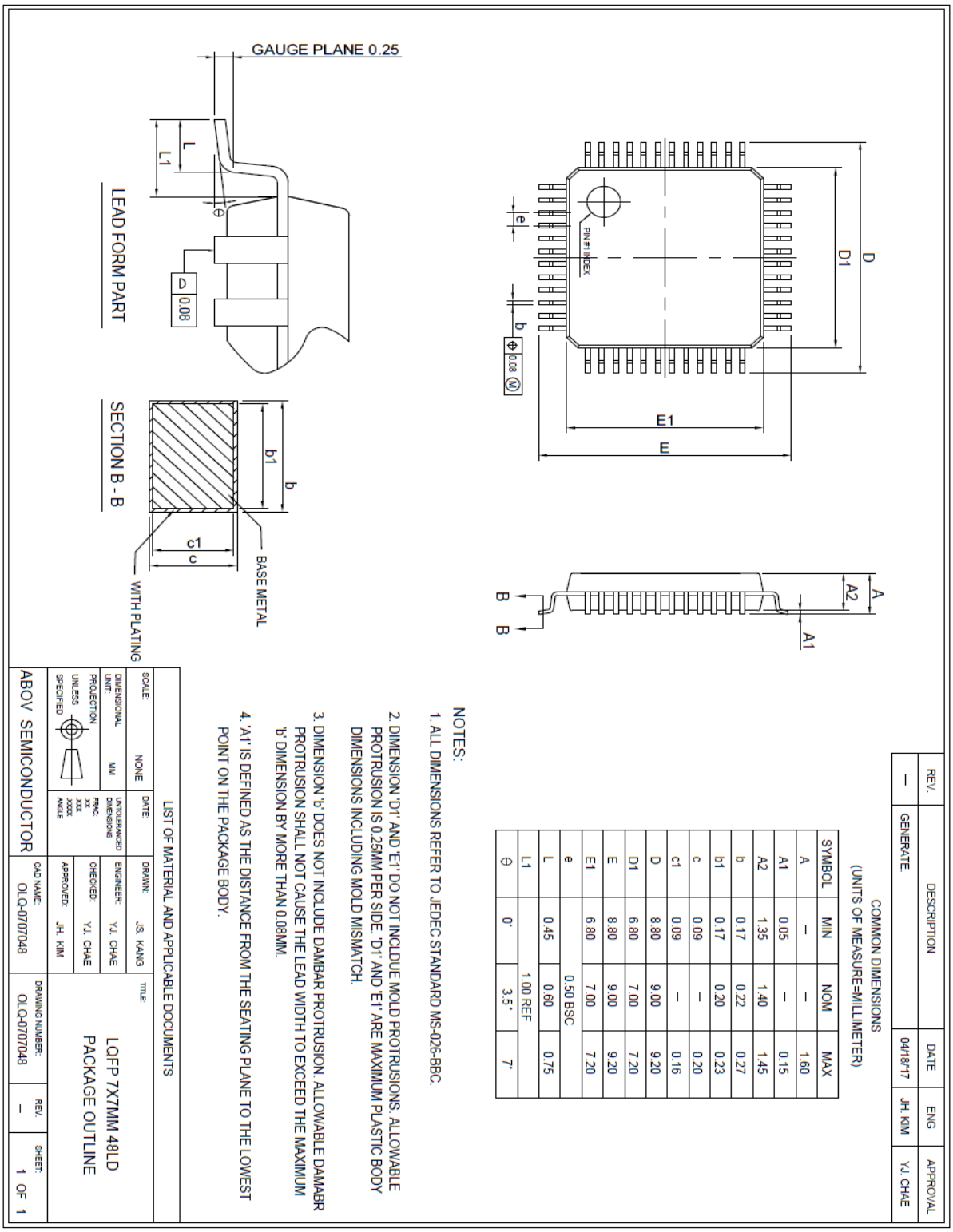
Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	AV_{DD}		3.0	5	5.5	V
Reference voltage	AV_{REF}		3.0	5	5.5	V
Resolution				12		Bit
Operating current	AI_{DD}				2.8	mA
Analog input range			0		AV_{DD}	V
Conversion rate				-	1.6	Msps
Operating Frequency	f_{ACLK}				25	MHz
DC Accuracy	INL			±2.5		LSB
	DNL			±1.0		LSB
Offset Error				±1.5		LSB
Full Scale Error				±1.5		LSB
SNDR	SNDR			68		dB
THD				-70		dB

NOTES:

1. DNL: Maximum deviation between actual steps and the ideal one.
2. INL: Integral Linearity Error: maximum deviation between any actual transition and the end point

17 Package information

17.1 48 LQFP package information



SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: YJ. CHAE	
PROJECTION UNLESS SPECIFIED	FRAC: XX .XX .XXX ANGLE	CHECKED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-0707048	APPROVED: JH. KIM	DRAWING NUMBER: OLQ-0707048 / REV: — / SHEET: 1 OF 1

Figure 29. 48 LQFP Package Outline

17.2 32 LQFP package information

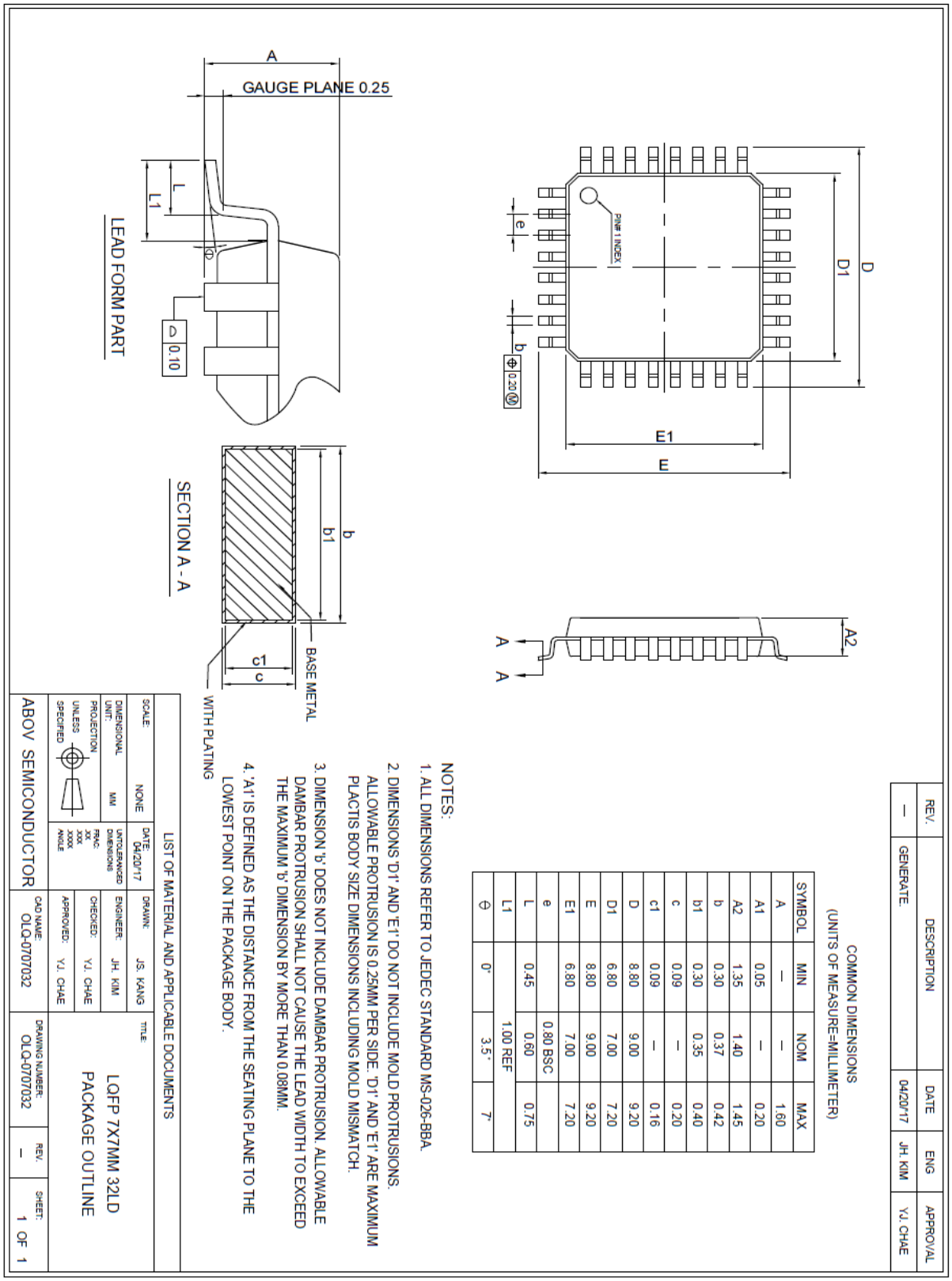


Figure 30. 32 LQFP Package Outline

18 Ordering information

Table 29. AC33Mx064T Series Device Ordering Information

Device name	Flash	SRAM	UART	SPI	I2C	MPWM	ADC	I/O ports	Package
AC33M4064T	64KB	8KB	2	1	1	1	2-unit 11 ch	44	LQFP-48
AC33M3064T*	64KB	8KB	2	1	1	1	2-unit 7 ch	28	LQFP-32

* For available options or further information on the device with a "*" mark, please contact the ABOV sales offices.

AC 33 M x 064 T L B

(1) (2) (3) (4) (5) (6) (7) (8)

(1) (2) (3) (4) (5) (6) (7) (8)

Head	CPU type		Application		# of pins		Memory size		Operation. Temp.(℃)		PKG type		Material	
AC	33	Cortex-M3	M	Motor	3	32pin	064	64KB	T	105	L	LQFP	B	Green product
					4	48pin								

Figure 31. Meaning of Product Code

19 Development tools

This chapter introduces wide range of development tools for AC33Mx064T. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

19.1 Compiler

ABOV semiconductor does not provide any compiler for AC33Mx064T. However, since AC33Mx064T have ARM's high-speed 32-bit Cortex-M3 Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

19.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's AC33Mx064T MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 32. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

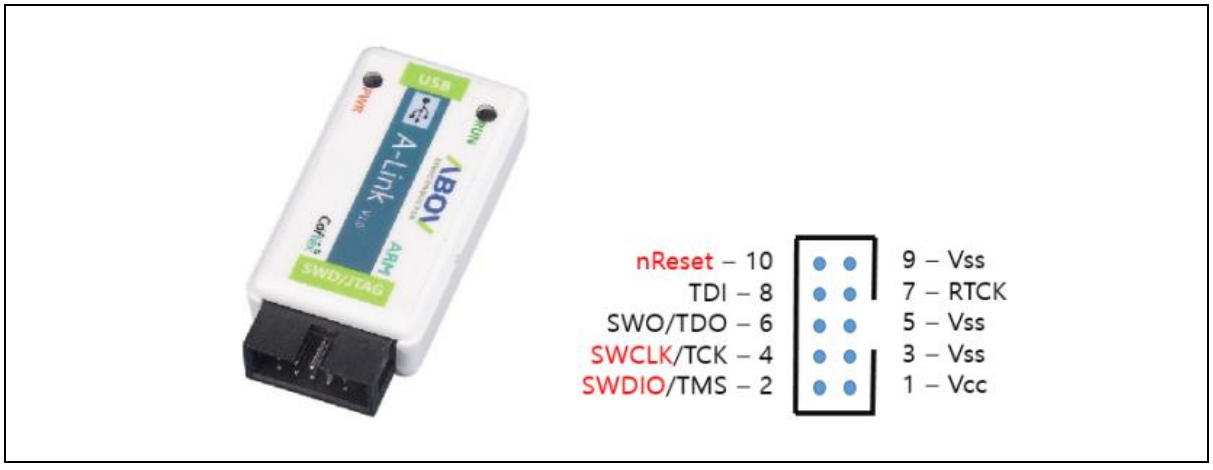


Figure 32. A-Link and Pin Descriptions

19.3 Programmer

19.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2~5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

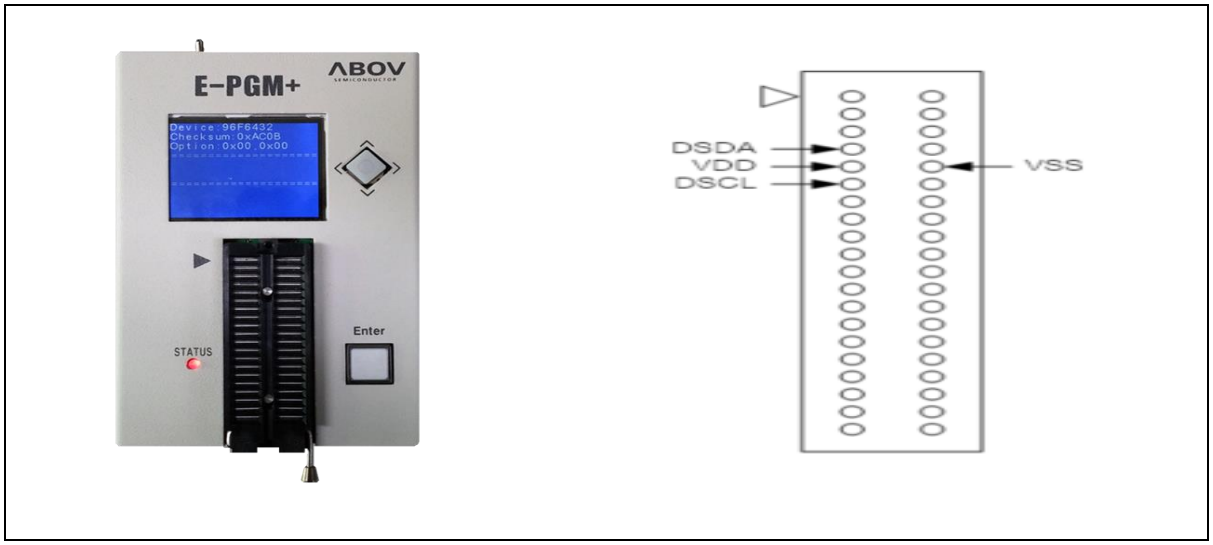


Figure 33. E-PGM+ (Single Writer) and Pin Descriptions

19.3.2 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Figure 34. E-Gang4 and E-Gang6 (for Mass Production)

Revision history

Date	Version	Description
2014/10/06	0.1	File created
2014/10/24	0.1.1	MPWM and ADC revised
2014/10/24	0.1.2	Micellanous update
2014/10/24	0.1.4	DMA control register updated. Peripehral select table update
2015/1/25	0.1.6	Typo error correction
2015/2/2	0.1.7	Pin assign and pin map changed
2015/3/3	0.1.8	Typo error correction
2015/3/6	0.1.9	ADC: Input corrected (AN0~AN10) Timers: Timing diagrams are added. MPWM: Timing diagrams are revised.
2015/3/6	0.1.10	Correction of NMIR explanation, Addition of Revision ID(CHIPID2) Renumbering of Figures.
2015/3/9	0.1.11	The polarity of PSHRT bit in MP.DTR register was inverted. Description of MPWM wave form was revised. PROTKEY value in PSR register was corrected.
2015/6/4	0.1.12	ADC: Correct Input ch number (8-ch→7-ch) .
2015/6/23	0.1.13	LQFP-32 Package was added. The timing charts of MPWM deadtime were added.
2015/6/25	0.1.14	The explanation of SCU was modified. Clock, reset diagram and POR were added. Power down mode was removed.
2015/12/15	0.1.15	The explanations of FM.MR and MPWM duty were modified. The spec of VOL and VOH were changed.
2016/03/24	1.0	Clock configuration procedure was modified.
2016/07/19	1.1	Added debounce logic description in PCU Added MPWM note
2016/8/3	1.1.1	Typo error correction
2016/10/27	1.1.2	Modified MP.Duty, MP.SR, MP.OLR Explanation . Modified figure of MPWM functional description.
2017/4/6	1.1.3	Description of SMR contects was corrected PCC.MR's PC11(BOOT) reset value changed.
2017/8/8	1.2.0	Package figure changed
2017/8/22	1.2.1	Package figure Modified
2017/12/20	1.2.2	Modified description of STSEL in ADC.MR register. Added description of CLKDIV in ADC.CCR register
2018/1/11	1.2.3	Modified description of Un.IDTR register (UART) Modified description of DMAEN bit in And.MR register (ADC)
2018/2/21	1.2.4	Added meaning of product code
2020/06/10	1.00	1st creation (PMO)
2021/10/1	1.01	Modified description of PLL 80MHz -> 48MHz. Added meaning of Figure 11. Clock Tree Configuration

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