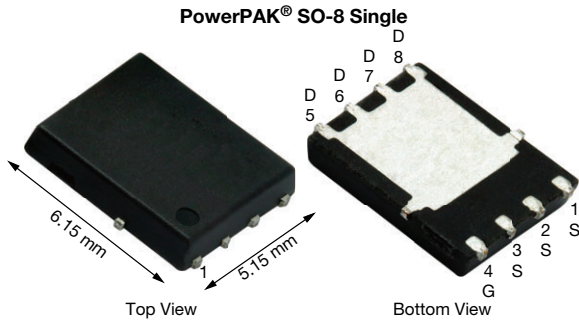


## N-Channel 45 V (D-S) MOSFET



### FEATURES

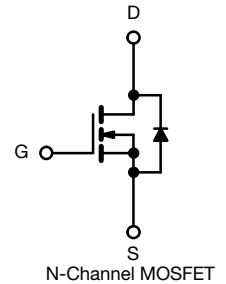
- TrenchFET® Gen IV power MOSFET
- 45 V Drain-source break-down voltage
- Tuned for low  $Q_g$  and  $Q_{oss}$
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- Motor drive control



PRODUCT SUMMARY	
$V_{DS}$ (V)	45
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00271
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.00397
$Q_g$ typ. (nC)	21.4
$I_D$ (A) <sup>a</sup>	110
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR150DP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	45	V
Gate-source voltage	$V_{GS}$	+20, -16	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	110
		$T_C = 70$ °C	88
		$T_A = 25$ °C	30.9 <sup>b, c</sup>
		$T_A = 70$ °C	24.6 <sup>b, c</sup>
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	300	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	4.7 <sup>b, c</sup>
Single pulse avalanche current	$I_{AS}$	30	mJ
Single pulse avalanche Energy	$E_{AS}$	45	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	65.7
		$T_C = 70$ °C	42
		$T_A = 25$ °C	5.2 <sup>b, c</sup>
		$T_A = 70$ °C	3.3 <sup>b, c</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b, f</sup>	$t \leq 10$ s	$R_{thJA}$	20	24	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	1.5	1.9	

### Notes

- Based on  $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 62.5 °C/W
- Package limited



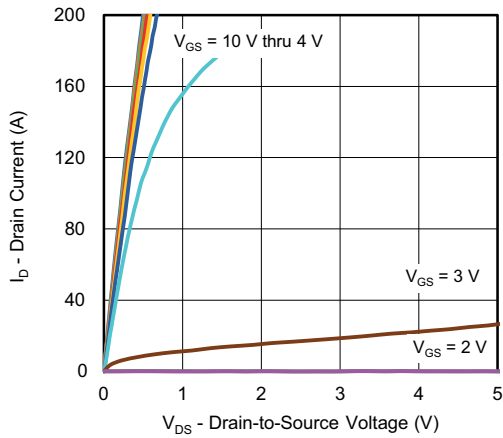
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	45	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 1\text{ mA}$	-	28	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-5.4	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.1	-	2.3	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = +20, -16\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 45\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 45\text{ V}, V_{GS} = 0\text{ V}, T_J = 75\text{ }^\circ\text{C}$	-	-	20	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	50	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	-	0.00225	0.00271	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	-	0.00305	0.00397	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$	-	72	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{ISS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	4000	-	pF
Output capacitance	$C_{OSS}$		-	630	-	
Reverse transfer capacitance	$C_{RSS}$		-	56	-	
$C_{RSS}/C_{ISS}$ ratio			-	0.014	0.028	
Total gate charge	$Q_g$	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	-	46.7	70	nC
		$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	-	21.4	32	
Gate-source charge	$Q_{gs}$		-	11.1	-	
Gate-drain charge	$Q_{gd}$		-	3.6	-	
Output charge	$Q_{OSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	-	28	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.5	1.15	2	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	15	30	ns
Rise time	$t_r$		-	6	12	
Turn-off delay time	$t_{d(off)}$		-	30	60	
Fall time	$t_f$		-	6	12	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	30	60	
Rise time	$t_r$		-	67	134	
Turn-off delay time	$t_{d(off)}$		-	28	56	
Fall time	$t_f$		-	10	20	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	59.7	A
Pulse diode forward current ( $t_p = 100\text{ }\mu\text{s}$ )	$I_{SM}$		-	-	300	
Body diode voltage	$V_{SD}$	$I_S = 5\text{ A}$	-	0.72	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 15\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	32	64	ns
Body diode reverse recovery charge	$Q_{rr}$		-	24	48	nC
Reverse recovery fall time	$t_a$		-	17	-	ns
Reverse recovery rise time	$t_b$		-	18	-	

**Notes**

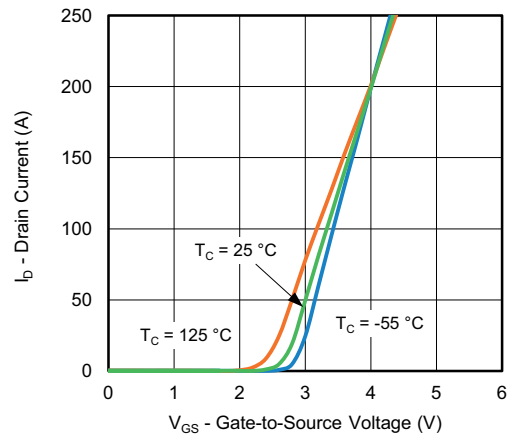
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

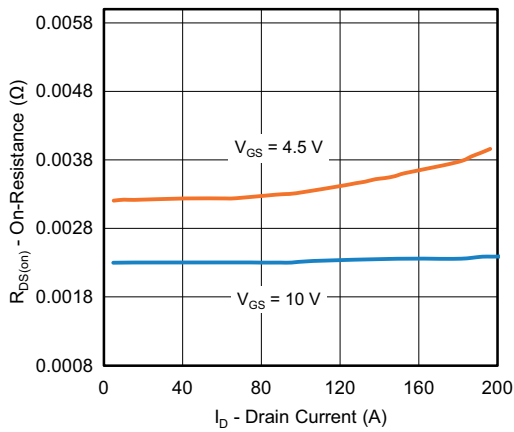
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



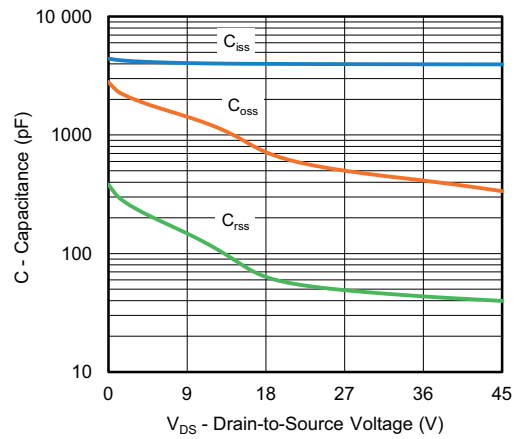
**Output Characteristics**



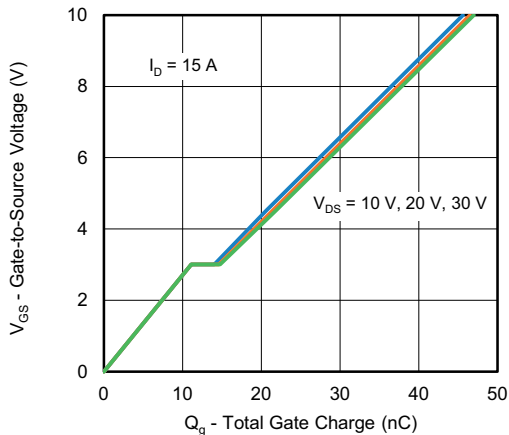
**Transfer Characteristics**



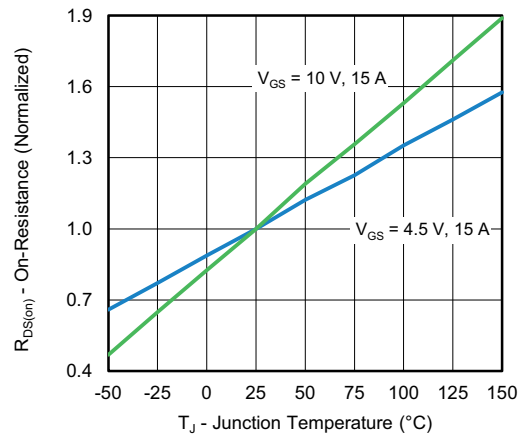
**On-Resistance vs. Drain Current**



**Capacitance**



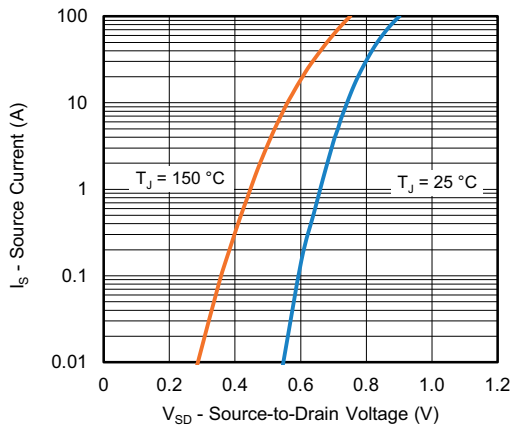
**Gate Charge**



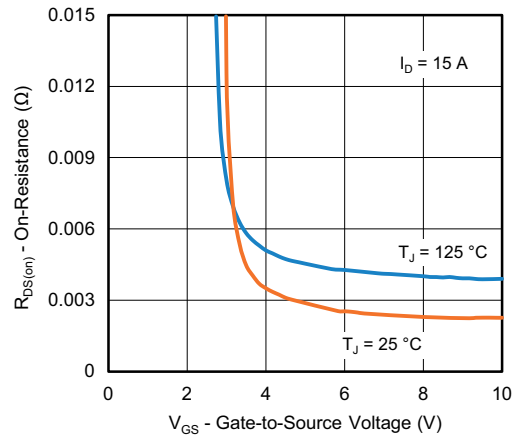
**On-Resistance vs. Junction Temperature**



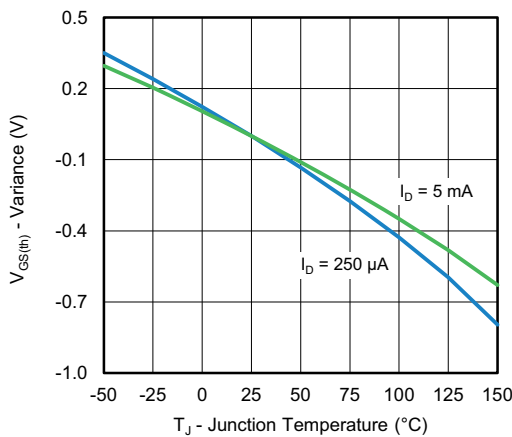
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



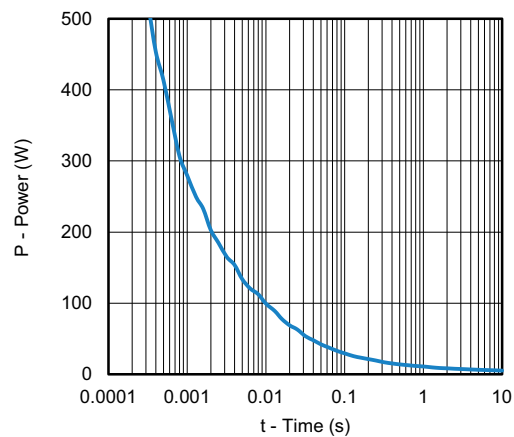
**Source-Drain Diode Forward Voltage**



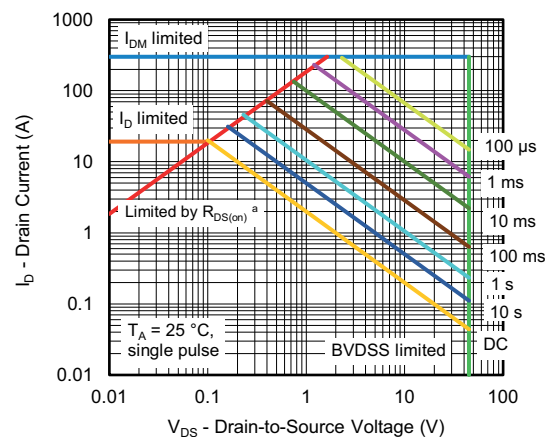
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**



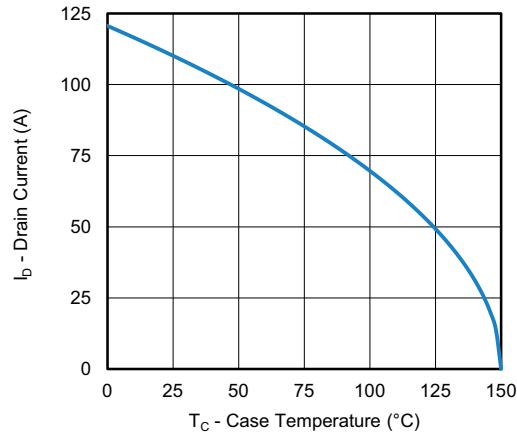
**Safe Operating Area**

**Note**

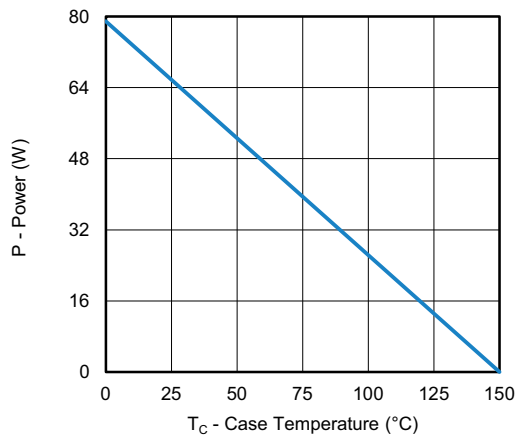
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



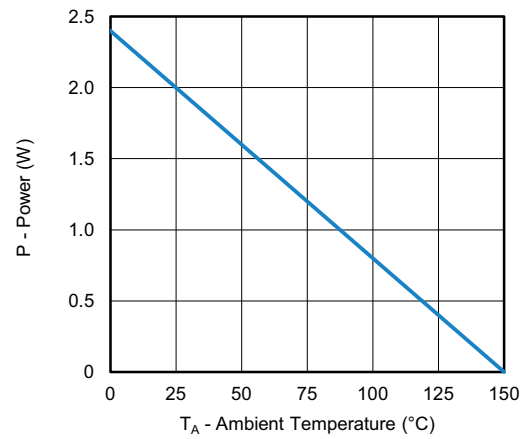
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**



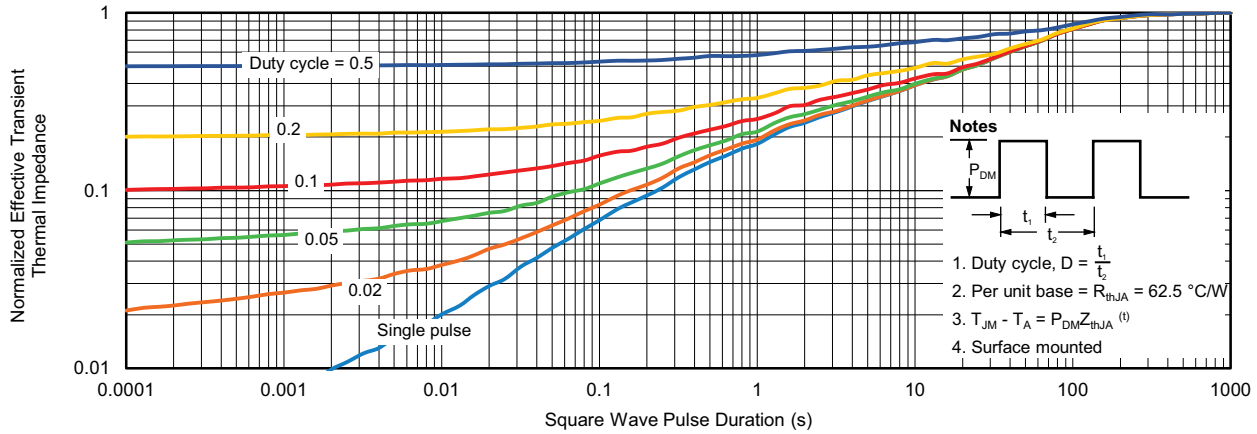
**Power, Junction-to-Ambient**

**Note**

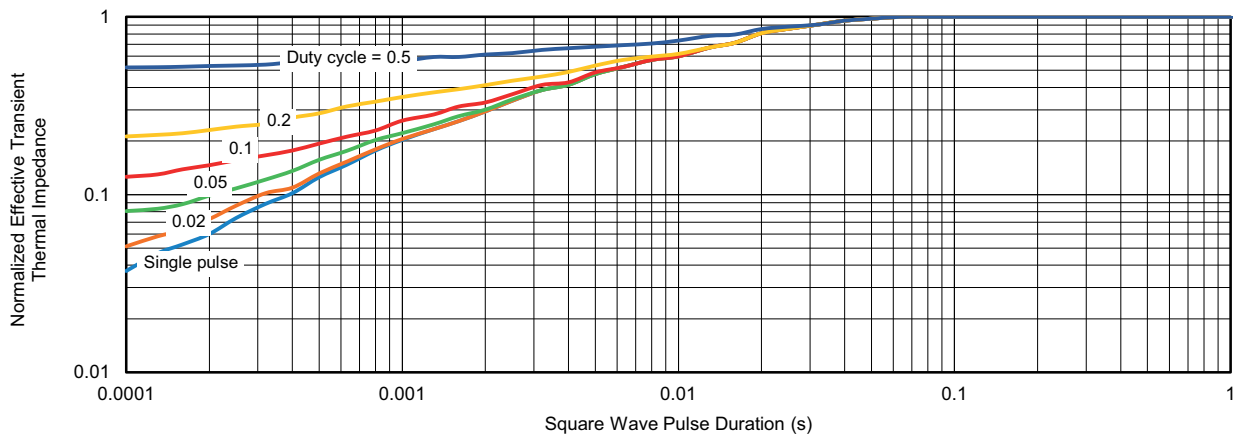
- a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

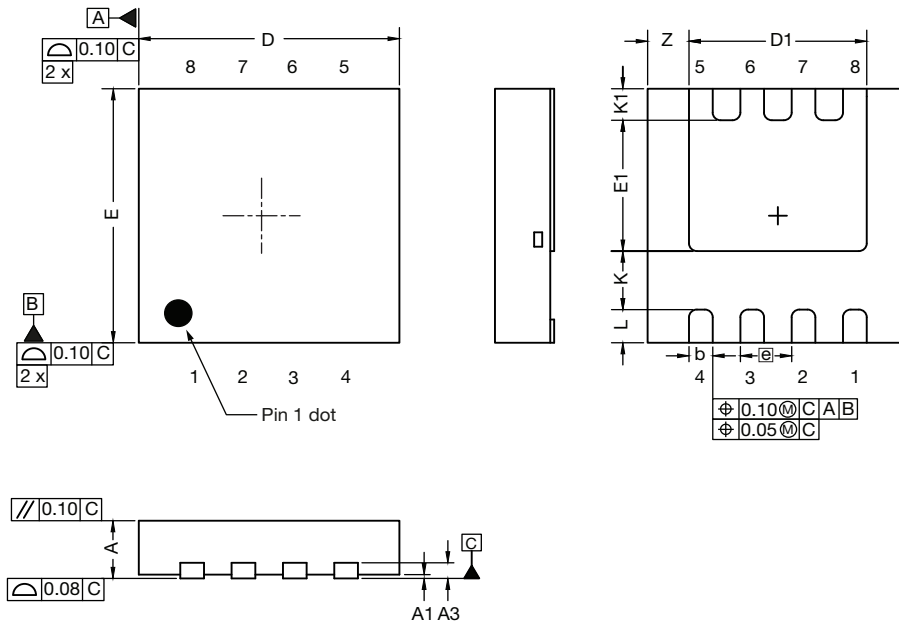


**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?77131](http://www.vishay.com/ppg?77131).



## Case Outline for PowerPAK® 1212-SWLH and PowerPAK® 1212-8SH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: S20-0930-Rev. C, 07-Dec-2020  
DWG: 6062

## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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