10 pA, Ultra Low Leakage and Quiescent Current, Load Switch with Reverse Blocking

DESCRIPTION

The SiP32431 and SiP32432 are ultra low leakage and quiescent current slew rate controlled high side switches with reverse blocking capability. The switches are of a low on resistance p-channel MOSFET that supports continuous current up to 1.4 A.

The SiP32431 and SiP32432 operate with an input voltage from 1.5 V to 5.5 V.

The SiP32431 and SiP32432 feature low input logic level to interface with low control voltage from microprocessors. The SiP32431 is of logic high enable control, while SiP32432 is of logic low enable control. Both devices have a very low operating current, typically 10 pA at 3.3 V power supply.

The SiP32431 and SiP32432 are available in lead (Pb)-free package options including 6 pin SC-70-6, and 4 pin TDFN4 1.2 mm x 1.6 mm DFN4 packages. The operation temperature range is specified from -40 °C to +85 °C.

The SiP32431 and SiP32432 compact package options, operation voltage range, and low operating current make it a good fit for battery power applications.

FEATURES

- 1.5 V to 5.5 V input voltage range
- No bias power rail required
- Low on-resistance $R_{DS(on)}$, typically 105 mΩ at 5 V and 135 mΩ at 3 V for TDFN4 1.2 mm x 1.6 mm package
- Typical 147 mΩ at 5 V and 178 mΩ at 3 V for SC-70-6 package
- Slew rate controlled turn-on time: 100 µs
- Ultra low leakage and quiescent current:
  - V_{IN} quiescent current = 0.01 nA
  - V_{IN} shutdown leakage = 0.20 nA
- Reverse blocking capability
- SC-70-6 and TDFN4 1.2 mm x 1.6 mm packages
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Wireless sensor network
- Smart meters
- Wearable
- Internet of things
- Portable medical devices
- Security systems
- Battery powered devices
- Portable Instruments

TYPICAL APPLICATION CIRCUIT

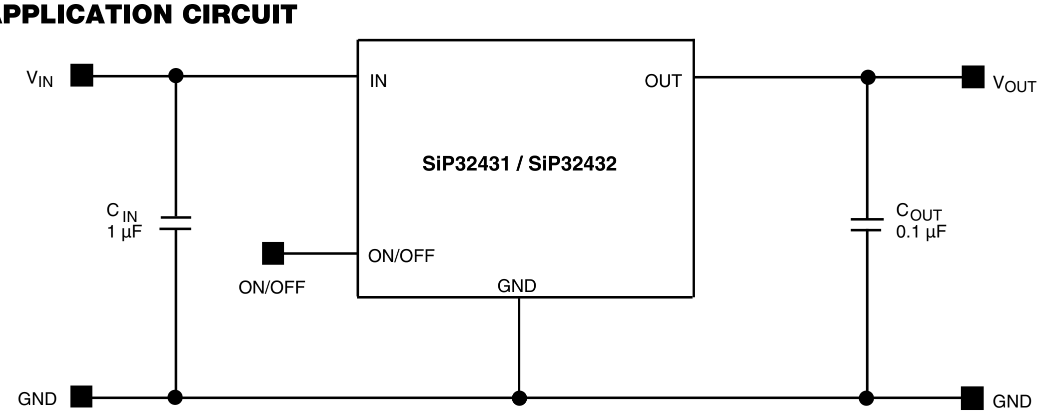

Fig. 1 - SiP32431, SiP32432 Typical Application Circuit

ORDERING INFORMATION				
PART NUMBER	**MARKING**	**ENABLE**	**PACKAGE**	**TEMPERATURE RANGE**
SiP32431DR3-T1GE3	MAxx	High enable	SC-70-6	-40 °C to +85 °C
SiP32432DR3-T1GE3	MDxx	Low enable		
SiP32431DNP3-T1GE4	Dx	High enable	TDFN4 1.2 mm x 1.6 mm	
SiP32432DNP3-T1GE4	Vx	Low enable		

Notes
- x = lot code

- -GE3 denotes halogen-free and RoHS-compliant
- Please use the SiP32431DR3-T1GE3 to replace SiP32431DR3-T1-E3

ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
Supply input voltage (V_{IN})		-0.3 to +6	V
Enable input voltage ($V_{ON/OFF}$)		-0.3 to +6	
Output voltage (V_{OUT})		-0.3 to +6	
Maximum continuous switch current ($I_{max.}$)	SC-70-6 package	1.2	A
	TDFN4 1.2 mm x 1.6 mm	1.4	
Maximum pulsed current (I_{DM}) V_{IN} (pulsed at 1 ms, 10 % duty cycle)	$V_{IN} \geq 2.5$ V	3	
	$V_{IN} < 2.5$ V	1.6	
ESD rating (HBM)		4000	V
Junction temperature (T_J)		-40 to +125	°C
Thermal resistance (θ_{JA}) [a]	6 pin SC-70-6 [b]	220	°C/W
	4 pin TDFN4 1.2 mm x 1.6 mm [c]	170	
Power dissipation (P_D) [a]	6 pin SC-70- 6 [b]	250	mW
	4 pin TDFN4 1.2 mm x 1.6 mm [c]	324	

Notes

a. Device mounted with all leads and power pad soldered or welded to PC board
b. Derate 4.5 mW/°C above T_A = 70 °C
c. Derate 5.9 mW/°C above T_A = 70 °C, see PCB layout

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating / conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

PARAMETER	LIMIT	UNIT
Input voltage range (V_{IN})	1.5 to 5.5	V
Operating temperature range	-40 to +85	°C

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 5, T_A = -40 °C to +85 °C (Typical values are at T_A = 25 °C)		LIMITS -40 °C to +85 °C MIN. [a]	TYP. [b]	MAX. [a]	UNIT
Operating voltage [c]	V_{IN}			1.5	-	5.5	V
Quiescent current	I_Q	V_{IN} = 3.3 V, $V_{on/off}$ = 3.3 V		-	0.01	100	nA
		V_{IN} = 5 V, $V_{on/off}$ = 5 V		-	0.05	1000	
Off supply current	$I_{Q(off)}$	V_{IN} = 3.3 V, $V_{on/off}$ = 0 V, OUT = open		-	0.01	100	
		V_{IN} = 5 V, $V_{on/off}$ = 0 V, OUT = open		-	-	1000	
Off switch current	$I_{SD(off)}$	V_{IN} = 3.3 V, $V_{on/off}$ = 0 V, OUT = 1 V		-	0.2	100	
		V_{IN} = 5 V, $V_{on/off}$ = 0 V, OUT = 0 V		-	-	1000	
Reverse blocking current	I_{RB}	V_{OUT} = 5.5 V, V_{IN} = 0, $V_{on/off}$ = inactive		-	130	1000	
On-resistance	$R_{DS(on)}$	V_{IN} = 5 V, I_L = 500 mA, T_A = 25 °C	SC-70-6	-	147	230	mΩ
			TDFN4	-	105		
		V_{IN} = 4.2 V, I_L = 500 mA, T_A = 25 °C	SC-70-6	-	155	250	
			TDFN4	-	110		
		V_{IN} = 3 V, I_L = 500 mA, T_A = 25 °C	SC-70-6	-	178	290	
			TDFN4	-	135		
		V_{IN} = 1.8 V, I_L = 500 mA, T_A = 25 °C	SC-70-6	-	275	480	
			TDFN4	-	230		
		V_{IN} = 1.5 V, I_L = 500 mA, T_A = 25 °C	SC-70-6	-	395	520	
			TDFN4	-	350		
On-resistance temp.-coefficient	TD_{RDS}			-	2800	-	ppm/°C
On / off input low voltage [c]	V_{IL}	$V_{IN} \geq$ 1.5 V to < 1.8 V		-	-	0.3	V
		$V_{IN} \geq$ 1.8 V to < 2.7 V		-	-	0.4	
		$V_{IN} \geq$ 2.7 V to $\leq$ 5.5 V		-	-	0.6	
On / off input low voltage c	V_{IH}	$V_{IN} \geq$ 1.5 V to < 2.7 V		1.3	-	-	
		$V_{IN} \geq$ 2.7 V to < 4.2 V		1.5	-	-	
		$V_{IN} \geq$ 4.2 V to $\leq$ 5.5 V		1.8	-	-	
On / off input leakage	$I_{ON/OFF}$	$V_{on/off}$ = 3.3 V		-	0.014	100	nA
		$V_{on/off}$ = 5.5 V		-	0.042	1000	
Output turn-on delay time	$t_{d(on)}$	V_{IN} = 5 V, R_{load} = 10 Ω, T_A = 25 °C		-	20	40	μs
Output turn-on rise time	$t_{(on)}$			-	140	180	
Output turn-off delay time	$t_{d(off)}$			-	4	10	

Notes

a. The algebriac convention whereby the most negative value is a minimum and the most positive a maximum
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
c. For V_{IN} outside this range consult typical on / off threshold curve

PIN CONFIGURATION

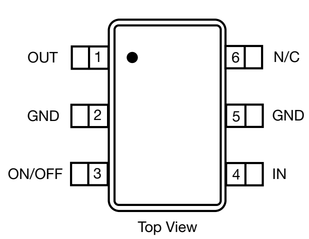

Fig. 2 - SC-70-6 Package

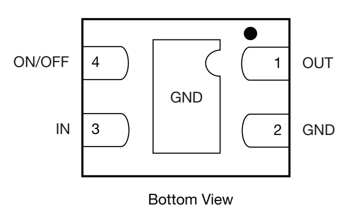

Fig. 3 - TDFN4 1.2 mm x 1.6 mm Package

PIN DESCRIPTION

PIN NUMBER SC-70-6	TDFN4	NAME	FUNCTION
4	3	IN	This pin is the p-channel MOSFET source connection. Bypass to ground through a 1 μF capacitor

PIN DESCRIPTION			
PIN NUMBER		NAME	FUNCTION
SC-70-6	TDFN4		
2, 5	2	GND	Ground connection
3	4	ON / OFF	Enable input
1	1	OUT	This pin is the p-channel MOSFET drain connection. Bypass to ground through a 0.1 μF capacitor

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

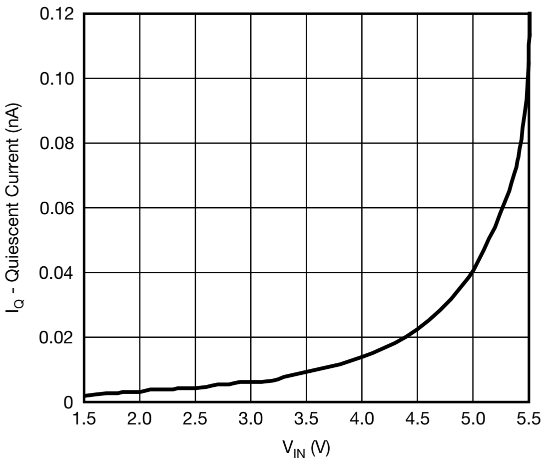

Fig. 4 - Quiescent Current vs. Input Voltage

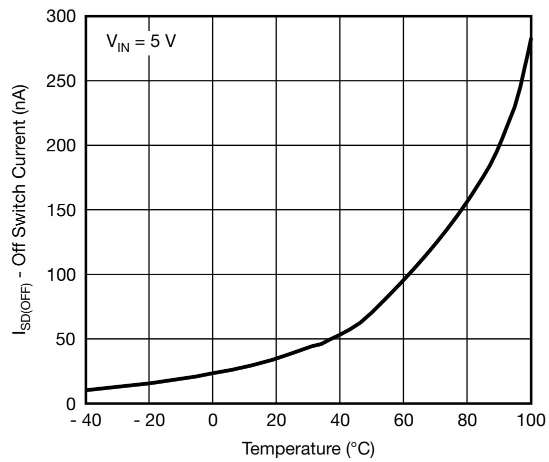

Fig. 7 - Off Switch Current vs. Temperature

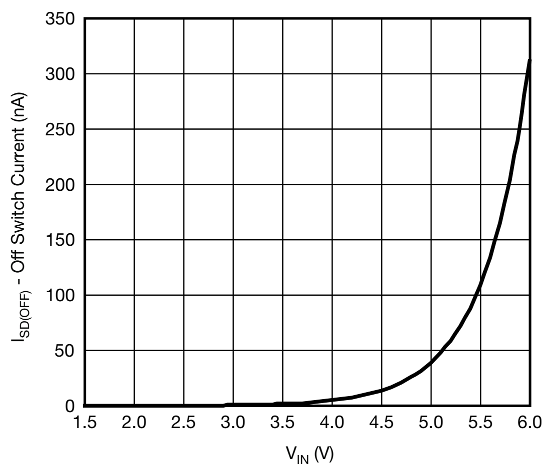

Fig. 5 - Off Switch Current vs. Input Voltage

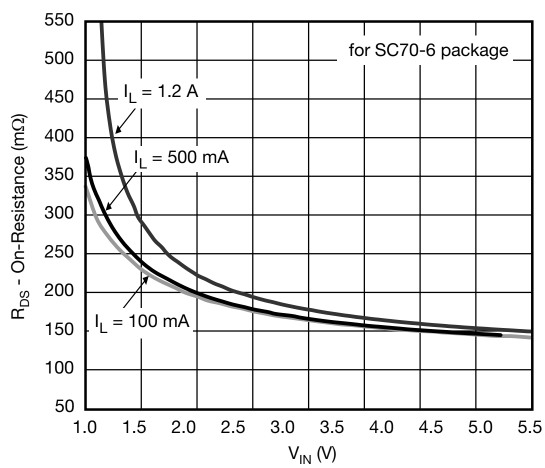

Fig. 8 - $R_{DS(on)}$ vs. V_{IN} for SC-70-6 Package

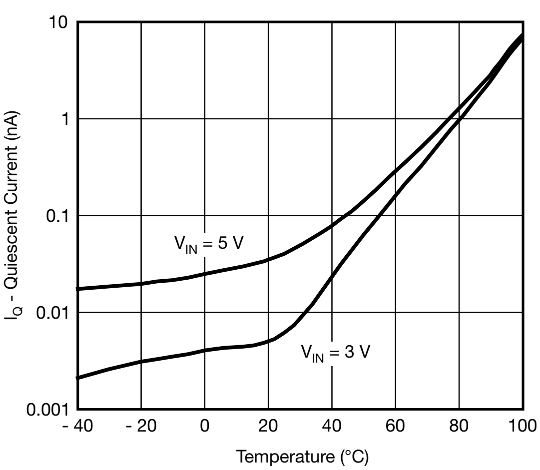

Fig. 6 - Quiescent Current vs. Temperature

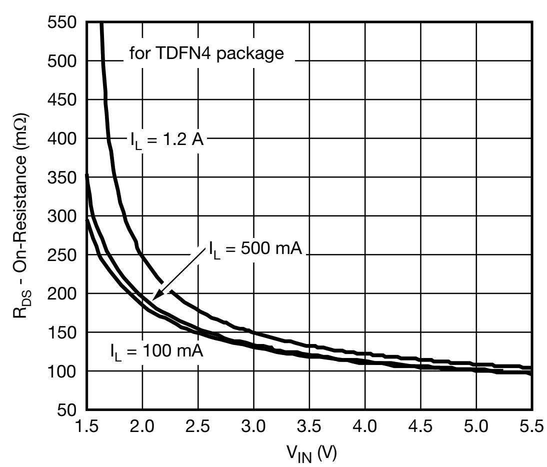

Fig. 9 - $R_{DS(on)}$ vs. Input Voltage

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

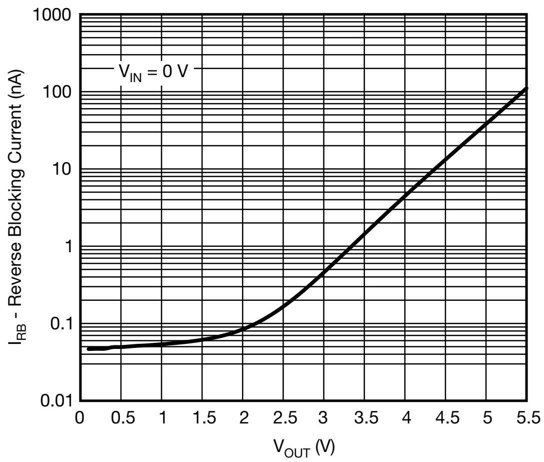

Fig. 10 - Reverse Blocking Current vs. V_{OUT}

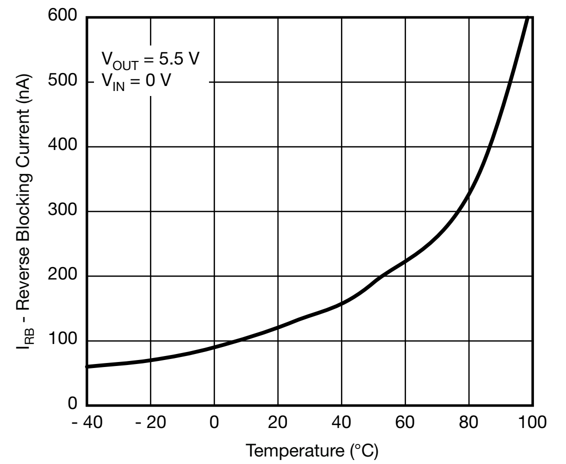

Fig. 13 - Reverse Blocking Current vs. Temperature

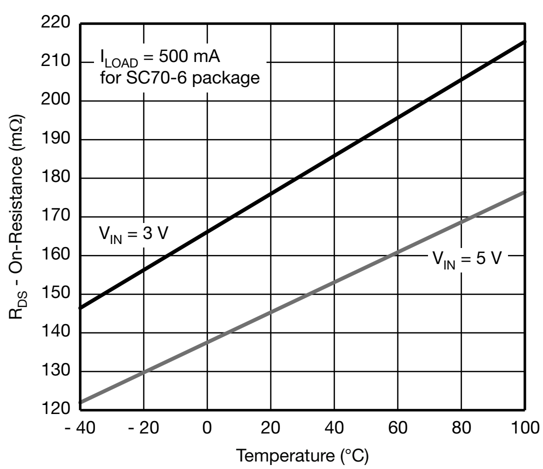

Fig. 11 - $R_{DS(on)}$ vs. Temperature

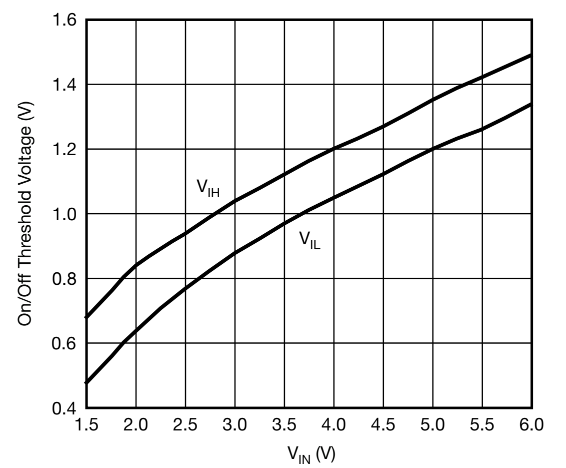

Fig. 14 - On / Off Threshold vs. Input Voltage

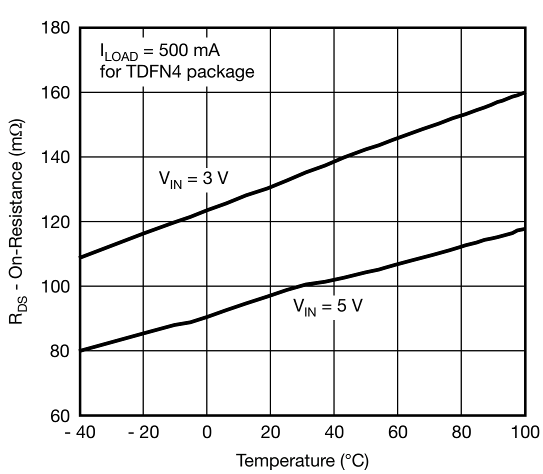

Fig. 12 - $R_{DS(on)}$ vs. Temperature

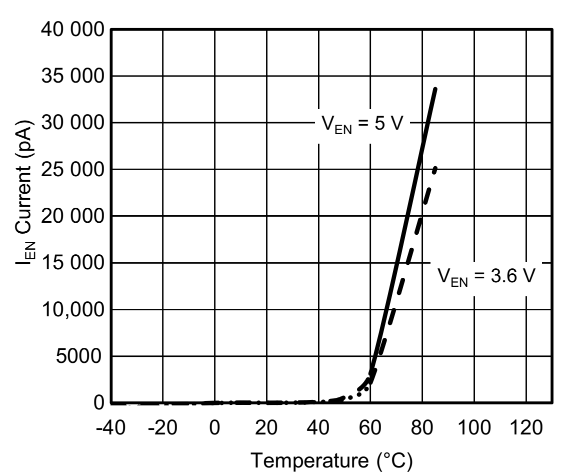

Fig. 15 - I_{EN} Current vs. Temperature

TYPICAL WAVEFORMS

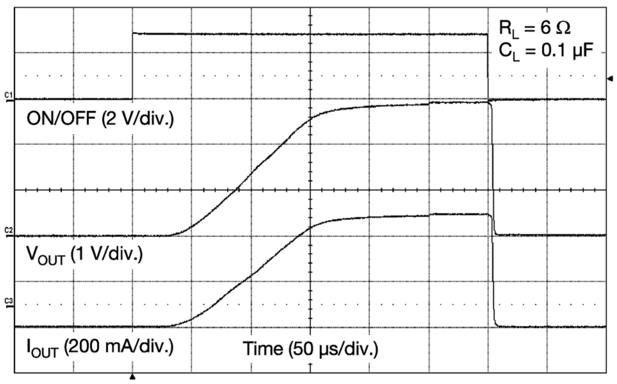

Fig. 16 - Switching (V_{IN} = 3 V)

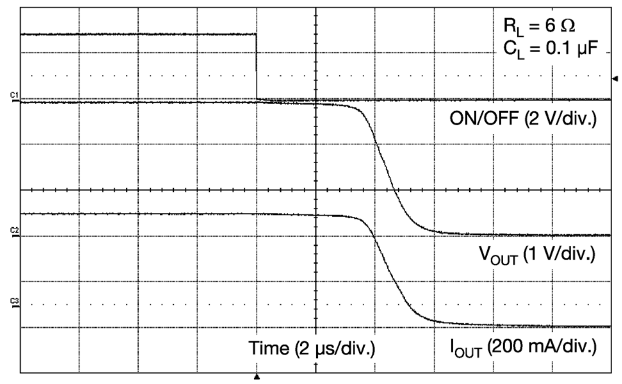

Fig. 18 - Turn-Off (V_{IN} = 3 V)

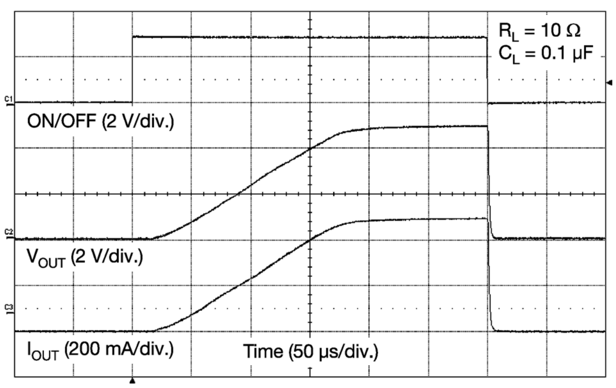

Fig. 17 - Switching (V_{IN} = 5 V)

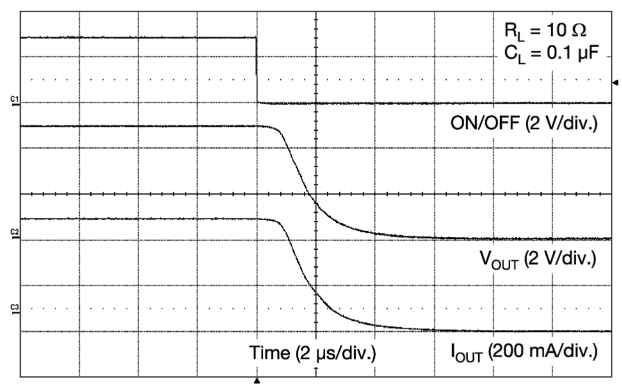

Fig. 19 - Turn-Off (V_{IN} = 5 V)

BLOCK DIAGRAM

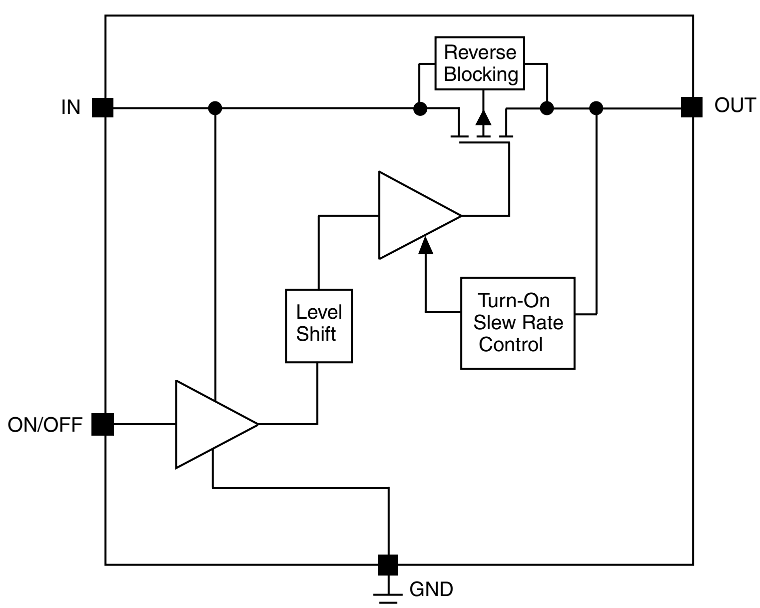

Fig. 20 - Functional Block Diagram

PCB LAYOUT

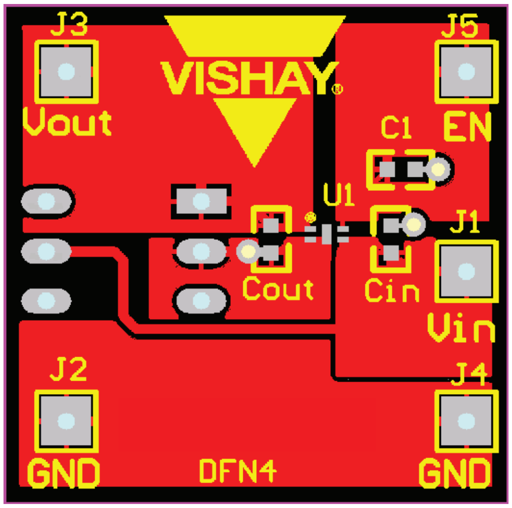

Fig. 21 - Top, TDFN4 1.2 mm x 1.6 mm PCB Layout

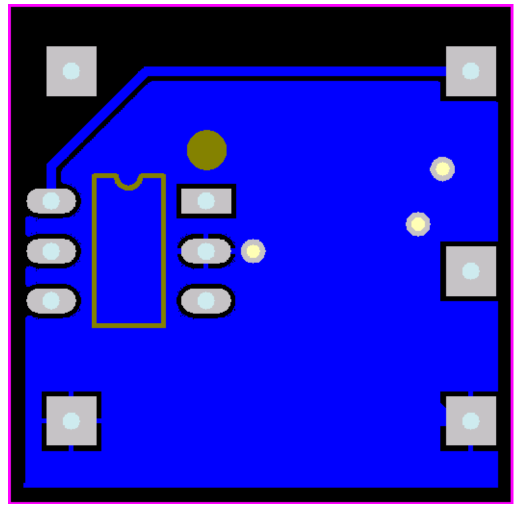

Fig. 22 - Bottom, TDFN4 1.2 mm x 1.6 mm PCB Layout

DETAILED DESCRIPTION

The SiP32431 and SiP32432 are p-channel MOSFET power switches designed for high-side slew rate controlled load-switching applications. Once turned on, the slew-rate control circuitry is activated and current is ramped in a linear fashion until it reaches the level required for the output load condition. This is accomplished by first elevating the gate voltage of the MOSFET up to its threshold voltage and then by linearly increasing the gate voltage until the MOSFET becomes fully enhanced. At this point, the gate voltage is then quickly increased to the full input voltage to reduce $R_{DS(on)}$ of the MOSFET switch and minimize any associated power losses.

APPLICATION INFORMATION

Input Capacitor

While a bypass capacitor on the input is not required, a 1 μF or larger capacitor for C_{IN} is recommended in almost all applications. The bypass capacitor should be placed as physically close as possible to the input pin to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 μF capacitor or larger across V_{OUT} and GND is recommended to insure proper slew operation. C_{OUT} may be increased without limit to accommodate any load transient condition with only minimal affect on the SiP32431 and SiP32432 turn on slew rate time. There are no ESR or capacitor type requirement.

Enable

The on / off pin is compatible with both TTL and CMOS logic voltage levels.

Protection Against Reverse Voltage Condition

The SiP32431 and SiP32432 contain a body snatcher that normally connects the body to the source (IN) when the device is enabled. In case where the device is disabled but the V_{OUT} is higher than the V_{IN}, the n-type body is switched to out, reverse bias the body diode to prevent the current from going back to the input.

Thermal Considerations

The physical limitations of the layout and assembly of the device limit the maximum current levels as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation, the power pad of the TDFN4 package should be connected to a heat sink on the printed circuit board.

The maximum power dissipation in any application is dependent on the maximum junction temperature, $T_{J\,(max.)}$ = 125 °C, the junction-to-ambient thermal resistance for the TDFN4 1.2 mm x 1.6 mm package, θ_{J-A} = 170 °C/W, and the ambient temperature, T_A, which may be formulaically expressed as:

$$P\ (max.) = \frac{T_{J\,(max.)} - T_A}{\theta_{J-A}} = \frac{125 - T_A}{170}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 324 mW.

So long as the load current is below the absolute maximum limits, the maximum continuous switch current becomes a function two things: the package power dissipation and the $R_{DS(on)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(on)}$ at 25 °C occurs at an input voltage of 1.5 V and is equal to 520 mΩ. The $R_{DS(on)}$ at 70 °C can be extrapolated from this data using the following formula

$R_{DS(on)}$ (at 70 °C) = $R_{DS(on)}$ (at 25 °C) x (1 + T_C x ΔT)

Where T_C is 3300 ppm/°C. Continuing with the calculation we have

$R_{DS(on)}$ (at 70 °C) = 520 mΩ x (1 + 0.0033 x (70 °C - 25 °C)) = 597 mΩ

The maximum current limit is then determined by

$$I_{LOAD\ (max.)} < \sqrt{\frac{P\ (max.)}{R_{DS(on)}}}$$

which in case is 0.74 A. Under the stated input voltage condition, if the 0.74 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

PRODUCT SUMMARY				
Part number	SiP32431DN	SiP32431DR	SiP32432DN	SiP32432DR
Description	1.5 V to 5.5 V, 105 mΩ, 10 pA I_Q, bidirectional off isolation, EN active high	1.5 V to 5.5 V, 147 mΩ, 10 pA I_Q, bidirectional off isolation, EN active high	1.5 V to 5.5 V, 105 mΩ, 10 pA I_Q, bidirectional off isolation, EN active low	1.5 V to 5.5 V, 147 mΩ, 10 pA I_Q, bidirectional off isolation, EN active low
Configuration	Single	Single	Single	Single
Slew rate time (µs)	140	140	140	140
On delay time (µs)	20	20	20	20
Input voltage min. (V)	1.5	1.5	1.5	1.5
Input voltage max. (V)	5.5	5.5	5.5	5.5
On-resistance at input voltage min. (mΩ)	350	395	350	395
On-resistance at input voltage max. (mΩ)	105	147	105	147
Quiescent current at input voltage min. (µA)	0.000002	0.000002	0.000002	0.000002
Quiescent current at input voltage max. (µA)	0.00004	0.00004	0.00004	0.00004
Output discharge (yes / no)	No	No	No	No
Reverse blocking (yes / no)	Yes	Yes	Yes	Yes
Continuous current (A)	1.4	1.4	1.4	1.4
Package type	TDFN4	SC-70-6	TDFN4	SC-70-6
Package size (W, L, H) (mm)	1.2 x 1.6 x 0.5	2.0 x 2.0 x 0.5	1.2 x 1.6 x 0.5	2.0 x 2.0 x 0.5
Status code	2	2	2	2
Product type	Slew rate	Slew rate	Slew rate	Slew rate
Applications	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable

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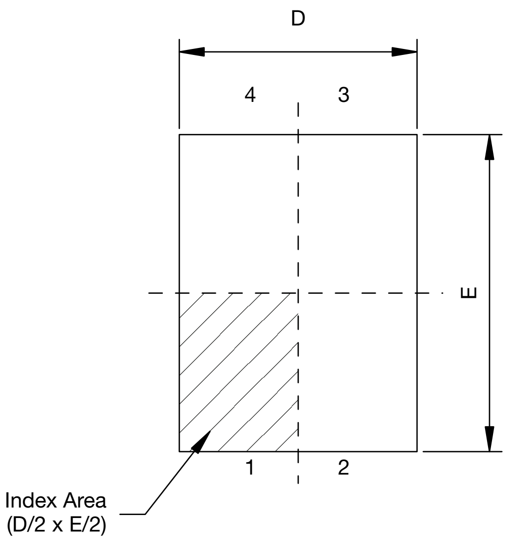
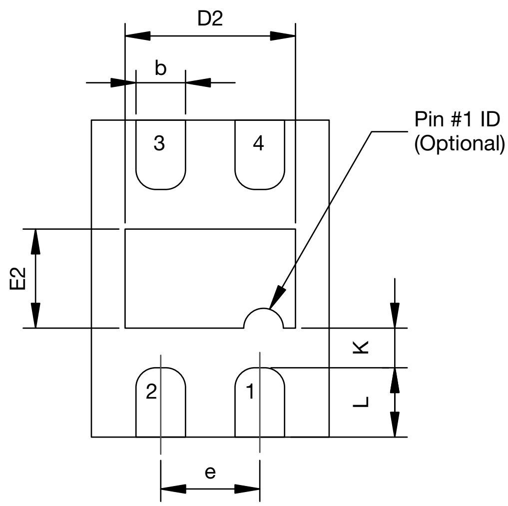
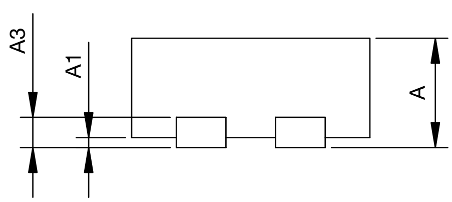
TDFN4 1.2 x 1.6 Case Outline



Top View



Bottom View



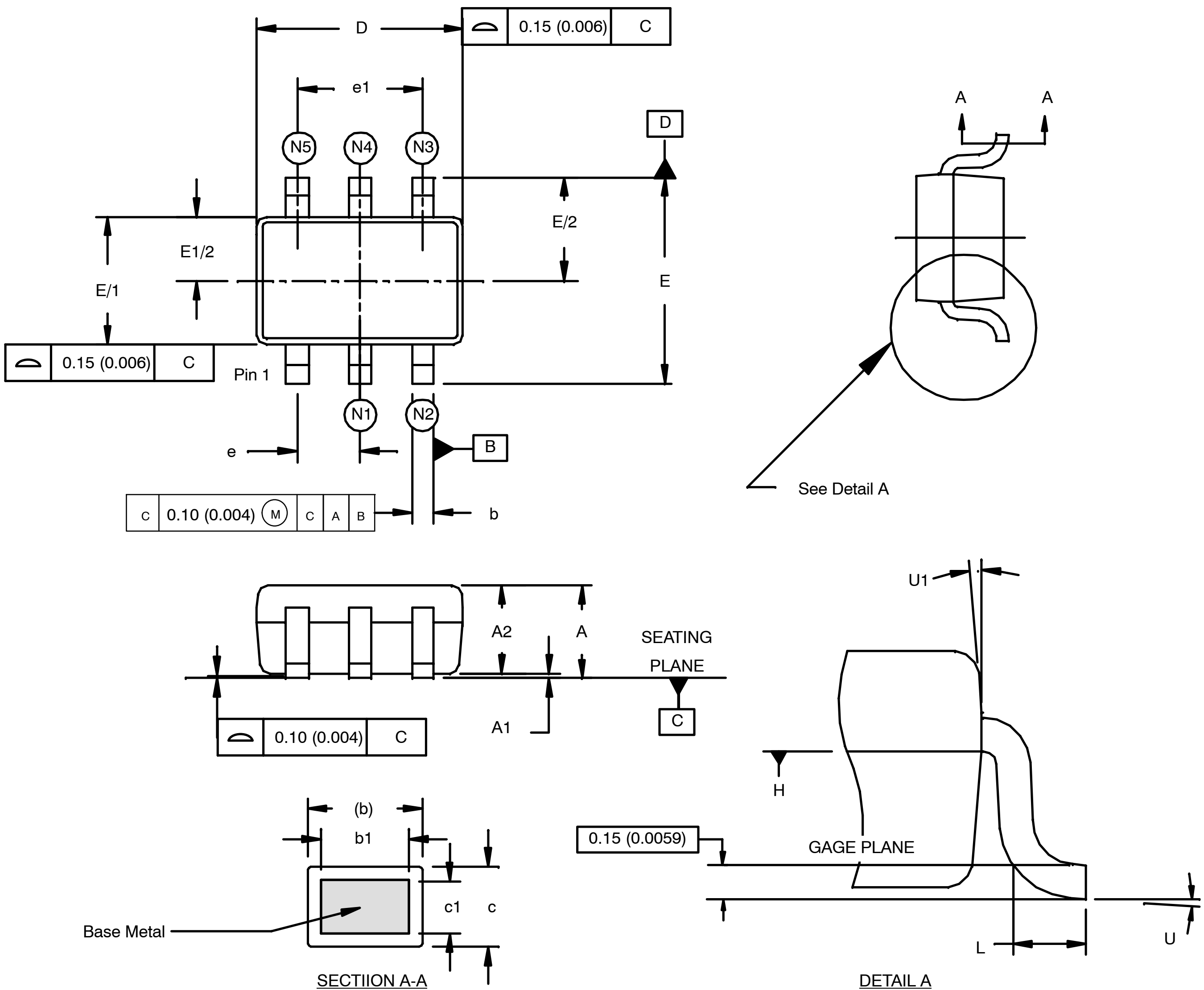
Side View

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.45	0.55	0.60	0.017	0.022	0.024
A1	0.00	-	0.05	0.00	-	0.002
A3	0.15 REF. or 0.127 REF. (1)			0.006 or 0.005 (1)		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.15	1.20	1.25	0.045	0.047	0.049
D2	0.81	0.86	0.91	0.032	0.034	0.036
e	0.50 BSC			0.020		
E	1.55	1.60	1.65	0.061	0.063	0.065
E2	0.45	0.50	0.55	0.018	0.020	0.022
K	0.25 typ.			0.010 typ.		
L	0.25	0.30	0.35	0.010	0.012	0.014
ECN: T16-0143-Rev. C, 18-Apr-16 DWG: 5995						

Note

(1) The dimension depends on the leadframe that assembly house used.

SC-70: 3/4/5/6-LEADS (PIC ONLY)



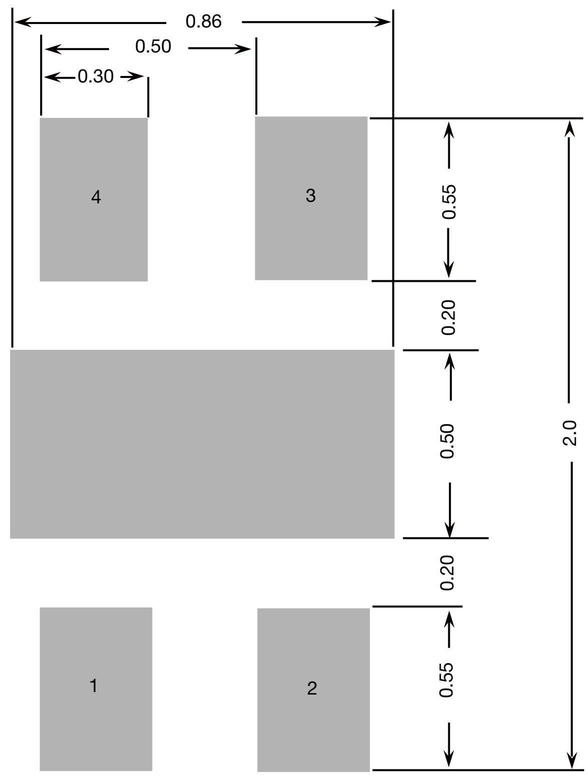
Pin Code	LEAD COUNT			
	3	4	5	6
N1	–	–	2	2
N2	2	2	3	3
N3	–	3	4	4
N4	3	–	–	5
N5	–	4	5	6

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Controlling dimensions: millimeters converted to inch dimensions are not necessarily exact.
3. Dimension “D” does not include mold flash, protrusion or gate burr. Mold flash, protrusion or gate burr shall not exceed 0.15 mm (0.006 inch) per side.
4. The package top shall be smaller than the package bottom. Dimension “D” and “E1” are determined at the outer most extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.80	–	1.10	0.031	–	0.043
A1	0.00	–	0.10	0.000	–	0.004
A2	0.80	0.90	1.00	0.031	0.035	0.040
b	0.15	–	0.30	0.006	–	0.012
b1	0.15	0.20	0.25	0.006	0.008	0.010
c	0.08	–	0.25	0.003	–	0.010
c1	0.08	0.13	0.20	0.003	0.005	0.008
D	1.90	2.10	2.15	0.074	0.082	0.084
E	2.00	2.10	2.20	0.078	0.082	0.086
E_1	1.15	1.25	1.35	0.045	0.050	0.055
e	0.65 BSC			0.0255 BSC		
e_1	1.30 BSC			0.0512 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
U	0°	–	8°	0°	–	8°
U1	4°		10°	4°		10°
ECN: S-42145—Rev. A, 22-Nov-04 DWG: 5941						

RECOMMENDED MINIMUM PADS FOR TDFN4 1.2 x 1.6



Recommended Minimum Pads
Dimensions in mm

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