Z0103MN

Logic level four-quadrant triac

Rev. 04 — 6 September 2010 Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate 4-Q triac in a SOT223 surface-mountable plastic package

1.2 Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage of 600V
- Sensitive gate in four quadrants
- Surface-mountable package

1.3 Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

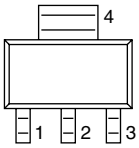
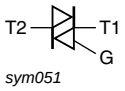
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 89$ °C; see Figure 2; see Figure 1	-	-	1	A
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; see Figure 8	-	-	3	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; see Figure 8	-	-	3	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; see Figure 8	-	-	3	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; see Figure 8	-	-	5	mA

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 SOT223 (SC-73)	 sym051
2	T2	main terminal 2		
3	G	gate		
4	T2	main terminal 2		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
Z0103MN	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 89$ °C; see Figure 2; see Figure 1	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms	-	8.5	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; see Figure 3; see Figure 4	-	8	A
I^2t	I2t for fusing	$t_p = 10$ ms; sine-wave pulse	-	0.32	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 1$ A; $I_G = 20$ mA; $dI_G/dt = 100$ mA/µs; T2+ G-	-	50	A/µs
		$I_T = 1$ A; $I_G = 20$ mA; $dI_G/dt = 100$ mA/µs; T2+ G+	-	50	A/µs
		$I_T = 1$ A; $I_G = 20$ mA; $dI_G/dt = 100$ mA/µs; T2- G+	-	20	A/µs
		$I_T = 1$ A; $I_G = 20$ mA; $dI_G/dt = 100$ mA/µs; T2- G-	-	50	A/µs
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C

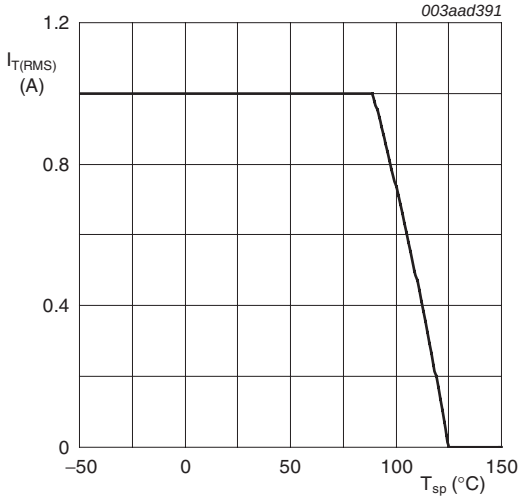
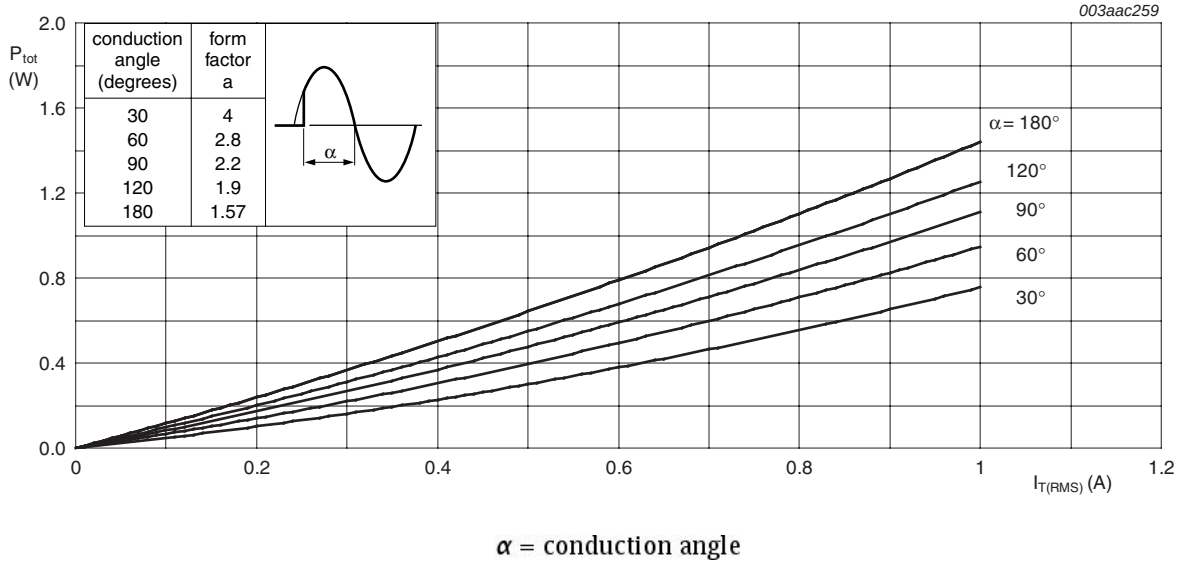
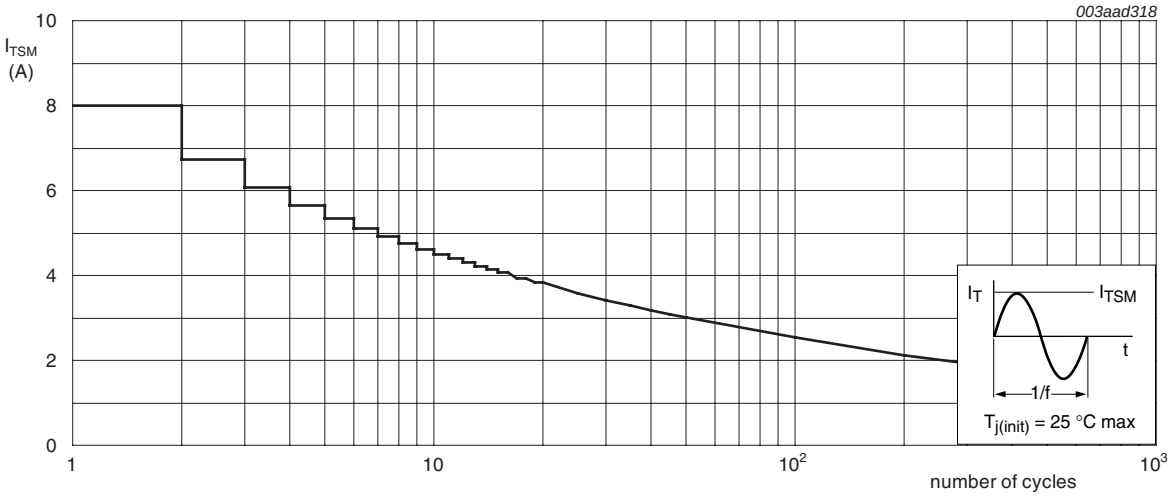


Fig 1. Maximum permissible RMS on-state current as a function of solder point temperature; typical values.



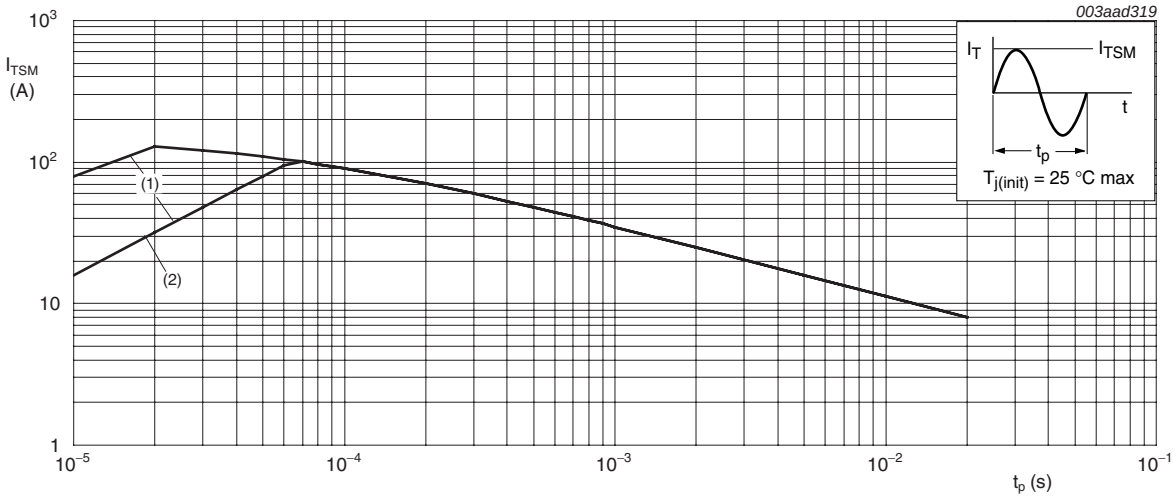
α = conduction angle

Fig 2. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig 3. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



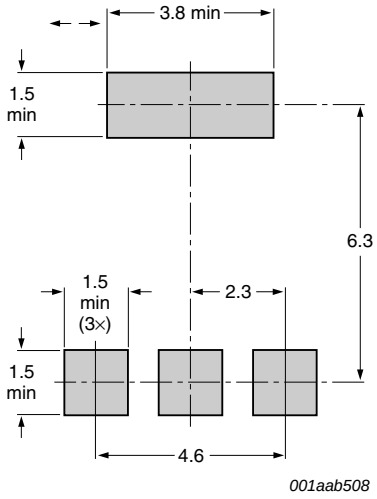
$t_p \leq 20$ ms; (1) is dI_T/dt limit; (2) is T2 − G + quadrant limit

Fig 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

5. Thermal characteristics

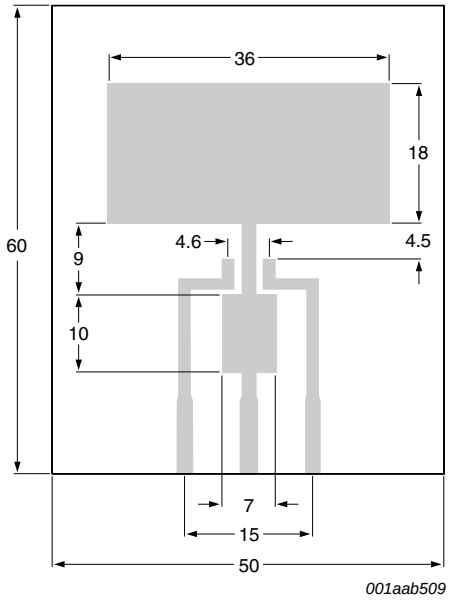
Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 7	-	-	25	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; printed-circuit board mounted; in free air; see Figure 5	-	156	-	K/W
		pad area; printed-circuit board mounted; in free air; see Figure 6	-	70	-	K/W



All dimensions are in mm

Fig 5. Minimum footprint SOT223



All dimensions are in mm

Printed-circuit board:

FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick),

Fig 6. Printed-circuit board pad area SOT223

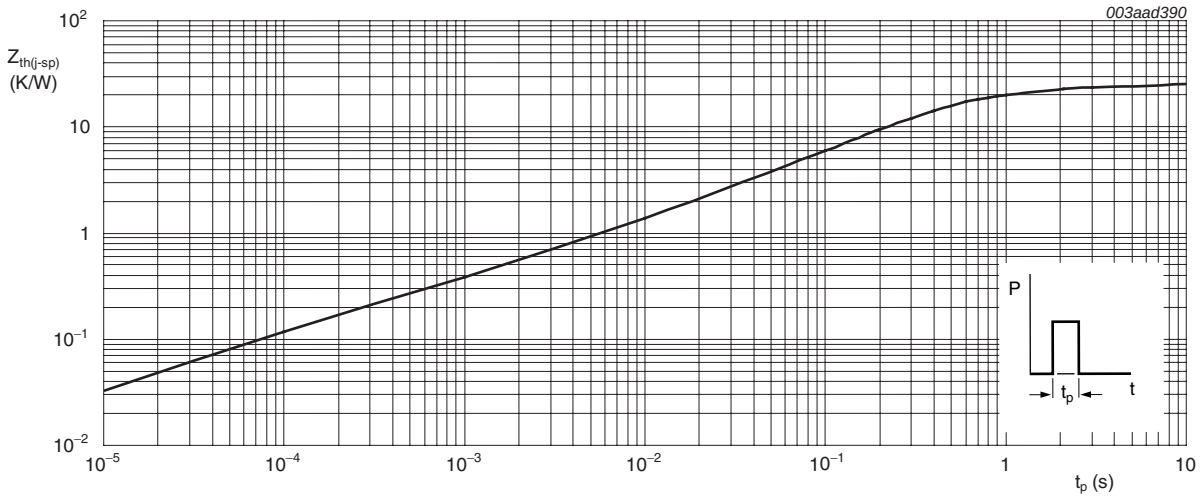
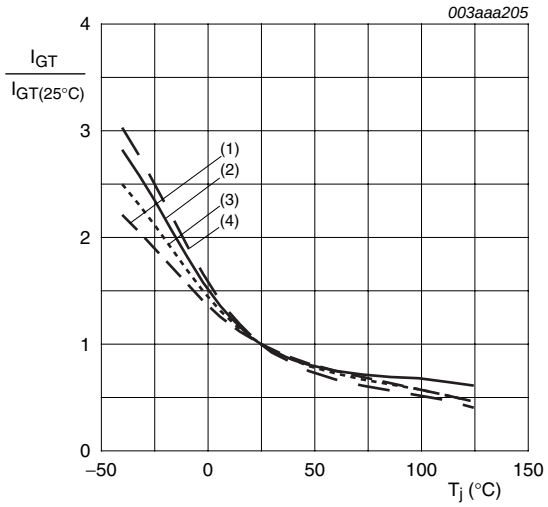


Fig 7. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; see Figure 8	-	-	3	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; see Figure 8	-	-	3	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; see Figure 8	-	-	3	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; see Figure 8	-	-	5	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; see Figure 9	-	-	7	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; see Figure 9	-	-	15	mA
		V_D = 12 V; I_G = 0.1 A; T2- G+; T_j = 25 °C; see Figure 9	-	-	7	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; see Figure 9	-	-	7	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; see Figure 13	-	-	7	mA
V_T	on-state voltage	I_T = 1 A; see Figure 10	-	1.3	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; see Figure 11	-	-	1.3	V
		V_D = 600 V; I_T = 0.1 A; T_j = 125 °C	0.2	-	-	V
I_D	off-state current	V_D = 600 V; T_j = 125 °C	-	-	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 110 °C; gate open circuit; see Figure 12	10	-	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	V_D = 400 V; T_j = 110 °C; dI_{com}/dt = 0.44 A/ms; gate open circuit	0.5	-	-	V/µs



(1) T2- G+

(2) T2- G-

(3) T2+ G-

(4) T2+ G+

Fig 8. Normalized gate trigger current as a function of junction temperature

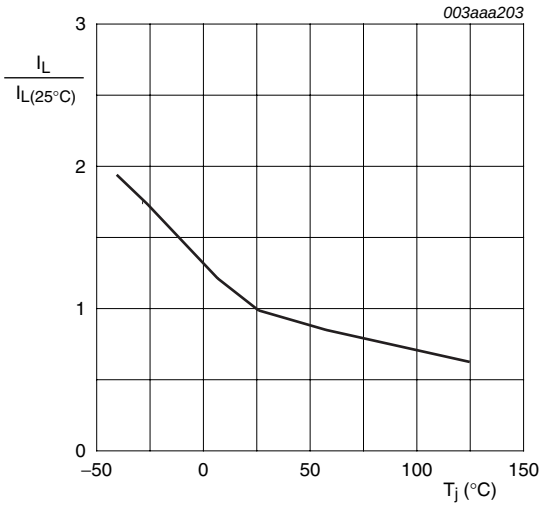
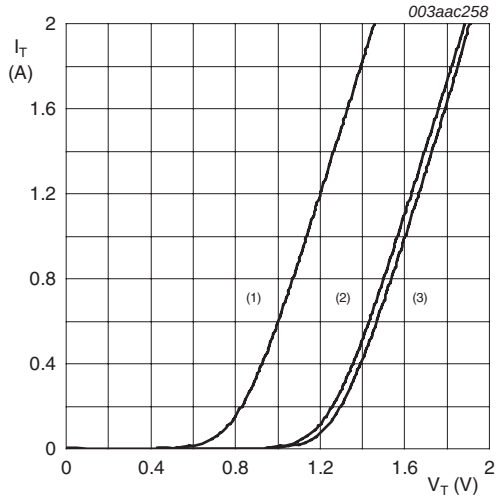


Fig 9. Normalized latching current as a function of junction temperature



V_o = 1.0 V

R_s = 0.21 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig 10. On-state current as a function of on-state voltage

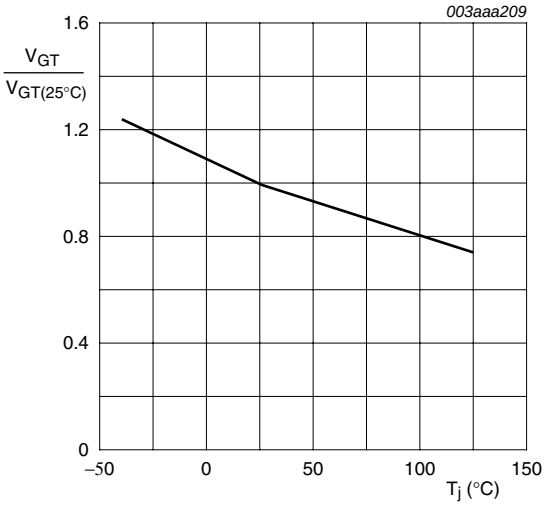
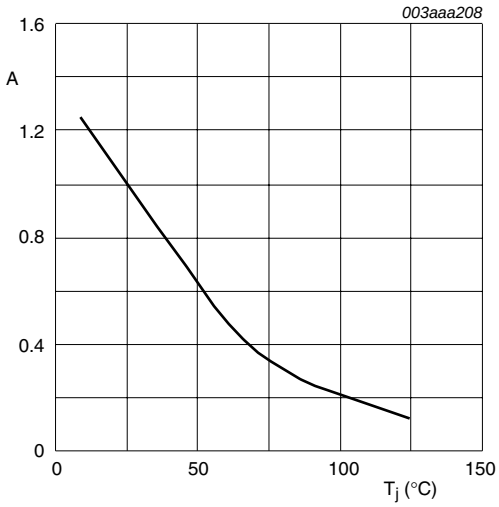


Fig 11. Normalized gate trigger voltage as a function of junction temperature



$$A = \frac{dV_D / dt}{dV_{D(25°C)} / dt}$$

Fig 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

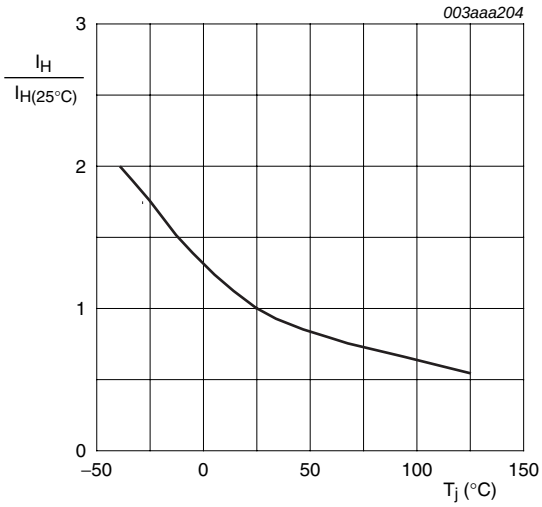
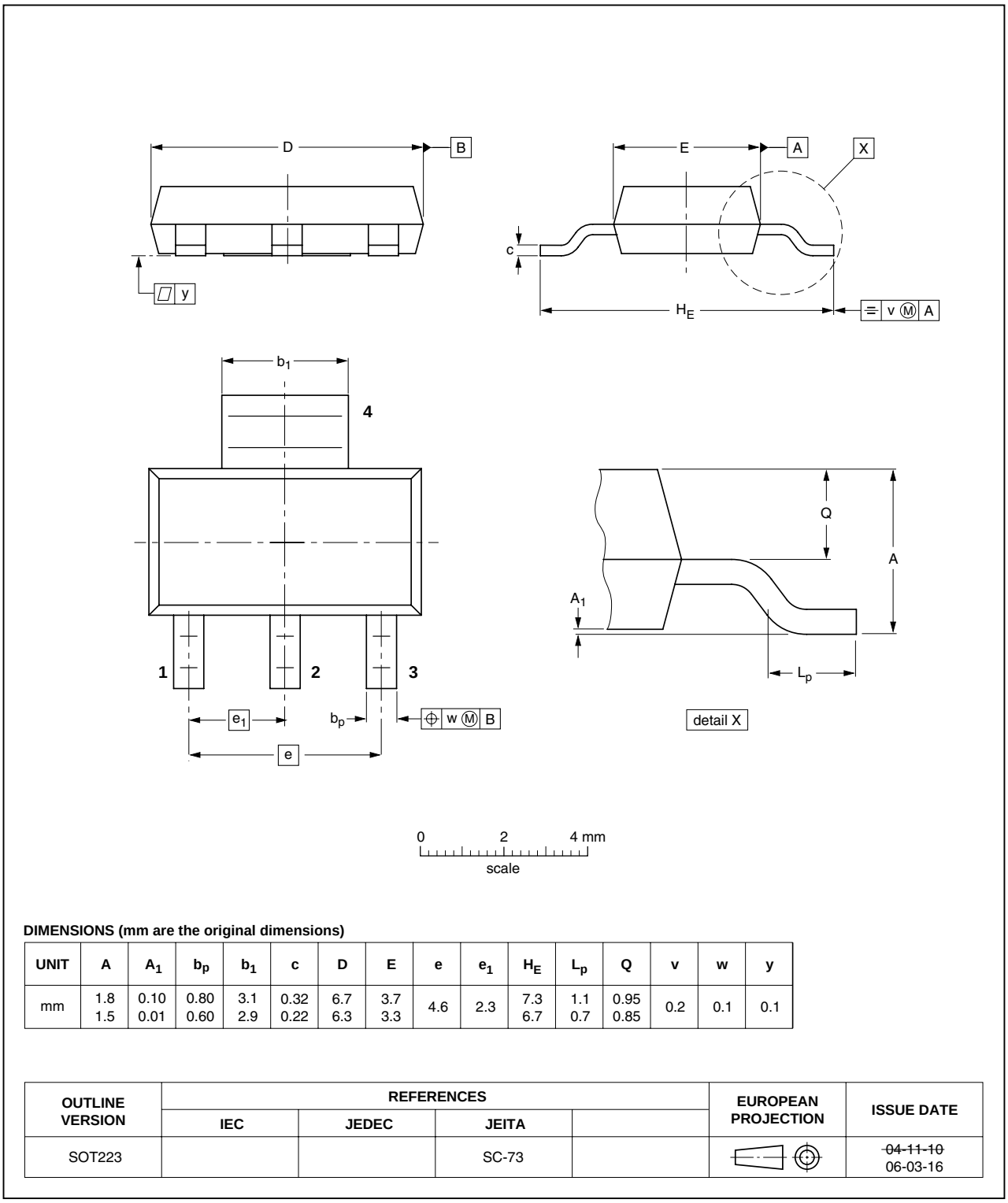


Fig 13. Normalized holding current as a function of junction temperature

7. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig 14. Package outline SOT223 (SC-73)

8. Soldering

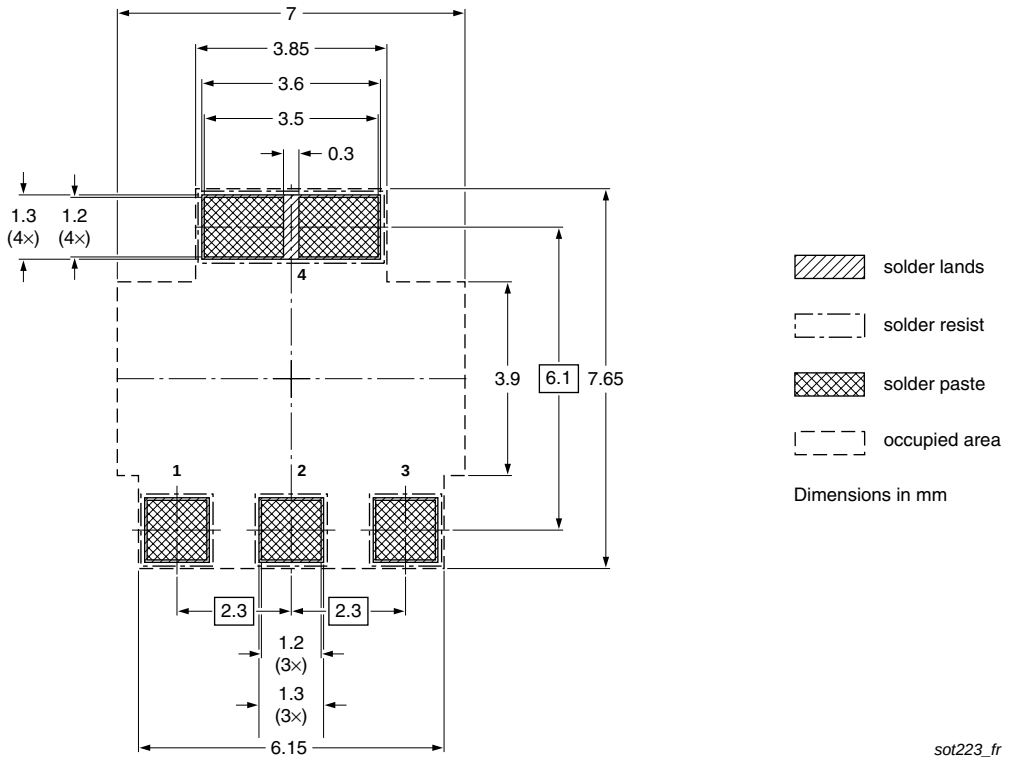


Fig 15. Reflow soldering footprint for SOT223 (SC-73)

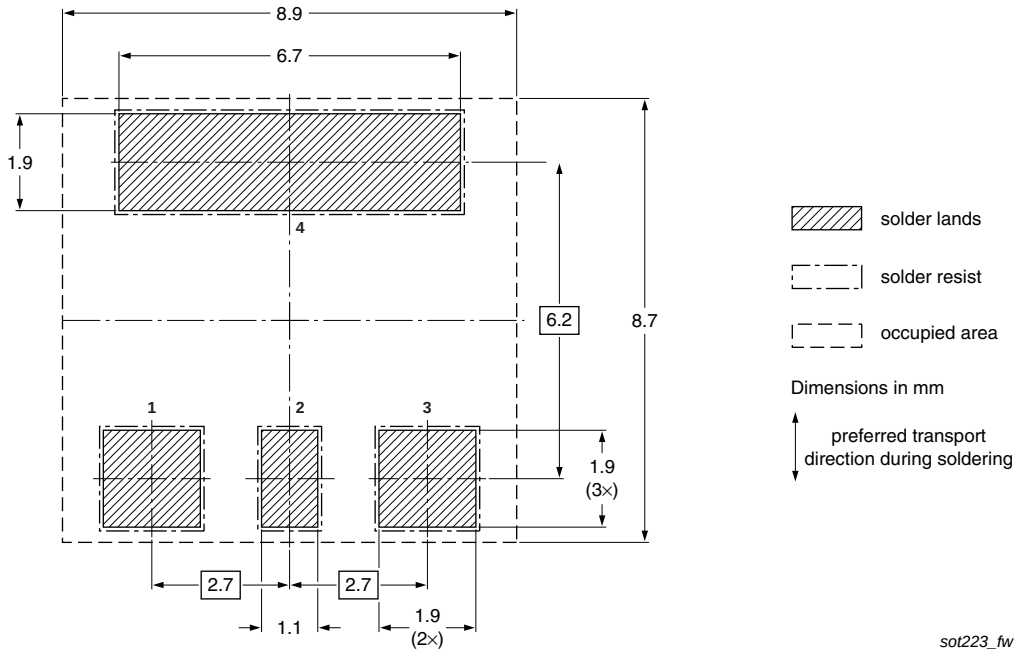


Fig 16. Wave soldering footprint for SOT223 (SC-73)

9. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
Z0103MN v.4	20100906	Product data sheet	-	Z0103MN v.3
Modifications:	• Various changes to content.			
Z0103MN v.3	20090805	Product data sheet	-	Z0103_07_09_SERIES v.2

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10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

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