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S1D13L01 Simple LCDC

Hardware Functional Specification

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Chapter 1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13L01 Series Simple LCD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 Operational Overview

The S1D13L01 is a simple LCD controller with an embedded 384K byte display buffer. The S1D13L01 supports both 8/16-bit direct/indirect CPU interfaces and a SPI CPU interface.

Resolutions supported are up to 480x272 at 24 bpp or 800x480 at 8 bpp for single layer display, or 400x240 at 24 bpp (Main Layer) and 400x240 at 8 bpp (PIP Layer) for two layer display. TFT panels are supported.

The S1D13L01 provides hardware rotation of the display memory transparent to the software application. The S1D13L01 supports both Alpha Blending and Transparency, and with PIP Layer Flashing both preset Blinking and Fade In/Out is achieved with simple register settings. With PIP Layer Flashing the displayed image looks rich, even when used with a low performance CPU.

Chapter 2 Features

2.1 Display Resolution

- 384K bytes of embedded VRAM for storing the image data
- Display Resolutions for one layer display (Main Layer Only):
  - Up to 480x272 at 24 bpp
  - Up to 800x480 at 8 bpp
- Display Resolutions for two layer display (Main and PIP Layer):
  - Up to 400x240 at 24 bpp (Main Layer) and 400x240 at 8 bpp (PIP Layer)

2.2 CPU Interface

- 8/16-bit Direct interface
- 8/16-bit Indirect interface
- SPI (Mode 0, Mode 3)

2.3 Input Data Format

- RGB 8:8:8, RGB 5:6:5, 8 bpp grayscale, or 8/16/24 bpp with Look-Up Table (LUT)

2.4 Display Interface

- Active Matrix TFT panels
  - 16/18/24-bit

2.5 Display Features

- Up to two display layers:
  - Main Layer
    - 8/16/24 bpp color depths with optional Look-up Table (LUT)
    - Independent rotation (0, 90, 180, 270° counter-clockwise)
  - PIP Layer
    - 8/16/24 bpp color depths with optional Look-up Table (LUT)
    - Independent rotation (0, 90, 180, 270° counter-clockwise)
    - Configurable PIP Effects allow automatic blink and fade in/out effects
- Alpha Blending
- Transparency
- Look-up Tables for Main and PIP Layers (256 address x 24 bpp)

2.6 Miscellaneous

- Single Clock Input: CLKI
- Embedded PLL
- Software initiated Power Save Modes
- General Purpose IO Pins are available
- Operating Temperature:
  S1D13L01F00A*** -40 to 85 °C

- Package:
  QFP15 128-pin (14mm x 14mm x 1.7mm)

Chapter 3 Typical System Implementation

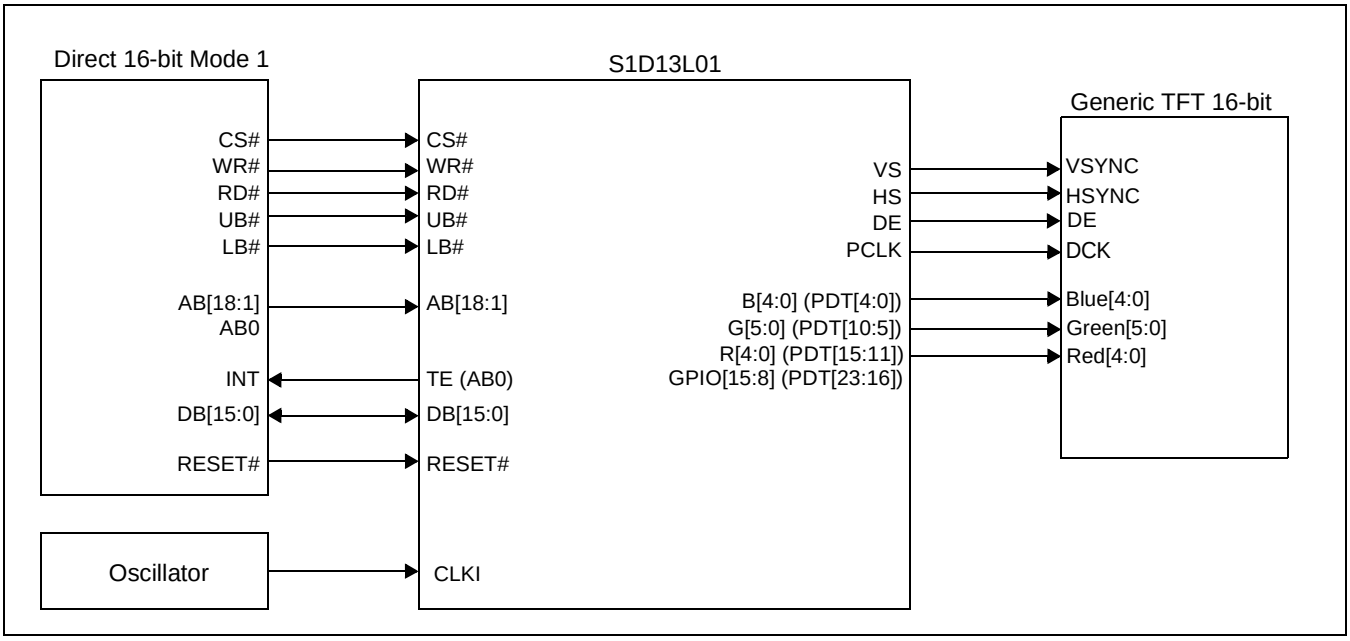


Figure 3-1: Typical System Diagram (Direct 16-bit Mode 1, Panel Generic TFT 16-bit)

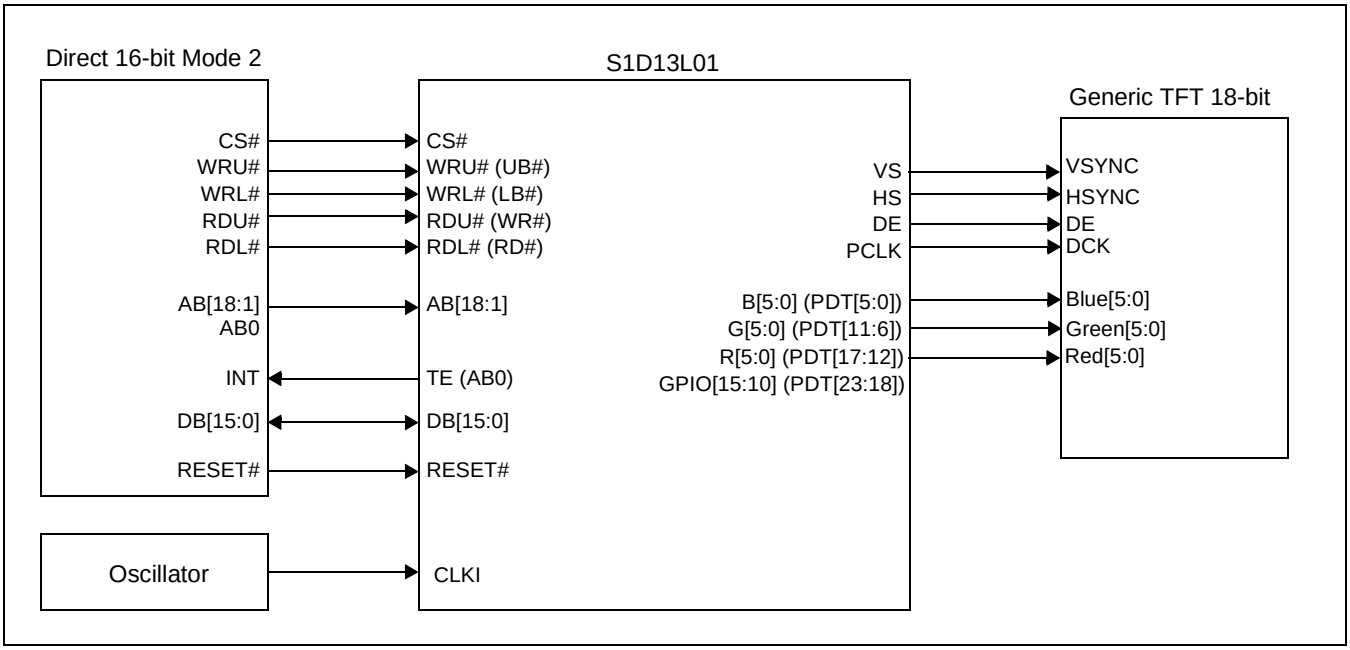


Figure 3-2: Typical System Diagram (Direct 16-bit Mode 2, Generic TFT 18-bit)

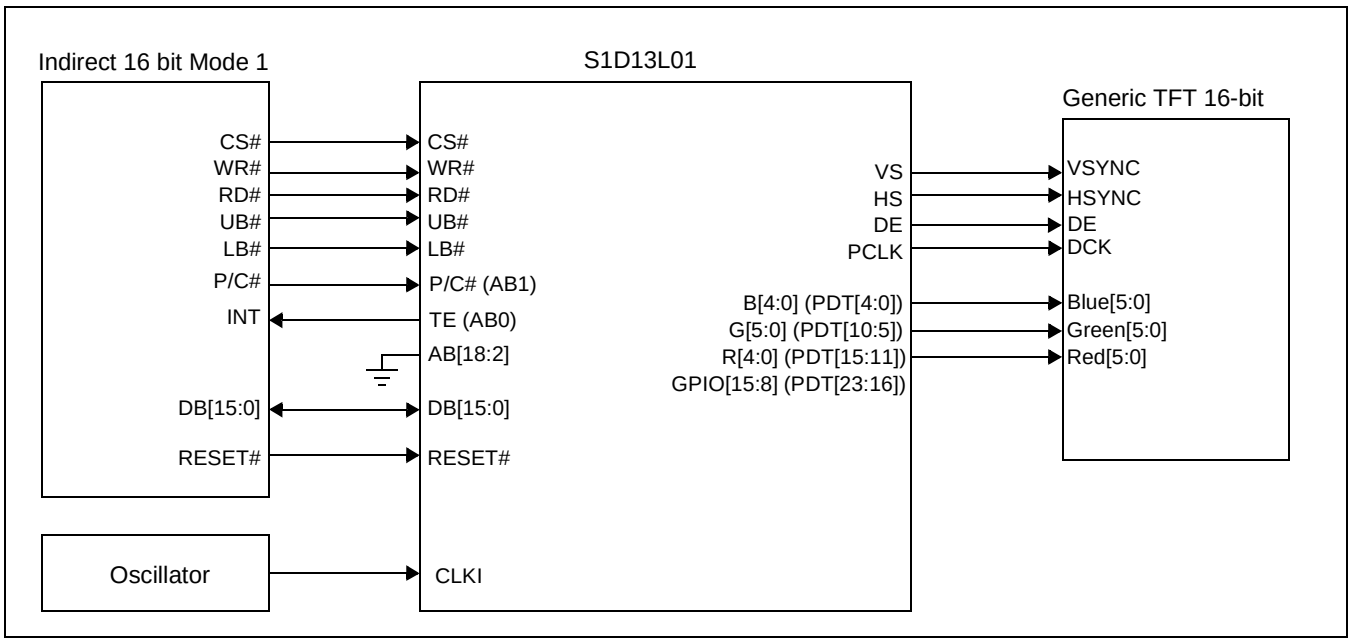


Figure 3-3: Typical System Diagram (Indirect 16-bit Mode 1, Generic TFT 16-bit)

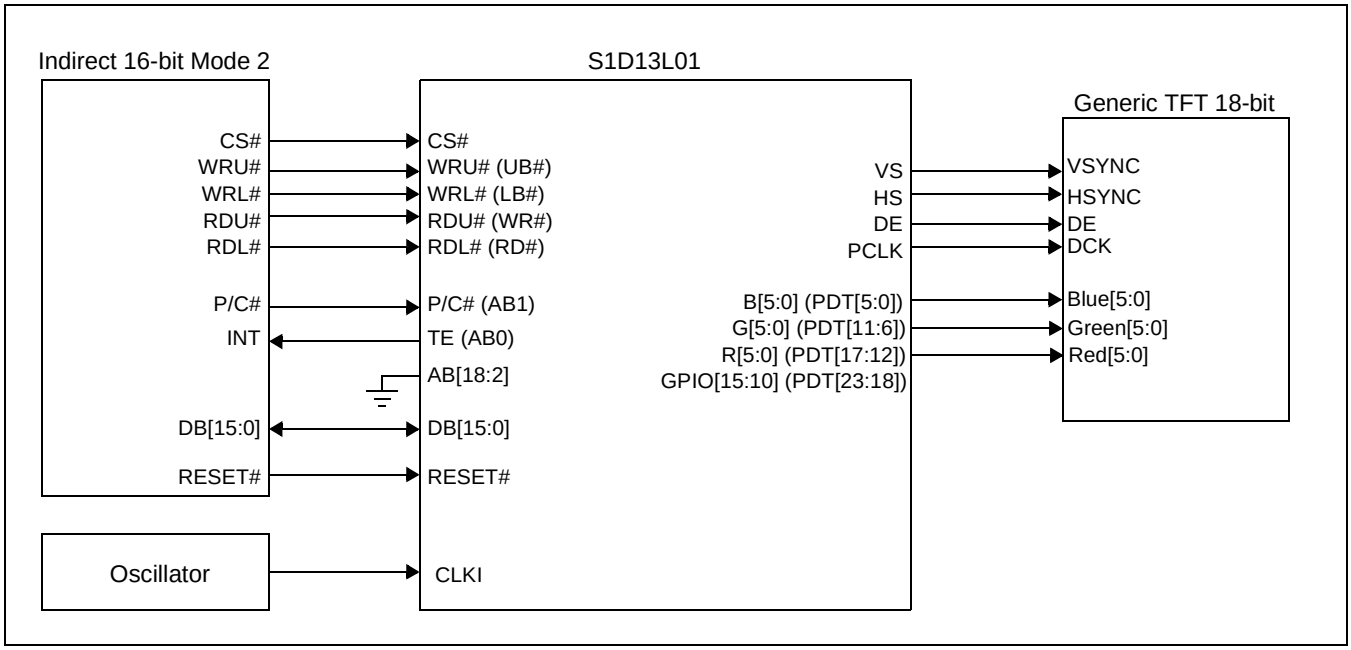


Figure 3-4: Typical System Diagram (Indirect 16-bit Mode 2, Generic TFT 18-bit)

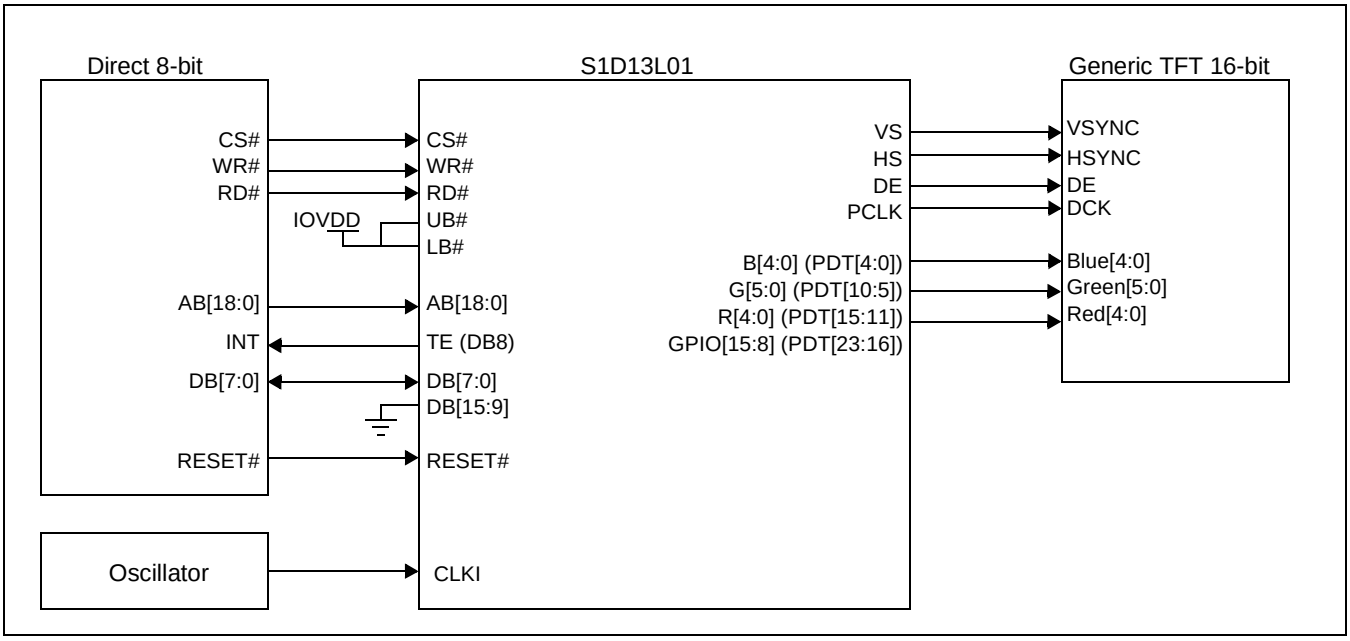


Figure 3-5: Typical System Diagram (Direct 8-bit, Generic TFT 16-bit)

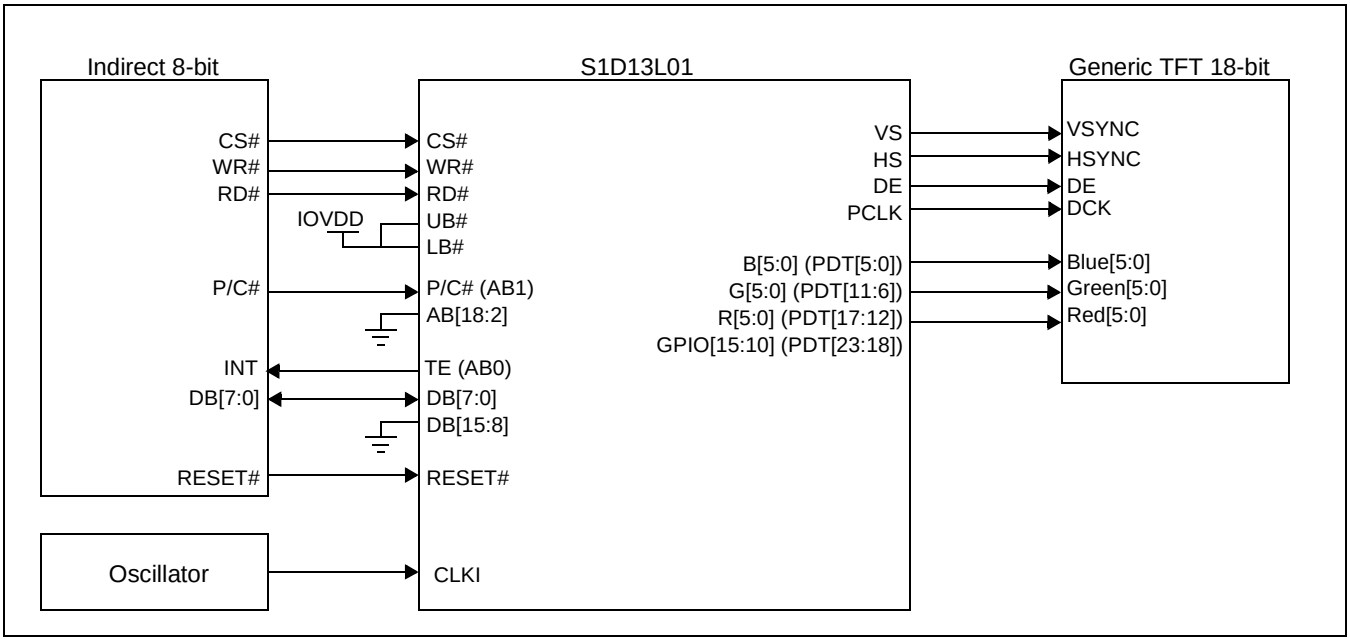


Figure 3-6: Typical System Diagram (Indirect 8-bit, Generic TFT 18-bit)

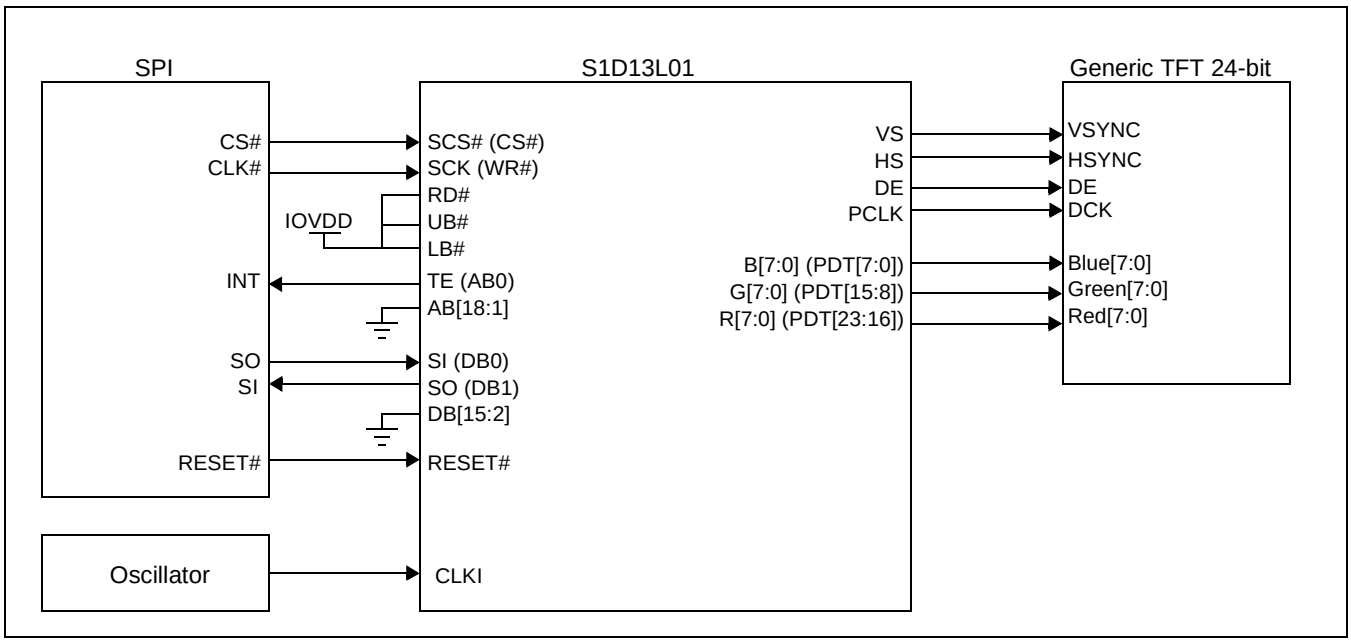


Figure 3-7: Typical System Diagram (SPI, Generic TFT 24-bit)

Chapter 4 Pins

4.1 Pinout Diagram

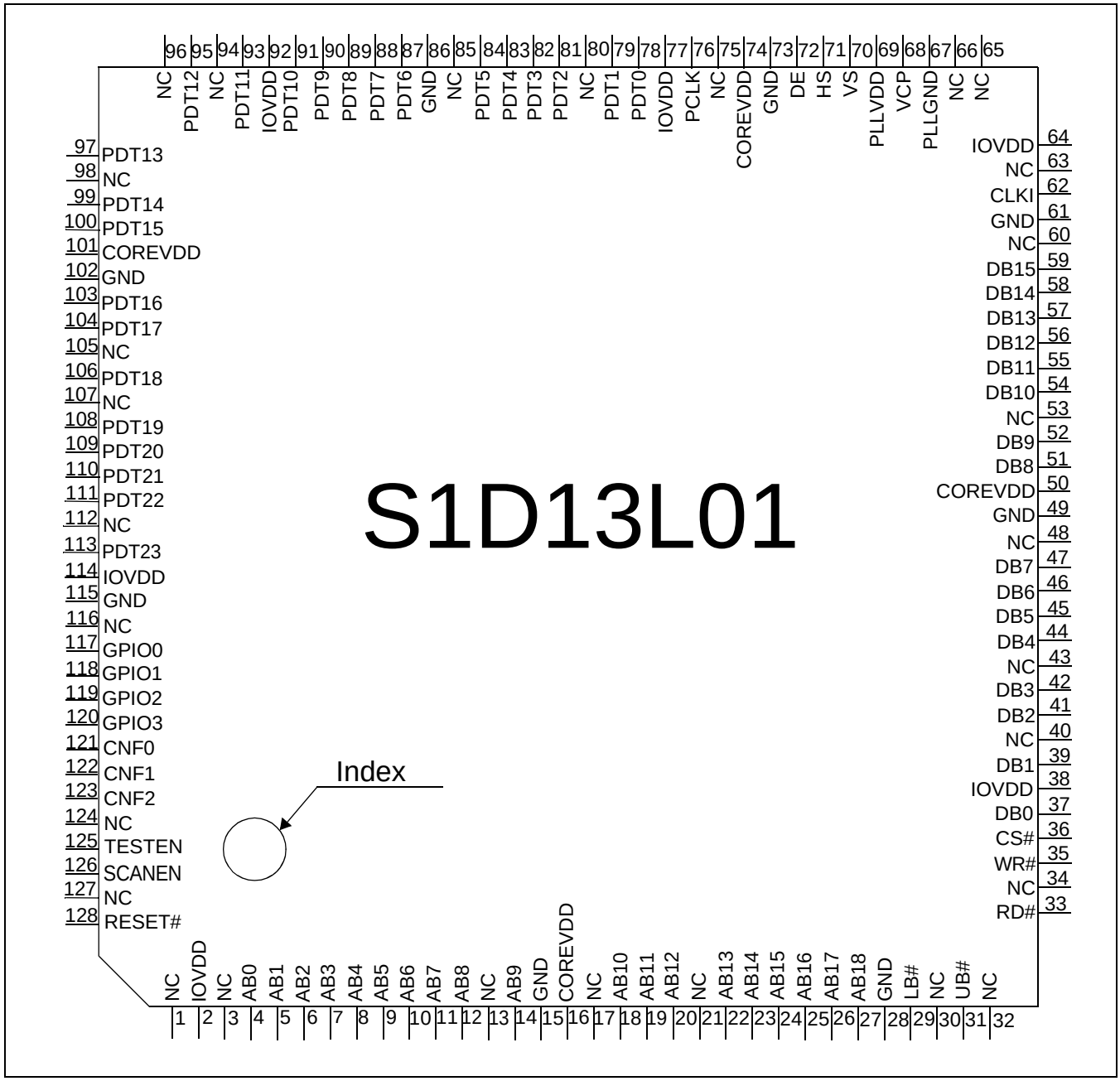


Figure 4-1 S1D13L01 Pinout Diagram (QFP15-128pin) - Top View

4.2 Pin Description

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
AP	=	Analog Power pin
G	=	Ground
AG	=	Analog Ground

RESET# / Power Save State

H	=	High level output
L	=	Low level output
Hi-Z	=	High Impedance
Q	=	Output Pin, retains output state
QB	=	IO Pin, if configured as output retains state

Table 4-1: Cell Description

Item	Description
HIS	H System LVCMOS Schmitt Input Buffer with Fail Safe
HISD	H System LVCMOS Schmitt Input Buffer with pull-down resistor and Fail Safe
HISU	H System LVCMOS Schmitt Input Buffer with pull-up resistor and Fail Safe
HID	H System LVCMOS Input Buffer with pull-down resistor and Fail Safe
HO	H System LVCOMOS Output buffer with Fail Safe
HB	H System LVCMOS Bidirectional Buffer with Fail Safe
HBD	H System LVCMOS Bidirectional Buffer with pull-down resistor and Fail Safe
LIDS	L System[2] LVCMOS Schmitt Input Buffer with pull-down resistor
LITR	L System Transparent Input Buffer

[1] H System is IOVDD (see Chapter 8, “D.C. Characteristics” on page 27).
[2] L System is COREVDD (see Chapter 8, “D.C. Characteristics” on page 27).
[3] LVCMOS is Low Voltage CMOS (see Chapter 8, “D.C. Characteristics” on page 27).

4.2.1 Host Interface

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	Pin#	Cell	Power	Power Save State	RESET# State	Description
CS#	I	36	HIS	IOVDD	—	—	This input pin is the Chip Select signal.
WR#	I	35	HIS	IOVDD	—	—	This input pin has multiple functions, WR#, RDU# and SCK. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
RD#	I	33	HISU	IOVDD	—	—	This input pin has multiple functions, RD# and RDL#. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
UB#	I	31	HISU	IOVDD	—	—	This input pin has multiple functions, UB# and WRU#. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
LB#	I	29	HISU	IOVDD	—	—	This input pin has multiple functions, LB# and WRL#. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
AB0	IO	4	HB	IOVDD	QB	—	This bidirectional pin has multiple functions, AB0 and TE. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
AB1	I	5	HID	IOVDD	—	—	This input pin has multiple functions, AB1 and P/C#. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
AB[18:2]	I	27~22, 20~18, 14,12~6	HID	IOVDD	—	—	These input pins are the host address bus AB[18:2]. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
DB0	IO	37	HB	IOVDD	—	—	This bidirectional pin has multiple functions, host data bus DB0 and SI. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
DB1	IO	39	HB	IOVDD	—	—	This bidirectional pin has multiple functions, host data bus DB1 and SO. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
DB[7:2]	IO	47~44, 42~41	HB	IOVDD	—	—	These bidirectional pins are the host data bus DB[7:2]. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
DB8	IO	51	HB	IOVDD	—	—	This bidirectional pin has multiple functions, host data bus DB8 and TE. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
DB[15:9]	IO	59~54,52	HB	IOVDD	—	—	These bidirectional pins are the host data bus DB[15:9]. See Section 4.4, “Host Interface Pin Mapping” on page 20 for details.
RESET#	I	128	HIS	IOVDD	—	—	Active low input to set all internal registers to the default state and to force all signals to their inactive states.

4.2.2 Panel Interface

Table 4-3: Panel Interface Pin Descriptions

Pin Name	Type	Pin#	Cell	Power	Power Save State	RESET# State	Description
PDT[11:0]	O	93, 91~87, 84~81, 79~78	HO	IOVDD	Q	L	These output pins are the panel data bus PDT[11:0]. See Section 4.5, “Panel Interface Pin Mapping” on page 21 for details.
PDT[23:12]	IO	113, 111~108, 106, 104~103, 100~99, 97,95	HBD	IOVDD	QB	L	These bidirectional pins have multiple functions, panel data bus PDT[23:12] and GPIO. See Section 4.5, “Panel Interface Pin Mapping” on page 21 for details.
VS	O	70	HO	IOVDD	Q	L	This output pin is VS, the panel vertical sync signal. See Section 4.5, “Panel Interface Pin Mapping” on page 21 for details.
HS	O	71	HO	IOVDD	Q	L	This output pin is HS, the panel horizontal sync signal. See Section 4.5, “Panel Interface Pin Mapping” on page 21 for details.
DE	O	72	HO	IOVDD	Q	L	This output pin has multiple functions, panel data bus enable DE and MOD. See Section 4.5, “Panel Interface Pin Mapping” on page 21 for details.
PDCLK	O	76	HO	IOVDD	Q	L	This output pin is PDCLK, pixel clock for panels. See Section 4.5, “Panel Interface Pin Mapping” on page 21 for details.

4.2.3 Clock Input

Table 4-4: Clock Input Pin Descriptions

Pin Name	Type	Pin#	Cell	Power	Power Save State	RESET# State	Description
CLKI	I	62	HIS	IOVDD	—	—	Input clock source for PLL or MCLK.

4.2.4 Miscellaneous

Table 4-5: Miscelaneous Pin Descriptions

Pin Name	Type	Pin#	Cell	Power	Power Save State	RESET# State	Description
TESTEN	I	125	LIDS	COREVDD	—	—	Test Enable input used for production test only. This pin must be connected directly to GND for normal operation.
SCANEN	I	126	HISD	IOVDD	—	—	Scan Enable input used for production test only. This pin must be connected directly to GND for normal operation.
VCP	O	68	LITR	PLLVDD	—	—	This pin is for production test only and should be left unconnected for normal operation.
CNF[2:0]	I	123~121	HIS	IOVDD	—	—	These inputs are used for power-on configuration. For details, see Table 4-7: “Summary of Power-On/Reset Options (Host Interface Selection),” on page 19. **Note:** These pins must be connected directly to IOVDD or GND.
GPIO[3:0]	IO	120~117	HBD	IOVDD	QB	—	These pins are a general purpose input/output. Default is input. See Section 10.6, “GPIO Setting Registers” on page 79 for details.
NC	—	1,3,13,17, 21,30,32, 34,40,43, 48,53,60, 63,65,66, 75,80,85, 94,96,98, 105,107, 112,116, 124,127	—	—	—	—	This pin must be left unconnected.

4.2.5 Power And Ground

Table 4-6: Power And Ground Pin Descriptions

Pin Name	Type	Pin#	Cell	Power	Power Save State	RESET# State	Description
IOVDD	P	2, 38, 64 77, 92, 114	P	—	—	—	IO power supply
COREVDD	P	16, 50, 74, 101	P	—	—	—	Core power supply
GND	G	15, 28, 49, 61, 73, 86, 102, 115	P	—	—	—	GND for digital
PLLVDD	AP	69	P	—	—	—	PLL Power Supply
PLLGND	AG	67	P	—	—	—	GND for PLL

4.3 Summary of Configuration Options

The CNF[2:0] pins are used for Host Interface selection and must be connected directly to IOVDD or GND.

Table 4-7: Summary of Power-On/Reset Options (Host Interface Selection)

Configuration Input	Power-On/Reset State	
	1 (connected to IOVDD)	0 (connected to GND)
CNF[2:0]	000: Direct 16-bit mode 1 001: Direct 16-bit mode 2 010: Indirect 16-bit mode 1 011: Indirect 16-bit mode 2 100: Direct 8-bit 101: Indirect 8-bit 110: Reserved 111: SPI	

4.4 Host Interface Pin Mapping

The S1D13L01 Host interface is selected by setting of the CNF[2:0] pins. For a summary of the Host interface options, see Section 4.3, “Summary of Configuration Options” on page 19.

Table 4-8: Host Interface Pin Mapping

S1D13L01 Pin Name	Direct 16-bit Mode 1	Direct 16-bit Mode 2	Indirect 16-bit Mode 1	Indirect 16-bit Mode 2	Direct 8-bit	Indirect 8-bit	SPI
CS#	CS#	CS#	CS#	CS#	CS#	CS#	SCS#
WR#	WR#	RDU#	WR#	RDU#	WR#	WR#	SCK
RD#	RD#	RDL#	RD#	RDL#	RD#	RD#	H
UB#	UB#	WRU#	UB#	WRU#	H	H	H
LB#	LB#	WRL#	LB#	WRL#	H	H	H
AB0	TE	TE	TE	TE	AB0	TE	TE
AB1	AB1	AB1	P/C#	P/C#	AB1	P/C#	Low
AB[18:2]	AB[18:2]	AB[18:2]	Low	Low	AB[18:2]	Low	Low
DB0	DB0	DB0	DB0	DB0	DB0	DB0	SI
DB1	DB1	DB1	DB1	DB1	DB1	DB1	SO
DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	DB[7:2]	L
DB8	DB8	DB8	DB8	DB8	TE	L	L
DB[15:9]	DB[15:9]	DB[15:9]	DB[15:9]	DB[15:9]	L	L	L

Where:

H = Connect directly to IOVDD.
L = Connect directly to GND.
Low = Internal pull-down for address bus is active.
TE is defined by REG[22h] bits 6-5.

4.5 Panel Interface Pin Mapping

Panel interface mode selection is specified by REG[20h] bits 3-0.

Table 4-9: Panel Interface Pin Mapping

S1D13L01 Pin	Generic TFT		
	16-bit	18-bit	24-bit
VS	VS	VS	VS
HS	HS	HS	HS
DE	DE	DE	DE
PDCLK	PCLK	PCLK	PCLK
PDT0	B0	B0	B0
PDT1	B1	B1	B1
PDT2	B2	B2	B2
PDT3	B3	B3	B3
PDT4	B4	B4	B4
PDT5	G0	B5	B5
PDT6	G1	G0	B6
PDT7	G2	G1	B7
PDT8	G3	G2	G0
PDT9	G4	G3	G1
PDT10	G5	G4	G2
PDT11	R0	G5	G3
PDT12	R1	R0	G4
PDT13	R2	R1	G5
PDT14	R3	R2	G6
PDT15	R4	R3	G7
PDT16	GPIO8	R4	R0
PDT17	GPIO9	R5	R1
PDT18	GPIO10	GPIO10	R2
PDT19	GPIO11	GPIO11	R3
PDT20	GPIO12	GPIO12	R4
PDT21	GPIO13	GPIO13	R5
PDT22	GPIO14	GPIO14	R6
PDT23	GPIO15	GPIO15	R7

Note

When PDT[23:12] are assigned as panel data bus, the internal pull down is inactive. When PDT[23:12] are assigned as GPIO, the internal pull down is controlled by REG[D4h].

Chapter 5 Logic Diagram

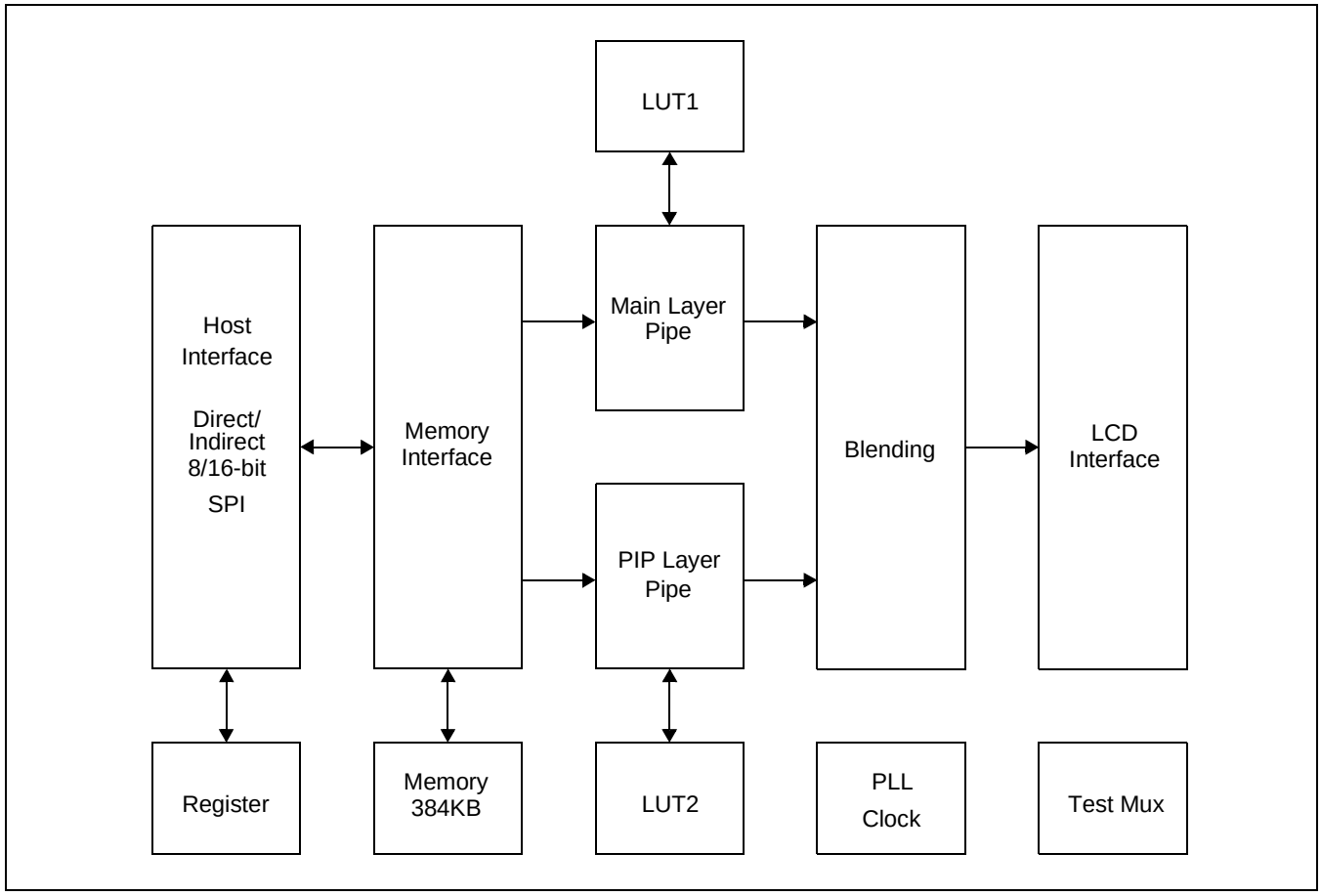


Figure 5-1: Block Diagram

Chapter 6 Embedded Memory

6.1 Memory Map

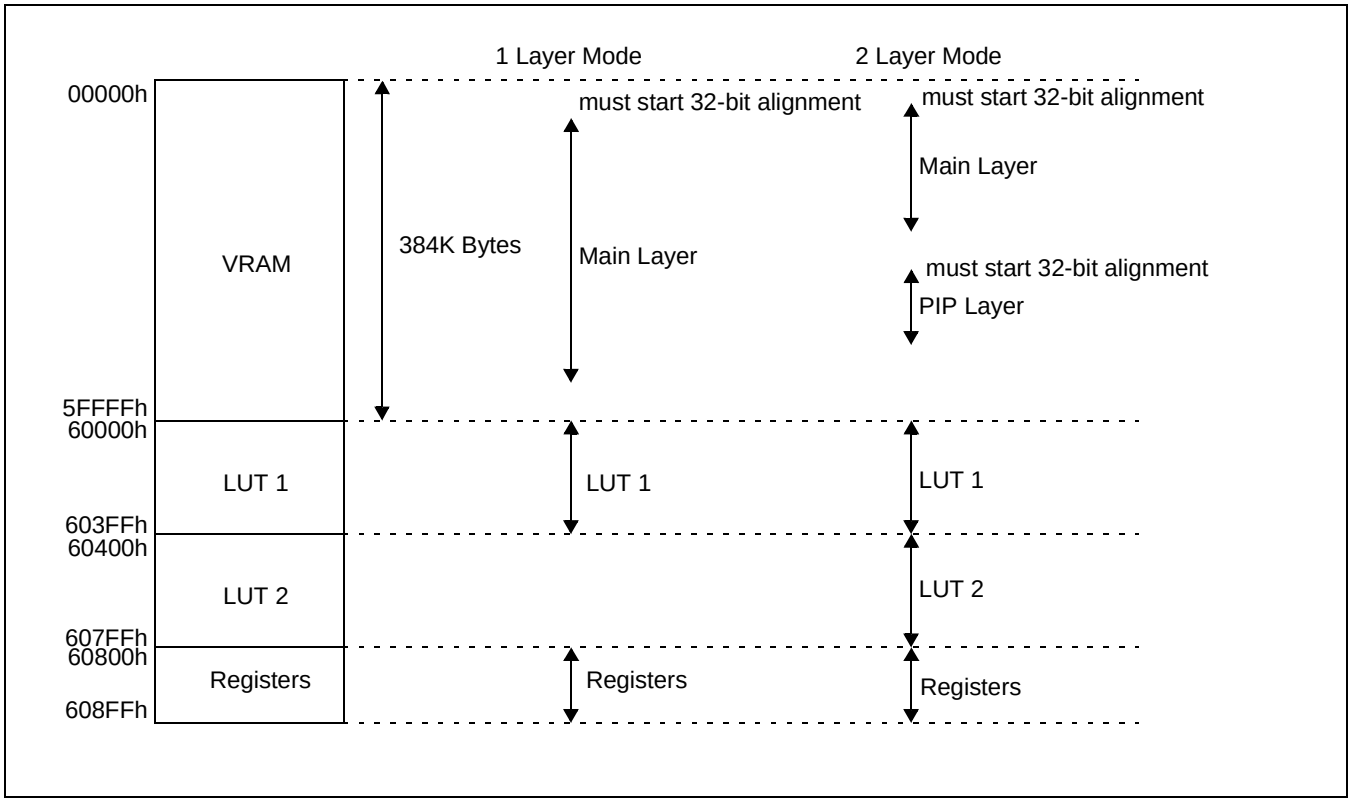


Figure 6-1: Memory Construction for Direct Interface

The S1D13L01 has 384K bytes of memory. The VRAM, Registers, and LUT are directly mapped.

6.2 Sample Maximum Resolution

When in 1 Layer Mode (PIP Layer off, REG[60h] bits 2-0 = 000b), all 384K bytes of VRAM are assigned for the Main Layer. The Main Layer start address (REG[42h] ~ REG[44h]) must maintain 32-bit alignment. Maximum Main Layer resolutions are shown in the following table.

Table 6-1: Maximum Main Layer Resolutions for 1 Layer Mode

Input Data Format	Horizontal	Vertical
RGB 8:8:8	480	273
RGB 5:6:5	480	409
8 bpp + LUT1	800	491

When in 2 Layer Mode (PIP Layer on, REG[60h] bits 2-0 = 001b ~ 111b), the 384K bytes of VRAM are assigned to both the Main Layer and PIP Layer. Both the Main Layer Start Address (REG[42h] ~ REG[44h]) and PIP Layer Start Address (REG[52h] ~ REG[54h]) must maintain 32-bit alignment. maximum combination resolutions for Main and PIP layer are shown in the following table.

Table 6-2: Maximum Combination Resolutions for 2 Layer Mode

Example	Layer	Input Data Format	Horizontal	Vertical
1	Main	RGB 8:8:8	400	240
	PIP	8 bpp + LUT2	400	240
2	Main	RGB 8:8:8	480	240
	PIP	RGB 5:6:5	200	110
3	Main	RGB 8:8:8	270	240
	PIP	RGB 8:8:8	270	240

Chapter 7 Clocks

7.1 Clock Tree

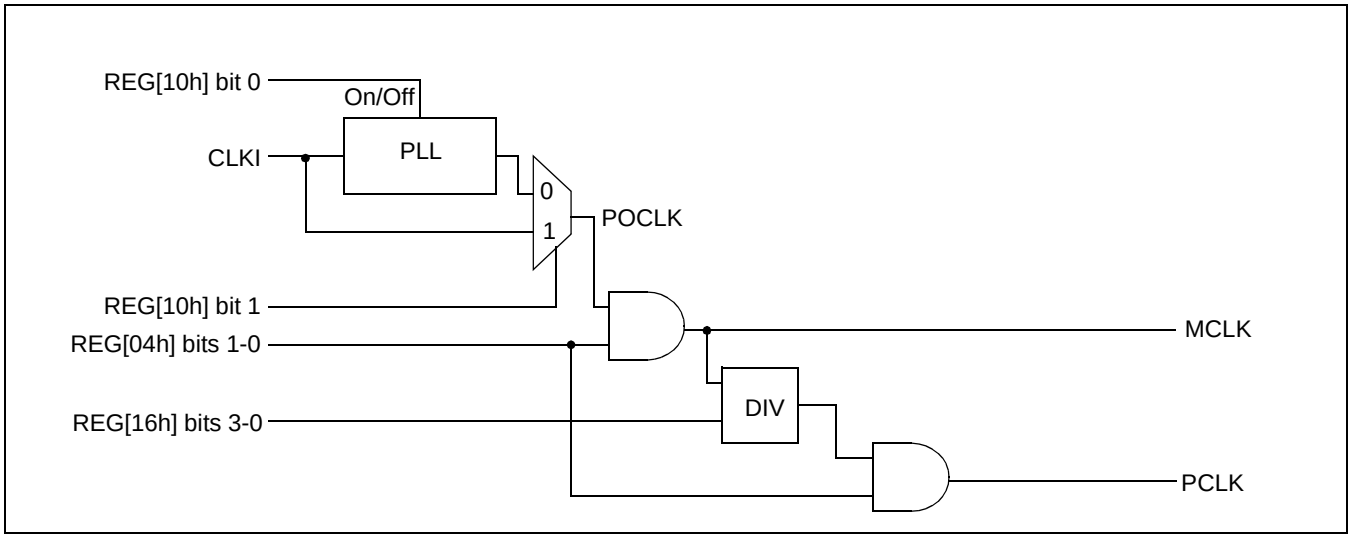


Figure 7-1: Clock Diagram

7.2 PLL Setting

PLL related registers (REG[10h] through REG[14h]) must be set as shown in the following figure.

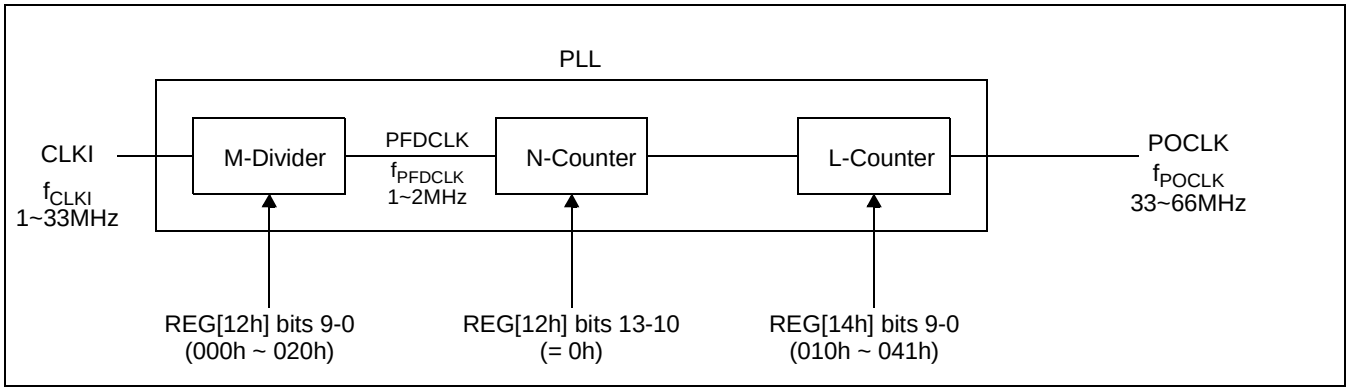


Figure 7-2: PLL Settings

Note
If the S1D13L01 is configured to use the PLL output as the MCLK source and the Host wants to turn off the input clock (CLKI), the Host must disable the PLL (REG[10h] bit 0 = 0b) before shutting off CLKI. This procedure ensures that the PLL Lock bit (REG[10h] bit 15) goes low. Once CLKI has been turned back on, the Host should re-enable the PLL.

7.3 Clock Setting Minimum Requirement

REG[16h], the Internal Clock Configuration Register, defines the PCLK (Pixel Clock) ratio from MCLK (Memory Clock). When the panel interface block requests more pixel data than the memory interface block can provide, garbage data will be displayed. This means that when the MCLK to PCLK divide ratio is too low (REG[16h] bits 3-0), the memory interface block cannot provide data to the PCLK at the rate set. Panel interface block requirements depend on PIP enable and rotation of both Main and PIP window. Following table shows minimum setting examples for REG[16h].

Table 7-1: REG[16] Minimum Setting Examples

Main Window	**Bpp**	8	8	16	16	24	24	24	24
	Rotation	0/180	90/270	0/180	90/270	0/180	90/270	0/180	90/270
	Hit Ratio	0.25	1.00	0.50	1.00	0.75	2.00	0.75	2.00
PIP Window	**Bpp**	-	8	8	16	8	16	24	24
	Rotation	-	0/180	0/180	0/180	0/180	0/180	0/180	90/270
	Hit Ratio	0.00	0.25	0.25	0.50	0.25	0.50	0.75	2.00
Total Hit Ratio		0.25	1.25	0.75	1.50	1.00	2.50	1.50	4.00
REG[16] Minimum Setting		0 (1:1)	1 (2:1)	0 (1:1)	1 (2:1)	0 (1:1)	2 (3:1)	1 (2:1)	3 (4:1)

Note
The above table does not take into account Host accessing. For actual settings, space must be reserved for Host accessing.

Chapter 8 D.C. Characteristics

8.1 Absolute Maximum Ratings

Table 8-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Core Supply Voltage	GND - 0.3 to 2.0	V
PLL V_{DD}	PLL Supply Voltage	GND - 0.3 to 2.0	V
IO V_{DD}	Host IO Supply Voltage	COREVDD to 4.0	V
V_{IN}	Input Voltage	GND - 0.3 to IOVDD + 0.3	V
V_{OUT}	Output Voltage	GND - 0.3 to IOVDD + 0.3	V
I_{OUT}	Output Current	±10	mA

8.2 Recommended Operating Conditions

Table 8-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Core Supply Voltage	GND = 0 V	1.35	1.5	1.65	V
PLL V_{DD}	PLL Supply Voltage	GND = 0 V	1.35	1.5	1.65	V
IO V_{DD}	Host IO Supply Voltage	GND = 0 V	1.62	1.8/3.3	3.6	V
V_{IN}	Input Voltage	—	GND	—	IOVDD	V
T_{OPR}	Operating Temperature	S1D13L01F00A***	-40	25	85	°C
T_{stg}	Storage Temperature	S1D13L01F00A***	-65		150	°C

8.3 Electrical Characteristics

The following characteristics are for: T_{OPR} = -40 to 85 °C (S1D13L01F00A***)

Table 8-3: IOVDD = 3.3V ± 0.3V, GND = 0V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Off State Leakage Current	—	-5	—	5	
IOV_{OH}	High Level Output Voltage	IOVDD = Min. IOH = -4mA	IOVDD-0.4	—	—	V
IOV_{OL}	Low Level Output Voltage	IOVDD = Min. IOL = 4mA	—	—	0.4	V
V_{IH}	High Level Input Voltage	LVCMOS Level, IOVDD = Max.	2.2	—	IOVDD+0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level, IOVDD = Min.	-0.3	—	0.8	
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	1.2	—	2.52	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.75	—	1.98	
ΔV	Hysteresis Voltage	LVCMOS Schmitt	0.3	—	—	V
R_{PU}	Pull-up Resistance	VI = 0V	20	50	120	kΩ
R_{PD}	Pull-down Resistance	VI = IOVDD	20	50	120	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, IOVDD = 0V	—	—	10	pF

Table 8-4: IOVDD = 1.8V ± 0.18V, GND = 0V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Off State Leakage Current	—	-5	—	5	
IOV_{OH}	High Level Output Voltage	IOVDD = Min. IOH = -1.8mA	IOVDD-0.4	—	—	V
IOV_{OL}	Low Level Output Voltage	IOVDD = Min. IOL = 1.8mA	—	—	0.4	V
V_{IH}	High Level Input Voltage	LVCMOS Level, IOVDD = Max.	1.39	—	IOVDD+0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level, IOVDD = Min.	-0.3	—	0.48	
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	0.57	—	1.48	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.41	—	1.28	
ΔV	Hysteresis Voltage	LVCMOS Schmitt	0.17	—	—	V
R_{PU}	Pull-up Resistance	VI = 0V	36	100	244	kΩ
R_{PD}	Pull-down Resistance	VI = IOVDD	36	100	244	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, IOVDD = 0V	—	—	10	pF

Chapter 9 A.C. Characteristics

Conditions:

IOVDD = 1.62V ~ 3.60V
T_A = -40 °C to 85 °C (S1D13L01F00A***)
T_{rise} and T_{fall} for all inputs except Schmitt and CLKI must be ≤ 50 ns (10% ~ 90%)
T_{rise} and T_{fall} for all Schmitt must be ≤ 5 ms (10% ~ 90%)
C_L = 8pF ~ 30pF (Panel I/F)

9.1 Clock Timing

9.1.1 Input Clocks

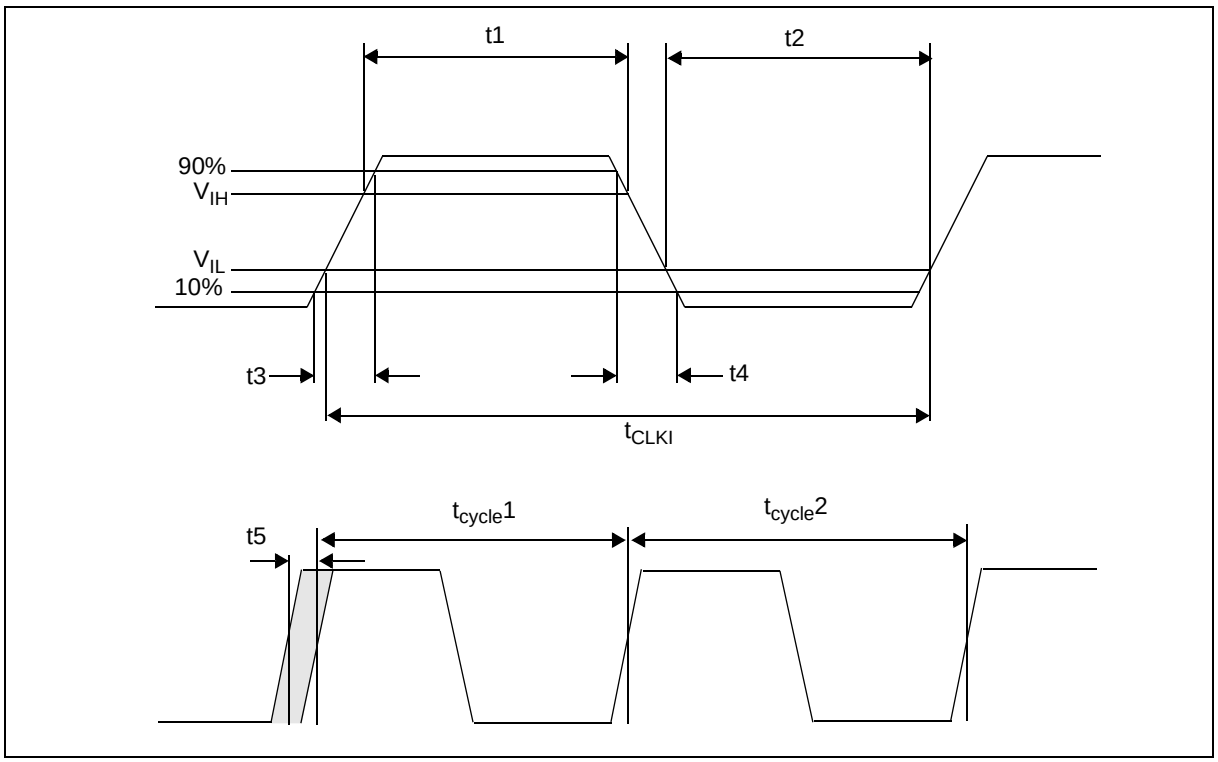


Figure 9-1 Clock Input Required (PLL)

Table 9-1: Clock Input Requirements for PLL (CLKI)

Symbol	Parameter	Min	Typ	Max	Units
f_{CLKI}	Input clock frequency	1	1	33	MHz
t_{CLKI}	Input clock period	—	$1/f_{CLKI}$	—	µs
t1	Input clock pulse width high	0.45	—	0.55	t_{CLKI}
t2	Input clock pulse width low	0.45	—	0.55	t_{CLKI}
t3	Input clock rise time (10% - 90%)	—	—	10	ns
t4	Input clock fall time (90% - 10%)	—	—	10	ns
t5	Input clock period jitter (see Note 1)	-300	—	300	ps

1. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).

Table 9-2: Clock Input Requirements for PLL Bypassed (CLKI)

Symbol	Parameter	Min	Typ	Max	Units
f_{CLKI}	Input clock frequency	—	—	66	MHz
t_{CLKI}	Input clock period	—	$1/f_{CLKI}$	—	µs
t1	Input clock pulse width high	6.8	—	—	ns
t2	Input clock pulse width low	6.8	—	—	ns
t3	Input clock rise time (10% - 90%)	—	—	5	ns
t4	Input clock fall time (90% - 10%)	—	—	5	ns

9.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

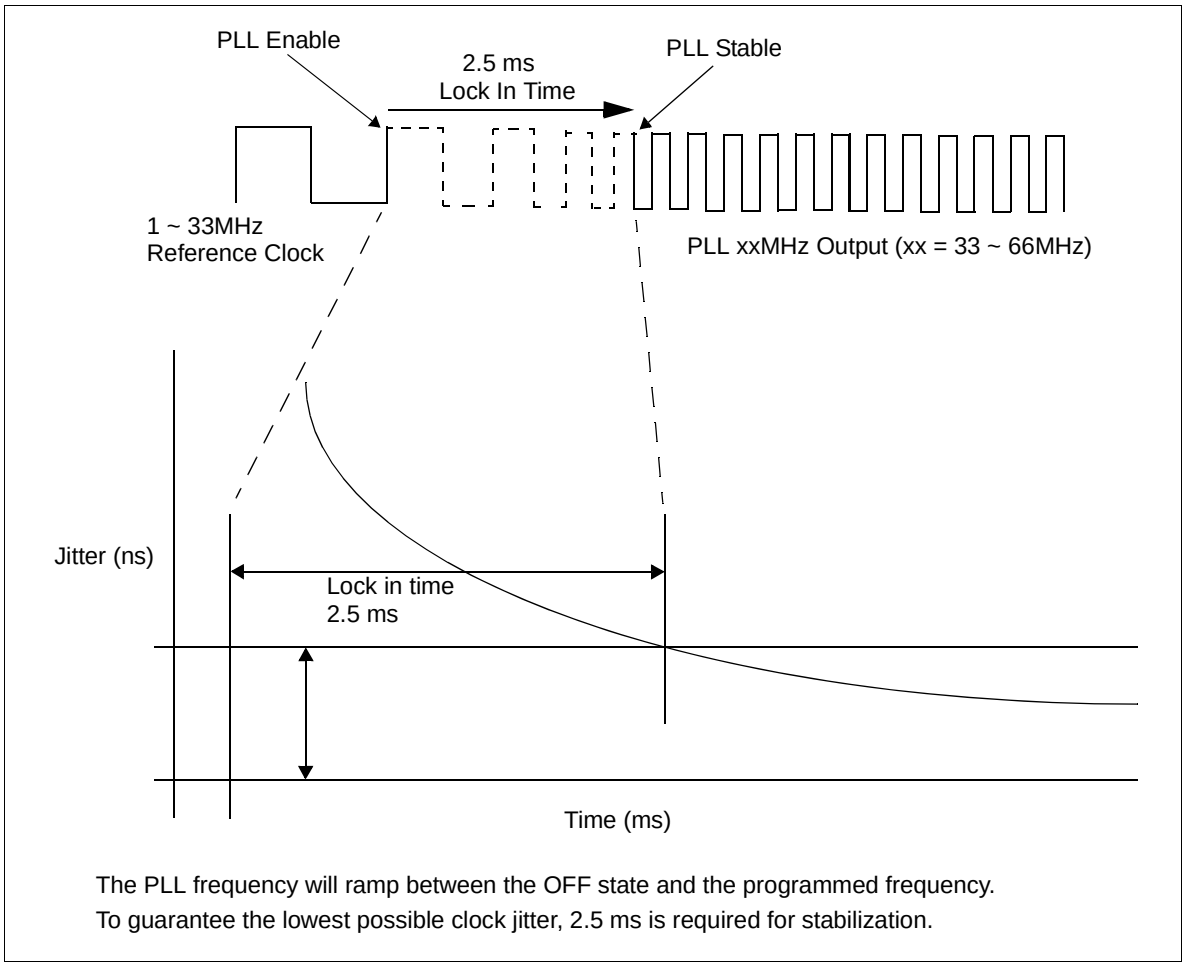


Figure 9-2: PLL Start-Up Time

Table 9-3: PLL Characteristics

Symbol	Parameter	Min	Max	Units
f_{PLLI}	PLL input clock frequency after M-Divider	1	2	MHz
f_{PLLI2}	PLL input clock frequency before M-Divider	1	33	MHz
f_{PLLO}	PLL output clock frequency	33	66	MHz
t_{PJref}	PLL output clock period jitter	-3	3	%
t_{PDuty}	PLL output clock duty cycle	30	70	%
t_{PStal}	PLL output stable time	—	2.5	ms

9.2 RESET# Timing

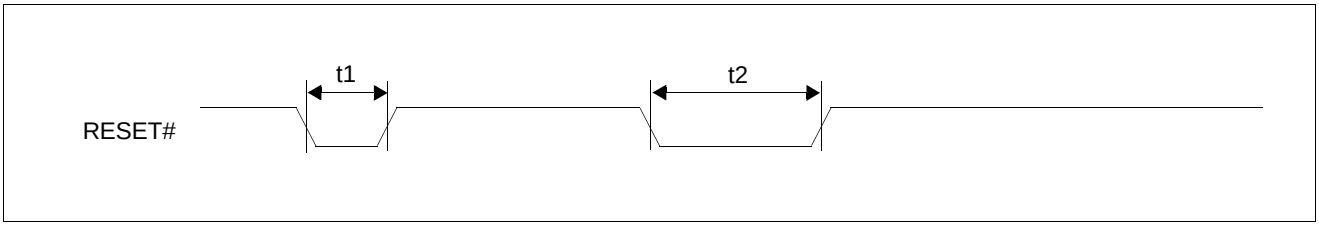


Figure 9-3 RESET# Timing

Table 9-4 RESET# Timing

Symbol	Parameter	Min	Max	Units
t1	Reset Pulse Width is ignored	—	42	ns
t2	Active Reset Pulse Width (see Note)	150	—	ns

1. The RESET# line should be held low longer than 150ns to guarantee reset.

9.3 Power Supply Sequence

9.3.1 Power-On Sequence

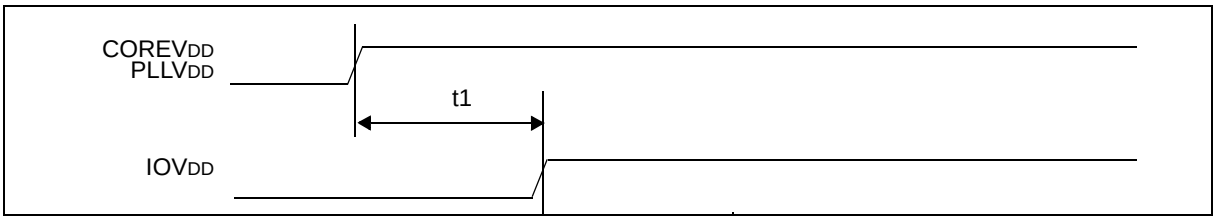


Figure 9-4: Power-On Sequence

Table 9-5: Power-On Sequence

Symbol	Parameter	Min	Max	Units
t1	IOVDD on delay from COREVDD, PLLVDD on	0	500	ms

Note
The sequence of COREVDD to IOVDD may be reversed as long as the timing is within the 500ms maximum.

9.3.2 Power-Off Sequence

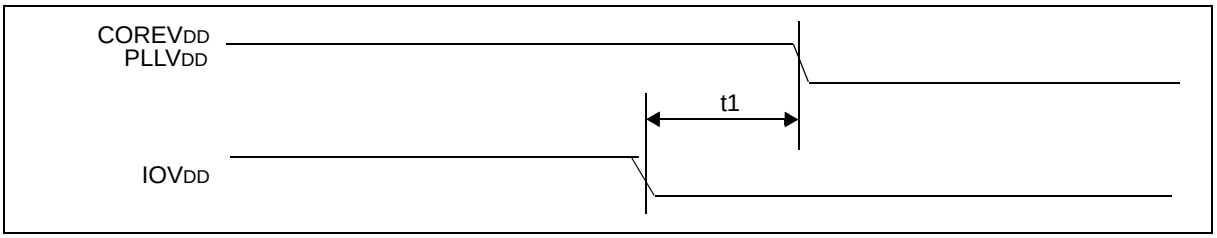


Figure 9-5: Power-Off Sequence

Table 9-6: Power-Off Sequence

Symbol	Parameter	Min	Max	Units
t1	COREVDD, PLLVDD off delay from IOVDD	0	500	ms

Note
The sequence of COREVDD to IOVDD may be reversed as long as the timing is within the 500ms maximum.

9.4 Host Interface Timing

9.4.1 Direct 16-bit Mode 1 Timing

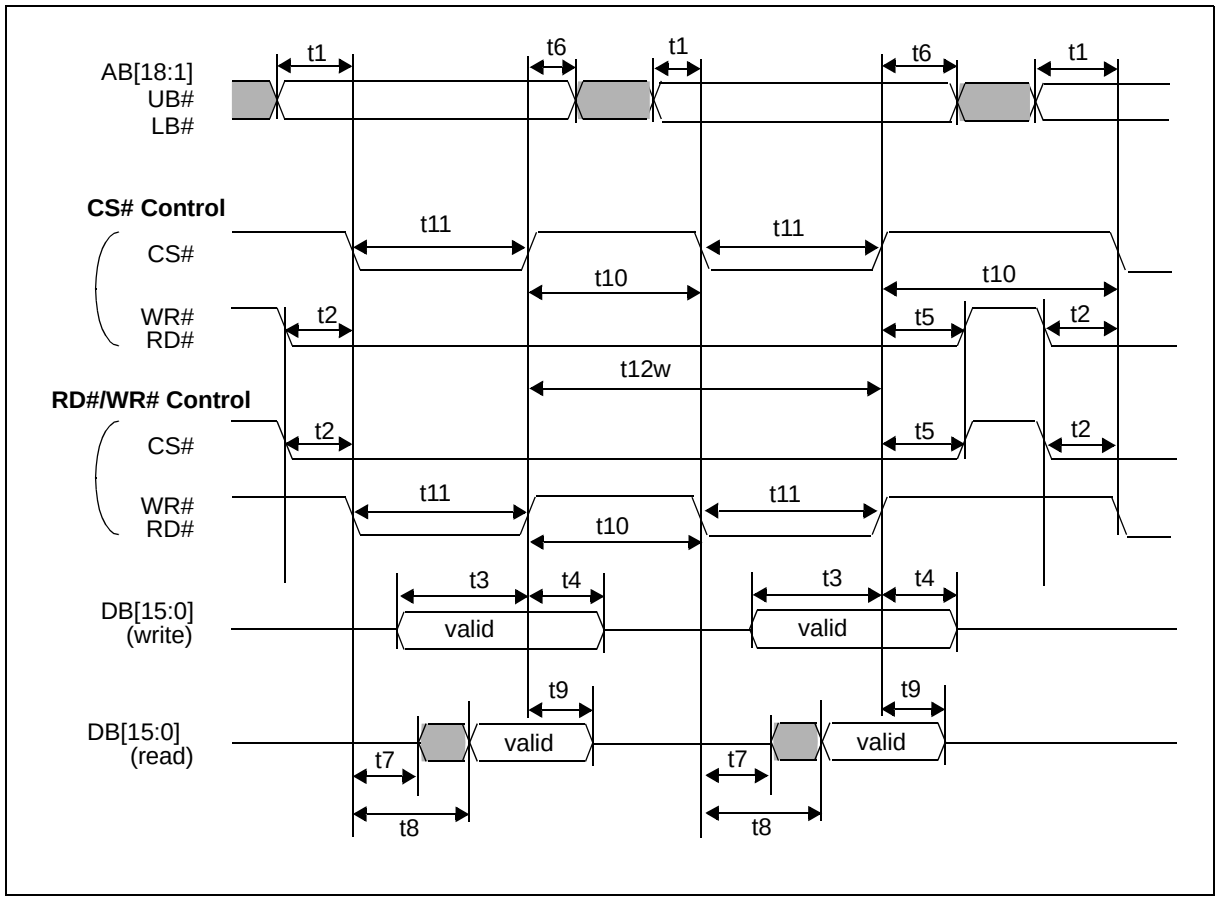


Figure 9-6: Direct 16-bit Mode 1 Timing

Table 9-7: Direct 16-bit Mode 1 Timing

Symbol	Parameter	3.3 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t1	AB[18:1], UB#, LB# setup time to CS# (WR#, RD#)	2	-	1	-	ns
t2	WR#,RD# (CS#) setup time to CS# (WR#, RD#)	1	-	1	-	ns
t3	DB[15:0] setup time to CS# (WR#) rising edge: write cycle	1	-	1	-	ns
t4	DB[15:0] hold time from CS# (WR#) rising edge: write cycle	7	-	8	-	ns
t5w	WR# (CS#) hold time from CS# (WR#) rising edge: write cycle	3	-	3	-	ns
t5r	RD# (CS#) hold time from CS# (RD#) rising edge: read cycle	0	-	0	-	ns
t6	AB[18:1], UB#, LB# hold time from CS# (WR#, RD#) rising edge	5	-	5	-	ns
t7	CS# (RD#) falling edge to DB[15:0] driven: read cycle	-	15	-	21	ns
t8	CS# (RD#) falling edge to valid Data: read cycle	-	$4xT_{mclk}+16$	-	$4xT_{mclk}+23$	ns
t9	DB[15:0] hold time from CS# (RD#) rising edge: read cycle	2	12	2	14	ns
t10w	End of write to next read/write	7	-	6	-	ns
t10r	End of read to next read/write	$T_{mclk}+9$	-	$T_{mclk}+10$	-	ns
t11w	CS# (WR#) pulse width for write cycle	3	-	5	-	ns
t12w	CS# (WR#) rise to next CS# (WR#) rise: write cycle	$3xT_{mclk}+6$	-	$3xT_{mclk}+6$	-	ns

T_{mclk} = period of internal MCLK clock signal

9.4.2 Direct 16-bit Mode 2 Timing

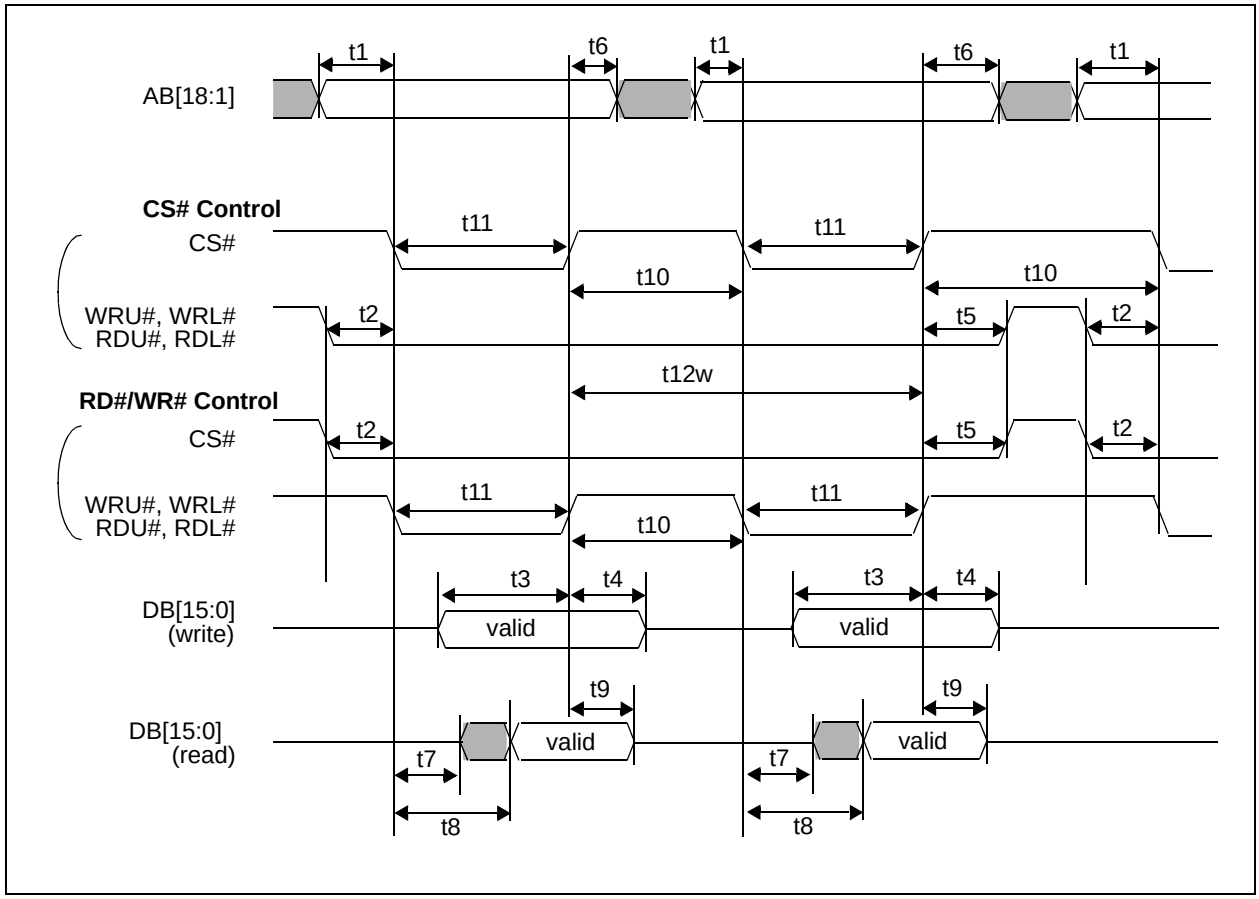


Figure 9-7: Direct 16-bit Mode 2 Timing

Table 9-8: Direct 16-bit Mode 2 Timing

Symbol	Parameter	3.3 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t1	AB[18:1] setup time to CS# (WRU#, WRL#, RDU#, RDL#)	2	-	1	-	ns
t2	WRU#, WRL#, RDU#, RDL# (CS#) setup time to CS# (WRU#, WRL#, RDU#, RDL#)	2	-	2	-	ns
t3	DB[15:0] setup time to CS# (WRU#, WRL#) rising edge: write cycle	1	-	1	-	ns
t4	DB[15:0] hold time from CS# (WRU#, WRL#) rising edge: write cycle	7	-	8	-	ns
t5w	WRU#, WRL# (CS#) hold time from CS# (WRU#, WRL#) rising edge: write cycle	3	-	3	-	ns
t5r	RDU#, RDL# (CS#) hold time from CS# (RDU#, RDL#) rising edge: read cycle	0	-	0	-	ns
t6	AB[18:1] hold time from CS# (WRU#, WRL#, RDU#, RDL#) rising edge	5	-	5	-	ns
t7	CS# (RDU#, RDL#) falling edge to DB[15:0] driven: read cycle	-	15	-	21	ns
t8	CS# (RDU#, RDL#) falling edge to valid Data: read cycle	-	$4xT_{mclk}+16$	-	$4xT_{mclk}+23$	ns
t9	DB[15:0] hold time from CS# (RDU#, RDL#) rising edge: read cycle	2	12	2	14	ns
t10w	End of write to next read/write	7	-	7	-	ns
t10r	End of read to next read/write	$T_{mclk}+9$	-	$T_{mclk}+10$	-	ns
t11w	CS# (WRU#, WRL#) pulse width for write cycle	3	-	5	-	ns
t12w	CS# (WRU#, WRL#) rise to next CS# (WRU#, WRL#) rise: write cycle	$3xT_{mclk}+6$	-	$3xT_{mclk}+6$	-	ns

T_{mclk} = period of internal MCLK clock signal

9.4.3 Indirect 16-bit Mode 1 Timing

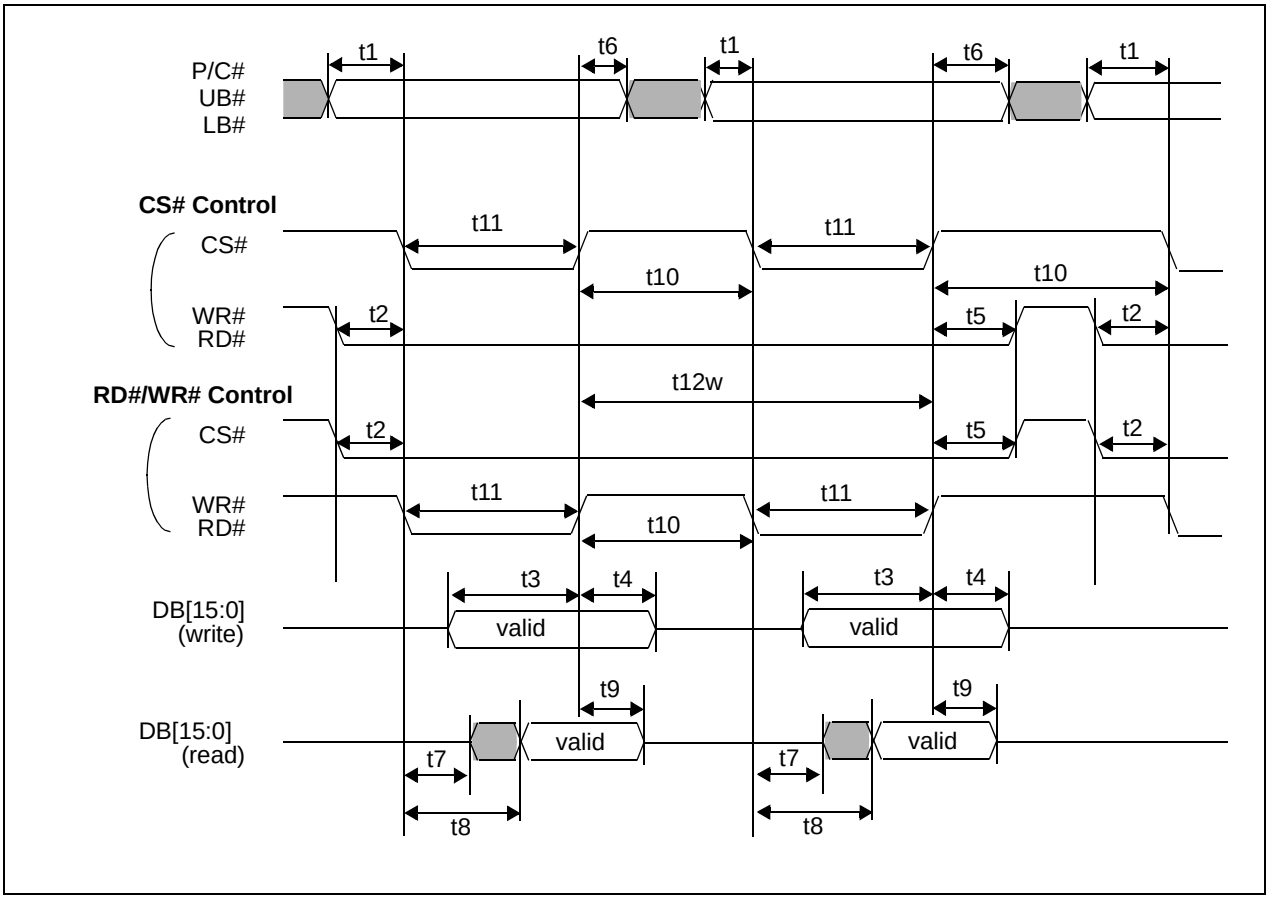


Figure 9-8: Indirect 16-bit Mode 1 Timing

Table 9-9: Indirect 16-bit Mode 1 Timing

Symbol	Parameter	3.3 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t1	P/C#, UB#, LB# setup time to CS# (WR#, RD#)	1	-	1	-	ns
t2	WR#, RD# (CS#) setup time to CS# (WR#, RD#)	1	-	1	-	ns
t3	DB[15:0] setup time to CS# (WR#) rising edge: write cycle	1	-	1	-	ns
t4	DB[15:0] hold time from CS# (WR#) rising edge: write cycle	7	-	8	-	ns
t5w	WR# (CS#) hold time from CS# (WR#) rising edge: write cycle	3	-	3	-	ns
t5r	RD# (CS#) hold time from CS# (RD#) rising edge: read cycle	0	-	0	-	ns
t6	P/C#, UB#, LB# hold time from CS# (WR#, RD#) rising edge	4	-	4	-	ns
t7	CS# (RD#) falling edge to DB[15:0] driven: read cycle	-	15	-	21	ns
t8	CS# (RD#) falling edge to valid Data: read cycle	-	$4xT_{mclk}+16$	-	$4xT_{mclk}+23$	ns
t9	DB[15:0] hold time from CS# (RD#) rising edge: read cycle	2	12	2	14	ns
t10w	End of write to next read/write	5	-	5	-	ns
t10r	End of read to next read/write	$T_{mclk}+9$	-	$T_{mclk}+10$	-	ns
t11w	CS# (WR#) pulse width for write cycle	3	-	5	-	ns
t12w	CS# (WR#) rise to next CS# (WR#) rise: write cycle	$3xT_{mclk}+6$	-	$3xT_{mclk}+6$	-	ns

T_{mclk} = period of internal MCLK clock signal

Table 9-10: Indirect 16-bit Mode 1 Function Select

P/C#	WR#	RD#	Comments
0	0	1	Command Write (register address)
1	0	1	Data (Parameter) Write
0	1	0	inhibit
1	1	0	Data (Parameter) Read

9.4.4 Indirect 16-bit Mode 2 Timing

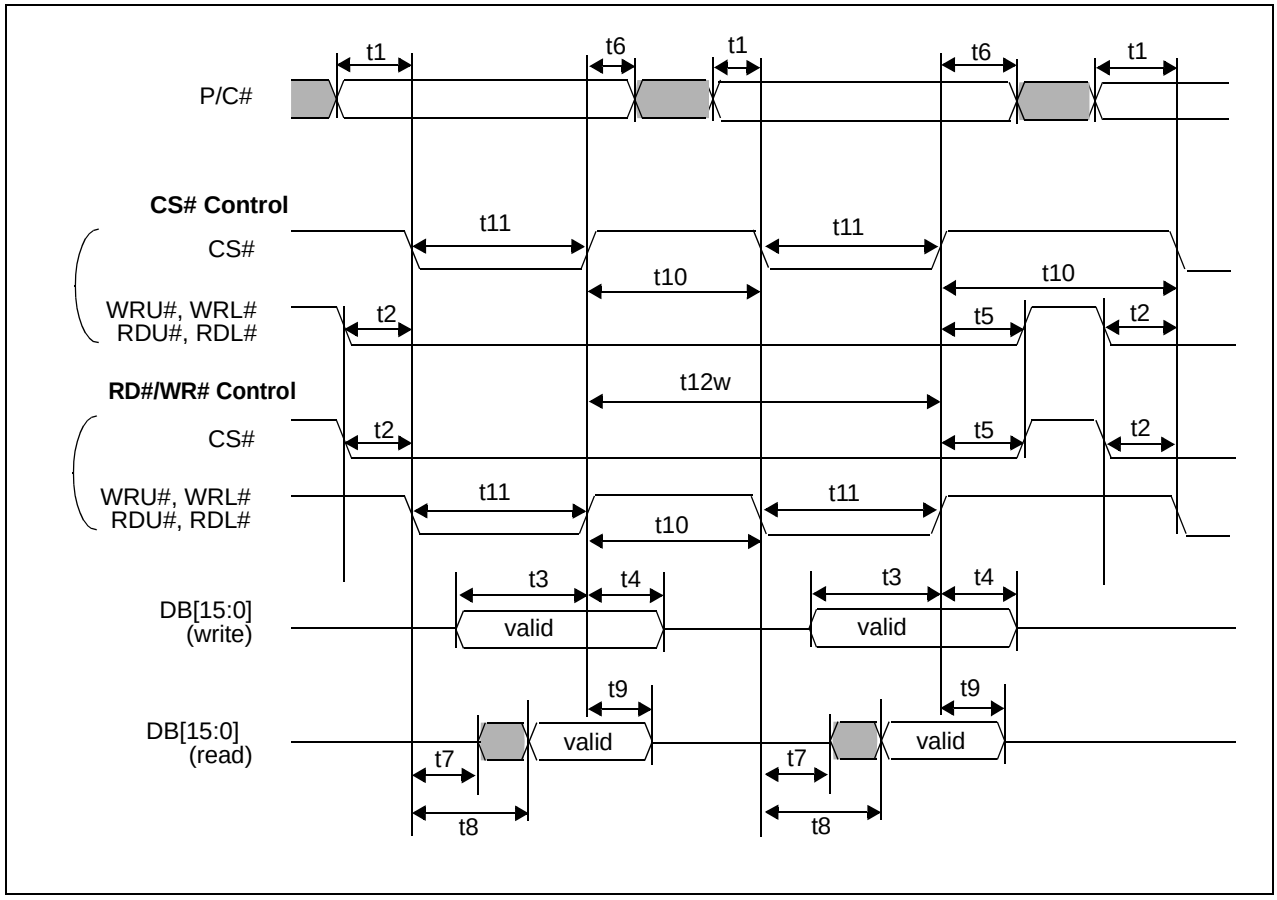


Figure 9-9: Indirect 16-bit Mode 2 Timing

Table 9-11: Indirect 16-bit Mode 2 Timing

Symbol	Parameter	3.3 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t1	P/C# setup time to CS# (WRU#, WRL#, RDU#, RDL#)	3	-	1	-	ns
t2	WRU#, WRL#, RDU#, RDL# (CS#) setup time to CS# (WRU#, WRL#, RDU#, RDL#)	2	-	2	-	ns
t3	DB[15:0] setup time to CS# (WRU#, WRL#) rising edge: write cycle	1	-	1	-	ns
t4	DB[15:0] hold time from CS# (WRU#, WRL#) rising edge: write cycle	7	-	8	-	ns
t5w	WRU#, WRL# (CS#) hold time from CS# (WRU#, WRL#) rising edge: write cycle	3	-	3	-	ns
t5r	RDU#, RDL# (CS#) hold time from CS# (RDU#, RDL#) rising edge: read cycle	0	-	0	-	ns
t6	P/C# hold time from CS# (WRU#, WRL#, RDU#, RDL#) rising edge	4	-	5	-	ns
t7	CS# (RDU#, RDL#) falling edge to DB[15:0] driven: read cycle	-	15	-	21	ns
t8	CS# (RDU#, RDL#) falling edge to valid Data: read cycle	-	$4xT_{mclk}+16$	-	$4xT_{mclk}+23$	ns
t9	DB[15:0] hold time from CS# (RDU#, RDL#) rising edge: read cycle	2	12	2	14	ns
t10w	End of write to next read/write	7	-	7	-	ns
t10r	End of read to next read/write	$T_{mclk}+9$	-	$T_{mclk}+10$	-	ns
t11w	CS# (WRU#, WRL#) pulse width for write cycle	3	-	5	-	ns
t12w	CS# (WRU#, WRL#) rise to next CS# (WRU#, WRL#) rise: write cycle	$3xT_{mclk}+6$	-	$3xT_{mclk}+6$	-	ns

T_{mclk} = period of internal MCLK clock signal

Table 9-12: Indirect 16-bit Mode 2 Function Select

P/C#	WRU#, WRL#	RDU#, RDL#	Comments
0	0	1	Command Write (register address)
1	0	1	Data (Parameter) Write
0	1	0	inhibit
1	1	0	Data (Parameter) Read

9.4.5 Direct 8-bit Timing

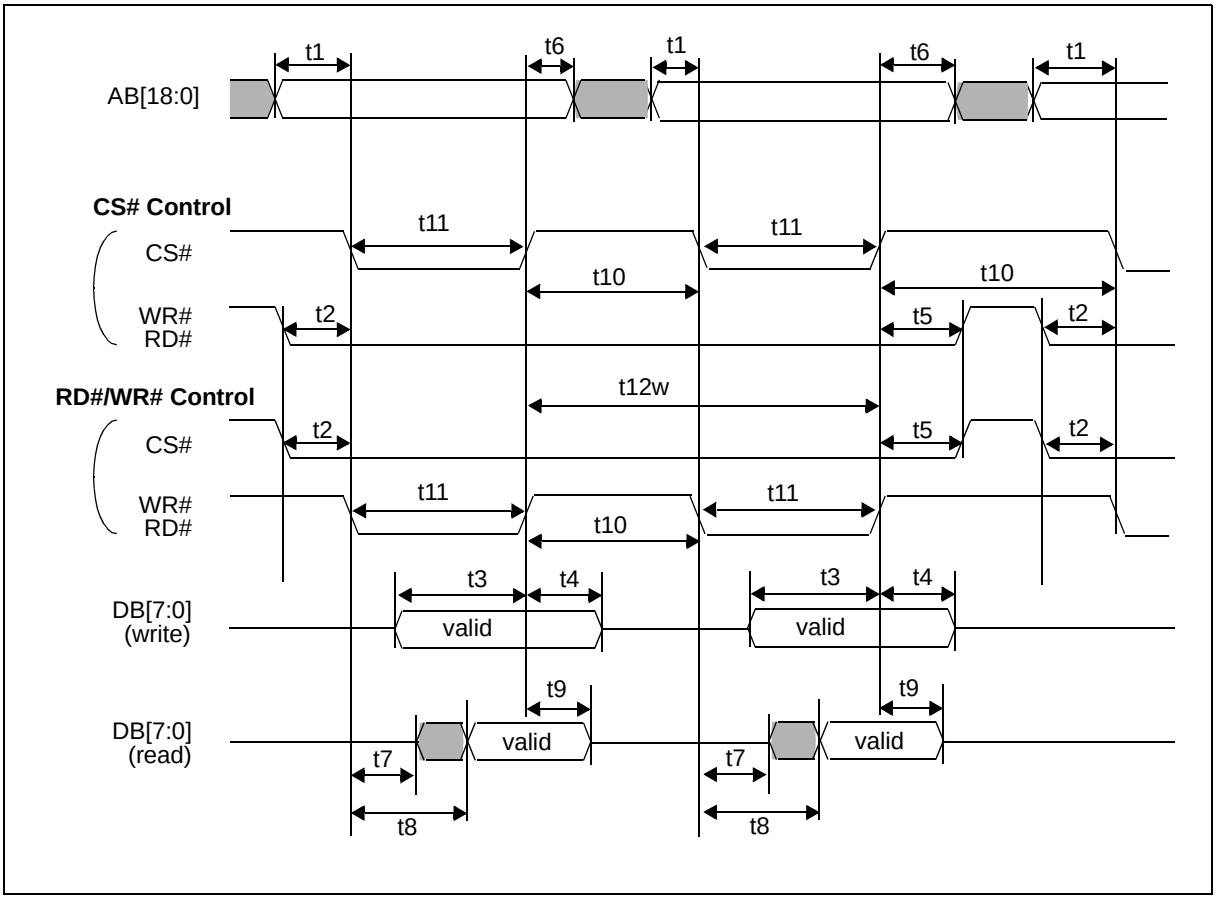


Figure 9-10: Direct 8-bit Timing

Table 9-13: Direct 8-bit Timing

Symbol	Parameter	3.3 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t1	AB[18:0] setup time to CS# (WR#, RD#)	2	-	1	-	ns
t2	WR#, RD# (CS#) setup time to CS# (WR#, RD#)	1	-	1	-	ns
t3	DB[7:0] setup time to CS# (WR#) rising edge: write cycle	1	-	1	-	ns
t4	DB[7:0] hold time from CS# (WR#) rising edge: write cycle	7	-	8	-	ns
t5w	WR# (CS#) hold time from CS# (WR#) rising edge: write cycle	3	-	3	-	ns
t5r	RD# (CS#) hold time from CS# (RD#) rising edge: read cycle	0	-	0	-	ns
t6	AB[18:0] hold time from CS# (WR#, RD#) rising edge	5	-	5	-	ns
t7	CS# (RD#) falling edge to DB[7:0] driven: read cycle	-	15	-	21	ns
t8	CS# (RD#) falling edge to valid Data: read cycle	-	$4xT_{mclk}+17$	-	$4xT_{mclk}+23$	ns
t9	DB[7:0] hold time from CS# (RD#) rising edge: read cycle	2	12	2	14	ns
t10w	End of write to next read/write	7	-	6	-	ns
t10r	End of read to next read/write	$T_{mclk}+9$	-	$T_{mclk}+10$	-	ns
t11w	CS# (WR#) pulse width for write cycle	3	-	5	-	ns
t12w	CS# (WR#) rise to next CS# (WR#) rise: write cycle	$3xT_{mclk}+6$	-	$3xT_{mclk}+6$	-	ns

T_{mclk} = period of internal MCLK clock signal

9.4.6 Indirect 8-bit Timing

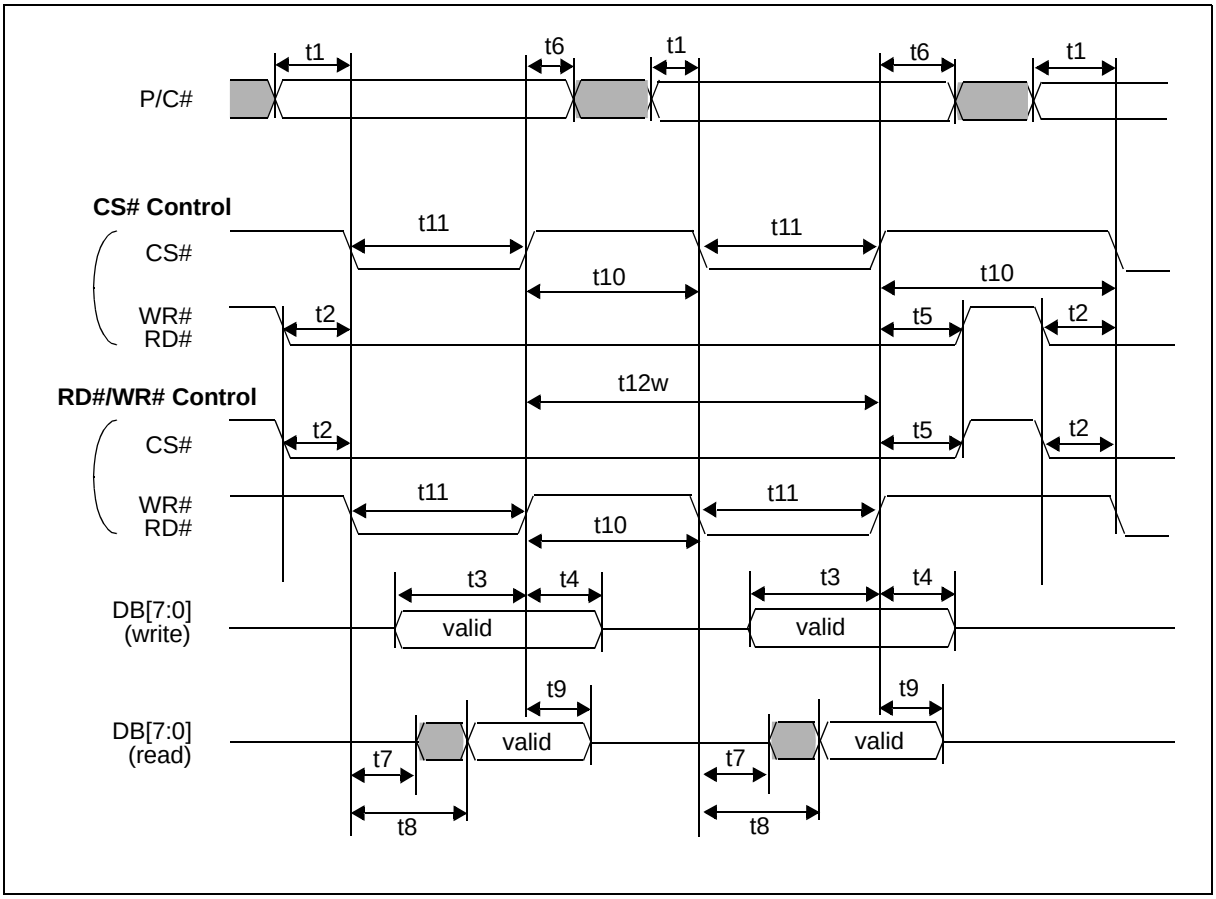


Figure 9-11: Indirect 8-bit Timing

Table 9-14: Indirect 8-bit Timing

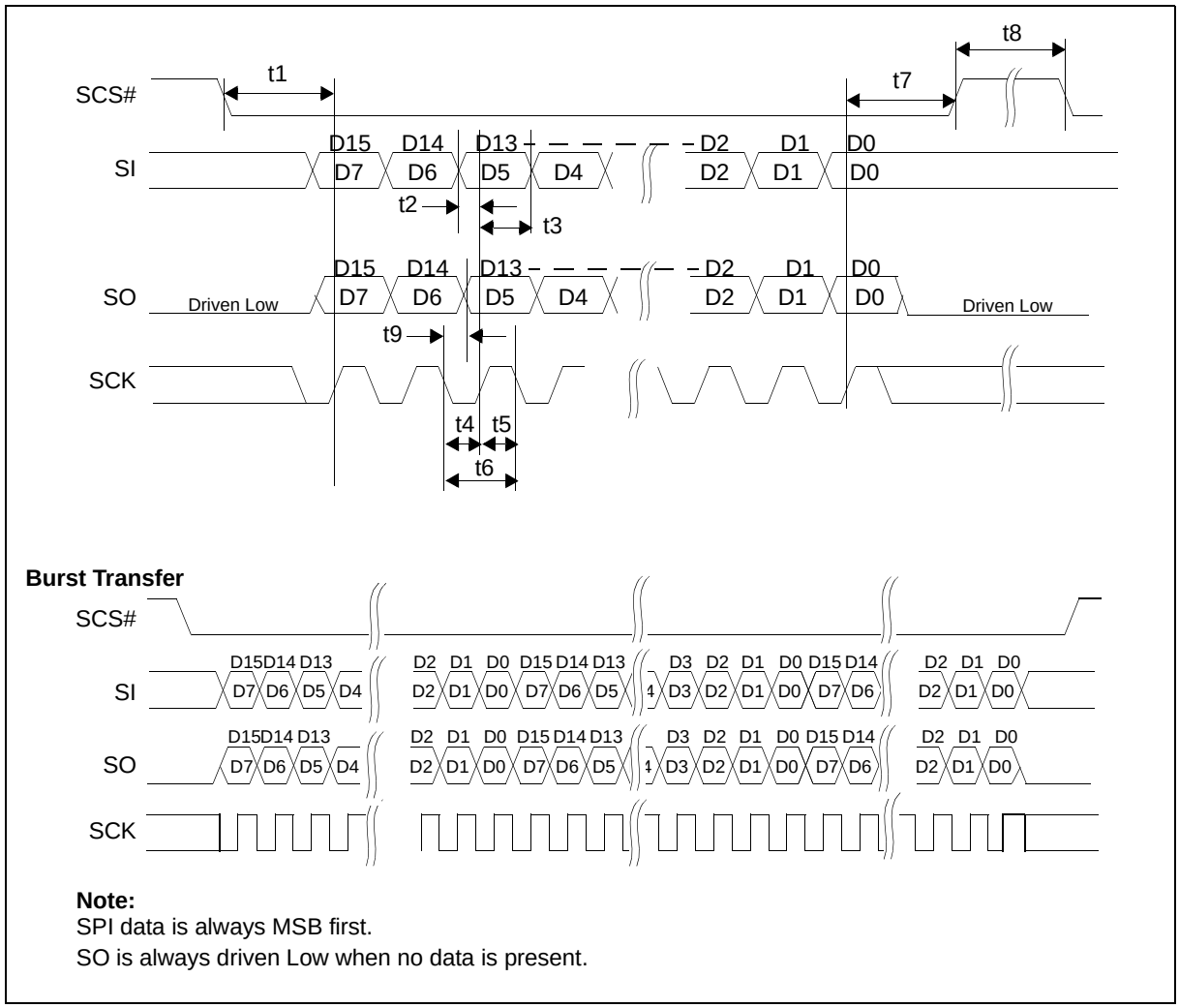
Symbol	Parameter	3.3 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t1	P/C# setup time to CS# (WR#, RD#)	1	-	1	-	ns
t2	WR#, RD# (CS#) setup time to CS# (WR#, RD#)	1	-	1	-	ns
t3	DB[7:0] setup time to CS# (WR#) rising edge: write cycle	1	-	1	-	ns
t4	DB[7:0] hold time from CS# (WR#) rising edge: write cycle	7	-	8	-	ns
t5w	WR# (CS#) hold time from CS# (WR#) rising edge: write cycle	3	-	3	-	ns
t5r	RD# (CS#) hold time from CS# (RD#) rising edge: read cycle	0	-	0	-	ns
t6	P/C# hold time from CS# (WR#, RD#) rising edge	4	-	4	-	ns
t7	CS# (RD#) falling edge to DB[7:0] driven: read cycle	-	15	-	21	ns
t8	CS# (RD#) falling edge to valid Data: read cycle	-	$4xT_{mclk}+17$	-	$4xT_{mclk}+23$	ns
t9	DB[7:0] hold time from CS# (RD#) rising edge: read cycle	2	12	2	14	ns
t10w	End of write to next read/write	5	-	5	-	ns
t10r	End of read to next read/write	$T_{mclk}+9$	-	$T_{mclk}+10$	-	ns
t11w	CS# (WR#) pulse width for write cycle	3	-	5	-	ns
t12w	CS# (WR#) rise to next CS# (WR#) rise: write cycle	$3xT_{mclk}+6$	-	$3xT_{mclk}+6$	-	ns

T_{mclk} = period of internal MCLK clock signal

Table 9-15: Indirect 8-bit Function Select

P/C#	WR#	RD#	Comments
0	0	1	Command Write (register address)
1	0	1	Data (Parameter) Write
0	1	0	inhibit
1	1	0	Data (Parameter) Read

9.4.7 SPI Timing



Note:
SPI data is always MSB first.
SO is always driven Low when no data is present.

Figure 9-12: SPI Timing

Table 9-16: SPI Timing

Symbol	Parameter	3.3 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t1	Chip select setup time	2	-	3	-	ns
t2	SI Data setup time	1	-	1	-	ns
t3	SI Data hold time	7	-	8	-	ns
t4	Serial clock pulse width low (high)	15	-	15	-	ns
t5	Serial clock pulse width high (low)	15	-	15	-	ns
t6	Serial clock period	30	-	30	-	ns
t7	Chip select hold time	7	-	8	-	ns
t8	Chip select de-assert to reassert	2	-	2	-	ns
t9	SCK falling edge to SO hold time	3	10	4	15	ns

NOTE: C_L = 10pF for SPI timing

Table 9-17: SPI Function Select

Command	Comments
10000000	8-bit Write
11000000	8-bit Read
10001000	16-bit Write
11001000	16-bit Read
the other	reserved

9.5 Panel Interface Timing

9.5.1 General TFT Panel Timing

The timing parameters required to drive a TFT display are shown below. Timing details for each supported panel type are provided in the following sections.

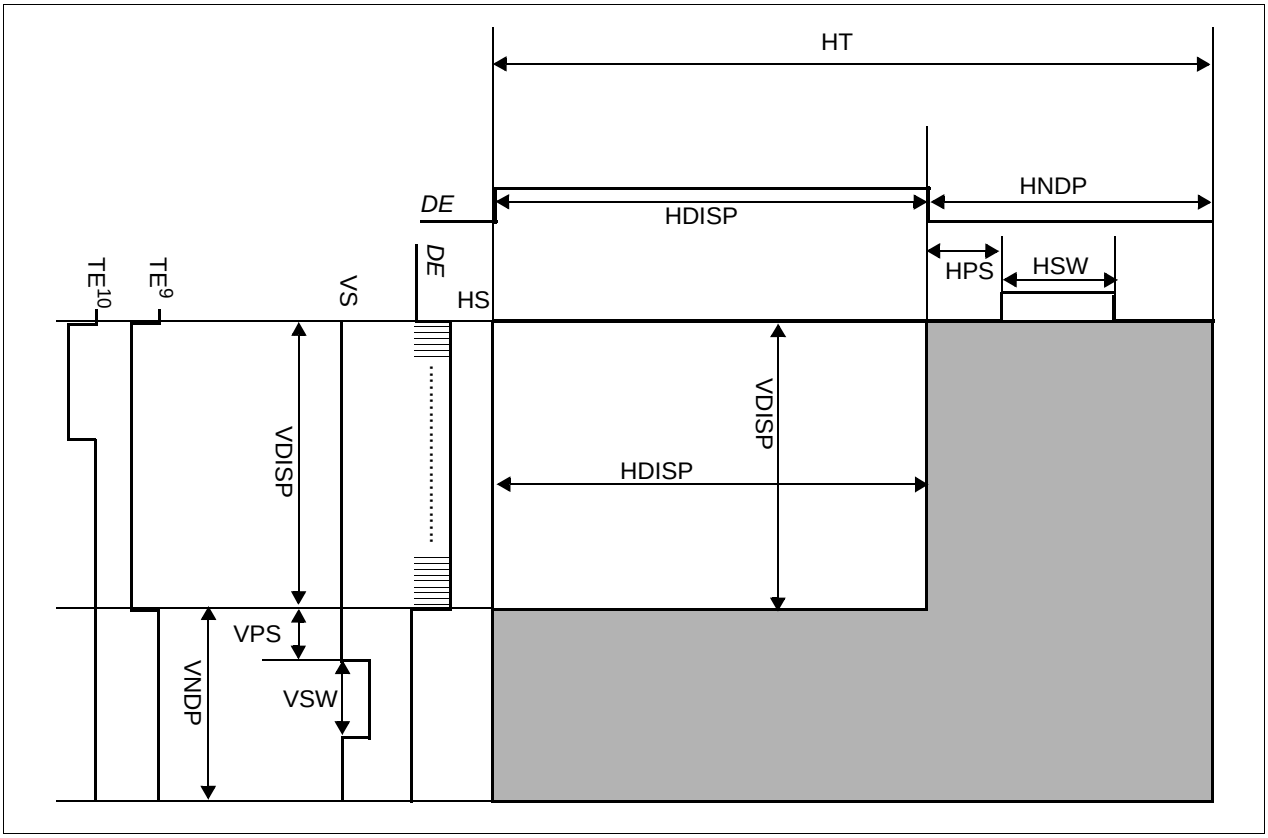


Figure 9-13: TFT Panel Timing Parameters

Table 9-18: TFT Panel Timing Parameter Definition and Register Summary

Symbol	Description	Derived From	Units
HDISP[8]	Horizontal Display Width	(REG[24h] bits 6-0) x 8	Ts
HNDP[3]	Horizontal Non-Display Period	REG[26h] bits 6-0	
HPS[2]	HS Pulse Start Position	REG[2Eh] bits 6-0	
HSW[2]	HS Pulse Width	REG[2Ch] bits 6-0	
VDISP[6,7]	Vertical Display Height	REG[28h] bits 9-0	Lines (HT)
VNDP[4,6]	Vertical Non-Display Period	REG[2Ah] bits 7-0	
VPS[5,7]	VS Pulse Start Position	REG[32h] bits 7-0	
VSW[5]	VS Pulse Width	REG[30h] bits 5-0	

1. T_S = pixel clock period.
2. (HPS + HSW) <= HNDP
3. HNDP > 0
4. VNDP > 0
5. (VPS + VSW) <= VNDP
6. VDISP + VNDP < 1024
7. VDISP + VPS < 1024
8. For TFT panels, HDISP must be set to a minimum of 8 pixels and must be increased by multiples of 8 pixels.
9. REG[22h] bits 6-5 = 01b
10. REG[22h] bits 6-5 = 10b

9.5.2 TFT 16/18/24-Bit Panel Timing

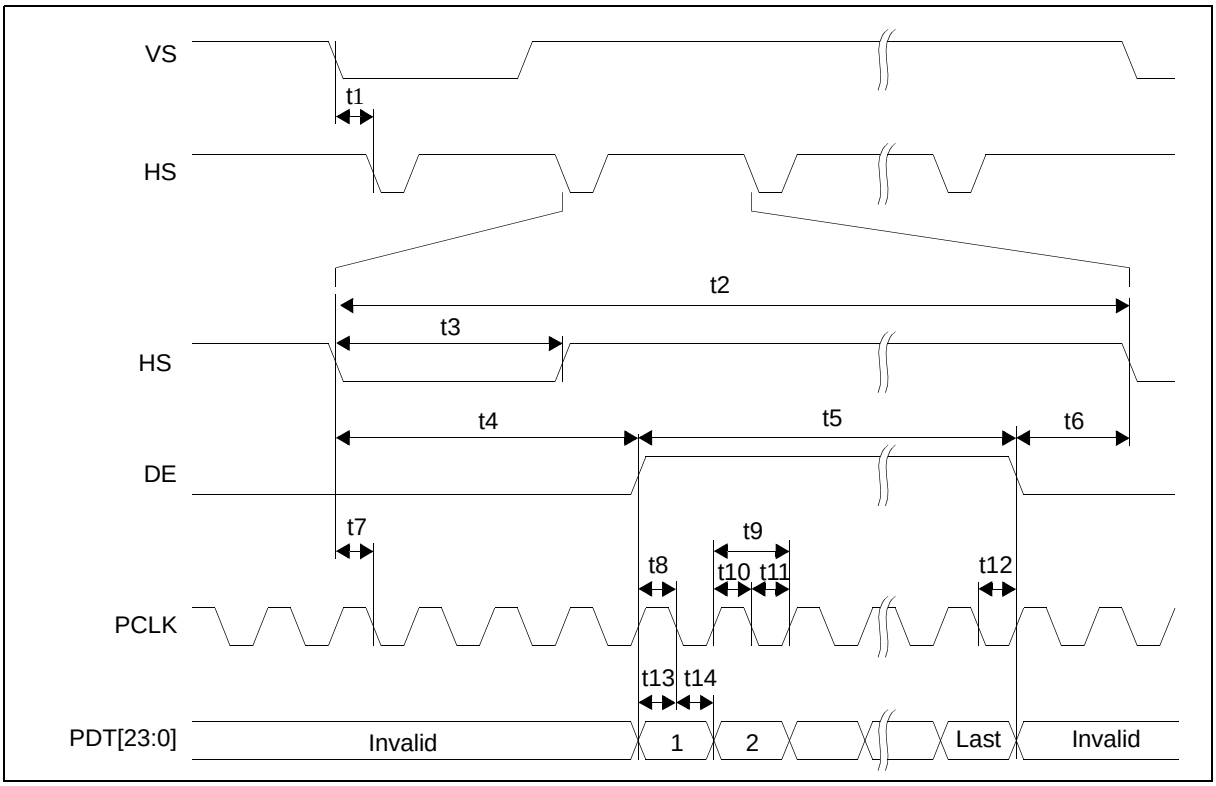


Figure 9-14: TFT 16/18/24-Bit Panel Horizontal Timing

Table 9-19: TFT 16/18/24-Bit Panel Horizontal Timing

Symbol	Parameter	Typ	Units
t1	VS falling edge to HS falling edge	HPS	Ts (Note 1)
t2	Horizontal total period	HDISP + HNDP	Ts
t3	HS pulse width	HPW	Ts
t4	HS falling edge to DE active	HNDP - HPS	Ts
t5	Horizontal display period	HDISP	Ts
t6	DE falling edge to HS falling edge	HPS	Ts
t7	HS setup time to PCLK falling edge (Note 2)	0.5	Ts
t8	DE setup to PCLK falling edge (Note 2)	0.5	Ts
t9	PCLK period	1	Ts
t10	PCLK pulse width high	0.5	Ts
t11	PCLK pulse width low	0.5	Ts
t12	DE hold from PCLK falling edge (Note 2)	0.5	Ts
t13	Data setup to PCLK falling edge (Note 2)	0.5	Ts
t14	Data hold from PCLK falling edge (Note 2)	0.5	Ts

1. Ts = pixel clock period
2. PCLK polarity (REG[20h] bit 5) = 0

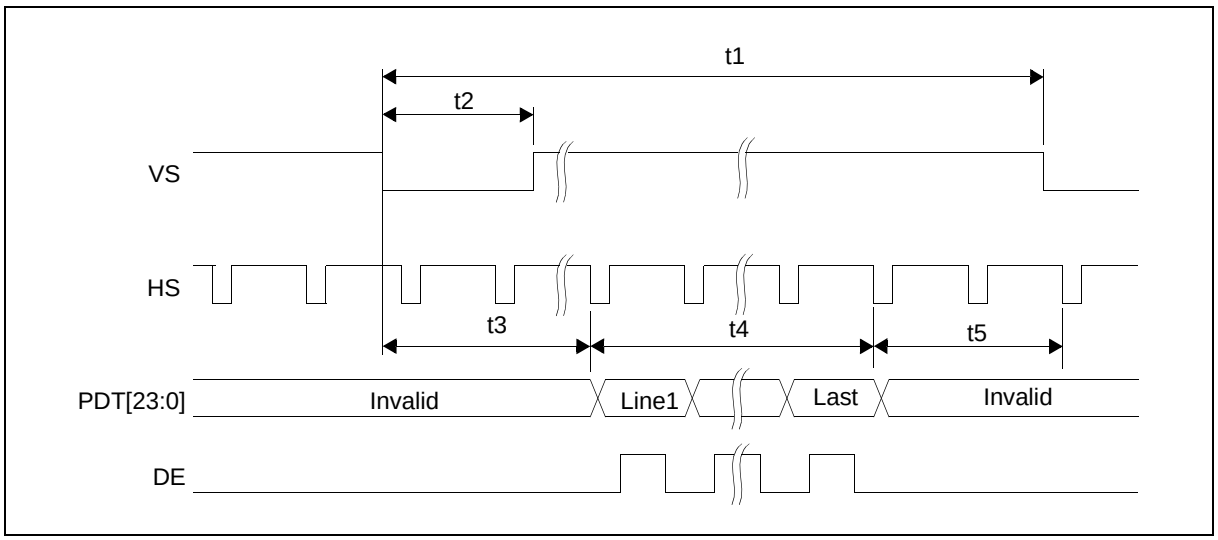


Figure 9-15: TFT 16/18/24-Bit Panel Vertical Timing

Table 9-20: TFT 16/18/24-Bit Panel Vertical Timing

Symbol	Parameter	Min	Typ	Units
t1	Vertical total period	—	VDISP + VNDP	Line
t2	VS pulse width	—	VSW	Line
t3	Vertical display start position	—	VNDP - VPS	Line
t4	Vertical display period	—	VDISP	Line
t5	Vertical Non Display Period after Display Area	VPS	VNDP	Line

Chapter 10 Registers

10.1 General

All registers except the Look-Up Table start at offset 608XXh (i.e. REG[04h] is located at 60804h) .
The Look-Up Table starts at offset 60XXX (i.e. LUT[000h] is located at 60000h). See Chapter 6, “Embedded Memory” on page 23 for details.

Note

1. For 8-bit addressing, all register accesses are Little Endian. The lower byte will be at memory address 60XXXh, and the upper byte will be at memory address 60XXXh + 1.
2. When the Host interface is indirect, the address is incremented automatically (burst write).
3. Although registers REG[20h] ~ REG[32h] are asynchronously read/writable in any power save mode (REG[04h] bits 1-0 = xxb), all register changes are synchronized with the VS signal and take effect in NMM mode when the panel interface is active (REG[04h] bits 1-0 = 1xb).
4. Do not access memory or LUT1/2 during PSM0.

Table 10-1: S1D13L01 Register Set

Register	Pg	Register	Pg
Configuration Registers			
REG[04h] Power Save Configuration Register	54	REG[06h] Software Reset Register	54
Clock Configuration Registers			
REG[10h] PLL Setting Register 0	55	REG[12h] PLL Setting Register 1	56
REG[14h] PLL Setting Register 2	57	REG[16h] Internal Clock Configuration Register	58
REG[18h] Reserved	58	REG[1Ah] Reserved	58
REG[1Ch] Reserved	59		
Panel Configuration Registers			
REG[20h] Panel Setting Miscellaneous Register	60	REG[22h] Display Settings Register	61
REG[24h] Horizontal Display Width Register (HDISP)	64	REG[26h] Horizontal Non-Display Period Register (HNDP)	64
REG[28h] Vertical Display Height Register (VDISP)	64	REG[2Ah] Vertical Non-Display Period Register (VNDP)	65
REG[2Ch] HS Pulse Width Register (HSW)	65	REG[2Eh] HS Pulse Start Position Register (HPS)	66
REG[30h] VS Pulse Width Register (VSW)	66	REG[32h] VS Pulse Start Position Register (VPS)	67
REG[34h] TE Line Count Register	67		
Layer Configuration Registers			
REG[40h] Main Layer Setting Register	68	REG[42h] Main Layer Start Address Register 0	69
REG[44h] Main Layer Start Address Register 1	69	REG[46h] Main Layer Width Register	70
REG[48h] Main Layer Height Register	70	REG[50h] PIP Layer Setting Register	70
REG[52h] PIP Layer Start Address Register 0	71	REG[54h] PIP Layer Start Address Register 1	71
REG[56h] PIP Layer Width Register	72	REG[58h] PIP Layer Height Register	72
REG[5Ah] PIP Layer X Start Position Register	72	REG[5Ch] PIP Layer Y Start Position Register	73
REG[60h] PIP Enable Register	74	REG[62h] Alpha Blending Register	76
REG[64h] Transparency Register	77	REG[66h] Transparency Key Color Register 0	78
REG[68h] Transparency Key Color Register 1	78		
GPIO Setting Registers			
REG[D0h] GPIO Configuration Register	79	REG[D2h] GPIO Status and Control Register	79
REG[D4h] GPIO Pull-Down Control Register	79		

Table 10-1: S1D13L01 Register Set

Register	Pg	Register	Pg
Look-Up Table Registers			
LUT[000h] Look-Up Table 1 Address 00h Register 0	80	LUT[002h] Look-Up Table 1 Address 00h Register 1	80
LUT[004h] Look-Up Table 1 Address 01h Register 0	81	LUT[006h] Look-Up Table 1 Address 01h Register 1	81
		• • •	
LUT[3F8h] Look-Up Table 1 Address FEh Register 0	82	LUT[3FAh] Look-Up Table 1 Address FEh Register 1	82
LUT[3FCh] Look-Up Table 1 Address FFh Register 0	82	LUT[3FEh] Look-Up Table 1 Address FFh Register 1	82
LUT[400h] Look-Up Table 2 Address 00h Register 0	83	LUT[402h] Look-Up Table 2 Address 00h Register 1	83
LUT[404h] Look-Up Table 2 Address 01h Register 0	83	LUT[406h] Look-Up Table 2 Address 01h Register 1	83
		• • •	
LUT[7F8h] Look-Up Table 2 Address FEh Register 0	84	LUT[7FAh] Look-Up Table 2 Address FEh Register 1	84
LUT[7FCh] Look-Up Table 2 Address FFh Register 0	85	LUT[7FEh] Look-Up Table 2 Address FFh Register 1	85

Where:

	Must be in PSM0 for writes (PSM0, PSM1 or NMM for reads)
	Must be in PSM1 or NMM for reads/writes
	No power save mode restrictions for reads/writes.

10.2 Configuration Registers

REG[04h] Power Save Configuration Register
Address 60804h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						Power Save bits 1-0	

bits 1-0 Power Save bits [1:0]
These bits select the power save mode of the S1D13L01. They control the clock-gating logic of the S1D13L01. The panel interface output and display pipes are enabled/disabled by REG[22h] bit 0, Panel Interface Enable.

Table 10-2: Power Save Selection

REG[04h] bits 1-0	Mode	Description
00b	**PSM0**	**read/write registers can NOT read/write memory (MCLK inactive) Panel I/F clock is inactive (PCLK inactive)**
01b	**PSM1**	**read/write registers read/write memory (MCLK active) Panel I/F clock is inactive (PCLK inactive)**
1xb	**NMM**	**read/write registers read/write memory (MCLK active) Panel I/F clock is active (PCLK active)**

Note
Do not access memory or LUT1/2 during PSM0.

REG[06h] Software Reset Register
Address 60806h Default = 0000h Write Only

15	14	13	12	11	10	9	8
n/a							Software Reset (WO)
7	6	5	4	3	2	1	0
n/a							

bit 8 Software Reset (Write Only)
When this bit is written 0b, there is no effect in hardware.
When this bit is written 1b, the internal sequencer, state machine and all registers are reset to default values.

10.3 Clock Configuration Registers

REG[10h] PLL Setting Register 0
Address 60810h Default = 0000h Read/Write

PLL Lock (RO)	n/a						
15	14	13	12	11	10	9	8
n/a						PLL Bypass	PLL Enable
7	6	5	4	3	2	1	0

Note
The S1D13L01 must be in Power Save Mode 0 (REG[04h] bits 1-0 = 00b) before changing this register.

bit 15 PLL Lock (Read Only)
This bit indicates whether the PLL output is stable.
When this bit = 0b, the PLL output is not stable. In this state the display buffer, LUT and registers must not be accessed.
When this bit = 1b, the PLL output is stable.

bit 1 PLL Bypass
When this bit = 0b (PLL is selected), the Power Save bits can only be changed when the PLL output is running (REG[10h] bit 0 = 1b) and it is stable (after 2.5 ms lock time, REG[10h] bit 15 = 1b).
When this bit = 1b (CLKI is selected), the Power Save bits (REG[04h] bits 1-0) can be programmed at any time.

bit 0 PLL Enable
When this bit = 0b, the PLL is disabled.
When this bit = 1b, the PLL enabled.

Note
If the S1D13L01 is configured to use the PLL output as the MCLK source and the Host wants to turn off the input clock (CLKI), the Host must disable the PLL (REG[10h] bit 0 = 0b) before shutting off CLKI. This procedure ensures that the PLL Lock bit (REG[10h] bit 15) goes low. Once CLKI has been turned back on, the Host should re-enable the PLL.

REG[12h] PLL Setting Register 1
Address 60812h Default = 0000h Read/Write

n/a		N-Counter bits 3-0				M-Divider bits 9-8	
15	14	13	12	11	10	9	8
M-Divider bits 7-0							
7	6	5	4	3	2	1	0

Note
The S1D13L01 must be in Power Save Mode 0 (REG[04h] bits 1-0 = 00b) and the PLL disabled (REG[10h] bit 0 = 0b) before changing this register.

bits 13-10 N-Counter bits [3:0]
These bits must be set to 0000b.

bits 9-0 M-Divider bits [9:0]
These bits determine the divide ratio between CLKI and the actual input clock to the PLL. These bits must be set such that the internal input clock to the PLL (PFDCLK) is between 1MHz and 2MHz. For further details, see Section 7.2, “PLL Setting” on page 25.

$$PFDCLK = CLKI \div (M\text{-}Divider + 1)$$
$$= CLKI \div MM$$

Table 10-3: PLL M-Divide Selection

REG[12h] bits 9-0	M-Divide Ratio
000h (default)	1:1
001h	2:1
002h	3:1
003h	4:1
• • •	• • •
020h	33:1
021h to 13Fh	Reserved

REG[14h] PLL Setting Register 2
Address 60814h Default = 0029h Read/Write

n/a						L-Counter bits 9-8	
15	14	13	12	11	10	9	8
L-Counter bits 7-0							
7	6	5	4	3	2	1	0

Note
The S1D13L01 must be in Power Save Mode 0 (REG[04h] bits 1-0 = 00b) and the PLL disabled (REG[10h] bit 0 = 0b) before changing this register.

bits 9-0 L-Counter bits [9:0]
These bits must be set between 010h ~ 041h. These bits are used to configure the PLL Output (POCLK) and must be set according to the following formula. For further details, see Section 7.2, “PLL Setting” on page 25.

$$\begin{aligned} POCLK &= (L\text{-}Counter + 1) \times (N\text{-}Counter + 1) \times PFDCLK \\ &= LL \times NN (= 1) \times CLKI \div MM \\ &= LL \times CLKI \div MM \end{aligned}$$

For example, CLKI input is 1MHz and target POCLK is 42MHz. Because PFDCLK is between 1MHz and 2MHz, MM (REG[12h] bits 9-0) is 000h. Because target POCLK = 42MHz and PFDCLK = 1MHz, LL (REG[14h] bits 9-0) is 29h.

Table 10-4: PLL L-Counter Selection

REG[14h] bits 9-0	L-Counter Ratio
000h to 00Fh	Reserved
010h	17:1
011h	18:1
012h	19:1
• • •	• • •
029h (default)	42:1
• • •	• • •
041h	66:1
042h to 13Fh	Reserved

REG[16h] Internal Clock Configuration Register
Address 60816h Default = 0005h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				PCLK Divide Select bits 3-0			

Note
The S1D13L01 must be in Power Save Mode 0 (REG[04h] bits 1-0 = 00b) before changing this register.

bits 3-0 PCLK Divide Select bits [3:0]
These bits determine the divide used to generate the Pixel Clock (PCLK) from the Memory Clock (MCLK).

Table 10-5: PCLK Divide Selection

REG[16h] bits 3-0	MCLK to PCLK Frequency Ratio
0000b	1:1
0001b	2:1
0010b	3:1
0011b	4:1
• • •	
1110b	15:1
1111b	16:1

REG[18h] Reserved
Address 60818h Default = 0408h Read/Write

15	14	13	12	11	10	9	8
Reserved bits 15-8							
15	14	13	12	11	10	9	8
Reserved bits 7-0							

bits 15-0 Reserved
The value of this register must be 0408h.

REG[1Ah] Reserved
Address 6081Ah Default = 0400h Read/Write

15	14	13	12	11	10	9	8
Reserved bits 15-8							
7	6	5	4	3	2	1	0
Reserved bits 7-0							

bits 15-0 Reserved
The value of this register must be 0400h.

REG[1Ch] Reserved

Address 6081Ch Default = 1000h Read/Write

Reserved bits 15-8							
15	14	13	12	11	10	9	8
Reserved bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Reserved

The value of this register must be 1000h.

10.4 Panel Configuration Registers

REG[20h] Panel Setting Miscellaneous Register
Address 60820h Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
DE Polarity bits 1-0		PCLK Polarity	n/a	Panel Data Enable	Panel Data Width bits 1-0		Panel Port Enable
7	6	5	4	3	2	1	0

Note
The S1D13L01 must be in Power Save Mode 0 or Power Save Mode 1 (REG[04h] bits 1-0 = 00b or 01b) before changing this register.

bits 7-6 DE Polarity bits [1:0]
These bits define status of DE.

Table 10-6: DE Polarity Selection

REG[20h] bits 7-6	DE Polarity
00b	Low active
01b	High active
10b	Fixed to Low
11b	Fixed to High

bit 5 PCLK Polarity
When this bit = 0b, the LCD data outputs transition on the rising edge of PCLK.
When this bit = 1b, the LCD data outputs transitions on the falling edge of PCLK.

bit 3 Panel Data Enable
This bit selects whether the LCD panel data is enabled.
When this bit = 0b, panel data is disable.
When this bit = 1b, panel data is enable.

This bit should be set to “1b” before setting Panel Interface Enable (REG[22h] bit0 = 1b).

bits 2-1 Panel Data Width bits [1:0]
These bits select the data width size of the LCD panel.

Table 10-7: Panel Selection

Panel Data Width (REG[20h] bits 2-1)	Panel
01b	TFT 16-bit
10b	TFT 18-bit
11b	TFT 24-bit

bit 0 Panel Port Enable

This bit selects whether the Panel port is enabled or not.
When this bit = 0b, TFT panel is disable.
When this bit = 1b, TFT panel is enable.

This bit should be set to “1b” before setting Panel Interface Enable (REG[22h] bit0 = 1b).

REG[22h] Display Settings Register

Address 60822h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							TE Output Pin Disable
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TE Status (RO)	TE Function bits 1-0		Display Blank	n/a	Display Blank Polarity	SW Video Invert	Panel Interface Enable

Note

This register takes effect on the next frame, synchronized with VS

bit 8 TE Output Pin Disable

This bit determines whether the status of TE is output to either the AB0 or DB8 pin based on the Host Interface configuration. This bit does not have any effect on the TE Status bit, REG[22h] bit 7. For a host interface pin mapping summary, see Section 4.4, “Host Interface Pin Mapping” on page 20.
When this bit = 0b, the status of TE is output on the configured pin.
When this bit = 1b, the status of TE is not output on the configured pin.

bit 7 TE Status (Read Only)

This bit indicates the status of TE which is configured by the TE Function bits (REG[22h] bits 6-5). This bit is not affected by the setting of the TE Output Pin Disable bit, REG[22h] bit 8.

When this bit = 0b, the selected condition in not occurring.

When this bit = 1b, the selected condition is occurring.

Note

When REG[22] bits 6-5 = 10b (Line Count)

- TE always stays High when REG[34h] = 0
- TE always stays Low when REG[34h] > (VDISP+VNDP-1)

bits 6-5 TE Function bits [1:0]

These bits determine the function of TE. The status of TE is indicated by the TE Status bit (see REG[22h] bit 7) and can be output on either the AB0 or DB8 pin based on the Host Interface configuration. The TE Output Pin Disable bit allows TE output to be disabled if not required. For a host interface pin mapping summary, see Section 4.4, “Host Interface Pin Mapping” on page 20.

Table 10-8: TE Function Selection

REG[22h] bits 6-5	TE Function Description
00b	**Disabled:** TE output is disabled and the pin output is low.
01b	**VNDP:** TE output is high (1) when the display is in the Vertical Non-Display Period (VNDP) and low (0) when the display is in Vertical Display Period (VDISP).
10b	**Line Count:** TE output is high (1) when the internal vertical line counter is greater than the value specified by the TE Line Count bits (REG[34h] bits 9-0), otherwise TE output is low (0). The internal vertical line counter counts from 0 to (VDISP+VNDP-1) then rolls back to 0.
11b	Reserved

bit 4 Display Blank

When this bit = 0b, the LCD data is masked.

When this bit = 1b, all applicable LCD data outputs (see Table 4-9: “Panel Interface Pin Mapping,” on page 21) are forced to zero or one. Table 10-9: “Display Control Summary” summarizes the changes to the signals on PDT[23:0] for each combination of bits.

bit 2 Display Blank Polarity

When this bit = 0b, the display blank function operates normally.

When this bit = 1b, the display blank function switches polarity. Table 10-9: “Display Control Summary,” on page 63 summarizes the changes to the signals on PDT[23:0] for each combination of bits.

bit 1 Software Video Invert

When this bit = 0b, video data is normal.

When this bit = 1b, video data is inverted. Table 10-9: “Display Control Summary,” on page 63 summarizes the changes to the signals on PDT[23:0] for each combination of bits.

Note

Video data is inverted after the Look-Up Table

bit 0 Panel Interface Enable

This bit enables/disables the panel interface output pins and the display pipes of the S1D13L01.

When this bit is 0b (default), PDT[23:0], HS, VS, DE and PCLK are fixed to H or L (see table below) and the display pipes are disabled.

Before setting this bit to 1b to enable the panel output and display pipes, make sure that the Power Save bits are in NMM mode (PCLK is running). The panel output pins and display pipes will be enabled on the next internal frame synchronization pulse.

When the panel output is disabled by setting this bit back to 0b, the display pipes and panel output pins will turn off on the next internal frame synchronization pulse.

When going into power savings mode, software must ensure that at least one frame period has elapsed between setting this bit to 0b and setting the Power Save bits (REG[04h] bits 1-0) to PSM1 mode. Otherwise, if PSM1 mode is entered (PCLK is turned off) too early (before next frame synchronization pulse which is clocked by PCLK), the display pipes and panel output pins will not be turned off.

Table 10-9: Display Control Summary

Display Blank (REG[22h] bit 4)	Display Blank Polarity (REG[22h] bit 2)	Software Video Invert (REG[22h] bit 1)	Panel I/F Enable (REG[22h] bit 0)	Output Data PDT[23:0]	HS, VS, DE, PCLK
0b	xb	0b	1b	Normal	Normal
		1b	1b	Inverted	Normal
1b	0b	0b	1b	All 0	Normal
		1b	1b	All 1	Normal
	1b	0b	1b	All 1	Normal
		1b	1b	All 0	Normal
xb	xb	0b	0b	All 0	All 0
		1b	0b	All 1	All 1

REG[24h] Horizontal Display Width Register (HDISP)

Address 60824h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a	Horizontal Display Width bits 6-0						

bits 6-0 Horizontal Display Width bits [6:0]

These bits specify the LCD panel Horizontal Display Width (HDISP), in 8 pixel resolution.

REG[24h] bits 6-0 = horizontal display width in pixels ÷ 8

Note

For TFT panels, HDISP must be set to a minimum of 8 pixels (bits 6-0 = 01h) and must be increased by multiples of 8 pixels.

REG[26h] Horizontal Non-Display Period Register (HNDP)

Address 60826h Default = 0003h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a	Horizontal Non-Display Period bits 6-0						

bits 6-0 Horizontal Non-Display Period bits [6:0]

These bits specify the LCD panel Horizontal Non-Display Period (HNDP), in pixels.

REG[26h] bits 6-0 = horizontal non-display period in PCLK’s

Note

The minimum Horizontal Non-Display Period is 3 pixels (REG[26h] bits 6-0 = 03h).

HS Start + HS Width <= HNDP

REG[28h] Vertical Display Height Register (VDISP)

Address 60828h Default = 0001h Read/Write

15	14	13	12	11	10	9	8
n/a						Vertical Display Height bits 9-8	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Vertical Display Height bits 7-0							

bits 9-0 Vertical Display Height bits [9:0]

These bits specify the LCD panel Vertical Display Height (VDISP), in lines.

REG[28h] bits 9-0 = vertical display height in lines

Note

1. Minimum value = 1 line
2. This register must be set such that the following formulae are valid:

   VDISP + VNDP < 1024

   VDISP + VPS < 1024

REG[2Ah] Vertical Non-Display Period Register (VNDP)

Address 6082Ah Default = 0002h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Vertical Non-Display Period bits 7-0							

bits 7-0 Vertical Non-Display Period bits [7:0]

These bits specify the LCD panel Vertical Non-Display Period (VNDP), in lines.

REG[2Ah] bits 7-0 = vertical non-display period in lines

Note

1. Minimum value = 2 lines
2. This register must be set such that the following formula is valid:

   VDISP + VNDP < 1024

REG[2Ch] HS Pulse Width Register (HSW)

Address 6082Ch Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
HS Pulse Polarity	HS Pulse Width bits 6-0						

bit 7 HS Pulse Polarity

This bit selects the polarity of the horizontal sync signal. This bit is set according to the horizontal sync signal of the panel.

When this bit = 0b, the horizontal sync signal is active low.

When this bit = 1b, the horizontal sync signal is active high.

bits 6-0 HS Pulse Width bits [6:0]

These bits specify the width of the panel horizontal sync signal (HSW), in pixels. The horizontal sync signal is typically HS, depending on the panel type. The minimum value for these bits is 1b.

REG[2Ch] bits 6-0 = HS pulse width in PCLK's

These bits must be set as follows:

For TFT panels

HS Pulse Start + HS Pulse Width ≤ HNDP

REG[2Eh] HS Pulse Start Position Register (HPS)

Address 6082Eh Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a	HS Pulse Start Position bits 6-0						
7	6	5	4	3	2	1	0

bits 6-0 HS Pulse Start Position bits [6:0]

These bits specify the start position of the horizontal sync signal (HPS) with respect to the start of the Horizontal Non-Display Period, in pixels.

REG[2Eh] bits 6-0 = HS pulse start position in PCLK's

These bits must be set as follows:

For TFT panels

HS Pulse Start + HS Pulse Width ≤ HNDP

REG[30h] VS Pulse Width Register (VSW)

Address 60830h Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
VS Pulse Polarity	n/a	VS Pulse Width bits 5-0					
7	6	5	4	3	2	1	0

bit 7 VS Pulse Polarity

This bit selects the polarity of the vertical sync signal. This bit is set according to the vertical sync signal of the panel.

When this bit = 0b, the vertical sync signal is active low.

When this bit = 1b, the vertical sync signal is active high.

bits 5-0 VS Pulse Width bits [5:0]

These bits specify the width of the panel vertical sync signal (VSW), in lines. The vertical sync signal is typically VS, depending on the panel type.

REG[30h] bits 5-0 = VS pulse width in lines

REG[32h] VS Pulse Start Position Register (VPS)

Address 60832h Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
VS Pulse Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 VS Pulse Start Position bits [7:0]

These bits specify the start position of the vertical sync signal (VPS) with respect to the start of Vertical Non-Display Period, in lines.

For TFT panels: REG[32h] bits 7-0 = VS pulse start position in lines

REG[34h] TE Line Count Register

Address 60834h Default = 0000h Read/Write

n/a						TE Line Count bits 9-8	
15	14	13	12	11	10	9	8
TE Line Count bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 TE Line Count bits [9:0]

When the TE Function is configured for Line Count (REG[22h] bits 6-5 = 10b), these bits specify the line count value that is compared with the internal vertical line counter to determine whether TE output is high (1) or low (0). The internal line counter counts from 0 to (VDISP+VNDP-1).

10.5 Layer Configuration Registers

REG[40h] Main Layer Setting Register
Address 60840h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							Multi-Byte Layer Registers Synchronous Latching Disable

7	6	5	4	3	2	1	0
n/a			Main Layer Rotation Select bits 1-0		Main Layer Color Depth bits 2-0		

Note
This register takes effect on the next frame, synchronized with VS.

bit 8 Multi-Byte Layer Registers Synchronous Latching Disable

The asynchronous multi-byte layer registers can be written and read any time independent of the value of this bit. Synchronous copies of the multi-byte layer registers are internally kept for use by the display engine. The display engine latches the values of the synchronous copies on every frame sync.

When this bit = 0b, Synchronous latching of multi-byte layer registers is performed on writes to any register. Any writes to registers will cause the asynchronous multi-byte layer register values to be latched into the internal synchronous copies.
When this bit = 1b, Synchronous latching of multi-byte layer registers is disabled. Synchronous latching will occur when REG[40h] bit 8 is written back to 0b.

Multi-byte layer registers consist of the following:

Main Start Address [18:0] (REG[42h] ~ REG[44h])
PIP Start Address [18:0] (REG[52h] ~ REG[54h])
PIP Width [9:0] (REG[56h] ~ REG[57h])
PIP Height [9:0] (REG[58h] ~ REG[59h])
PIP Start X [9:0] (REG[5Ah] ~ REG[5Bh])
PIP Start Y [9:0] (REG[5Ch] ~ REG[5Dh])

bits 4-3 Main Layer Rotation Select bits [1:0]

These bits specify the rotation orientation for the Main Layer (counterclockwise).

Table 10-10: Main Layer Rotation Selection

REG[40h] bits 4-3	Main Layer Rotation
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

bits 2-0 Main Layer Color Depth bits [2:0]

These bits specify the color depth for the Main layer.

Table 10-11: Main Layer Color Depth Selection

REG[40h] bits 2-0	Main Layer Color Depth
000b	RGB 8:8:8 (default)
001b	RGB 5:6:5
010b	Reserved
011b	Reserved
100b	24 bpp + LUT1
101b	16 bpp + LUT1
110b	8 bpp + LUT1
111b	Reserved

REG[42h] Main Layer Start Address Register 0

Address 60842h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Main Layer Start Address bits 15-8							
7	6	5	4	3	2	1	0
Main Layer Start Address bits 7-0							

REG[44h] Main Layer Start Address Register 1

Address 60844h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a					Main Layer Start Address bits 18-16		

Note

These registers take effect on the next frame, synchronized with VS.

REG[44h] bits 2-0
REG[42h] bits 15-0 Main Layer Start Address bits [18:0]

Main Layer Start Address bits in embedded RAM. The Start Address bits must be 32-bit aligned, so the Main Layer Start Address bits 1-0 must be set to 00b.

REG[46h] Main Layer Width Register
Address 60846h Default = 0000h Read Only

15	14	13	12	11	10	9	8
n/a						Main Layer Width bits 9-8	
7	6	5	4	3	2	1	0
Main Layer Width bits 7-0							

bits 9-0 Main Layer Width bits [9:0] (Read Only)
These bits indicate the width of the Main Layer, in pixels. When Main Layer rotation is set for 0° or 180° (REG[40h] bits 4-3 = 00b or 10b), these bits are based on the value in the REG[24h]. When Main Layer rotation is set for 90° or 270° (REG[40h] bits 4-3 = 01b or 11b), these bits are based on the value in the REG[28h].

Note
When REG[24h] or REG[28h] are updated, there is up to a two frame delay before the value in this register is updated.

REG[48h] Main Layer Height Register
Address 60848h Default = 0001h Read Only

15	14	13	12	11	10	9	8
n/a						Main Layer Height bits 9-8	
7	6	5	4	3	2	1	0
Main Layer Height bits 7-0							

bits 9-0 Main Layer Height bits [9:0] (Read Only)
These bits indicate the height of the Main Layer, in lines. When Main Layer rotation is set for 0° or 180° (REG[40h] bits 4-3 = 00b or 10b), these bits are based on the value in the REG[28h]. When Main Layer rotation is set for 90° or 270° (REG[40h] bits 4-3 = 01b or 11b), these bits are based on the value in the REG[24h].

Note
When REG[24h] or REG[28h] are updated, there is up to a two frame delay before the value in this register is updated.

REG[50h] PIP Layer Setting Register
Address 60850h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a			PIP Layer Rotation Select bits 1-0		PIP Layer Color Depth bits 2-0		

Note
This register takes effect on the next frame, synchronized with VS.

bits 4-3 PIP Layer Rotation Select bits [1:0]
These bits specify the rotation orientation for the PIP layer (counterclockwise).

Table 10-12: PIP Layer Rotation Selection

REG[50h] bits 4-3	PIP Layer Rotation
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

bits 2-0 PIP Layer Color Depth bits [2:0]
These bits specify the color depth for the PIP Layer.

Table 10-13: PIP Layer Color Depth Selection

REG[50h] bits 2-0	PIP Layer Color Depth
000b	RGB 8:8:8 (default)
001b	RGB 5:6:5
010b	Reserved
011b	Reserved
100b	24 bpp + LUT2
101b	16 bpp + LUT2
110b	8 bpp + LUT2
111b	Reserved

REG[52h] PIP Layer Start Address Register 0
Address 60852h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
PIP Layer Start Address bits 15-8							
7	6	5	4	3	2	1	0
PIP Layer Start Address bits 7-0							

REG[54h] PIP Layer Start Address Register 1
Address 60854h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a					PIP Layer Start Address bits 18-16		

Note
These registers take effect on the next frame, synchronized with VS.

REG[54h] bits 2-0
REG[52h] bits 15-0 PIP Layer Start Address bits [18:0]
PIP Layer Start Address bits in embedded RAM. The Start Address bits must be 32-bit aligned, so the PIP Layer Start Address bits 1-0 must be set to 00b.

REG[56h] PIP Layer Width Register
Address 60856h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP Layer Width bits 9-8	
PIP Layer Width bits 7-0							
7	6	5	4	3	2	1	0

Note
This register takes effect on the next frame, synchronized with VS.

bits 9-0 PIP Layer Width bits [9:0]
These bits specify the width of the PIP Layer, in pixels.

REG[56h] bits 9-0 = PIP Layer Horizontal Display Period in number of pixels

REG[58h] PIP Layer Height Register
Address 60858h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP Layer Height bits 9-8	
PIP Layer Height bits 7-0							
7	6	5	4	3	2	1	0

Note
This register takes effect on the next frame, synchronized with VS.

bits 9-0 PIP Layer Height bits [9:0]
These bits specify the height of the PIP Layer, in lines.

REG[58h] bits 9-0 = PIP Layer Vertical Display Period in number of lines

REG[5Ah] PIP Layer X Start Position Register
Address 6085Ah Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP Layer X Start Position bits 9-8	
PIP Layer X Start Position bits 7-0							
7	6	5	4	3	2	1	0

Note
This register takes effect on the next frame, synchronized with VS.

bits 9-0 PIP Layer X Start Position bits [9:0]
These bits specify X start position of the PIP Layer on the panel, in pixels. See Section 14.5.1, “Location Address” on page 113 for details.

REG[5Ch] PIP Layer Y Start Position Register

Address 6085Ch Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						PIP Layer Y Start Position bits 9-8	
PIP Layer Y Start Position bits 7-0							
7	6	5	4	3	2	1	0

Note

This register takes effect on the next frame, synchronized with VS.

bits 9-0 PIP Layer Y Start Position bits [9:0]

These bits specify Y start position of the PIP Layer on the panel, in lines. See Section 14.5.1, “Location Address” on page 113 for details.

REG[60h] PIP Enable Register

Address 60860h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Blink/Fade Period bits 6-0							n/a
7	6	5	4	3	2	1	0
n/a				Blink/Fade Status (RO)	Blink/Fade Effect bits 2-0		

Note

This register takes effect on the next frame, synchronized with VS.

bits 15-9 Blink/Fade Period bits [6:0]

These bits define the PIP Layer blink/fade period, in 1 frame units.

REG[60h] bits 15-9 = blink/fade period in frames - 1

For PIP Effects Blink1 and Blink2, the blinking period is specified by these bits.
For PIP Effects Fade Out, Fade In, and Fade In/Out Continuous, the period between each alpha blend value increment/decrement (see REG[62h] bits 9-8) is specified by these bits.

bit 3 Blink/Fade Status (Read Only)

When this bit = 0b, the PIP layer is not blinking or fading.
When this bit = 1b, the PIP layer is in the process of blinking or fading.

This bit is normally used for the one-time Fade Out and Fade In PIP Effects to check when the fade-out or fade-in has finished. It is also used when transitioning from the Blink1, Blink2, and Fade In/Out Continuous effects to the Normal or Blank effects to check when the blinking or fading has finished.

bits 2-0 PIP Effect bits [2:0]

These bits select the effect applied to the PIP Layer. For further details, see Section 14.4, “PIP Effects” on page 108.

Table 10-14: PIP Effect Selection

REG[60h] bits 2-0	PIP Effect
000b	Blank
001b	Normal
010b	Blink 1
011b	Blink 2
100b	Fade Out
101b	Fade In
110b	Fade In/Out Continuous
111b	Reserved

Blank

Default setting. When this type is set, the PIP Layer disappears (turned off).

Normal

When this type is set, the PIP Layer is displayed (turned on). When the Alpha Blending ratio (REG[62h] bits 6-0) is changed while in this mode, the change to the PIP occurs on the next frame.

Blink 1
PIP Layer blinks, toggling between the current Alpha Blending ratio setting (“ON”) and alpha blending value = 0000000b (“OFF”). The period for switching between “ON” and “OFF” is specified by REG[60h] bits 15-9 Blink/Fade Period bits. The Blink1 setting should only be entered from Normal or Blank setting. To exit Blink1 state, the PIP Effect bits should be programmed to Normal or Blank.

Blink 2
PIP Layer pixel data will toggle between normal and invert. Alpha Blending ratio is effective even if PIP Layer image data is inverted. The period for switching between normal and invert is specified by REG[60h] PIP Enable Register bits 15-9 Blink/Fade Period bits. The Blink2 setting should only be entered from Normal or Blank setting. To exit Blink2 state, the PIP Effect bits should be programmed to Normal or Blank.

Fade Out
PIP Layer one-time fade-out. When this PIP Effect is selected, the alpha blending value for the PIP Layer starts counting down from the Alpha Blending Ratio setting to the minimum alpha blending value (0000000b). The time period between each decrement of the alpha blending value is specified by REG[60h] PIP Enable Register bits 15-9 Blink/Fade Period bits, and the decrement step is specified by REG[62h] Alpha Blending Register bits 9-8 Alpha Blending Step bits. During fade-out, the period and step can be changed dynamically to speed up or slow down the fade-out. To initiate another fade-out, the PIP Effect should be programmed to either Blank or Normal first and then back to Fade Out. After fade-out is finished, the PIP Effect can also be programmed to Fade In to initiate a fade-in.

Fade In
PIP Layer one-time fade-in. When this PIP Effect is selected, the alpha blending value for the PIP Layer starts counting up from the minimum alpha blending value (0000000b) to the Alpha Blending Ratio value. The time period between each increment of the alpha blending value is specified by REG[60h] PIP Enable Register bits 15-9 Blink/Fade Period bits, and the increment step is specified by REG[62h] Alpha Blending Register bits 9-8 Alpha Blending Step bits. During fade-in, the period and step can be changed dynamically to speed up or slow down the fade-out. The target Alpha Blending Ratio value can also be changed during fade-in to speed up or delay the fade-in. To initiate another fade-in, the PIP Effect should be programmed to either Blank or Normal first and then back to Fade In. After fade-in is finished, the PIP Effect can also be programmed to Fade Out to initiate a fade-out.

Fade In/Out Continuous
PIP Layer continuously repeats fade in and out. The Fade In/Out Continuous setting should only be entered from Normal or Blank setting. If the PIP Effect transitions from Blank to Fade In/Out Continuous, the PIP Layer will start with fade-in. If the PIP Effects transitions from Normal to Fade In/Out Continuous, the PIP Layer will start with fade-out. The time period between each increment/decrement of the alpha blending value is specified by REG[60h] PIP Enable Register bits 15-9 Blink/Fade Period bits, and the increment/decrement step is specified by REG[62h] Alpha Blending Register bits 9-8 Alpha Blending Step bits. The target alpha blend value during fade-in is specified by REG[62h] Alpha Blending Register bits 6-0 Alpha Blending Ratio bits. The period, step, and target alpha blend value can be changed dynamically to speed up or slow down and fades. To exit Fade In/Out Continuous state, the PIP Effect bits should be programmed to Normal or Blank.

REG[62h] Alpha Blending Register
Address 60862h Default = 0040h Read/Write

n/a						Alpha Blending Step bits 1-0	
15	14	13	12	11	10	9	8
n/a	Alpha Blending Ratio bits 6-0						
7	6	5	4	3	2	1	0

Note
This register takes effect on the next frame, synchronized with VS.

bits 9-8 Alpha Blending Step bits [1:0]
These bits specify the increment/decrement steps for the PIP Layer alpha blend value during fade-in or fade-out effects.

Table 10-15: Alpha Blending Step Selection

REG[62h] bits 9-8	Alpha Blending Step
00b	1
01b	2
10b	4
11b	8

Note
If the Alpha Blending Ratio is not set to “Full PIP” (REG[62h] bits 6-0 = 40h), these bits should be set such that the “step” value is evenly divisible into the Alpha Blending Ratio.

bits 6-0 Alpha Blending Ratio bits [6:0]
These bits define the alpha blending ratio. When these bits are set to a value other than 0000000b, the PIP Layer is enabled. For further information on alpha blending, see Section 14.3, “Alpha Blending” on page 107.

Table 10-16: Alpha Blending Ratio Selection

REG[62h] bits 6-0	Main Layer : PIP Layer
0000000b	64:0 (no PIP)
0000001b	63:1
0000010b	62:2
...	...
0111101b	3:61
0111110b	2:62
0111111b	1:63
1000000b	0:64 (full PIP)
1000001b ~ 1111111b	Reserved

Note
When PIP Layer Transparency is enabled (REG[64h] bit 0 = 1b), the alpha blending ratio has no effect on the Transparency Key Colors (see REG[66h] ~ REG[68h]).

REG[64h] Transparency Register

Address 60864h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							Transparency Enable

Note

This register takes effect on the next frame, synchronized with VS.

bit 0 Transparency Enable

This bit enables/disables the transparency function. For more information on transparency, see Section 14.2, “Transparency” on page 106.

When this bit = 0b, transparency is disabled.

When this bit = 1b, transparency is enabled.

REG[66h] Transparency Key Color Register 0
Address 60866h Default = 0000h Read/Write

Key Color Green bits 7-0							
15	14	13	12	11	10	9	8
Key Color Blue bits 7-0							
7	6	5	4	3	2	1	0

REG[68h] Transparency Key Color Register 1
Address 60868h Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Key Color Red bits 7-0							
7	6	5	4	3	2	1	0

Note
These registers take effect on the next frame, synchronized with VS.

REG[66h] bits 15-8 Key Color Green bits [7:0]
REG[66h] bits 7-0 Key Color Blue bits [7:0]
REG[68h] bits 7-0 Key Color Red bits [7:0]
When Transparency is enabled (REG[64h] Transparency Register bit 0 = 1b), these bits define the Key Color. The key color is compared with the PIP pixel color to determine whether the pixel will become transparent. The key color is not affected by the PIP Effect (see REG[60h]) or Alpha Blending (see REG[62h]). For further information on Transparency, see chapter 14.2, “Transparency” on page 106.

Table 10-17: Key Color Register Use

Mode	Panel Data Enable (REG[20h] bit 3)	PIP Color Depth (REG[50h] bits 2-0)	Key Color Register Use			Comments
			Red	Green	Blue	
RGB 8:8:8	1b	000b	REG[68h] bits 7-0	REG[66h] bits 15-8	REG[66h] bits 7-0	—
RGB 5:6:5	1b	001b	REG[68h] bits 7-3	REG[66h] bits 15-10	REG[66h] bits 7-3	—
24 bpp + LUT2	1b	100b	REG[68h] bits 7-0	REG[66h] bits 15-8	REG[66h] bits 7-0	For these modes, the Key Color register values are compared to the contents of the LUT. The LUT index is determined by the pixel value stored in display memory.
16 bpp + LUT2	1b	101b				
8 bpp + LUT2	1b	110b				

10.6 GPIO Setting Registers

GPIO[3:0] are dedicated GPIO pins.
GPIO[15:4] are activated based on the selected panel type and data width (see REG[20h] bits 3-0). For a summary of GPIO pin availability, see Section 4.5, “Panel Interface Pin Mapping” on page 21.

REG[D0h] GPIO Configuration Register
Address 608D0h Default = 0000h Read/Write

GPIO15 Config 15	GPIO14 Config 14	GPIO13 Config 13	GPIO12 Config 12	GPIO11 Config 11	GPIO10 Config 10	GPIO9 Config 9	GPIO8 Config 8
GPIO7 Config 7	GPIO6 Config 6	GPIO5 Config 5	GPIO4 Config 4	GPIO3 Config 3	GPIO2Config 2	GPIO1 Config 1	GPIO0 Config 0

bits 15-0 GPIO[15:0] Pin Configuration
These bits can be used to change individual GPIO pins between inputs/outputs.
When this bit = 0b (default), the corresponding GPIO pin is configured as an input pin.
When this bit = 1b, the corresponding GPIO pin is configured as an output pin.

REG[D2h] GPIO Status and Control Register
Address 608D2h Default = 0000h Read/Write

GPIO15 Status 15	GPIO14 Status 14	GPIO13 Status 13	GPIO12 Status 12	GPIO11 Status 11	GPIO10 Status 10	GPIO9 Status 9	GPIO8 Status 8
GPIO7 Status 7	GPIO6 Status 6	GPIO5 Status 5	GPIO4 Status 4	GPIO3 Status 3	GPIO2 Status 2	GPIO1 Status 1	GPIO0 Status 0

bits 15-0 GPIO[15:0] Pin Status
When GPIOx is configured as an output, writing a 1b to this bit drives GPIOx high and writing a 0b to this bit drives GPIOx low.
When GPIOx is configured as an input, a read from this bit returns the status of GPIOx.

Note
If a GPIO pin is programmed as a panel output signal (see Section 4.5, “Panel Interface Pin Mapping” on page 21), the corresponding input status bit will indicate the status of the panel output signal.

REG[D4h] GPIO Pull-Down Control Register
Address 608D4h Default = 0000h Read/Write

GPIO15 Pull-down Control 15	GPIO14 Pull-down Control 14	GPIO13 Pull-down Control 13	GPIO12 Pull-down Control 12	GPIO11 Pull-down Control 11	GPIO10 Pull-down Control 10	GPIO9 Pull-down Control 9	GPIO8 Pull-down Control 8
GPIO7 Pull-down Control 7	GPIO6 Pull-down Control 6	GPIO5 Pull-down Control 5	GPIO4 Pull-down Control 4	GPIO3 Pull-down Control 3	GPIO2 Pull-down Control 2	GPIO1 Pull-down Control 1	GPIO0 Pull-down Control 0

bits 15-0 GPIO[15:0] Pull-down Control
All GPIO pins have internal pull-down resistors. These bits individually control the state of the pull-down resistors.
When the bit = 0b, the pull-down resistor for the associated GPIO pin is inactive.
When the bit = 1b, the pull-down resistor for the associated GPIO pin is active.

10.7 Look-Up Table Registers

Note
Do not access LUT1 or LUT2 during PSM0.

LUT1: LUT[000h] ~ LUT[3FEh]

LUT[000h] Look-Up Table 1 Address 00h Register 0
Address 60000h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
LUT1 Address 00h Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT1 Address 00h Blue Data bits 7-0							

LUT[002h] Look-Up Table 1 Address 00h Register 1
Address 60002h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT1 Address 00h Red Data bits 7-0							

LUT[000h] bits 15-8 LUT1 Address 00h Green Data bits [7:0]
These bits contain the data to be written to the green component of the Look-Up Table 1 Address 00h.

LUT[000h] bits 7-0 LUT1 Address 00h Blue Data bits [7:0]
These bits contain the data to be written to the blue component of the Look-Up Table 1 Address 00h.

LUT[002h] bits 7-0 LUT1 Address 00h Red Data bits [7:0]
These bits contain the data to be written to the red component of the Look-Up Table 1 Address 00h.

LUT[004h] Look-Up Table 1 Address 01h Register 0

Address 60004h Default = 0000h Read/Write

LUT1 Address 01h Green Data bits 7-0							
15	14	13	12	11	10	9	8
LUT1 Address 01h Blue Data bits 7-0							
7	6	5	4	3	2	1	0

LUT[006h] Look-Up Table 1 Address 01h Register 1

Address 60006h Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
LUT1 Address 01h Red Data bits 7-0							
7	6	5	4	3	2	1	0

LUT[004h] bits 15-8 LUT1 Address 01h Green Data bits [7:0]
These bits contain the data to be written to the green component of the Look-Up Table 1 Address 01h.

LUT[004h] bits 7-0 LUT1 Address 01h Blue Data bits [7:0]
These bits contain the data to be written to the blue component of the Look-Up Table 1 Address 01h.

LUT[006h] bits 7-0 LUT1 Address 01h Red Data bits [7:0]
These bits contain the data to be written to the red component of the Look-Up Table 1 Address 01h.

LUT[3F8h] Look-Up Table 1 Address FEh Register 0

Address 603F8h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
LUT1 Address FEh Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT1 Address FEh Blue Data bits 7-0							

LUT[3FAh] Look-Up Table 1 Address FEh Register 1

Address 603FAh Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT1 Address FEh Red Data bits 7-0							

LUT[3F8h] bits 15-8 LUT1 Address FEh Green Data bits [7:0]
These bits contain the data to be written to the green component of the Look-Up Table 1 Address FEh.

LUT[3F8h] bits 7-0 LUT1 Address FEh Blue Data bits [7:0]
These bits contain the data to be written to the blue component of the Look-Up Table 1 Address FEh.

LUT[3FAh] bits 7-0 LUT1 Address FEh Red Data bits [7:0]
These bits contain the data to be written to the red component of the Look-Up Table 1 Address FEh.

LUT[3FCh] Look-Up Table 1 Address FFh Register 0

Address 603FCh Default = 0000h Read/Write

15	14	13	12	11	10	9	8
LUT1 Address FFh Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT1 Address FFh Blue Data bits 7-0							

LUT[3FEh] Look-Up Table 1 Address FFh Register 1

Address 603FEh Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT1 Address FFh Red Data bits 7-0							

LUT[3FCh] bits 15-8 LUT1 Address FFh Green Data bits [7:0]
These bits contain the data to be written to the green component of the Look-Up Table 1 Address FFh.

LUT[3FCh] bits 7-0 LUT1 Address FFh Blue Data bits [7:0]
These bits contain the data to be written to the blue component of the Look-Up Table 1 Address FFh.

LUT[3FEh] bits 7-0 LUT1 Address FFh Red Data bits [7:0]
These bits contain the data to be written to the red component of the Look-Up Table 1 Address FFh.

LUT2: LUT[400h] ~ LUT[7FEh]

LUT[400h] Look-Up Table 2 Address 00h Register 0
Address 60400h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
LUT2 Address 00h Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT2 Address 00h Blue Data bits 7-0							

LUT[402h] Look-Up Table 2 Address 00h Register 1
Address 60402h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT2 Address 00h Red Data bits 7-0							

LUT[400h] bits 15-8 LUT2 Address 00h Green Data bits [7:0]
These bits contain the data to be written to the green component of the Look-Up Table 2 Address 00h.

LUT[400h] bits 7-0 LUT2 Address 00h Blue Data bits [7:0]
These bits contain the data to be written to the blue component of the Look-Up Table 2 Address 00h.

LUT[402h] bits 7-0 LUT2 Address 00h Red Data bits [7:0]
These bits contain the data to be written to the red component of the Look-Up Table 2 Address 00h.

LUT[404h] Look-Up Table 2 Address 01h Register 0
Address 60404h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
LUT2 Address 01h Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT2 Address 01h Blue Data bits 7-0							

LUT[406h] Look-Up Table 2 Address 01h Register 1
Address 60406h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT2 Address 01h Red Data bits 7-0							

LUT[404h] bits 15-8 LUT2 Address 01h Green Data bits [7:0]
These bits contain the data to be written to the green component of the Look-Up Table 2 Address 01h.

LUT[404h] bits 7-0 LUT2 Address 01h Blue Data bits [7:0]
These bits contain the data to be written to the blue component of the Look-Up Table 2 Address 01h.

LUT[406h] bits 7-0 LUT2 Address 01h Red Data bits [7:0]
These bits contain the data to be written to the red component of the Look-Up Table 2 Address 01h.

LUT[7F8h] Look-Up Table 2 Address FEh Register 0

Address 607F8h Default = 0000h Read/Write

15	14	13	12	11	10	9	8
LUT2 Address FEh Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT2 Address FEh Blue Data bits 7-0							

LUT[7FAh] Look-Up Table 2 Address FEh Register 1

Address 607FAh Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT2 Address FEh Red Data bits 7-0							

LUT[7F8h] bits 15-8 LUT2 Address FEh Green Data bits [7:0]
These bits contain the data to be written to the green component of the Look-Up Table 2 Address FEh.

LUT[7F8h] bits 7-0 LUT2 Address FEh Blue Data bits [7:0]
These bits contain the data to be written to the blue component of the Look-Up Table 2 Address FEh.

LUT[7FAh] bits 7-0 LUT2 Address FEh Red Data bits [7:0]
These bits contain the data to be written to the red component of the Look-Up Table 2 Address FEh.

LUT[7FCh] Look-Up Table 2 Address FFh Register 0

Address 607FCh Default = 0000h Read/Write

15	14	13	12	11	10	9	8
LUT2 Address FFh Green Data bits 7-0							
7	6	5	4	3	2	1	0
LUT2 Address FFh Blue Data bits 7-0							

LUT[7FEh] Look-Up Table 2 Address FFh Register 1

Address 607FEh Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LUT2 Address FFh Red Data bits 7-0							

LUT[7FCh] bits 15-8 LUT2 Address FFh Green Data bits [7:0]
These bits contain the data to be written to the green component of the Look-Up Table 2 Address FFh.

LUT[7FCh] bits 7-0 LUT2 Address FFh Blue Data bits [7:0]
These bits contain the data to be written to the blue component of the Look-Up Table 2 Address FFh.

LUT[7FEh] bits 7-0 LUT2 Address FFh Red Data bits [7:0]
These bits contain the data to be written to the red component of the Look-Up Table 2 Address FFh.

Chapter 11 Indirect and Serial Host Interface Accessing Sequence

11.1 Indirect Interface

The Indirect Interface requires that the address be defined before the data is written or read. When any of memory, registers, or LUT are accessed, the address is incremented automatically making burst transfers an efficient way of accessing theS1D13L01. There is no boundary between the memory, registers, and LUT (see Chapter 6, “Embedded Memory” on page 23). Note that rectangular writes/reads are not supported.

11.1.1 Write Procedure

The following figures provide example procedures for performing single writes and burst writes. The examples are shown for the Indirect 16-bit Mode and Indirect 8-bit interfaces.

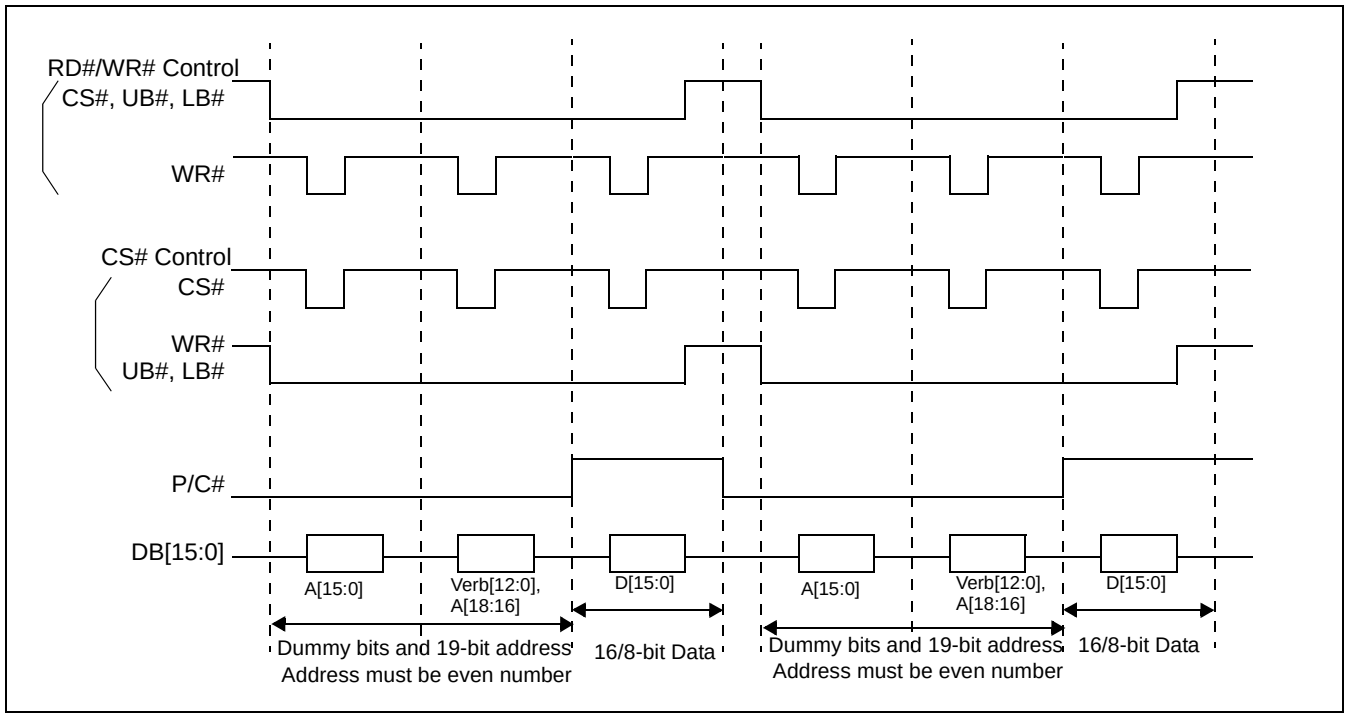


Figure 11-1: Indirect 16-bit Mode 1 Single Write Example Sequence

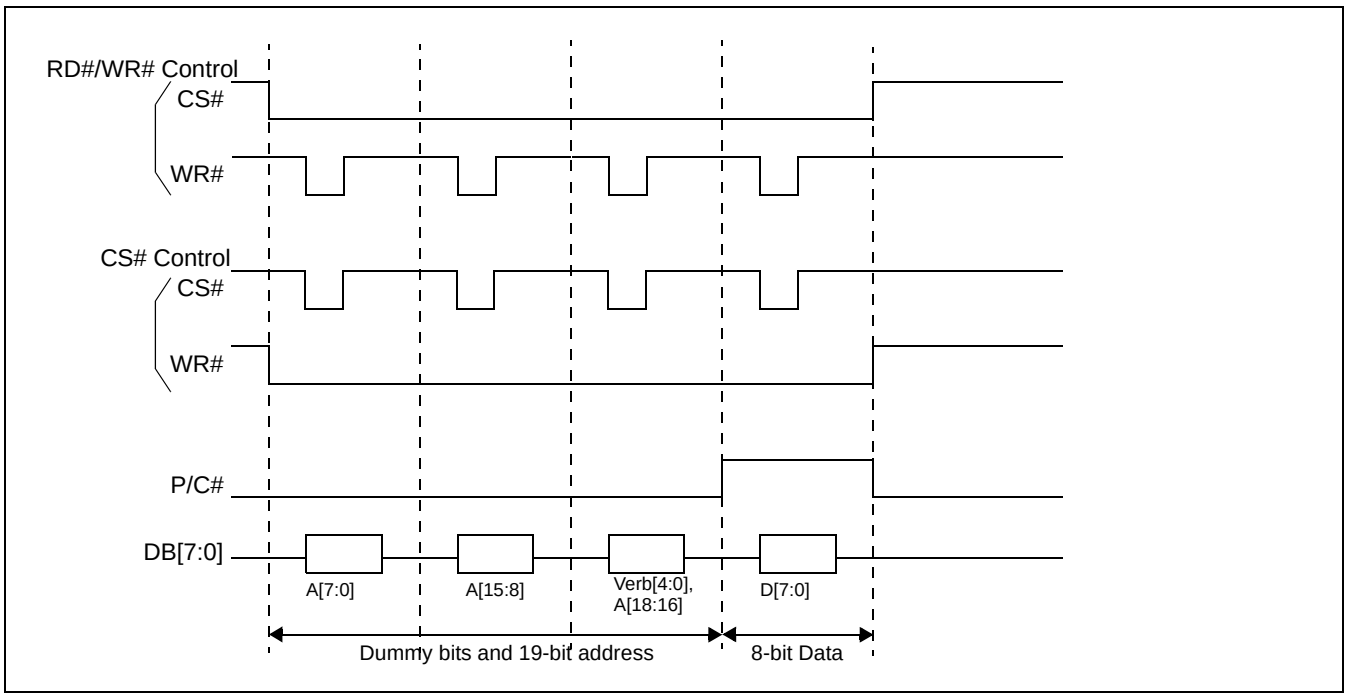


Figure 11-2: Indirect 8-bit Single Write Example Sequence

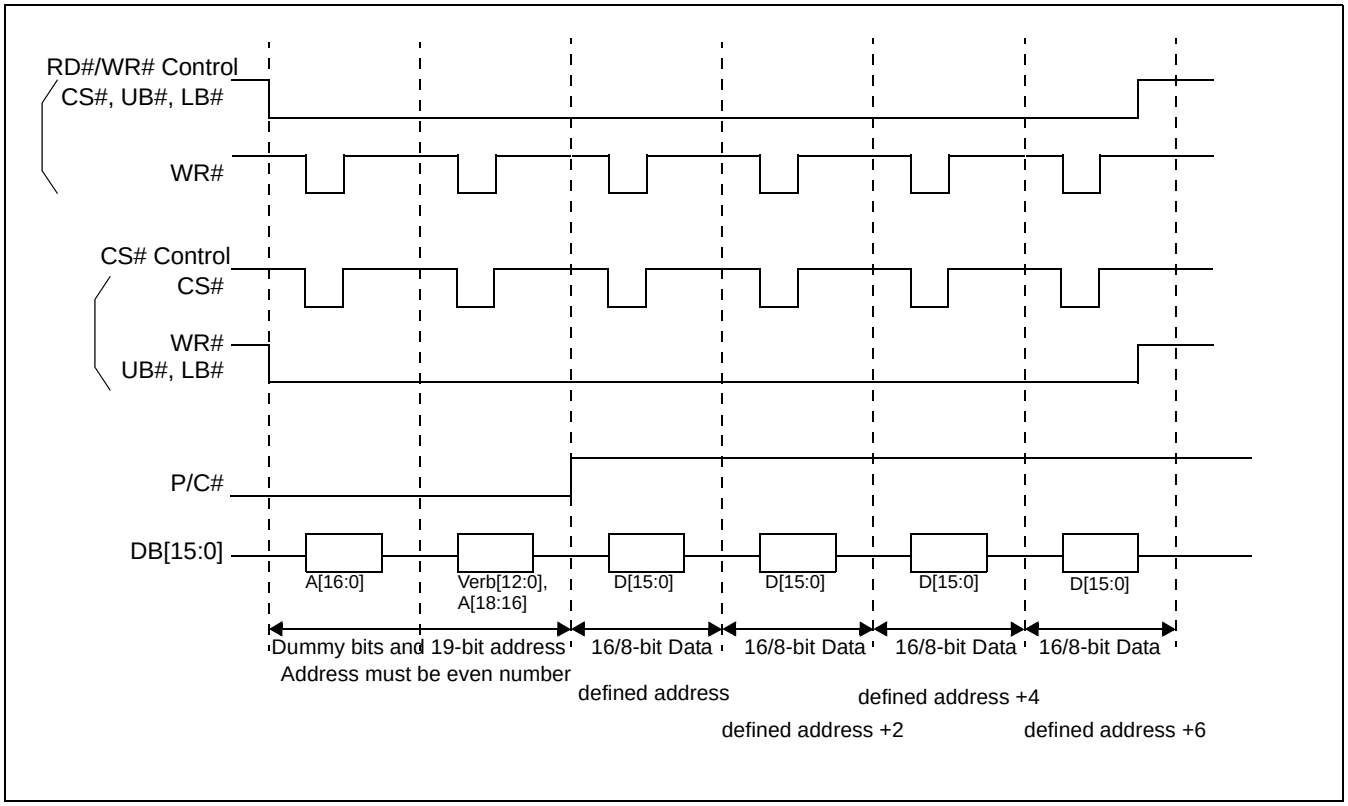


Figure 11-3: Indirect 16-bit Mode 1 Burst Write Example Sequence

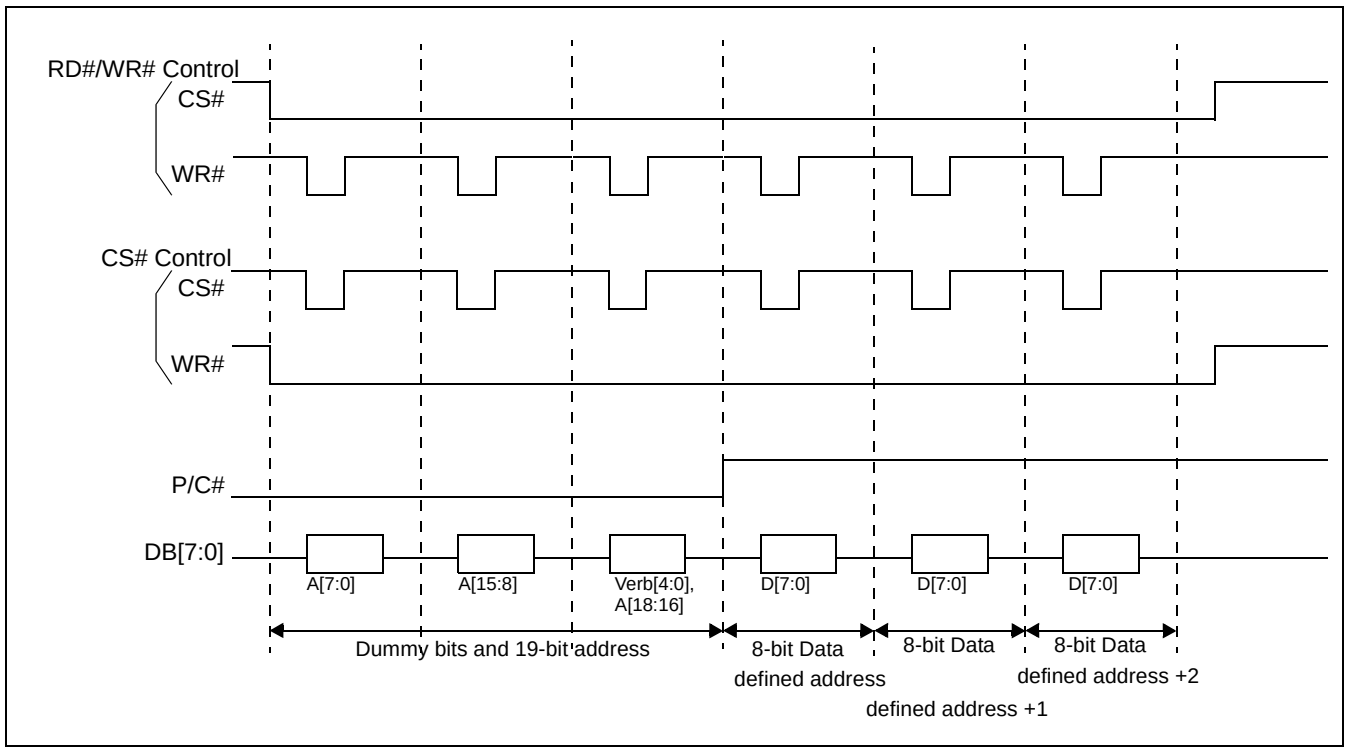


Figure 11-4: Indirect 8-bit Burst Write Example Sequence

11.1.2 Read Procedure

The following figures provide example procedures for performing single reads and burst reads. The examples are shown for the Indirect 16-bit Mode and Indirect 8-bit interfaces.

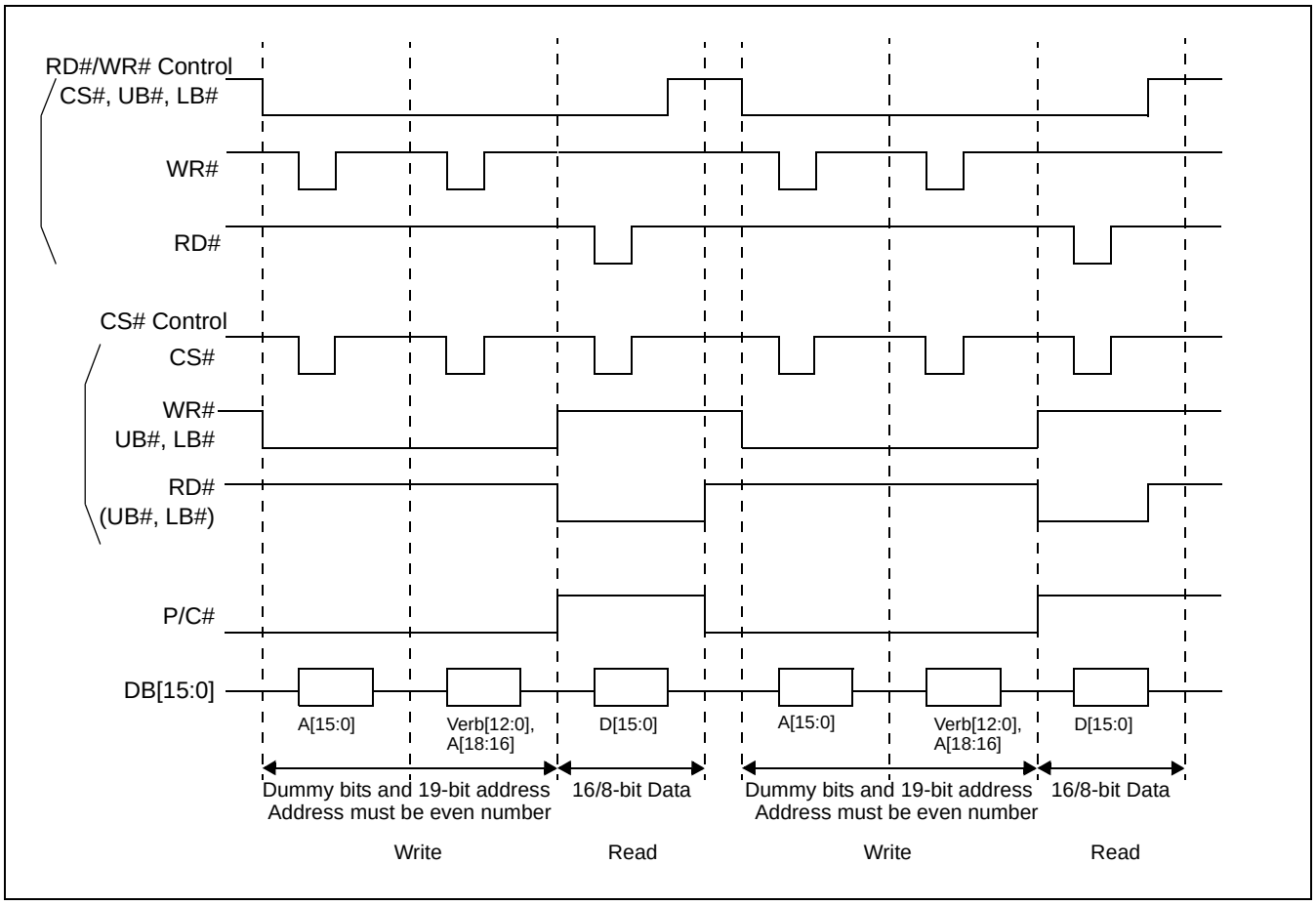


Figure 11-5: Indirect 16-bit Mode 1 Single Read Example Sequence

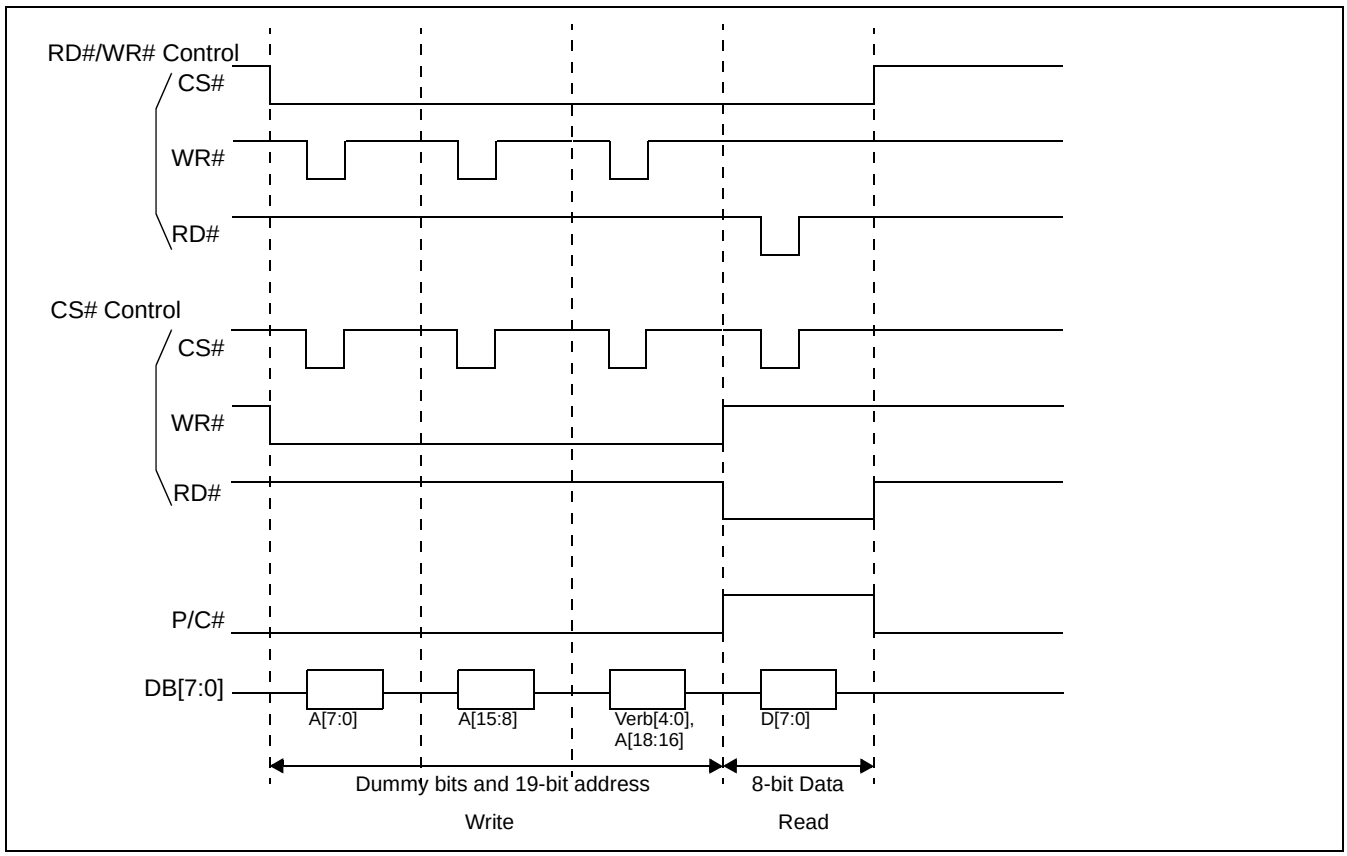


Figure 11-6: Indirect 8-bit Single Read Example Sequence

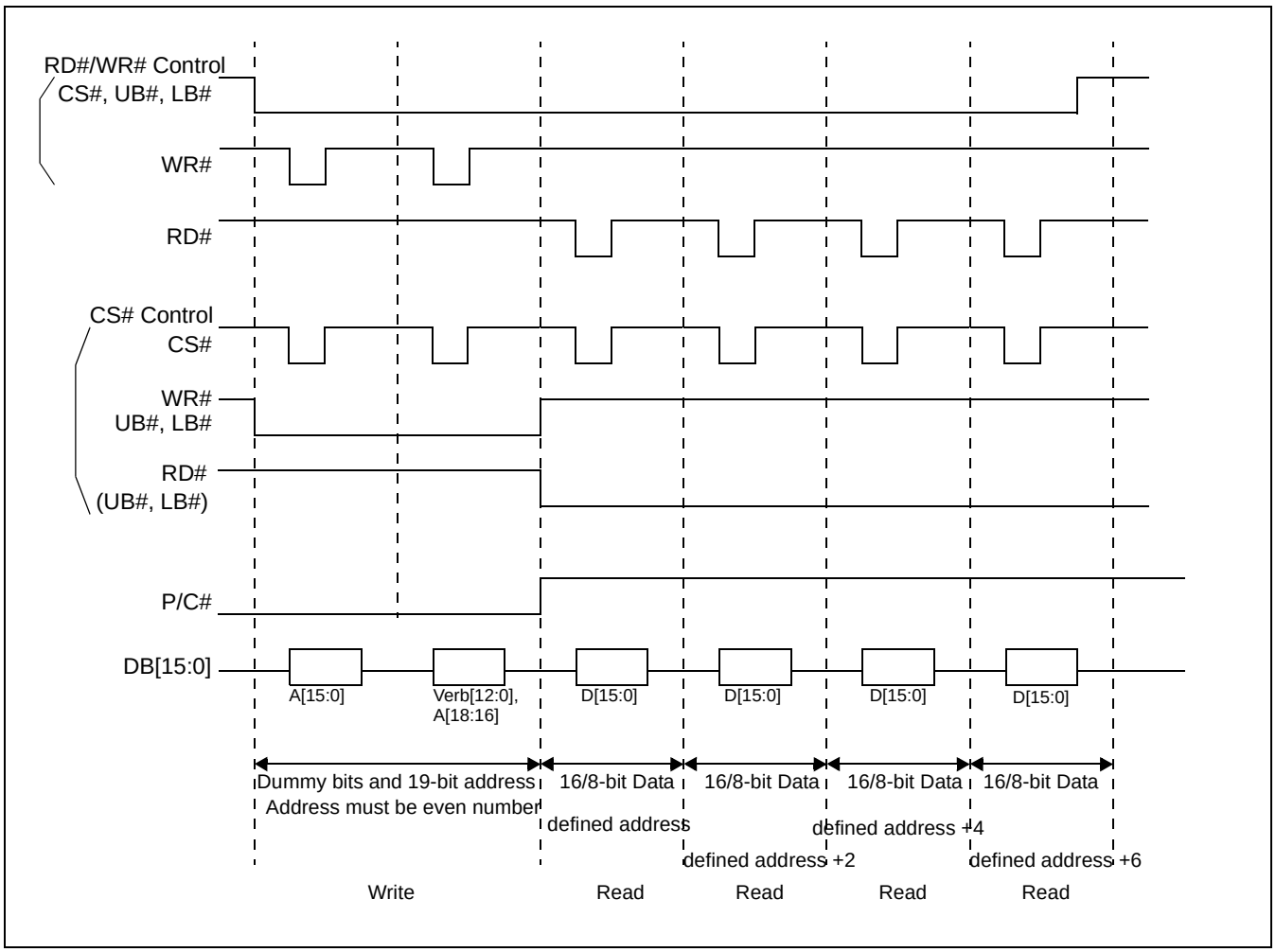


Figure 11-7: Indirect 16-bit Mode 1 Burst Read Example Sequence

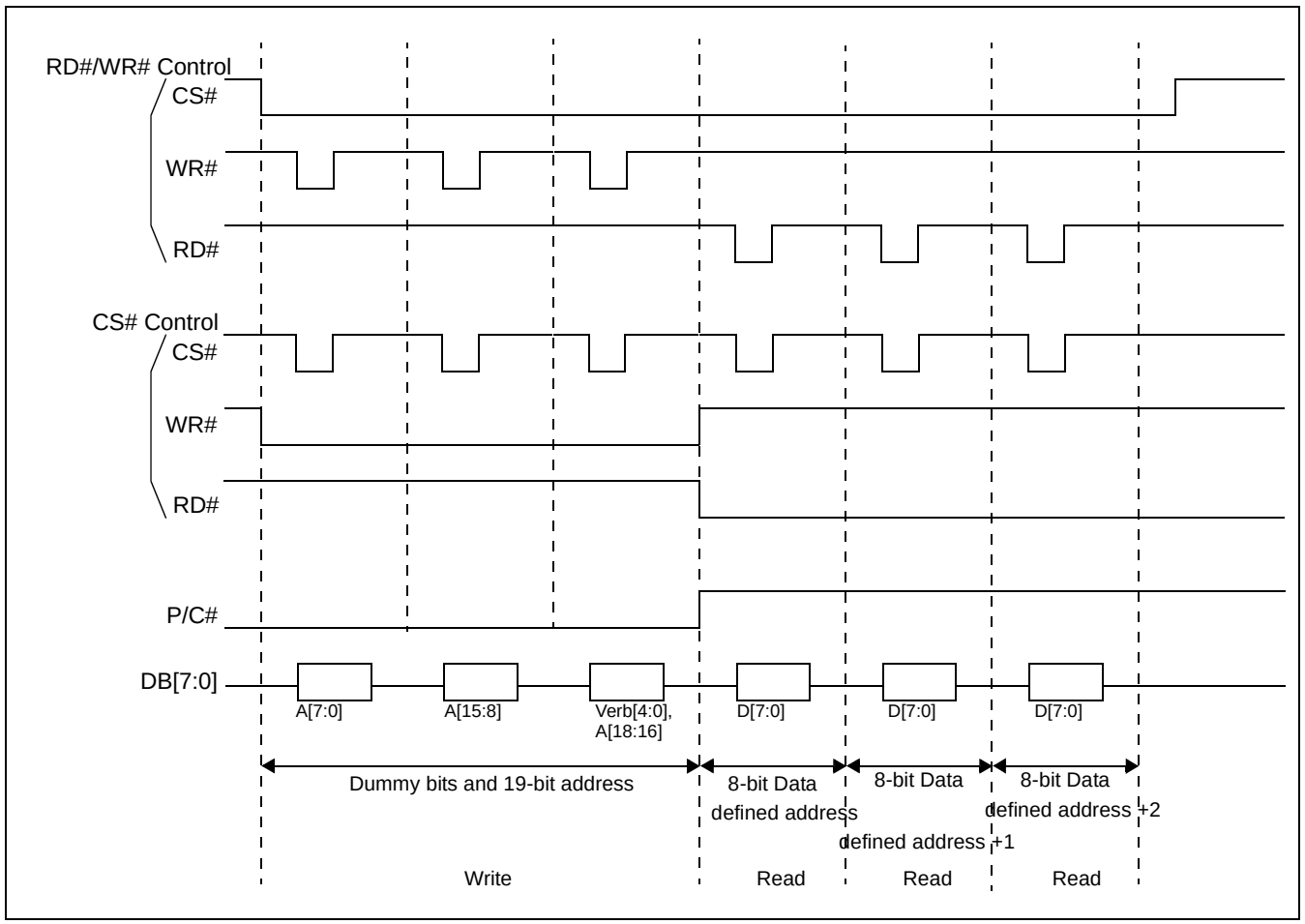


Figure 11-8: Indirect 8-bit Burst Read Example Sequence

11.2 SPI

The SPI host interface supports both Mode 0 and Mode 3.

Mode 0 and Mode 3 latch the data on the rising edge of the clock and shift the data on the falling edge of the clock. The idle state of SCK is low for Mode 0, and high for Mode 3. This means that Mode 0 always starts with latching the data and Mode 3 always starts with shifting the data. For both Mode 0 and Mode 3, the MSB is first. The accessing cycle always starts after the SCS# falling edge. When the accessing cycle starts, the first byte must be command 8-bit, the second byte must be verbose 5-bit and upper address 3-bit, the third byte must be middle address 8-bit, the fourth byte must be lower address 8-bit. From the fifth byte on, it depends on the command in the first byte. The accessing cycle is broken by SCS# rising edge.

When burst accessing, the address is incremented automatically.
When Reading, the first byte (or word) is dummy data. Actual data will come on the second byte (or word).

If there is a difference between command and data (or address) bit counts, the data will be ignored when it is larger. The accessing cycle is broken by SCS# when data is smaller.

For 16-bit read/write, the address must be an even number.

Table 11-1: SPI Function Select

Command	Comments
10000000b	8-bit Write
11000000b	8-bit Read
10001000b	16-bit Write
11001000b	16-bit Read
all other values	Reserved

11.2.1 Write Procedure

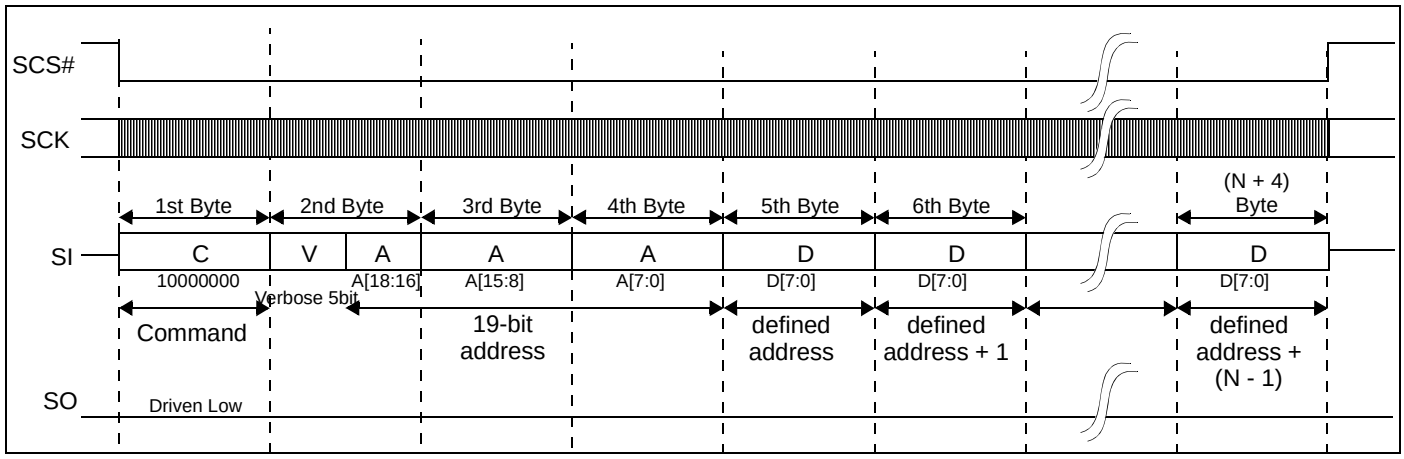


Figure 11-9: SPI 8-bit Write Example Sequence to Write N Bytes (N = 1 or greater)

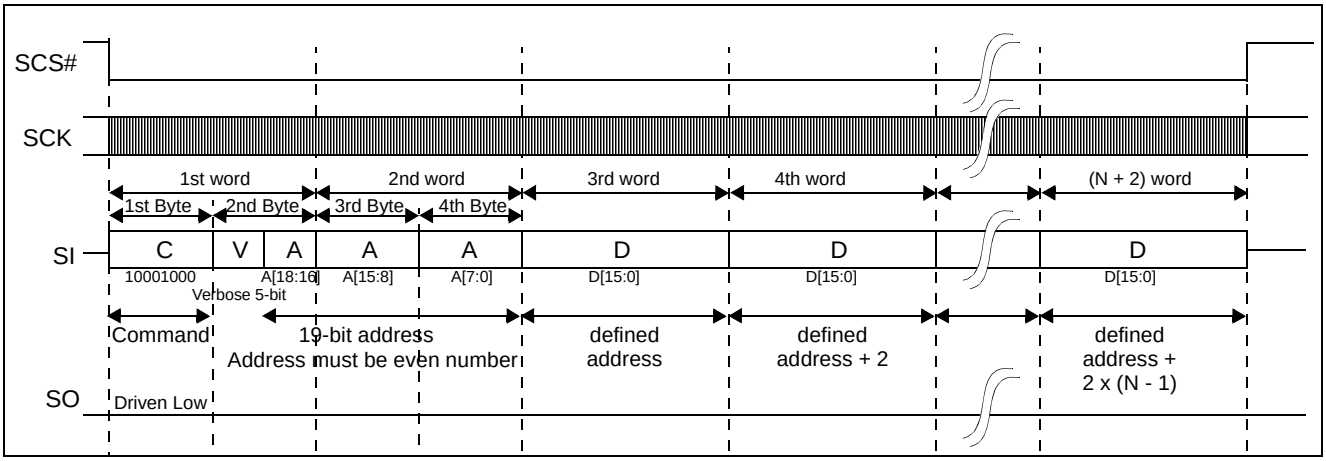


Figure 11-10: SPI 16-bit Write Example Sequence to Write N Words (N = 1 or greater)

11.2.2 Read Procedure

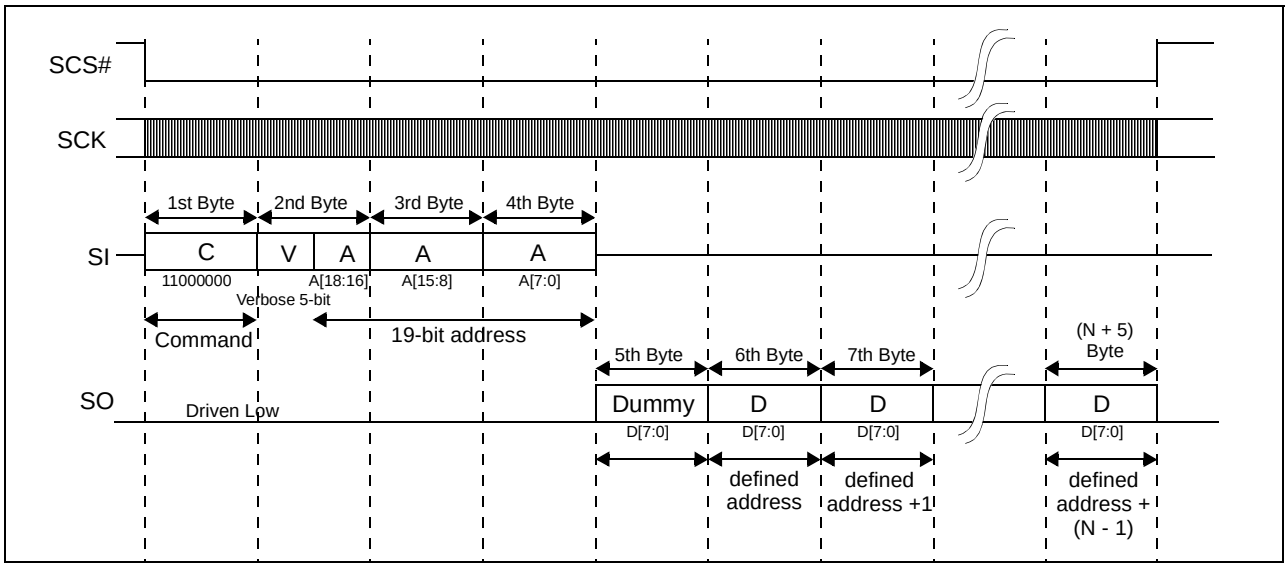


Figure 11-11: SPI 8-bit Read Example Sequence to Read N Words (N = 1 or greater)

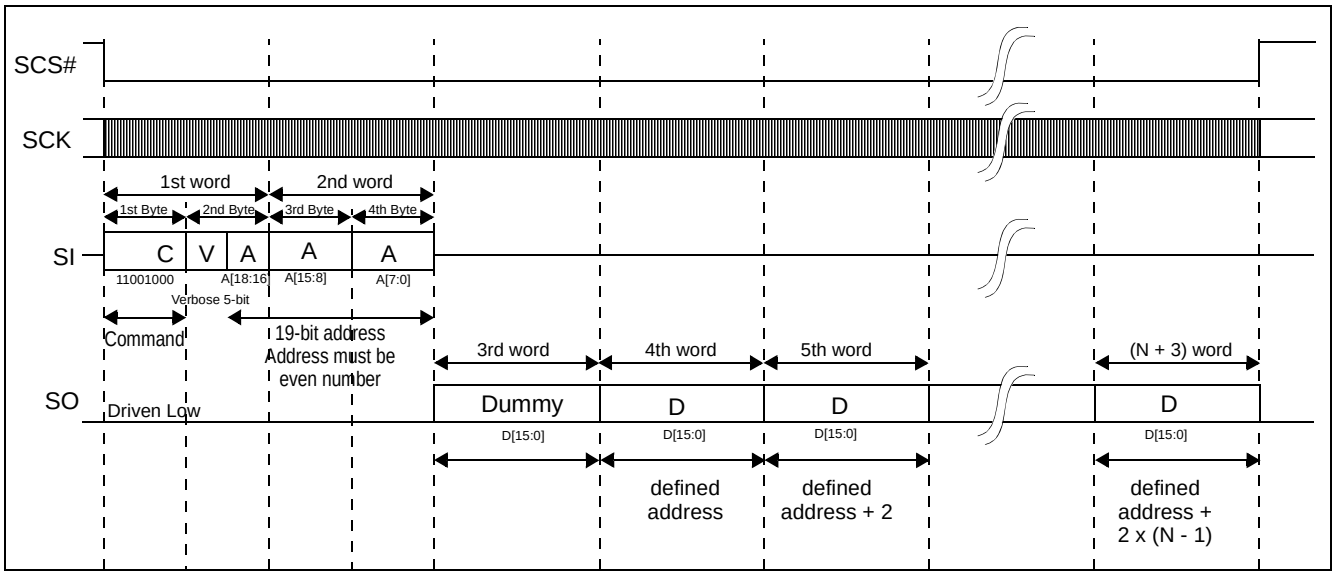


Figure 11-12: SPI 16-bit Read Example Sequence to Read N Words (N = 1 or greater)

Chapter 12 Image Data Formats

12.1 Image Data Formats for Host Interface

The following diagrams show the display data formats for the Host Interface. The display start addresses of both the PIP and Main Layers must be 32-bit aligned, AB[1:0] = 00b.

12.1.1 RGB 8:8:8 Data Format

When the Host inputs data using the RGB 8:8:8 data format, the destination layer (Main or PIP) should be set to the RGB 8:8:8 color depth, REG[40h] bits 2-0 = 000b or REG[50h] bits 2-0 = 000b.

Table 12-1: RGB 8:8:8 Data Format for 16-bit Host Interface

Cycle	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	G_n^7	G_n^6	G_n^5	G_n^4	G_n^3	G_n^2	G_n^1	G_n^0	B_n^7	B_n^6	B_n^5	B_n^4	B_n^3	B_n^2	B_n^1	B_n^0
m+1	B_{n+1}^7	B_{n+1}^6	B_{n+1}^5	B_{n+1}^4	B_{n+1}^3	B_{n+1}^2	B_{n+1}^1	B_{n+1}^0	R_n^7	R_n^6	R_n^5	R_n^4	R_n^3	R_n^2	R_n^1	R_n^0
m+2	R_{n+1}^7	R_{n+1}^6	R_{n+1}^5	R_{n+1}^4	R_{n+1}^3	R_{n+1}^2	R_{n+1}^1	R_{n+1}^0	G_{n+1}^7	G_{n+1}^6	G_{n+1}^5	G_{n+1}^4	G_{n+1}^3	G_{n+1}^2	G_{n+1}^1	G_{n+1}^0

Table 12-2: RGB 8:8:8 Data Format for 8-bit Host Interface

Cycle	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	B_n^7	B_n^6	B_n^5	B_n^4	B_n^3	B_n^2	B_n^1	B_n^0
m+1	G_n^7	G_n^6	G_n^5	G_n^4	G_n^3	G_n^2	G_n^1	G_n^0
m+2	R_n^7	R_n^6	R_n^5	R_n^4	R_n^3	R_n^2	R_n^1	R_n^0
m+3	B_{n+1}^7	B_{n+1}^6	B_{n+1}^5	B_{n+1}^4	B_{n+1}^3	B_{n+1}^2	B_{n+1}^1	B_{n+1}^0
m+4	G_{n+1}^7	G_{n+1}^6	G_{n+1}^5	G_{n+1}^4	G_{n+1}^3	G_{n+1}^2	G_{n+1}^1	G_{n+1}^0
m+5	R_{n+1}^7	R_{n+1}^6	R_{n+1}^5	R_{n+1}^4	R_{n+1}^3	R_{n+1}^2	R_{n+1}^1	R_{n+1}^0

12.1.2 RGB 5:6:5 Data Format

When the Host inputs data using the RGB 5:6:5 data format, the destination layer (Main or PIP) should be set to the RGB 5:6:5 color depth, REG[40h] bits 2-0 = 001b or REG[50h] bits 2-0 = 001b.

Table 12-3: RGB 5:6:5 Data Format for 16-bit Host Interface

Cycle	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	R_n^4	R_n^3	R_n^2	R_n^1	R_n^0	G_n^5	G_n^4	G_n^3	G_n^2	G_n^1	G_n^0	B_n^4	B_n^3	B_n^2	B_n^1	B_n^0
m+1	R_{n+1}^4	R_{n+1}^3	R_{n+1}^2	R_{n+1}^1	R_{n+1}^0	G_{n+1}^5	G_{n+1}^4	G_{n+1}^3	G_{n+1}^2	G_{n+1}^1	G_{n+1}^0	B_{n+1}^4	B_{n+1}^3	B_{n+1}^2	B_{n+1}^1	B_{n+1}^0
m+2	R_{n+2}^4	R_{n+2}^3	R_{n+2}^2	R_{n+2}^1	R_{n+2}^0	G_{n+2}^5	G_{n+2}^4	G_{n+2}^3	G_{n+2}^2	G_{n+2}^1	G_{n+2}^0	B_{n+2}^4	B_{n+2}^3	B_{n+2}^2	B_{n+2}^1	B_{n+2}^0

Table 12-4: RGB 5:6:5 Data Format for 8-bit Host Interface

Cycle	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	G_n^2	G_n^1	G_n^0	B_n^4	B_n^3	B_n^2	B_n^1	B_n^0
m+1	R_n^4	R_n^3	R_n^2	R_n^1	R_n^0	G_n^5	G_n^4	G_n^3
m+2	G_{n+1}^2	G_{n+1}^1	G_{n+1}^0	B_{n+1}^4	B_{n+1}^3	B_{n+1}^2	B_{n+1}^1	B_{n+1}^0
m+3	R_{n+1}^4	R_{n+1}^3	R_{n+1}^2	R_{n+1}^1	R_{n+1}^0	G_{n+1}^5	G_{n+1}^4	G_{n+1}^3

12.1.3 24 bpp + LUT Data Format

When the Host inputs data using the 24 bpp + LUT data format, the destination layer (Main or PIP) should be set to the 24 bpp + LUTx color depth, REG[40h] bits 2-0 = 100b or REG[50h] bits 2-0 = 100b.

Table 12-5: 24 bpp + LUT Data Format for 16-bit Host Interface

Cycle	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	LG_n^7	LG_n^6	LG_n^5	LG_n^4	LG_n^3	LG_n^2	LG_n^1	LG_n^0	LB_n^7	LB_n^6	LB_n^5	LB_n^4	LB_n^3	LB_n^2	LB_n^1	LB_n^0
m+1	LB_{n+1}^7	LB_{n+1}^6	LB_{n+1}^5	LB_{n+1}^4	LB_{n+1}^3	LB_{n+1}^2	LB_{n+1}^1	LB_{n+1}^0	LR_n^7	LR_n^6	LR_n^5	LR_n^4	LR_n^3	LR_n^2	LR_n^1	LR_n^0
m+2	LR_{n+1}^7	LR_{n+1}^6	LR_{n+1}^5	LR_{n+1}^4	LR_{n+1}^3	LR_{n+1}^2	LR_{n+1}^1	LR_{n+1}^0	LG_{n+1}^7	LG_{n+1}^6	LG_{n+1}^5	LG_{n+1}^4	LG_{n+1}^3	LG_{n+1}^2	LG_{n+1}^1	LG_{n+1}^0

Table 12-6: 24 bpp + LUT Data Format for 8-bit Host Interface

Cycle	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	LB_n^7	LB_n^6	LB_n^5	LB_n^4	LB_n^3	LB_n^2	LB_n^1	LB_n^0
m+1	LG_n^7	LG_n^6	LG_n^5	LG_n^4	LG_n^3	LG_n^2	LG_n^1	LG_n^0
m+2	LR_n^7	LR_n^6	LR_n^5	LR_n^4	LR_n^3	LR_n^2	LR_n^1	LR_n^0
m+3	LB_{n+1}^7	LB_{n+1}^6	LB_{n+1}^5	LB_{n+1}^4	LB_{n+1}^3	LB_{n+1}^2	LB_{n+1}^1	LB_{n+1}^0
m+4	LG_{n+1}^7	LG_{n+1}^6	LG_{n+1}^5	LG_{n+1}^4	LG_{n+1}^3	LG_{n+1}^2	LG_{n+1}^1	LG_{n+1}^0
m+5	LR_{n+1}^7	LR_{n+1}^6	LR_{n+1}^5	LR_{n+1}^4	LR_{n+1}^3	LR_{n+1}^2	LR_{n+1}^1	LR_{n+1}^0

12.1.4 16 bpp + LUT Data Format

When the Host inputs data using the 16 bpp + LUT data format, the destination layer (Main or PIP) should be set to the 16 bpp + LUTx color depth, REG[40h] bits 2-0 = 101b or REG[50h] bits 2-0 = 101b.

Table 12-7: 16 bpp + LUT Data Format for 16-bit Host Interface

Cycle	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	LR_n^4	LR_n^3	LR_n^2	LR_n^1	LR_n^0	LG_n^5	LG_n^4	LG_n^3	LG_n^2	LG_n^1	LG_n^0	LB_n^4	LB_n^3	LB_n^2	LB_n^1	LB_n^0
m+1	LR_{n+1}^4	LR_{n+1}^3	LR_{n+1}^2	LR_{n+1}^1	LR_{n+1}^0	LG_{n+1}^5	LG_{n+1}^4	LG_{n+1}^3	LG_{n+1}^2	LG_{n+1}^1	LG_{n+1}^0	LB_{n+1}^4	LB_{n+1}^3	LB_{n+1}^2	LB_{n+1}^1	LB_{n+1}^0
m+2	LR_{n+2}^4	LR_{n+2}^3	LR_{n+2}^2	LR_{n+2}^1	LR_{n+2}^0	LG_{n+2}^5	LG_{n+2}^4	LG_{n+2}^3	LG_{n+2}^2	LG_{n+2}^1	LG_{n+2}^0	LB_{n+2}^4	LB_{n+2}^3	LB_{n+2}^2	LB_{n+2}^1	LB_{n+2}^0

Table 12-8: 16 bpp + LUT Data Format for 8-bit Host Interface

Cycle	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	LG_n^2	LG_n^1	LG_n^0	LB_n^4	LB_n^3	LB_n^2	LB_n^1	LB_n^0
m+1	LR_n^4	LR_n^3	LR_n^2	LR_n^1	LR_n^0	LG_n^5	LG_n^4	LG_n^3
m+2	LG_{n+1}^2	LG_{n+1}^1	LG_{n+1}^0	LB_{n+1}^4	LB_{n+1}^3	LB_{n+1}^2	LB_{n+1}^1	LB_{n+1}^0
m+3	LR_{n+1}^4	LR_{n+1}^3	LR_{n+1}^2	LR_{n+1}^1	LR_{n+1}^0	LG_{n+1}^5	LG_{n+1}^4	LG_{n+1}^3

12.1.5 8 bpp + LUT Data Format

When the Host inputs data using the 8 bpp + LUT data format, the destination layer (Main or PIP) should be set to the 8 bpp + LUTx color depth, REG[40h] bits 2-0 = 110b or REG[50h] bits 2-0 = 110b.

Table 12-9: 8 bpp + LUT Data Format for 16-bit Host Interface

Cycle	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	LA_{n+1}^{7}	LA_{n+1}^{6}	LA_{n+1}^{5}	LA_{n+1}^{4}	LA_{n+1}^{3}	LA_{n+1}^{2}	LA_{n+1}^{1}	LA_{n+1}^{0}	LA_{n}^{7}	LA_{n}^{6}	LA_{n}^{5}	LA_{n}^{4}	LA_{n}^{3}	LA_{n}^{2}	LA_{n}^{1}	LA_{n}^{0}
m+1	LA_{n+3}^{7}	LA_{n+3}^{6}	LA_{n+3}^{5}	LA_{n+3}^{4}	LA_{n+3}^{3}	LA_{n+3}^{2}	LA_{n+3}^{1}	LA_{n+3}^{0}	LA_{n+2}^{7}	LA_{n+2}^{6}	LA_{n+2}^{5}	LA_{n+2}^{4}	LA_{n+2}^{3}	LA_{n+2}^{2}	LA_{n+2}^{1}	LA_{n+2}^{0}
m+2	LA_{n+5}^{7}	LA_{n+5}^{6}	LA_{n+5}^{5}	LA_{n+5}^{4}	LA_{n+5}^{3}	LA_{n+5}^{2}	LA_{n+5}^{1}	LA_{n+5}^{0}	LA_{n+4}^{7}	LA_{n+4}^{6}	LA_{n+4}^{5}	LA_{n+4}^{4}	LA_{n+4}^{3}	LA_{n+4}^{2}	LA_{n+4}^{1}	LA_{n+4}^{0}

Table 12-10: 8 bpp + LUT Data Format for 8-bit Host Interface

Cycle	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
m	LA_{n}^{7}	LA_{n}^{6}	LA_{n}^{5}	LA_{n}^{4}	LA_{n}^{3}	LA_{n}^{2}	LA_{n}^{1}	LA_{n}^{0}
m+1	LA_{n+1}^{7}	LA_{n+1}^{6}	LA_{n+1}^{5}	LA_{n+1}^{4}	LA_{n+1}^{3}	LA_{n+1}^{2}	LA_{n+1}^{1}	LA_{n+1}^{0}
m+2	LA_{n+2}^{7}	LA_{n+2}^{6}	LA_{n+2}^{5}	LA_{n+2}^{4}	LA_{n+2}^{3}	LA_{n+2}^{2}	LA_{n+2}^{1}	LA_{n+2}^{0}

12.2 Data Expansion

Between VRAM and the panel interface, data is expanded (or bit covered) to 24-bit by copying the MSBs to the LSBs as follows.

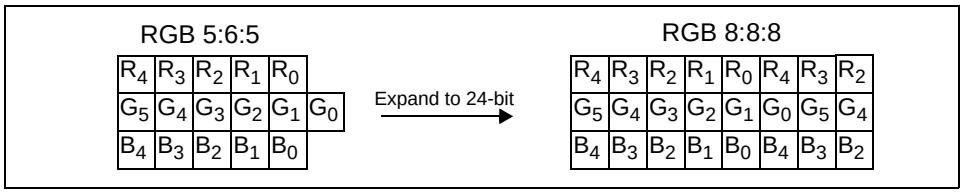


Figure 12-1: Data Path Image

12.3 Color Depth

To define color depth, the following registers need to be set. REG[40h] (REG[50h]) bits 2-0 define the data format in memory and if the LUT is used or not. REG[20h] bits 3-0 define panel data format. See the following figure for details.

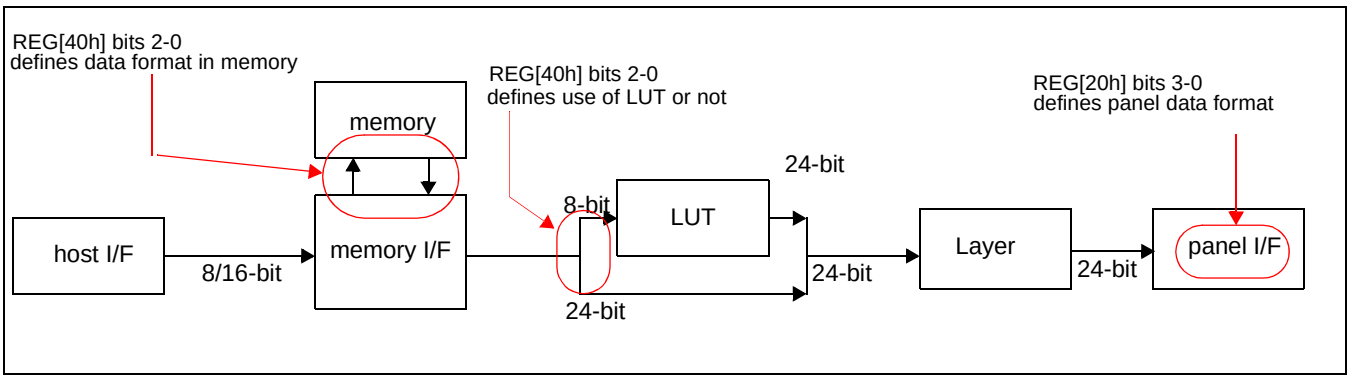


Figure 12-2: Color Depth Registers for Main layer

All image data is handled as 24-bits, 8-bits for each color. The master logic output is 24-bits from which slave logic takes the required data bits. The slave logic removes any unused bits from the least significant bits of data. For example, the memory interface block outputs data as 24-bits, even if it is stored as RGB 5:6:5 in memory (see Section 12.2, “Data Expansion” on page 100 for details). When REG[20h] bits 3-0 select the TFT 16-bit panel, the interface block uses 5-bits for red and blue, and 6-bits for green from the most significant bits, even if RGB 8:8:8 format is in memory.

Chapter 13 Look-Up Table Architecture

The Main and PIP Layers can be configured for a variety of color depths (see REG[40h] and REG[50h]). Some color depths use a Look-up Table (LUT) architecture to determine the output color. Each layer has its own LUT: Main Layer uses LUT1, PIP Layer uses LUT2.

13.1 24 bpp LUT

When the Main or PIP Layer is configured for 24 bpp + LUTx (REG[40h] bits 2-0 = 100b or REG[50h] bits 2-0 = 100b), the following LUT architecture is used.

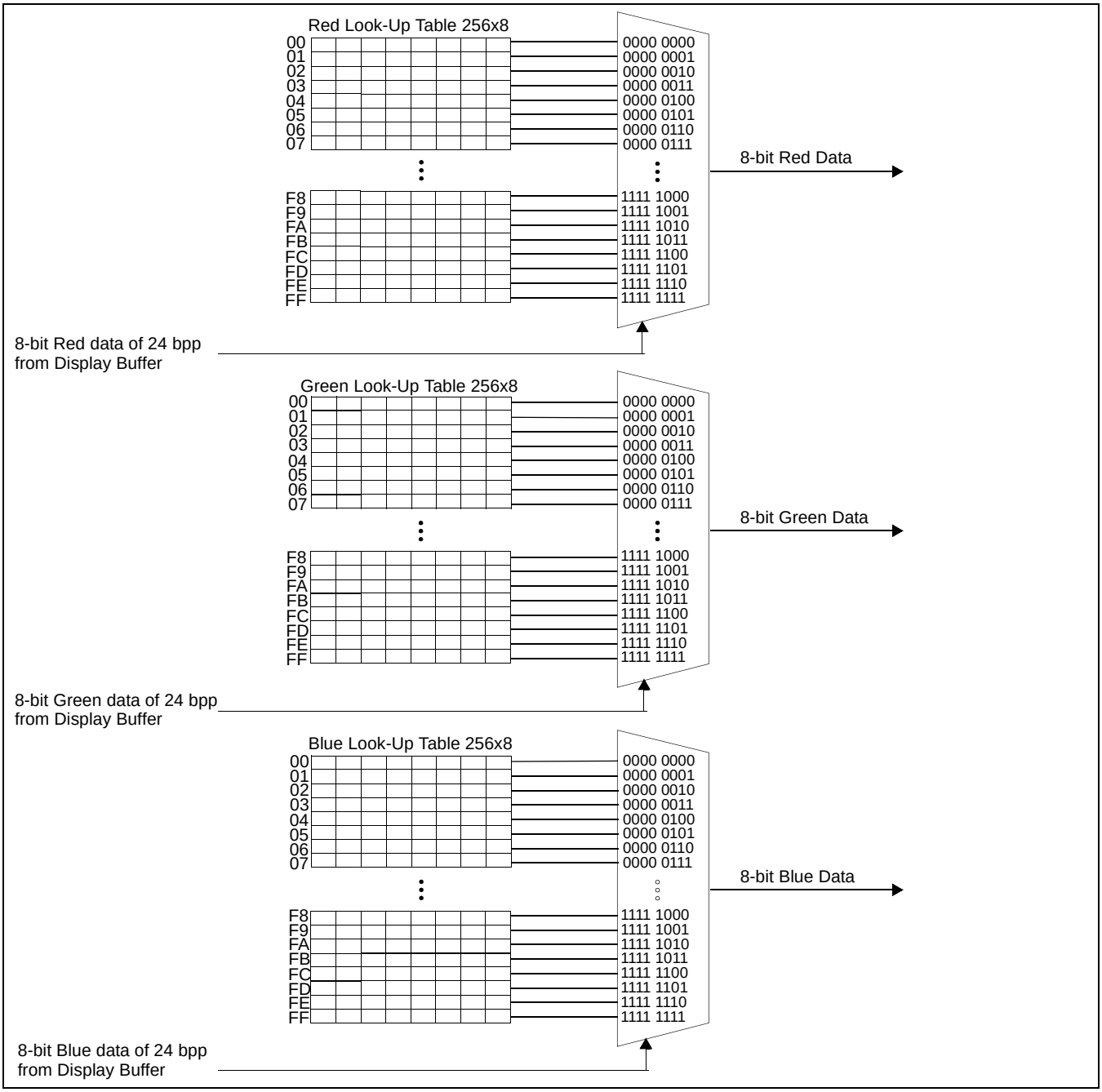


Figure 13-1: 24 bpp LUT

13.2 16 bpp LUT

When the Main or PIP Layer is configured for 16 bpp + LUTx (REG[40h] bits 2-0 = 101b or REG[50h] bits 2-0 = 101b), the following LUT architecture is used.

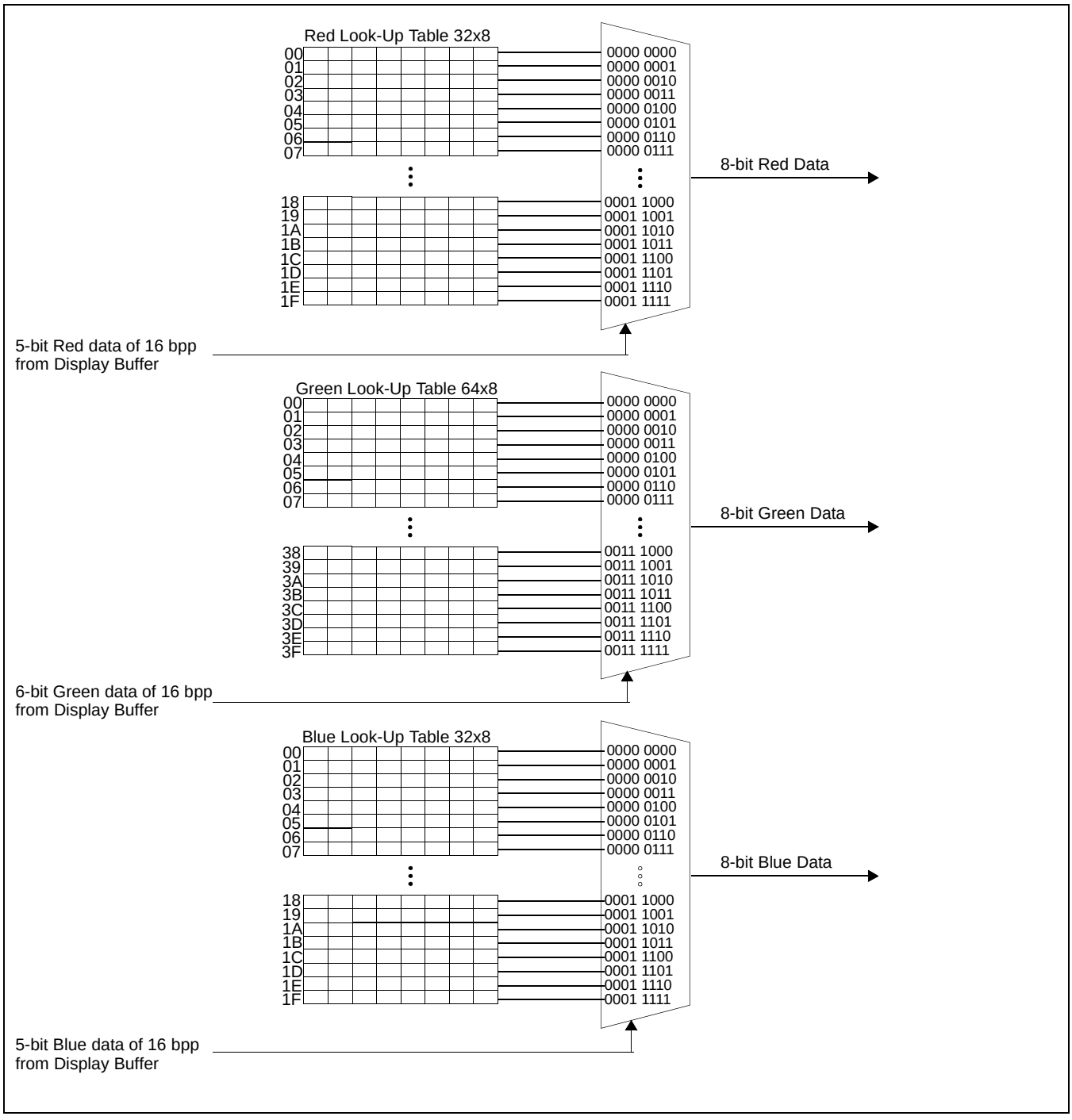


Figure 13-2: 16 bpp LUT

13.3 8 bpp LUT in Color Mode

When the S1D13L01 is configured for a color LCD panel (REG[20h] bit 3 = 1b) and the Main or PIP Layer is configured for 8 bpp + LUTx (REG[40h] bits 2-0 = 110b or REG[50h] bits 2-0 = 110b), the following LUT architecture is used.

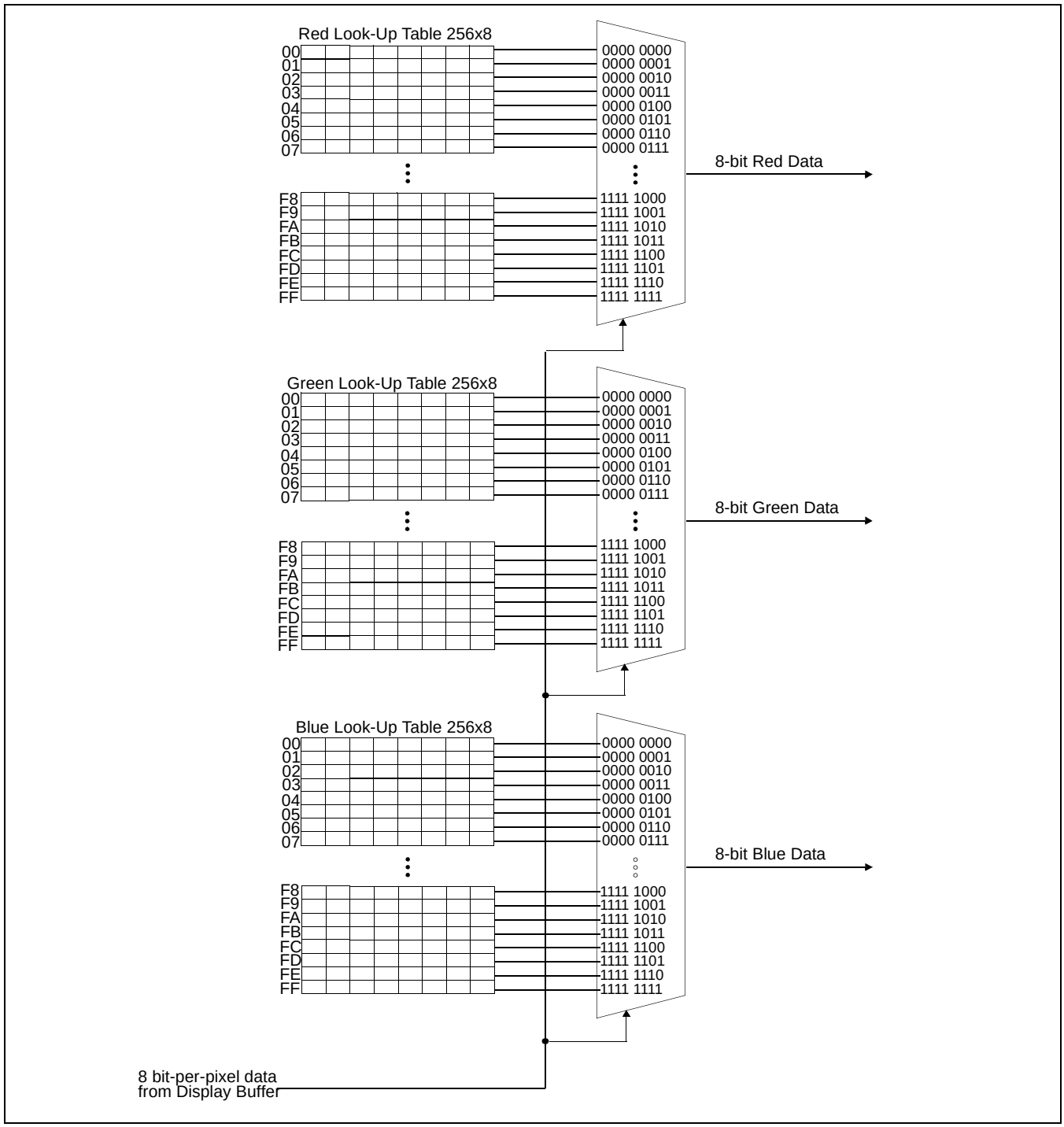


Figure 13-3: 8 bpp LUT in Color Mode

Chapter 14 Display Features

14.1 PIP (Picture-in-Picture) Layer

REG[60h] PIP Enable Register bits 2-0 are the PIP Effect bits. When the PIP Effect bits are 000b, the PIP (picture-in-picture) Layer is not displayed (set to Blank). The PIP Layer is displayed when the PIP Effect bits are not 000b. PIP Effect settings include Normal, Blink1, Blink2, Fade Out, Fade In, and Fade In/Out Continuous. PIP Layer is displayed on top of the Main Layer. Its width and height are specified by REG[56h] and REG[58h], respectively, and its (X,Y) position within the Main Layer is specified by REG[5Ah] and REG[5Ch]. The PIP Layer is alpha-blended with the Main Layer, and the alpha-blend value is specified by REG[62h] Alpha Blending Register bits 6-0. The example below shows the PIP Effect bits set to Normal with maximum alpha-blend value (solid PIP Layer).

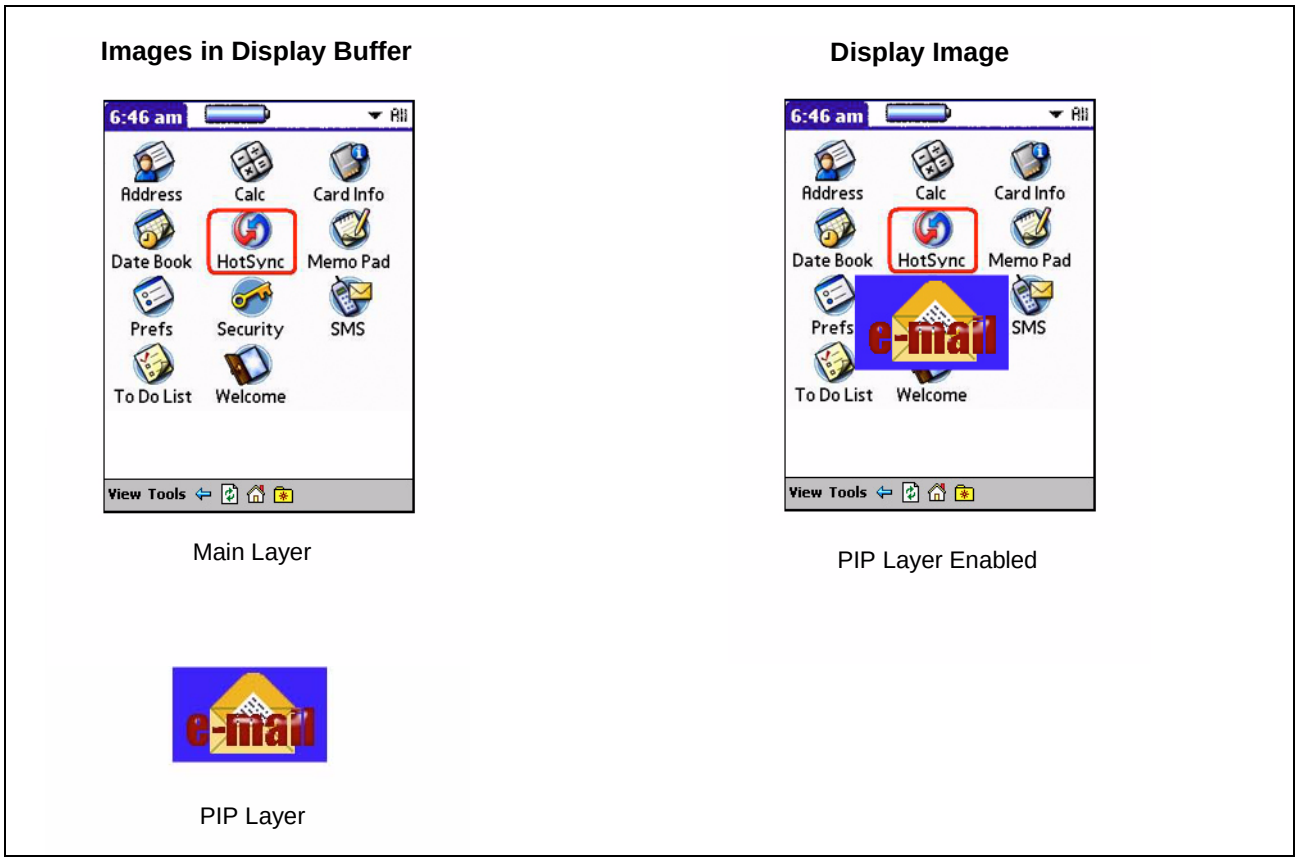


Figure 14-1: PIP Layer

14.2 Transparency

REG[64h] bit 0 is the Transparency Enable bit. When this bit is enabled, the color defined by REG[66h] and REG[68h] are assigned as the Key Color. The Key Color is not affected by either the Alpha Blending or PIP Effect features. The PIP Layer must be enabled through REG[60h] bits 2-0.

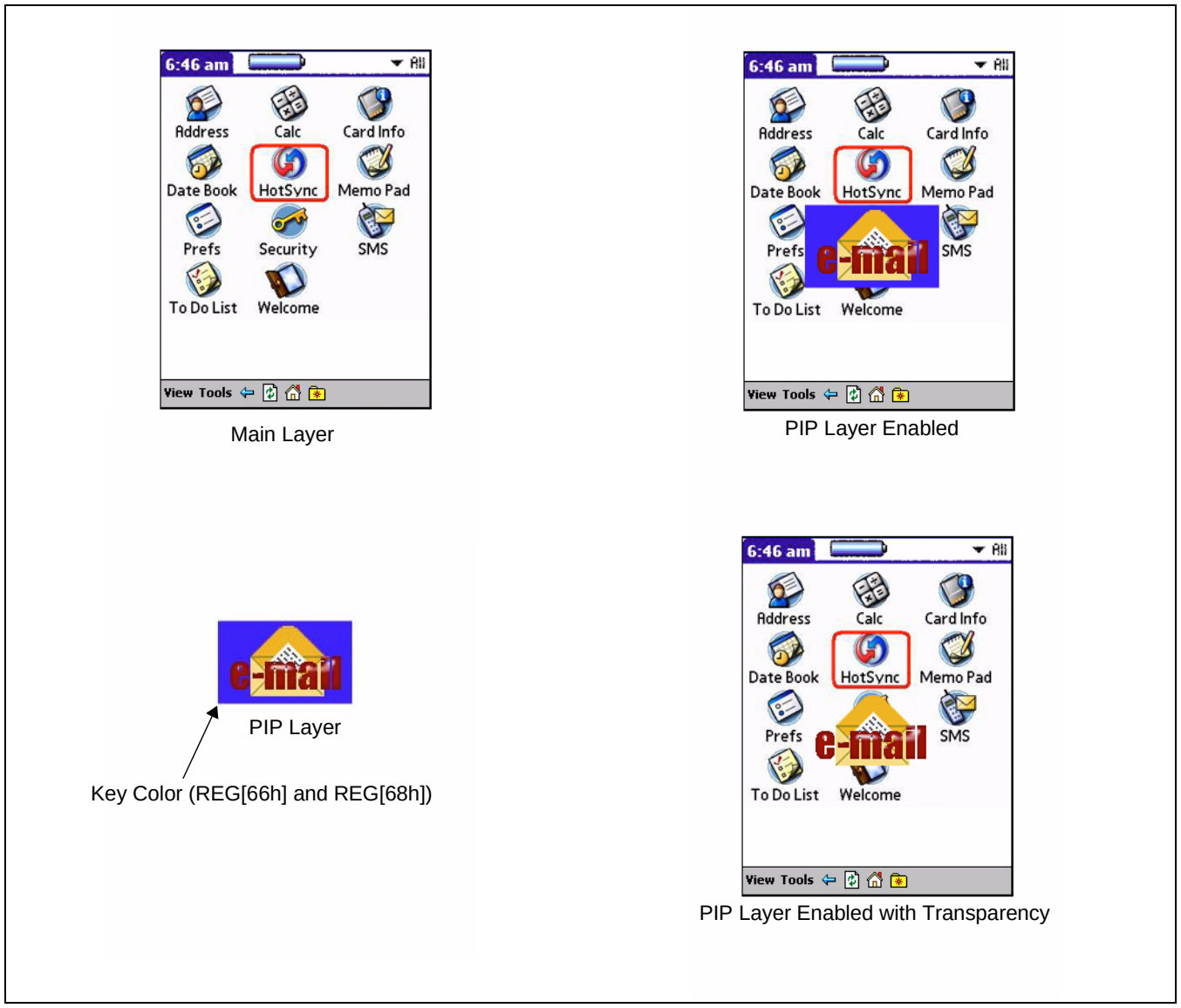


Figure 14-2: Transparency

14.3 Alpha Blending

Alpha Blending ratio is defined by REG[62h] bits 6-0. Alpha Blending can be used with Transparency. Alpha Blending does not affect Key Color.

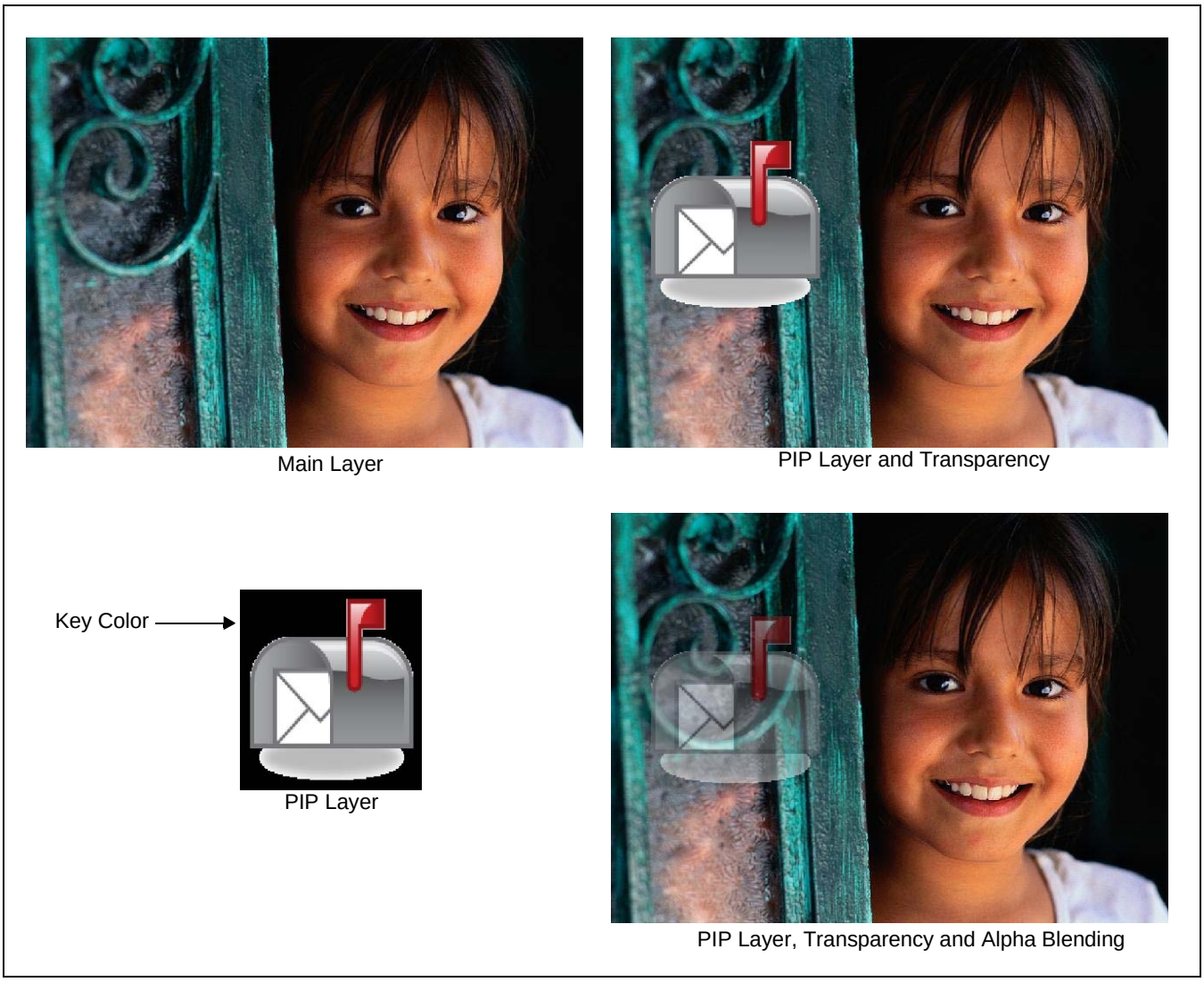


Figure 14-3: PIP Layer Alpha Blending

14.4 PIP Effects

PIP Effect is defined by REG[60h] bits 2-0. PIP Effect settings include Blank (PIP is off), Normal (PIP is solid on), Blink1, Blink2, Fade Out, Fade In, Fade In/Out Continuous. See the following figures for details on blink and fade PIP effects. PIP effects can be used with Transparency.

14.4.1 Blinking and Fading Effects

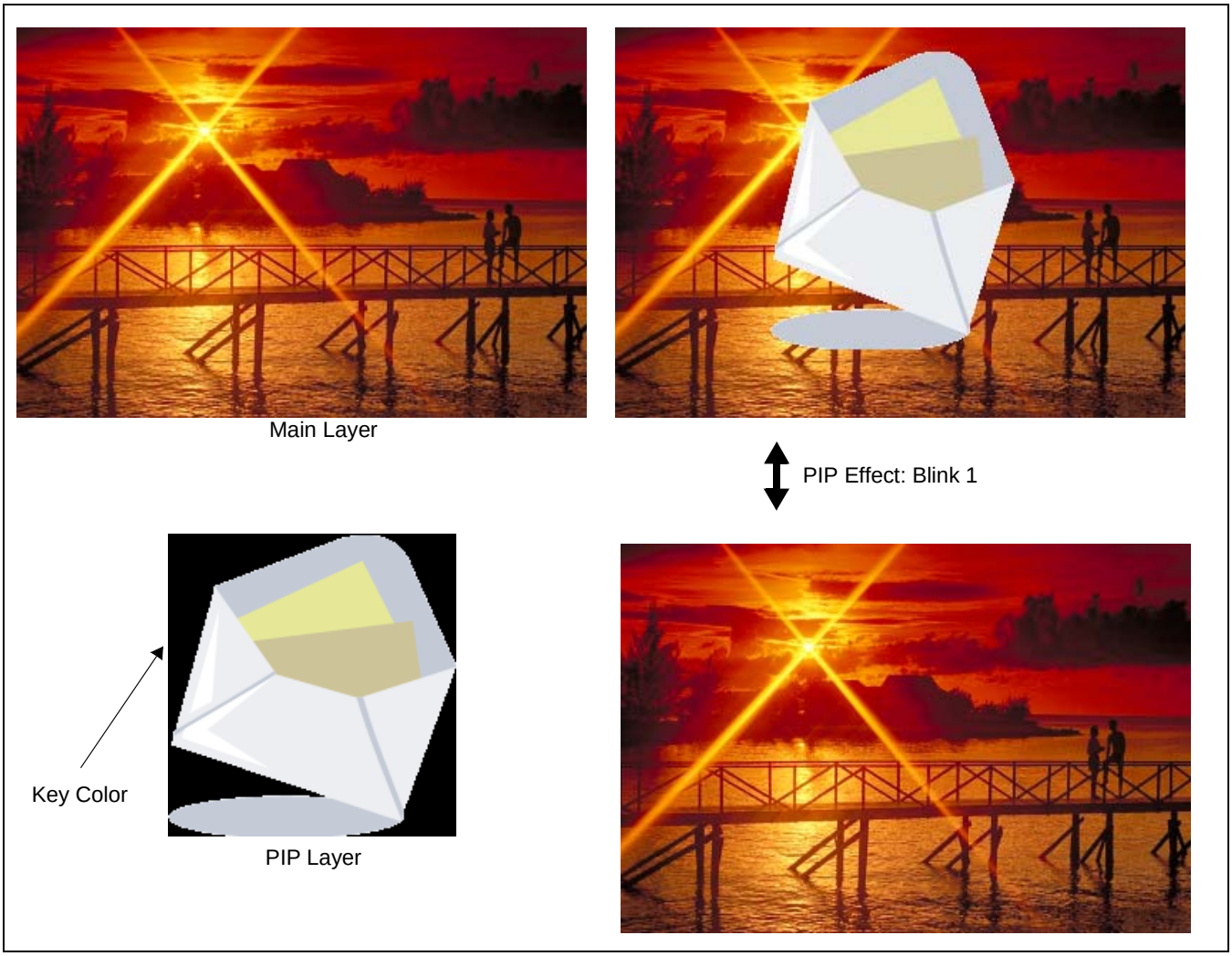


Figure 14-4: PIP Effect: Blink 1

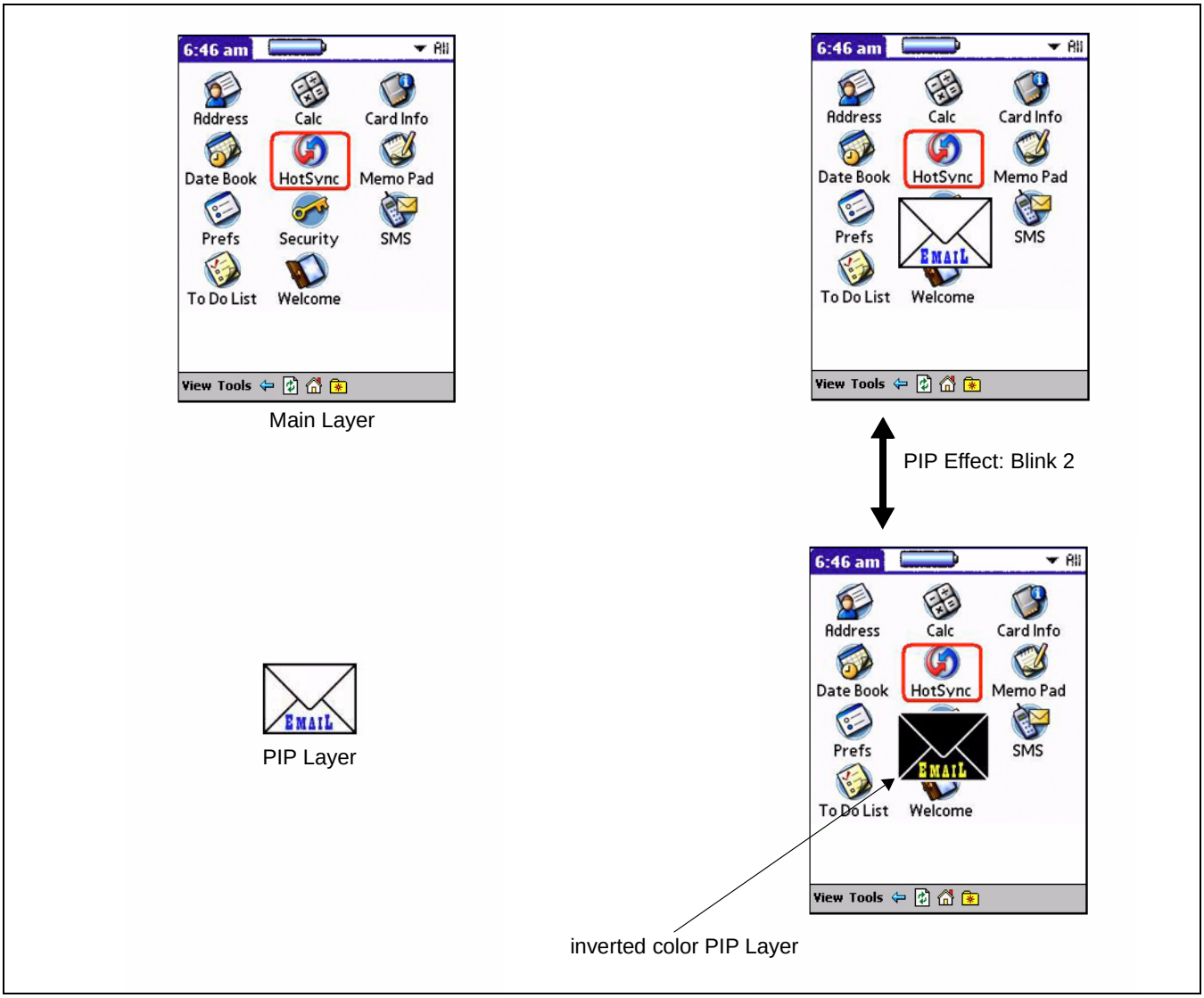


Figure 14-5: PIP Effect: Blink 2

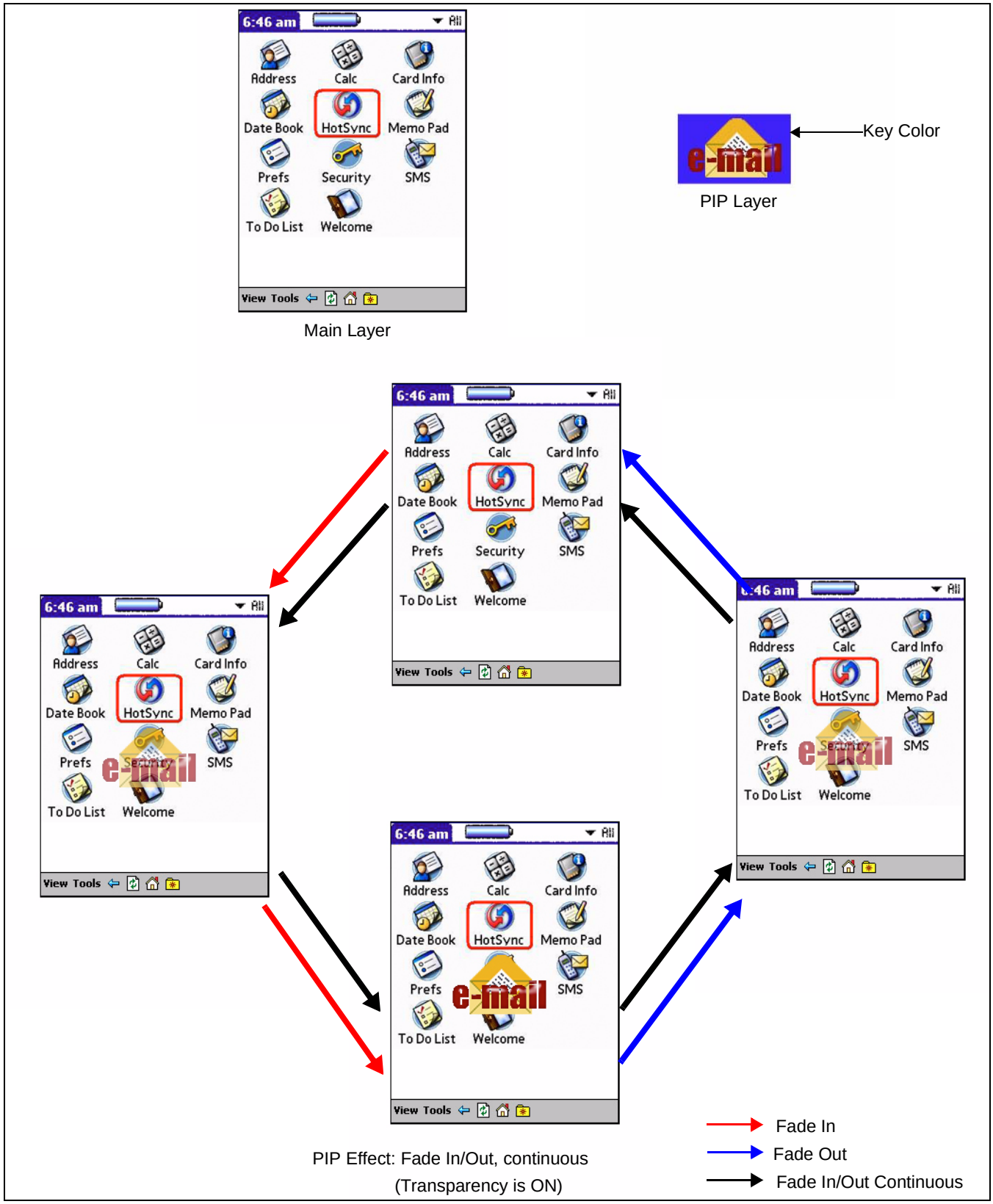


Figure 14-6: PIP Effects: Fade In, Fade Out, Fade In/Out Continuous

14.4.2 Blink/Fade Period

The blink/fade period is defined by REG[60h] bits 15-9 as follows.

$$\text{Blink/Fade Period (frames)} = (\text{REG[60h] bits 15-9}) + 1$$

For PIP Effects Blink1 and Blink2, the blinking period is specified by these bits.

For PIP Effects Fade Out, Fade In, and Fade In/Out Continuous, the period between each alpha-blend value increment/decrement is specified by these bits. During blinking or fading, the Blink/Fade Period can be dynamically changed to speed up or slow down the blinking/fading.

14.4.3 Fade Steps

For fading effects, the alpha-blend value to increment/decrement for each Blink/Fade Period is specified by REG[62h] Alpha Blending Register bits 9-8 Alpha Blending Step bits.

The alpha-blend value can be incremented/decremented in steps of +/-1, +/-2, +/-4, or +/-8.

During fading, the Alpha Blending Step bits can be dynamically changed to speed up or slow down the fading.

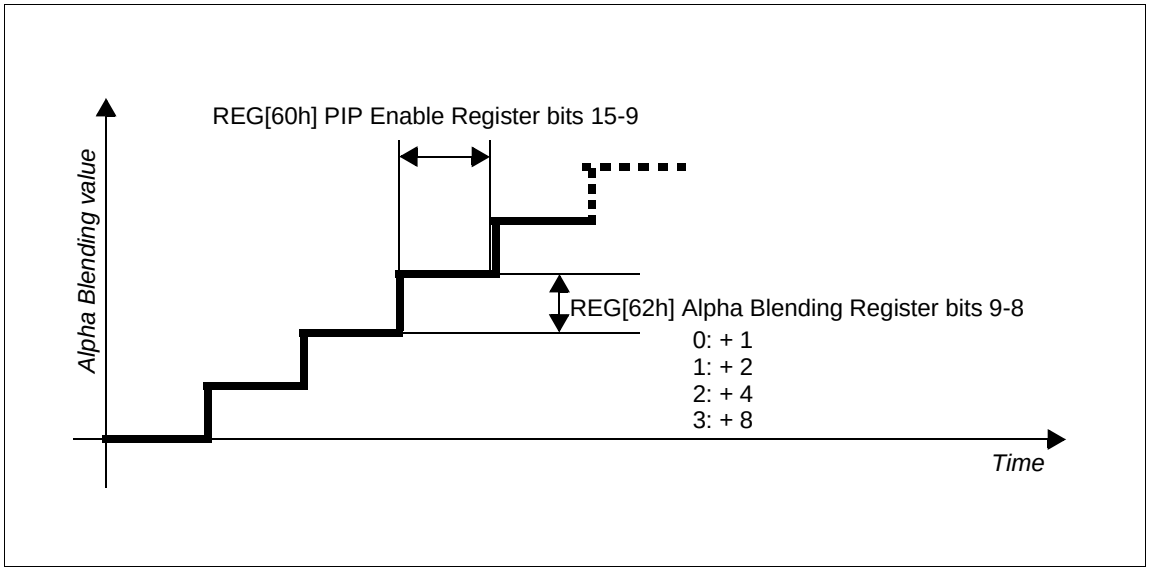


Figure 14-7: Example of Fade-In Steps

14.4.4 PIP Effect State Transitions

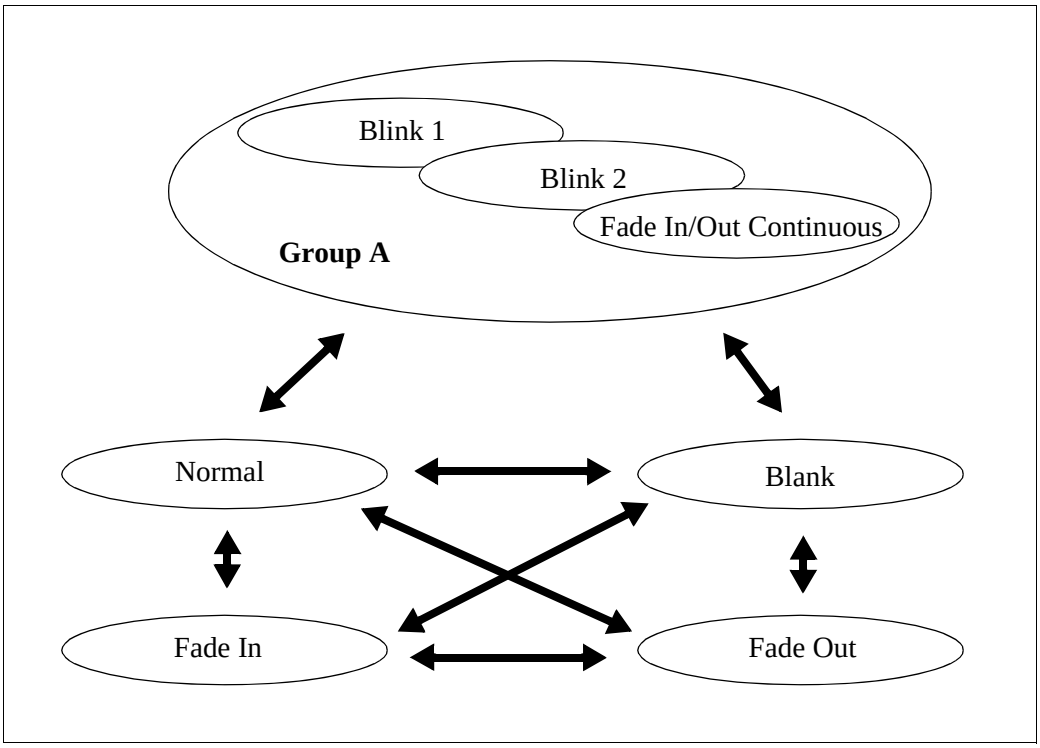


Figure 14-8: PIP Effect State Transition Diagram

From Normal or Blank state, the PIP Effect can be set to all the other states.

To stop Blink1, Blink2, or Fade In/Out Continuous (Group A states), the PIP Effect bits should be programmed to Normal or Blank. The Blink/Fade Status bit in REG[60h] bit 3 indicates if the PIP Layer is busy blinking or fading in/out. In the Group A states, the Blink/Fade Status bit is always 1. When the PIP Effect is set to Normal or Blank from the Group A states, the Blink/Fade Status bit should be checked to determine when the PIP Layer has finished blinking or fading.

When the PIP Effect is set to Fade In from Normal or Blank state, the PIP Layer will start fade-in with alpha blend value of 0 and stops at alpha blend value specified by the Alpha Blending Register (REG[62h] bits 6-0). During fade-in, the Blink/Fade Status bit is 1. It goes to 0 when fade-in is finished. To perform another fade-in, the PIP Effect bits should be programmed to Normal or Blank and then back to Fade In.

When the PIP Effect is set to Fade Out from Normal or Blank state, the PIP Layer will start fade-out with alpha blend value specified by the Alpha Blending Register (REG[62h] bits 6-0) and stop at alpha-blend value of 0. During fade-out, the Blink/Fade Status bit is 1. It goes to 0 when fade-out is finished. To perform another fade-out, the PIP Effect bits should be programmed to Normal or Blank and then back to Fade Out.

14.5 Rotation

Both the Main and PIP layers can be rotated independent of each other.

14.5.1 Location Address

Location is defined from panel origin (top left corner of panel) to PIP Layer Origin (top left corner of PIP layer), in 1 pixel and 1 line resolution.

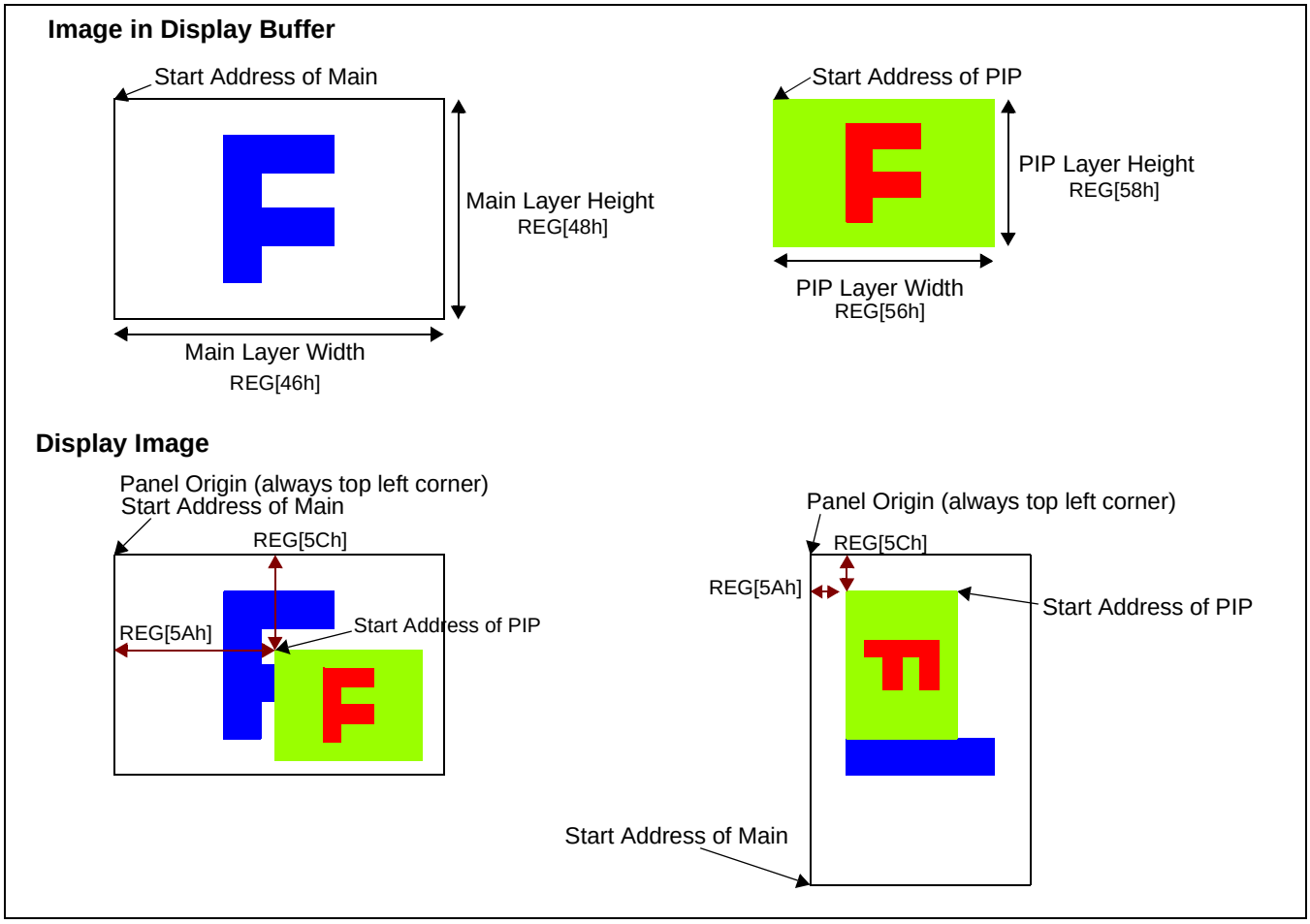


Figure 14-9: Relationship Between Layer Location Address and Rotation Layer

14.5.2 Start Address

For both the Main and PIP layer, the start address of the embedded RAM must be defined by REG[42h] ~ REG[44h] and REG[52h] ~ REG[54h]. All of the above registers must be 32-bit aligned. This means the two least significant bits must always be 00b.

14.6 Operating Modes

The following operating modes are possible for the S1D13L01.

Table 14-1: Operating Modes Summary

Operating Mode	Registers Accessible?	Memory Accessible? (MCLK active)	Panel I/F Clock Acitve? (PCLK active)
NMM - Panel Enabled	Yes	Yes	Yes
NMM Panel Disabled	Yes	Yes	Yes
PSM1	Yes	Yes	No
PSM0 (see Note)	Yes	No	No

Note
Do not access memory or LUT1/2 during PSM0.

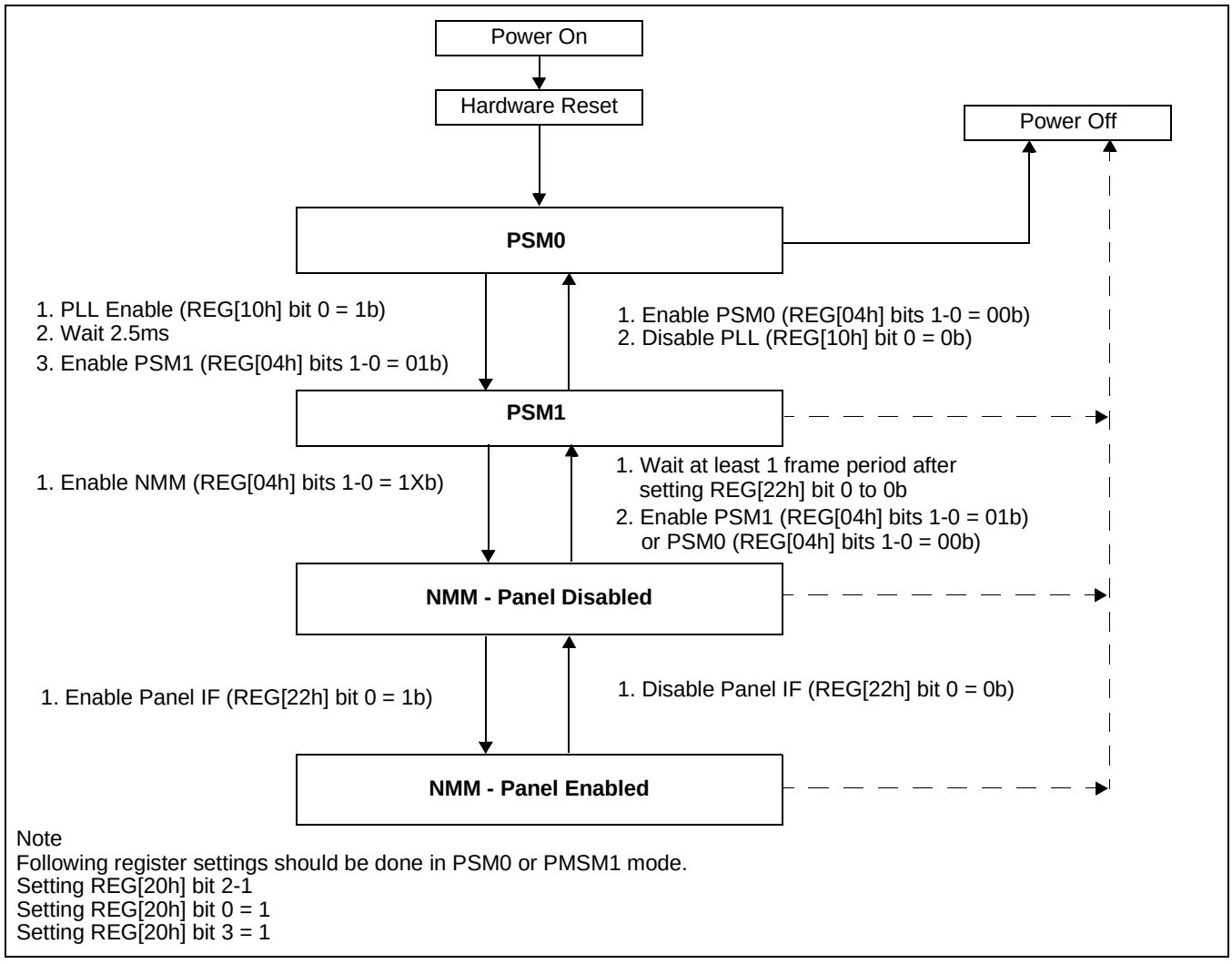
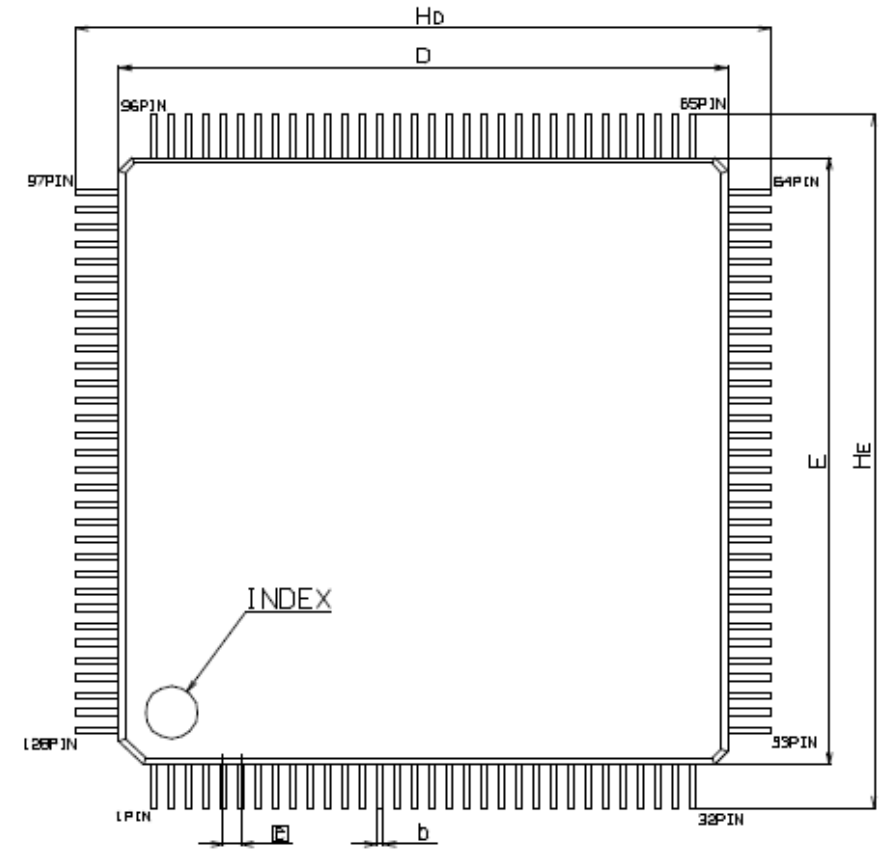


Figure 14-10: Switching Between Operating Modes

Chapter 15 Mechanical Data



Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	-	14	-
D	-	14	-
A_{max}	-	-	1.7
A_1	-	0.1	-
A_2	-	1.4	-
e	-	0.4	-
b	0.13	-	0.23
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.75
L_1	-	1	-
HE	-	16	-
HD	-	16	-
y	-	-	0.08

l = 1mm

Figure 15-1: Mechanical Data QFP15 128pin

Chapter 16 Change Record

XA9A-A-001-01 Revision 1.2- Issued: January 21, 2015

- chapter 14.6 Operating Modes updated Figure 14-10 .

XA9A-A-001-01 Revision 1.1 - Issued: June 20, 2014

- chapter 8.2 Operating Tempreatures updated Table 8-2 for operating temperature for S1D13L01F01.

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