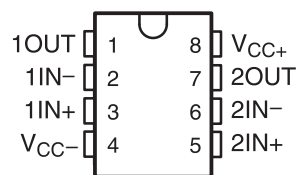
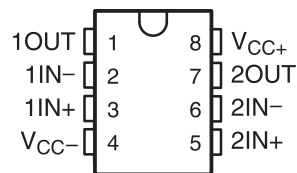


DUAL AUDIO OPERATIONAL AMPLIFIER

 Check for Samples: [RC4580-Q1](#)

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C3B
- Operating Voltage . . . $\pm 2\text{ V}$ to $\pm 18\text{ V}$
- Low Noise Voltage . . . $0.8\ \mu\text{Vrms}$ (TYP)
- Wide GBW . . . 12 MHz (TYP)
- Low THD . . . 0.0005% (TYP)
- Slew Rate . . . $5\text{ V}/\mu\text{s}$ (TYP)
- Suitable for Automotive Applications Such As Audio Preamp, Active Filter, Headphone Amplifier, Industrial Measurement Equipment
- Drop-In Replacement for NJM4580
- Pin and Function Compatible With LM833, NE5532, NJM4558/9, and NJM4560/2/5

**D PACKAGE
SOIC – 8
(TOP VIEW)**

**PW PACKAGE
TSSOP – 8
(TOP VIEW)**


DESCRIPTION

The RC4580-Q1 device is a dual operational amplifier that is designed optimally for audio applications, such as improving tone control. It offers low noise, high gain bandwidth, low harmonic distortion, and high output current. All of these features make the device ideally suited for audio electronics, such as audio preamplifiers and active filters, as well as industrial measurement equipment. When high output current is required, the RC4580-Q1 device can be used as a headphone amplifier. Due to its wide operating supply voltage, the RC4580-Q1 device can also be used in low-voltage applications.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2000	RC4580QDRQ1	R4580Q
-40°C to 125°C	TSSOP - PW	Reel of 2000	RC4580QPWRQ1	R4580Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



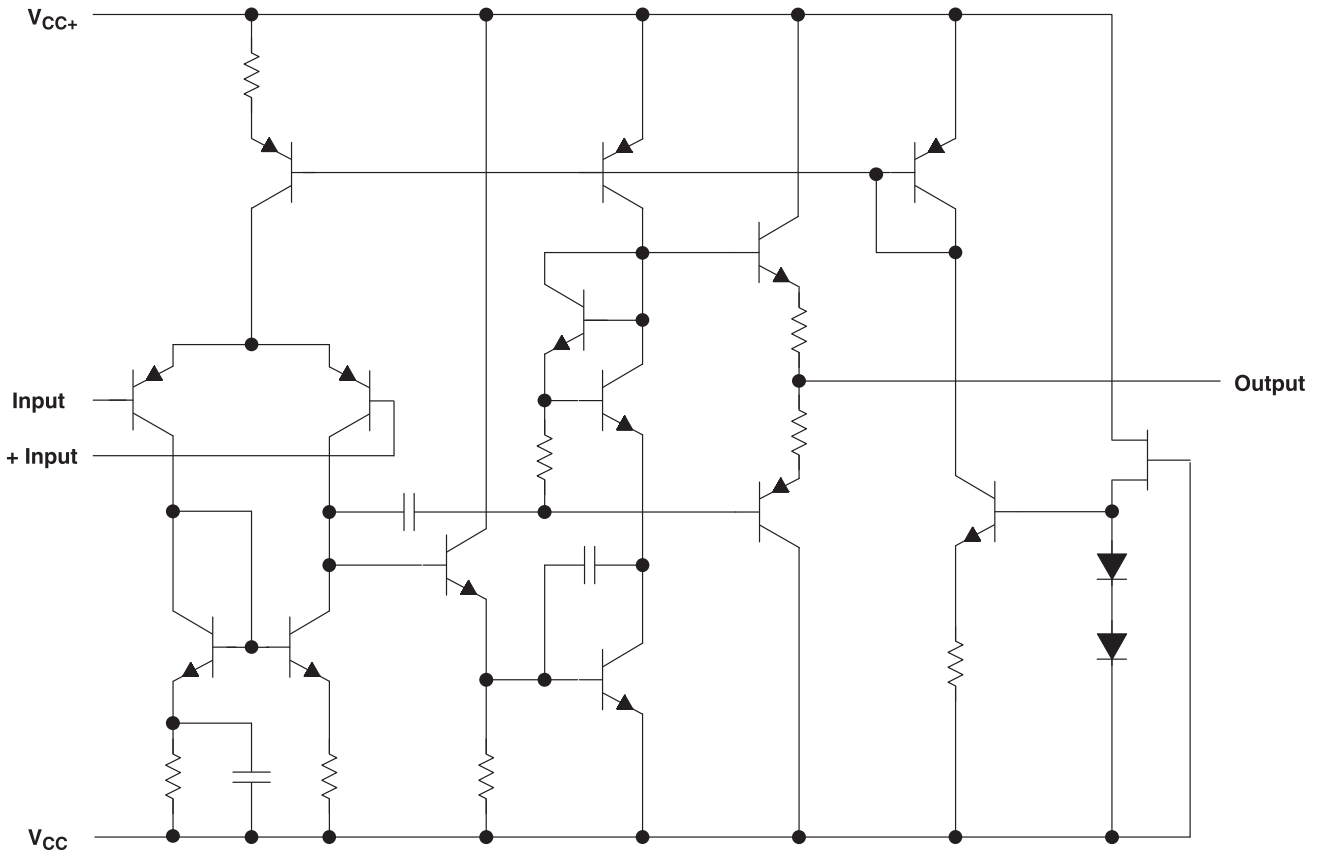
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Figure 1. EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		±18	V
	Input voltage (any input)		±15	V
V_{ID}	Differential input voltage		±30	V
	Output current		±50	mA
T_A	Ambient temperature range	-40	125	°C
T_{stg}	Storage temperature range	-60	125	°C
Electrostatic Discharge (ESD) Ratings	Human-body model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		RC4580-Q1		UNIT
		D (8 PINS)	PW (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	109	163	°C/W
θ_{Jctop}	Junction-to-case (top) thermal resistance	55.7	38	
θ_{JB}	Junction-to-board thermal resistance	49	90.6	
ψ_{JT}	Junction-to-top characterization parameter	10.6	1.3	
ψ_{JB}	Junction-to-board characterization parameter	48.6	88.9	
θ_{Jcbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	2	16	V
V_{CC-}		-2	-16	
V_{ICR}	Input common-mode voltage range	-13.5	13.5	V
T_A	Operating free-air temperature	-40	125	°C

ELECTRICAL CHARACTERISTICS

$V_{CC\pm} = \pm 15\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S = < 10\text{ k}\Omega$		0.5	3	mV
I_{IO}	Input offset current			5	200	nA
I_{IB}	Input bias current			100	500	nA
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	90	110		dB
V_{CM}	Output voltage swing	$R_L \geq 2\text{ k}\Omega$	± 12	± 13.5		V
V_{ICR}	Common-mode input voltage		± 12	± 13.5		V
CMRR	Common-mode rejection ratio	$R_S \leq 10\text{ k}\Omega$	80	110		dB
k_{SVR}	Supply-voltage rejection ratio ⁽¹⁾	$R_S \leq 10\text{ k}\Omega$	80	110		dB
I_{CC}	Total supply current (all amplifiers)			6	9	mA

(1) Measured with $V_{CC\pm}$ varied simultaneously

OPERATING CHARACTERISTICS

$V_{CC\pm} = \pm 15\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L \geq 2\text{ k}\Omega$	5	V/ μs
GBW	Gain-bandwidth product	$f = 10\text{ kHz}$	12	MHz
THD	Total harmonic distortion	$V_O = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_{VD} = 20\text{ dB}$	0.0005%	
V_n	Equivalent input noise voltage	RIAA, $R_S \leq 2.2\text{ k}\Omega$, 30-kHz LPF	0.8	μVrms

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

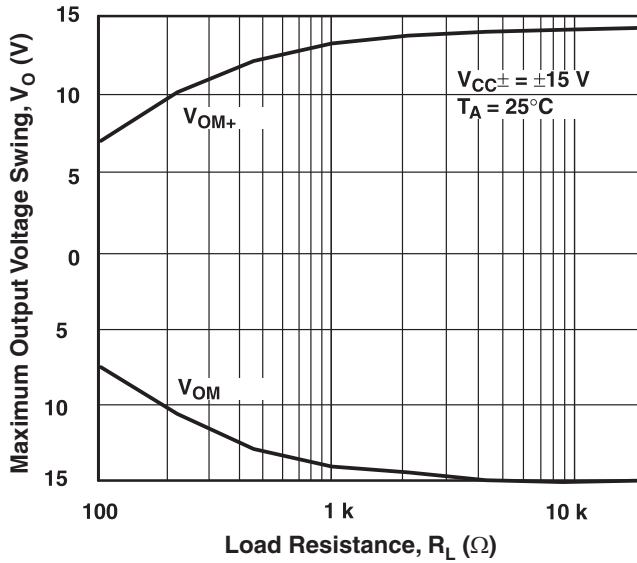


Figure 2.

MAXIMUM OUTPUT VOLTAGE SWING
vs
FREQUENCY

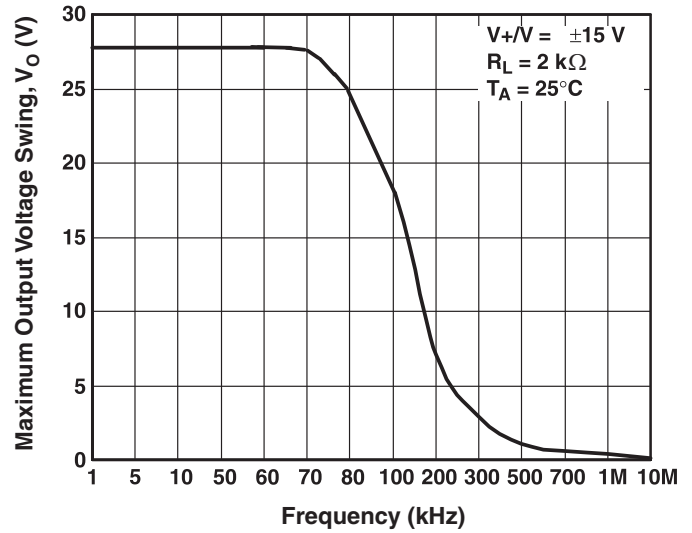


Figure 3.

OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

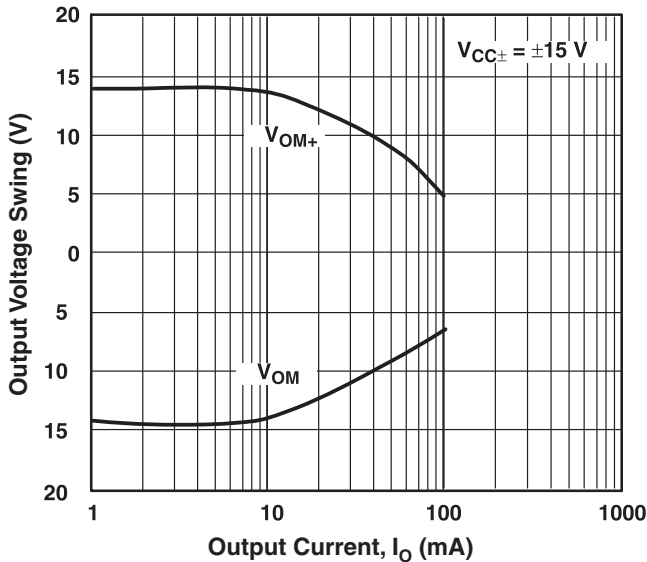


Figure 4.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

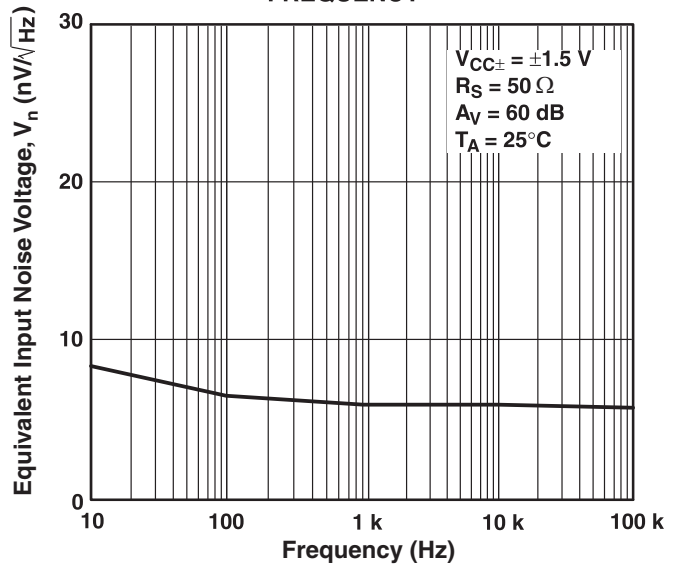


Figure 5.

TYPICAL CHARACTERISTICS (continued)

OPERATING CURRENT
vs
TEMPERATURE

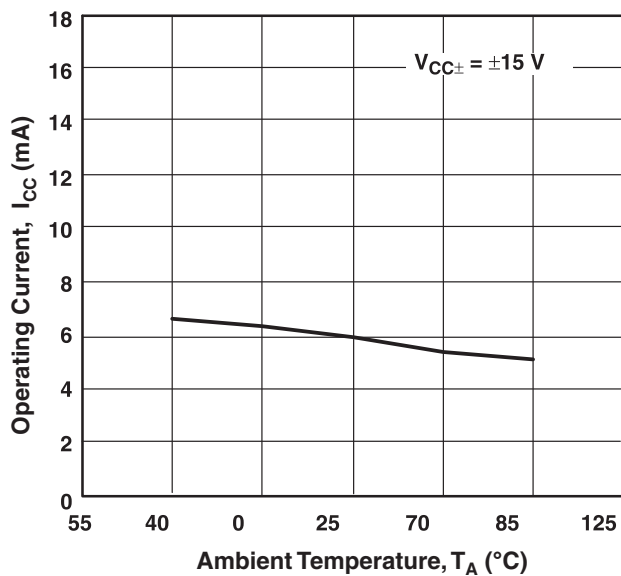


Figure 6.

OUTPUT VOLTAGE SWING
vs
TEMPERATURE

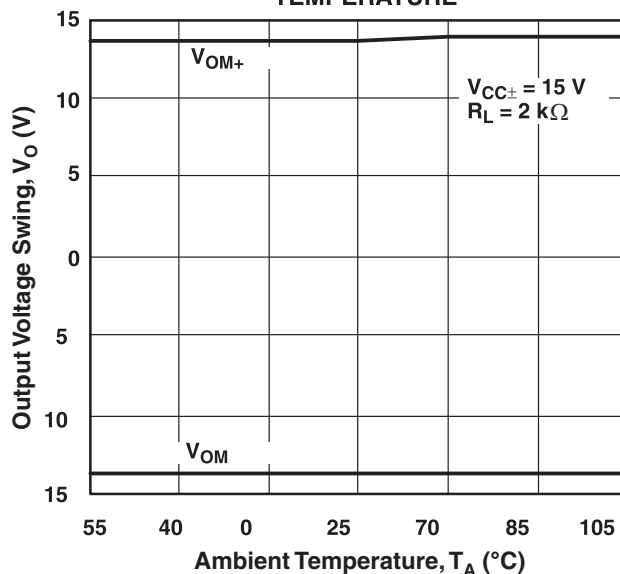


Figure 7.

INPUT OFFSET VOLTAGE
vs
TEMPERATURE

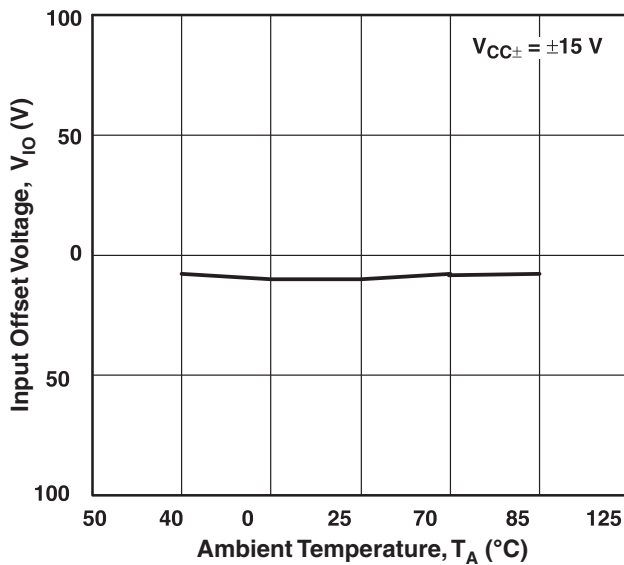


Figure 8.

INPUT BIAS CURRENT
vs
TEMPERATURE

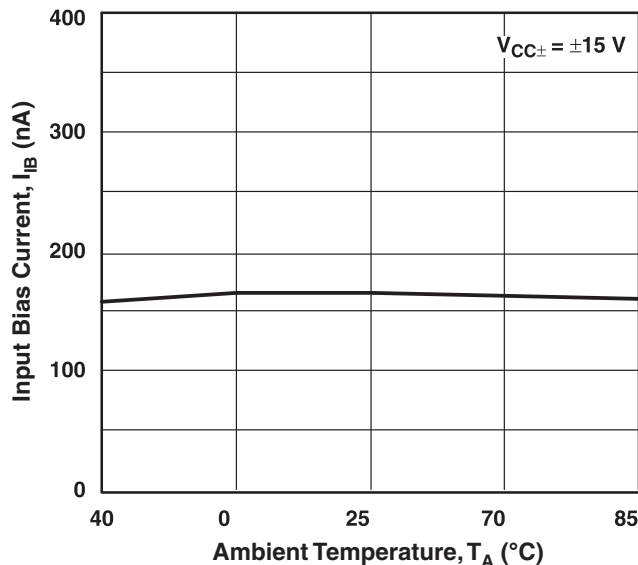


Figure 9.

TYPICAL CHARACTERISTICS (continued)

**MAXIMUM OUTPUT VOLTAGE SWING
vs
OPERATING VOLTAGE**

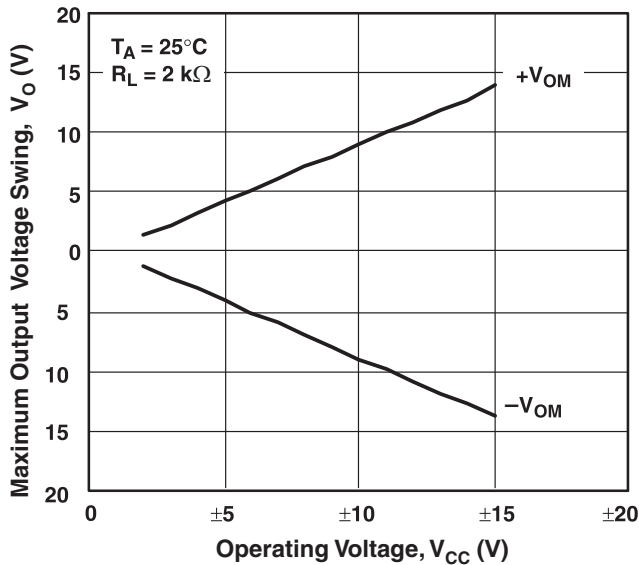


Figure 10.

**OPERATING CURRENT
vs
OPERATING VOLTAGE**

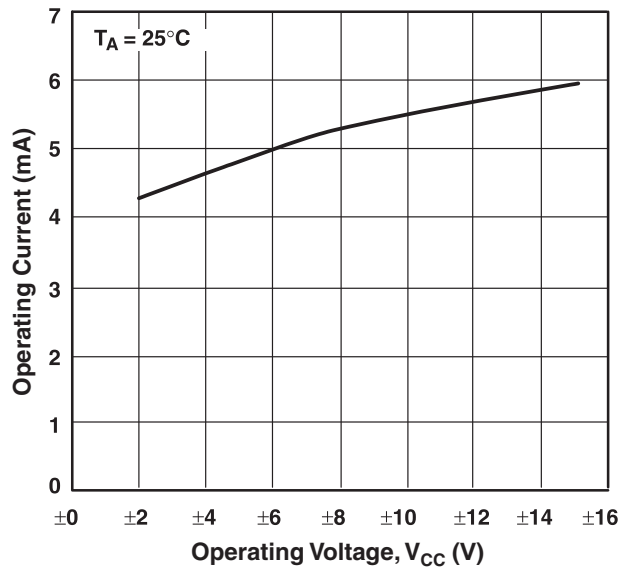


Figure 11.

**TOTAL HARMONIC DISTORTION
vs
OUTPUT VOLTAGE**

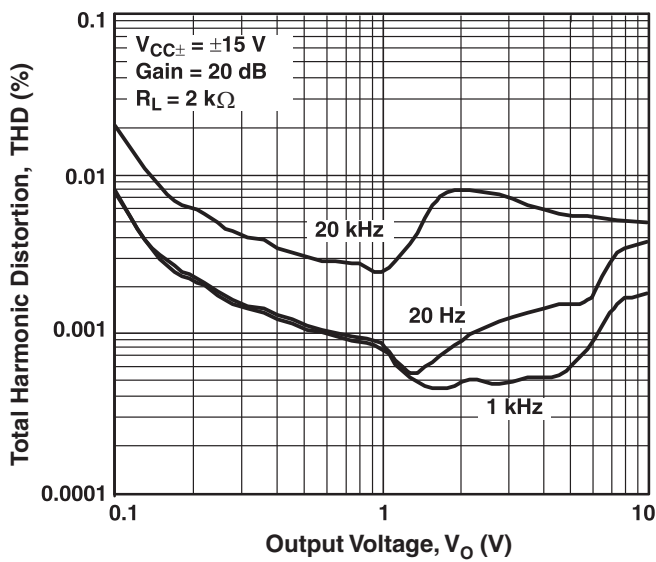


Figure 12.

**VOLTAGE GAIN, PHASE
vs
FREQUENCY**

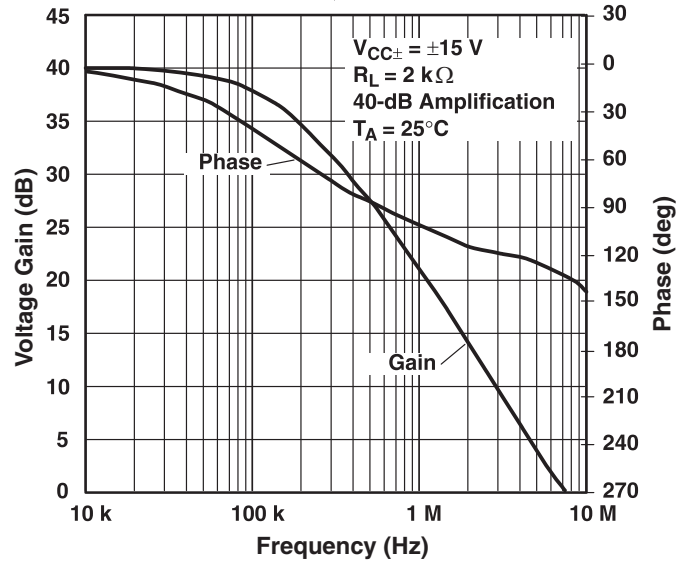


Figure 13.

REVISION HISTORY

Changes from Original (December 2010) to Revision A	Page
• Added AEC-Q100 info to the features; changed Suitable for Applications to Suitable for Automotive Applications	1
• Added PW pinout drawing	1
• Added second row for PW package to Ordering Information table	1
• Added ESDS	2
• Changed T_J to T_A	2
• Removed θ_{JA} row from Abs Max table because it is also listed in the thermal table	2
• Added ESD ratings to Abs Max table	2
• Added thermal table	3
• Changed $T_A = 25^\circ\text{C}$ to $T_A = -40^\circ\text{C}$ to 125°C in condition statement for Elec Char table and Op Char table	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4580QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580Q	Samples
RC4580QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF RC4580-Q1 :

- Catalog: [RC4580](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4580QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4580QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
RC4580QPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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