

A large, stylized '65xx' logo in red with a blue oval background, centered on the page.

65xx

**W65C21
(W65C21N and W65C21S)
Peripheral Interface Adapter (PIA)**



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INTRODUCTION

The WDC W65C21 (W65C21N and W65C21S) is a very flexible Peripheral Interface Adapter (PIA) for use with WDC's 65xx, 68xx, and other 8-bit microprocessor families. The W65C21 provides programmed microprocessor control of up to two peripheral devices (Port A and Port B). Peripheral device control is accomplished through two 8-bit bidirectional I/O Ports, with individually designed Data Direction Registers. The Data Direction Registers provide selection of data flow direction (input or output) at each respective I/O Port. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. The "handshake" interrupt control feature is provided by four peripheral control lines. This capability provides enhances control over data transfer functions between the microprocessor and peripheral devices, as well as bidirectional data transfer between W65C21 Peripheral Interface Adapters in multiprocessor systems.

FEATURES

- Low Power CMOS N-well silicon gate technology
- The W65C21N is plug replacement of NMOS and CMOS 6521 and 6821 devices with current limiting resistors
- The W65C21S is lower power, faster and direct drive outputs with no current limiting resistors.
- High speed/Low power replacement for Motorola/Rockwell/AMI/MOS Technology/MOSTEK/HITACHI/ ST Microelectronics/GTE/CMD 6520, 6521, 6820, 6821 PIA's
- Two 8-bit bidirectional I/O ports with individual data direction control.
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- Static to 14MHz operation, with high speed Port A, CA2 outputs.
- Industrial temperature range
- 40 Pin Plastic DIP and 44 Pin Plastic PLCC versions
- 5 volt \pm 10% supply requirements
- Compatible with the 65xx and 68xx family of microprocessors

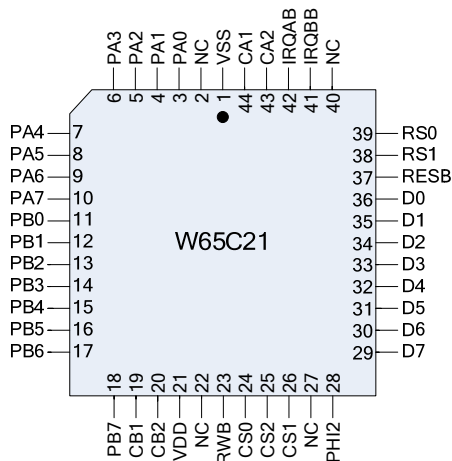


Figure 1 44 Pin PLCC Pin Configuration

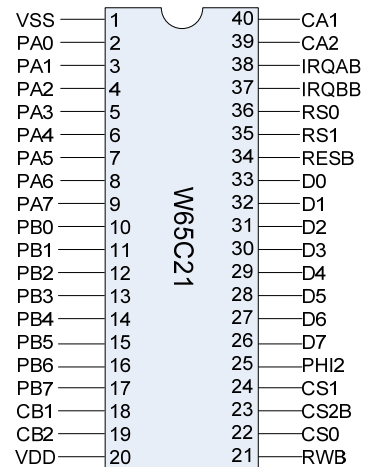


Figure 2 40 Pin DIP Pin Configuration

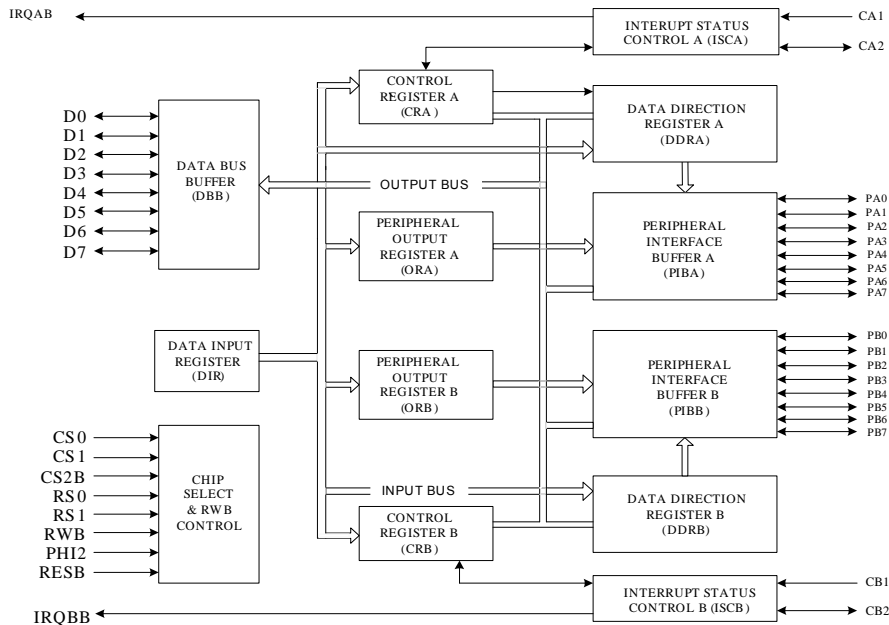


Figure 3 W65C21 PIA Block Diagram

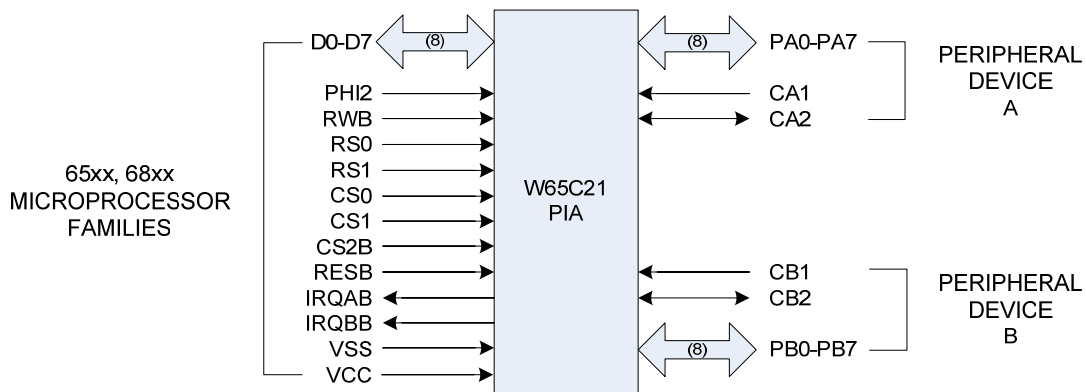


Figure 4 Interface Signals Relationship



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V _{DD}	-0.3 to +7.0	Vdc
Input Voltage	V _{IN}	-0.3 to V _{DD} +0.3	Vdc
Output Voltage	V _{OUT}	-0.3 to V _{DD} +0.3	Vdc
Operating Temp. Range - Industrial	T _A	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage; functional operation under these conditions is not implied.



W65C21N DC CHARACTERISTICS ($V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Min ²	Typ. ^{2,3}	Max ²	Unit ¹	Test Conditions
Input High Voltage	V_{IH}	2.0	3.0	$V_{DD} + 0.3$	V	$V_{DD} = 4.5V/5.5V$
Input Low Voltage	V_{IL}	-0.3	0.2	0.8	V	$V_{DD} = 4.5V/5.5V$
Input Leakage Current CA1, CB1, CS0, CS1, CS2B, RESB, RS0, RS1, RWB, PHI2	I_{IN}	-100	$<\pm 10.0$	100	nA	$V_{IN} = .4V$ to $2.4V$, $V_{DD} = 5.5V$
Three-State (Off State), Leakage Current D0-D7, PB0-PB7, CB2	I_{TSI}	-100	$<\pm 10.0$	100	nA	$V_{IN} = 0.4V$ to $2.4V$, $V_{DD} = 5.5V$
Input High Current PA0-PA7, CA2	I_{IH}	-600	-400	-200	μA	$V_{IH} = 2.4V$, $V_{DD} = 4.5V$
Input Low Current PA0-PA7, CA2	I_{IL}	-1.6	-0.9	-0.4	mA	$V_{IL} = 0.4V$, $V_{DD} = 5.5V$
Output High Voltage D0-D7, PA0-PA7, CA2, PB0-PB7, CB2	V_{OH}	2.4	--	--	V	$I_{OH} = -200\mu A$, $V_{DD} = 4.5V$
Output Low Voltage D0-D7, IRQAB, IRQBB, PA0-PA7, CA2, PB0- PB7, CB2	V_{OL}	--	--	0.4	V	$I_{OL} = 3.2mA$, $V_{DD} = 4.5V$
Output High Current (Sourcing) PA0-PA7, CA2	I_{OH}	-600	-400	-200	μA	$V_{OH} = 2.4V$, $V_{DD} = 4.5V$
Output High Current (Sourcing) PB0-PB7, CB2	I_{OH}	-20.0	-6.0	-3.2	mA	$V_{OH} = 1.5V$, $V_{DD} = 4.5V$
Output High Current (Sourcing) D0-D7	I_{OH}	-20.0	-10.0	-3.2	mA	$V_{OH} = V_{DD} - 0.4V$, $V_{DD} = 4.5V$
Output Low Current (Sinking) D0-D7, IRQAB, IRQBB, PA0-PA7, CA2, PB0-PB7, CB2	I_{OL}	3.2	12.0	20.0	mA	$V_{OL} = 0.4V$, $V_{DD} = 4.5V$
Output Leakage Current (Off State) IRQAB, IRQBB	I_{OFF}	-100	$<\pm 10.0$	100	nA	$V_{IN} = .4V$ to $2.4V$, $V_{DD} = 5.5V$
Power Dissipation	I_{DD}	--	100	500	μA	$V_{DD} = 5.5V$
Notes: 1. All units are direct current (DC) except for capacitance. 2. Negative sign indicates outward current flow, positive indicates inward flow. 3. Typical values are shown for 14MHz Test 4. All production test loads use test machine capacitance (~30pF) only. 5. Capacitance of all pins is estimated 5.0pF at a 1MHz sample.						



W65C21S DC CHARACTERISTICS ($V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Min ²	Typ. ^{2,3}	Max ²	Unit ¹	Test Conditions
Input High Voltage	V_{IH}	2.0	3.0	$V_{DD} + 0.3$	V	$V_{DD} = 4.5V/5.5V$
Input Low Voltage	V_{IL}	-0.3	0.2	0.8	V	$V_{DD} = 4.5V/5.5V$
Input Leakage Current CA1, CB1, CS0, CS1, CS2B, RESB, RS0, RS1, RWB, PHI2	I_{IN}	-100	$<\pm 10.0$	100	nA	$V_{IN} = .4V$ to $2.4V$, $V_{DD} = 5.5V$
Three-State (Off State), Leakage Current D0-D7, PB0-PB7, CB2	I_{TSL}	-100	$<\pm 10.0$	100	nA	$V_{IN} = 0.4V$ to $2.4V$, $V_{DD} = 5.5V$
Input High Current PA0-PA7, CA2	I_{IH}	-200	-110	-50.0	μA	$V_{IH} = 2.4V$, $V_{DD} = 4.5V$
Input Low Current PA0-PA7, CA2	I_{IL}	-400	-200	-100	mA	$V_{IL} = 0.4V$, $V_{DD} = 5.5V$
Output High Voltage D0-D7, PA0-PA7, CA2, PB0-PB7, CB2	V_{OH}	2.4	--	--	V	$I_{OH} = -200\mu A$, $V_{DD} = 4.5V$
Output Low Voltage D0-D7, IRQAB, IRQBB, PA0-PA7, CA2, PB0-PB7, CB2	V_{OL}	--	--	0.4	V	$I_{OL} = 3.2mA$, $V_{DD} = 4.5V$
Output High Current (Sourcing) PA0-PA7, CA2	I_{OH}	-8.0	-3.0	-1.6	mA	$V_{OH} = V_{DD} - 0.4V$, $V_{DD} = 4.5V$
Output High Current (Sourcing) PB0-PB7	I_{OH}	-8.0	-3.0	-1.6	mA	$V_{OH} = V_{DD} - 0.4V$, $V_{DD} = 4.5V$
Output High Current (Sourcing) D0-D7, CB2	I_{OH}	-20.0	-10.0	-3.2	mA	$V_{OH} = V_{DD} - 0.4V$, $V_{DD} = 4.5V$
Output Low Current (Sinking) D0-D7, IRQAB, IRQBB, PA0-PA7, CA2, PB0-PB7, CB2	I_{OL}	3.2	12.0	20.0	mA	$V_{OL} = 0.4V$, $V_{DD} = 4.5V$
Output Leakage Current (Off State) IRQAB, IRQBB	I_{OFF}	-100	$<\pm 10.0$	100	nA	$V_{IN} = .4V$ to $2.4V$, $V_{DD} = 5.5V$
Power Dissipation	I_{DD}	--	100	500	μA	$V_{DD} = 5.5V$
Notes: 1. All units are direct current (DC) except for capacitance. 2. Negative sign indicates outward current flow, positive indicates inward flow. 3. Typical values are shown for $V_{DD} = 5.0V$ and $T_A = 25^{\circ}C$ 4. All production test loads use test machine capacitance (~30pF) only. 5. Capacitance of all pins is estimated 5.0pF at a 1MHz sample.						



AC TIMING CHARACTERISTICS

Parameter	Symbol	14 MHz @ 5V		Unit
		Min	Max	
PHI2 Cycle	t _{CYC}	70	-	ns
PHI2 Pulse Width	t _C	35	-	ns
PHI2 Rise and Fall Time	t _{rc} t _{fc}	-	5	ns

READ TIMING

Parameter	Symbol	14 MHz @ 5V		Unit
		Min	Max	
Address Set-Up Time	t _{ACR}	8	-	ns
Address Hold Time	t _{CAR}	0	-	ns
Peripheral Data Setup Time	t _{PCR}	10	-	ns
Data Bus Delay Time	t _{CDR}	-	20	ns
Data Bus Hold Time	t _{HR}	5	-	ns

WRITE TIMING

Parameter	Symbol	14 MHz @ 5V		Unit
		Min	Max	
Address Set-Up Time	t _{ACW}	8	-	ns
Address Hold Time	t _{CAW}	0	-	ns
Data Bus Set-Up Time	t _{DCW}	10	-	ns
Data Bus Hold Time	t _{HW}	5	-	ns
Peripheral Data Delay Time	t _{CPW}	-	20	ns

PERIPHERAL INTERFACE TIMING

Parameter	Symbol	14 MHz @ 5V		Unit
		Min	Max	
PHI2 Low to CA2 Low Delay	t _{CA2}	-	20	ns
PHI2 Low to CA2 High Delay	t _{RS1}	-	20	ns
CA1 Active to CA2 High Delay	t _{RS2}	-	25	ns
PHI2 High to CB2 Low Delay	t _{CB2}	-	70	ns
Peripheral Data Valid to CB2 Low Delay	t _{DC}	5	-	ns
PHI2 High to CB2 High Delay	t _{RS1}	-	20	ns
CB1 Active to CB2 High Delay	t _{RS2}	-	25	ns
CA1, CA1, CB1, and CB2 Input Rise and Fall Time	t _r , t _f	-	10	ns
Interrupt Input Pulse Width	P _{WI}	-	70	ns
Interrupt Response Time	t _{RS3}	-	20	ns
Interrupt Clear Delay	t _{IR}	-	25	ns

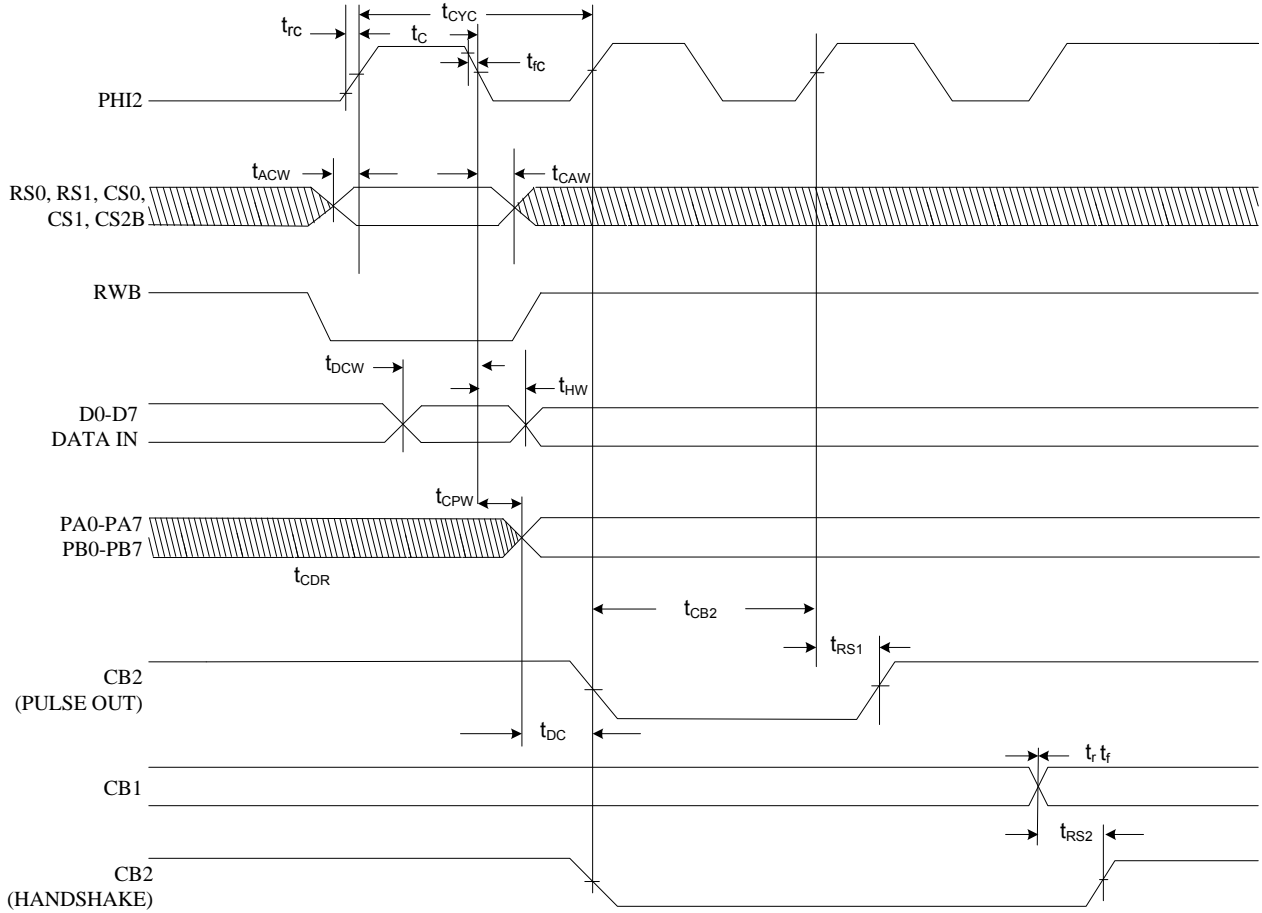


Figure 5 Write Timing Waveforms

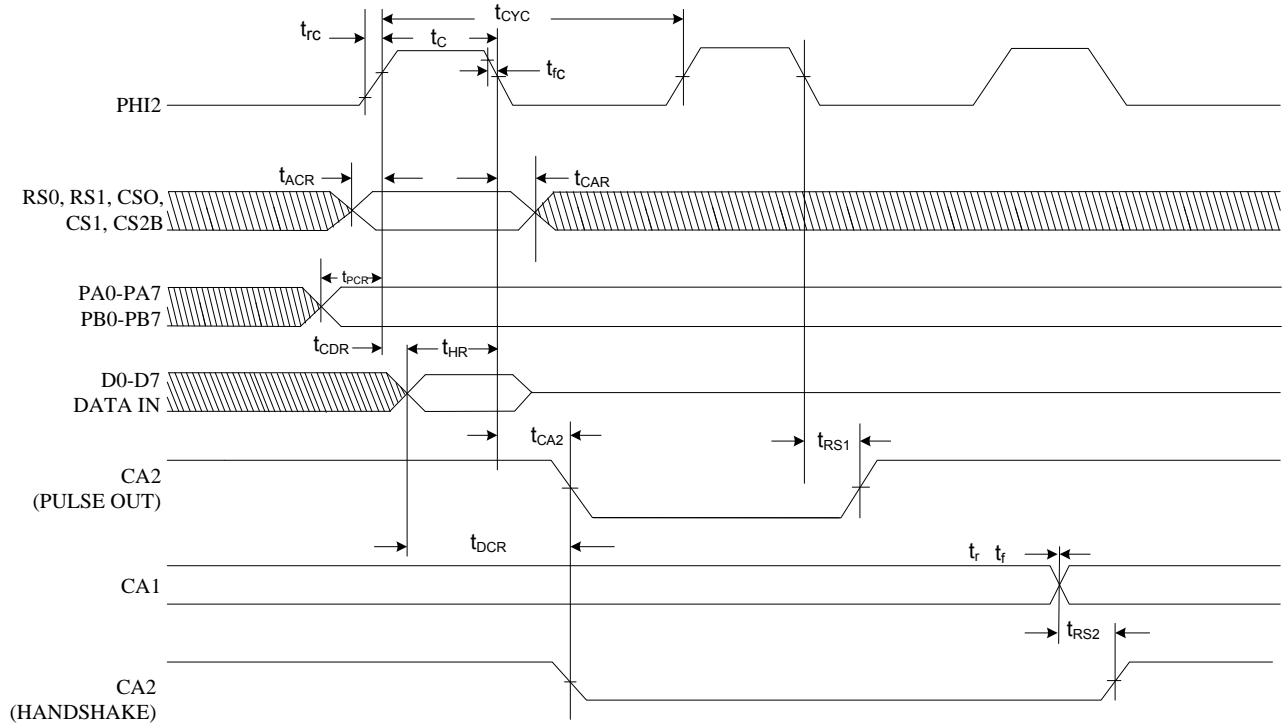


Figure 6 Read Timing Waveforms

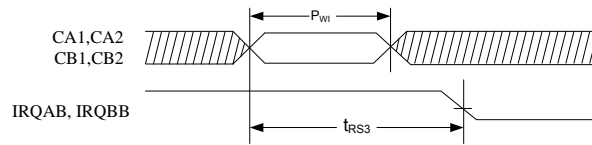


Figure 7 Interrupt Timing

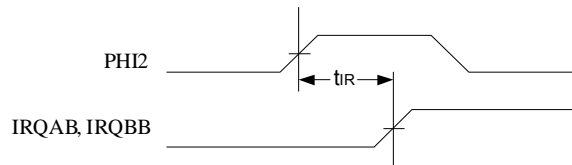


Figure 8 Interrupt Clear Timing



7	6	5	4	3	2	1	0
IRQA1	IRQA2	CA2 Control		DDRA Access		CA1 Control	

7	6	5	4	3	2	1	0
IRQB1	IRQB2	CB2 Control		DDRB Access		CB1 Control	

Table 1 Control Registers

REGISTER SELECT PIN		DATA DIRECTION REGISTER ACCESS CONTROL BIT		REGISTER SELECTED
RS1	RS0	CRA-2	CRB-2	
0	0	1	-	Peripheral Interface A
0	0	0	-	Data Direction Register A
0	1	-	-	Control Register A
1	0	-	1	Peripheral Interface B
1	0	-	0	Data Direction Register B
1	1	-	-	Control Register B

Table 2 Register Addressing

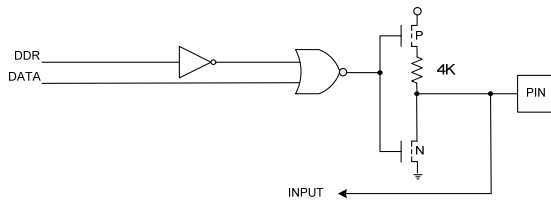


Figure 9A Port A, CA2 Buffers – W65C21N

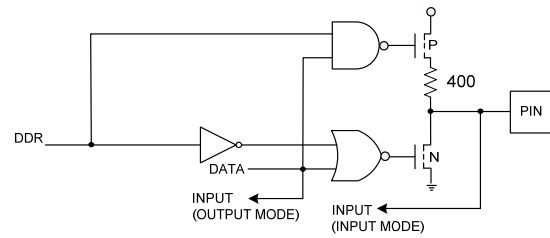


Figure 9B Port B, CB2 Buffers – W65C21N

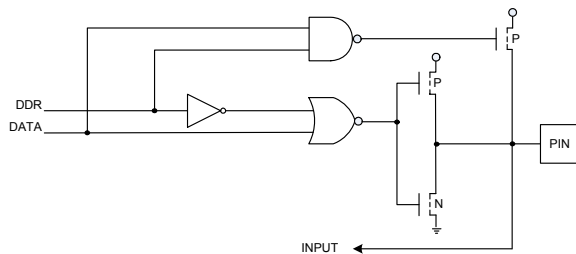


Figure 10A Port A, CA2 Buffers – W65C21S

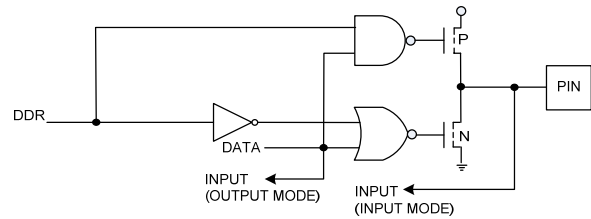


Figure 10B Port B, CB2 Buffers – W65C21S



SIGNAL DESCRIPTION

The PIA interfaces to the 65xx and 68xx microprocessor families with a reset line, a PHI2 clock line, a read/write line, two interrupt request lines, two register select lines, three chip select lines and an 8-bit bidirectional data bus. The PIA interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data buses. Figures 1 and 2 show the pin assignments for these interface signals and Figure 4 shows the interface relationship of these signals as they pertain to the CPU and the peripheral devices.

CHIP SELECT (CS0, CS1, CS2B)

The PIA is selected when CS0 and CS1 are high and CS2B is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIA is selected, data will be transferred between the data lines and PIA registers, and/or peripheral interface lines as determined by the RWB, RS0 and RS1 lines and the contents of Control Registers A and B.

CLOCK SIGNAL (PHI2)

The Phase 2 Clock Signal (PHI2) is the system clock that triggers all data transfers between the CPU and the PIA. PHI2 is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIA.

DATA BUS (D0-D7)

The eight bidirectional data bus lines are used to transfer data between the W65C21 and the microprocessor.

During a Read operation, the contents of the W65C21 internal Data Bus Buffer (DBB) are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines represent high impedance inputs over which data is transferred from the microprocessor to the Data Input Register (DIR). The Data Bus lines are in the high impedance state when the W65C21 is unselected.

INTERRUPT STATUS CONTROL – CA1, CA2 (Port A) and CB1, CB2 (Port B)

The two Interrupt Status Control lines for each Data Port are controlled by the Interrupt Status Control logic (A and B). This logic interprets the contents of the corresponding Control Register (CRA and CRB), allowing the Interrupt Status Control lines to perform various peripheral control functions.

PERIPHERAL DATA PORT A (PA0-PA7)

Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the W65C21 and a peripheral device. Each data port bus line may be individually programmed as either an input or output under control of the Data Direction Register (DDRA). Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port.



PERIPHERAL DATA PORT B (PA0-PA7)

Peripheral Data Port B is an 8-line, bidirectional bus used for the transfer of data, control and status information between the W65C21 and a peripheral device. Functional operation is identical to Peripheral Data Port A, thus allowing the W65C21 to independently control two peripheral devices.

READ/WRITE SIGNAL (RWB)

Read/Write (RWB) controls the direction of data transfers between the PIA and the data lines associated with the CPU and the peripheral devices. A high on the RWB line permits the peripheral devices to transfer data to the CPU from the PIA. A low on the RWB line allows data to be transferred from the CPU to the peripheral devices from the PIA.

REGISTER SELECT (RS0, RS1)

The Register Select inputs allow the microprocessor to select the W65C21 internal registers as presented Table 2. Full functionality is described under the Functional Description section for Register Access and Selection.

RESET SIGNAL (RESB)

A low signal (Logic 0) on the Reset line serves to initialize the W65C21, clearing all internal registers (to Logic 0) and placing all peripheral interface lines (PA and PB) in the input state.

FUNCTIONAL DESCRIPTION

The W65C21 PIA is organized into two independent sections referred to as the A Side and the B Side. Each section consists of Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB) and the buffers necessary to drive the Peripheral Interface buses.

Data Bus Buffers (DBB) interface data from the two sections to the data bus, while the Data Input Register (DIR) interfaces data from the DBB to the PIA registers. Chip Select and RWB control circuitry interface to the processor bus control lines. Figure 3 is a block diagram of the W65C21 PIA.

CONTROL REGISTERS (CRA AND CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The individual control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Status Control input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These two interrupt lines drive the interrupt input (IRQB or NMIB) of the microprocessor.

DATA BUS BUFFERS (DBB)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the microprocessor and the PIA. These buffers are tri-state and are capable of driving a two TTL load when operating in an output mode.



DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a “0” in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a “1” results in the line being an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a “1”, a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a “0”, a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

DATA INPUT REGISTER (DIR)

During a Write data operation, the microprocessor writes data into the W65C21 by placing data on the Data Bus. This data is then latched into the Data Input Register by the Phase Two (PHI2) clock. Once in the DIR, this data byte is transferred into one of six internal registers. This data transfer occurs after the trailing edge of the PHI2 clock pulse that latched the data into the DIR. This timing delay guarantees the data on the peripheral output lines (PA or PB) will make a smooth transition from low to high or high to low, and the output voltage will remain stable when there is to be no change in polarity.

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Table 3 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to logic 1. The active transition can be programmed by setting a “0” in bit 1 of the CRA if the interrupt flag (bit7 of CRA) is to be set on a negative transition of the CA1 signal or a “1” if it is to be set on a positive transition.

NOTE:

A negative transition is defined as a transition from a high to a low and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5=0) it acts to set the interrupt flag, bit 6 of CRA, to logic 1 on the active transition selected by bit 4 of CRA. These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bits allow the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5=1), CA2 can operate independently to generate a simple pulse each time the microprocessor is selected by setting CRA bit 4 to a 0 and CRA bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc., which make sequential data available on the Peripheral input lines.



A second output mode allows CA2 to be used in conjunction with CA1 to “handshake” between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output that can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively. CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5=1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the “handshaking” operates on data transfers from the processor into the peripheral device.

INTERRUPT REQUEST (IRQAB, IRQBB)

The active low Interrupt Request lines (IRQAB and IRQBB) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are open drain and are capable of sinking 3.2 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired OR configuration. The A and B in the titles of these lines correspond to the peripheral port B so that each interrupt request line services one peripheral data port.

Each interrupt Request line has two interrupt flag bits that can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2) The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set an active transition of the CA1 interrupt input signal. However, IRQAB can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and IRQAB can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a “Read Peripheral Output Register A” operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of IRQA control is shown in Table 3.

Control of IRQBB is performed in exactly the same manner as that described above for IRQAB. Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and IRQBB from this flag is controlled by CRB bit 0. Likewise, bit 6 (IRQB2) in CRB is set by an active transition on CB2 and IRQBB from this flag is controlled by CRB bit 3.

Also both bit 6 and bit 7 of CRB are reset by a “Read Peripheral B Output Register” operation. A summary of IRQBB control is shown in Table 3.

INTERRUPT STATUS CONTROL LOGIC (ISCA, ISCB)

The four interrupt/peripheral control lines (CA1, CA2, CB1, and CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register, thus allowing these lines to perform various control functions as described in Figure 6.



PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on a peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with a peripheral device's output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines that are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers that drive the Peripheral A I/O lines each contain two active pull-up transistors and one active pull-down transistor. The pull-up transistors are resistive in nature and therefore allow the output voltage to go to VCC for logic 1. The pull down transistors can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the W65C21S input pull-up transistors are connected to the I/O pin and will supply 50uA minimum pull-up current while the W65C22N will pull up greater than -200uA to drive two standard TTL loads.

When in the output mode Port A can drive with similar current as the Port B buffers and can be thought of as push-pull buffers. If Port A is clamped below 2.0V for logic 1 or above .8V for logic 0 the data read during a read operation may not correspond to the value wrote to the output registers. This is a difference between the Port A buffers and the Port B buffers and also is a difference with older versions of the PIA.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines that affect their use in peripheral interfacing.

The Peripheral B I/O buffers are push-pull devices, i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will go to the VDD power supply level.

Another difference between the PA0-PA7 lines and the PBO-PB7 lines is that they have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least two TTL load and may also be used as a source of up to 3.0 mA at 1.5 volts to directly drive the base of a transistor switch, such as a Darlington pair. Limiting resistors should be used on the W65C21S to prevent excessive current when clamping an output on both PA and PB port buffers.

The W65C21N have built in limiting resistors on PB0-PB7 and PA0-PA7 isn't designed for Darlington drive currents. Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state. All pins are read when in the input mode.



PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

All output data to a peripheral is stored in the corresponding Output Register (ORA or IRB). This data is then presented to the Peripheral Interface Buffer (A and B) and placed on the respective I/O port lines. Writing a “0” into any bit position of ORA or ORB results in the corresponding peripheral I/O Port line going low (<0.4V), providing that particular line is programmed as an output. Writing a “1” into a bit position results in the corresponding output going high.

READING THE PERIPHERAL PORT

Performing a Read operation with RS1=0, RS0=0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for this lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor or Read operation.

REGISTER ACCESS AND SELECTION

The two Register Select lines (RS0, RS1), in conjunction with the Control Registers (CRA, CRB) Data Direction Register access bits (see table 1, bit 2) select the various W65C21 registers to be accessed by the CPU, RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control Registers (CRA, CRB) the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB) in addition, the microprocessor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore is shown separately in Table 2.

CROSS REFERENCE GUIDE

The W65C21N is a replacement part for older PIA devices. The W65C21N Port A input buffers supply 200uA pull-up current at 2.4V in the input mode.

The W65C21S requires current limiting resistors should be used on the peripheral port pins (PA0-PA7 and PB0-PB7) when clamping an output on the W65C21S. This does not apply to the W65C21N

For the W65C21S only, the Port A input buffers supply 50 uA pull-up current at 2.4V when in the input mode and can supply the same drive current as the Port B buffers when in the output mode. The changes were made to both reduce the current for lower power CMOS systems and to speed up the output drivers for higher speed systems



CA1/CB1 CONTROL				
CRA (CRB)			ACTIVE TRANSITION OF INPUT SIGNAL*	IRQAB (IRQBB) INTERRUPT OUTPUTS
BIT 1	BIT 0			
0	0		Negative	Disable – remains high
0	1		Negative	Enable – goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0		Positive	Disable – remains high
1	1		Positive	Enable – as explained above

*Note: Bit 7 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of bit 0 in CRA (CRB).

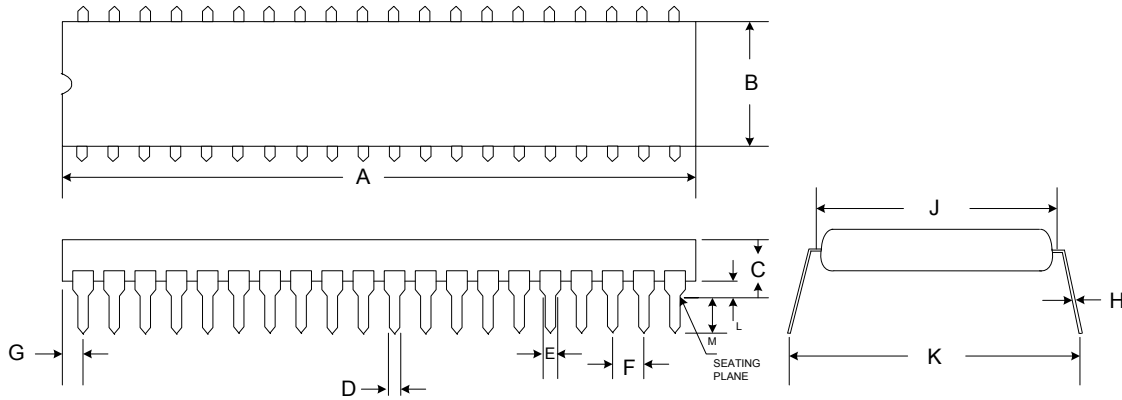
CA2/CB2 INPUT MODES				
CRA (CRB)			ACTIVE TRANSITION OF INPUT SIGNAL*	IRQAB (IRQBB) INTERRUPT OUTPUTS
BIT 5	BIT 4	BIT 3		
0	0	0	Negative	Disable – remains high
0	0	1	Negative	Enable – goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable – remains high
0	1	1	Positive	Enable – as explained above

*Note: Bit 6 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of bit 0 in CRA (CRB).

CA2 OUTPUT MODES				
CRA (CRB)			ACTIVE TRANSITION OF INPUT SIGNAL*	IRQAB (IRQBB) INTERRUPT OUTPUTS
BIT 5	BIT 4	BIT 3		
1	0	0	“Handshake on Read”	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor “Read A Data” operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a microprocessor “Read A Data” operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES				
CRA (CRB)			ACTIVE TRANSITION OF INPUT SIGNAL*	IRQAB (IRQBB) INTERRUPT OUTPUTS
BIT 5	BIT 4	BIT 3		
1	0	0	“Handshake on Read”	CB2 is set low on microprocessor “Write B Data” and is set high by an active transition of the CB1 input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor “Write B Data” operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Table 3 Interrupt Input/Peripheral Control Line Operation.



40 PIN PLASTIC PACKAGE				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
E	1.02	1.52	0.040	0.060
F	2.54	TYP	0.100	TYP
G	1.65	2.16	0.065	0.085
H	0.20	0.38	0.008	0.015
J	15.24	TYP	0.600	TYP
K				
L	0.51	1.02	0.020	0.040
M	2.92	3.43	0.115	0.135

Figure 9 Package Dimensions 40-Pin Plastic Dip



ORDERING INFORMATION

W65C21N6TPLG-14	
Description W65C = standard product	W65C
Product Identification Number 21N = NMOS Compatible 21S = Speed and Power Improved	21N
Foundry Process 6T = 0.6u TSMC Process	6T
Package P = Plastic Dual-In-Line, 40 pins PL = Plastic Leaded Chip Carrier, 44 pins	PL
RoHS/Green Compliance G = RoHS/Green Compliant (Wafer and Packaging)	G
Speed Designator -14 = 14MHz	-14

To receive general sales or technical support on standard product or information about our module library licenses, contact us at:

The Western Design Center, Inc.
2166 East Brown Road
Mesa, Arizona 85213 USA
Phone: 480-962-4545 Fax: 480-835-6442
e-mail: Information@WesternDesignCenter.com
www.WesternDesignCenter.com

WARNING: MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC ELECTRICAL CHARGE BUILDUPS. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive workstations.
3. Ground all assembly and repair tools.

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