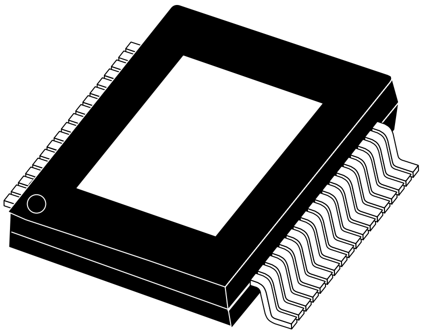
TDA7492

50 W + 50 W dual BTL class-D amplifier

Datasheet - production data



PowerSSO-36
with exposed pad up

Features

- 50 W + 50 W continuous output power at THD = 10% with R_L = 6 Ω and V_{CC} = 25 V
- 40 W + 40 W continuous output power at THD = 10% with R_L = 8 Ω and V_{CC} = 25 V
- Wide-range single-supply operation (8 - 26 V)
- High efficiency (η = 90%)
- Four selectable, fixed gain settings of nominally 21.6 dB, 27.6 dB, 31.1 dB and 33.6 dB
- Differential inputs minimize common-mode noise
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable
- ECOPACK®, environmentally friendly package

Description

The TDA7492 is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and exposed-pad-up (EPU) package, only a simple heatsink is required.

Table 1. Device summary

Order code	Operating temp. range	Package	Packaging
TDA7492	-40 to +85 °C	PowerSSO-36 EPU	Tube
TDA749213TR	-40 to +85 °C	PowerSSO-36 EPU	Tape and reel

This is information on a product in full production. www.st.com

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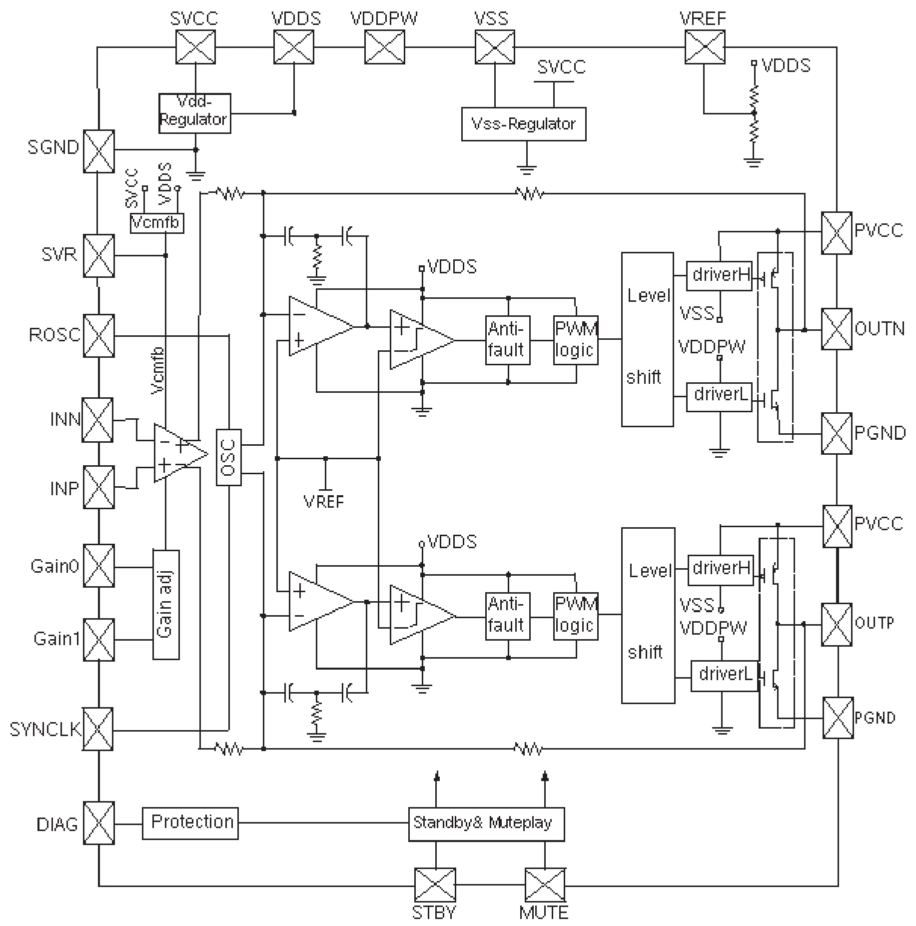
1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7492.

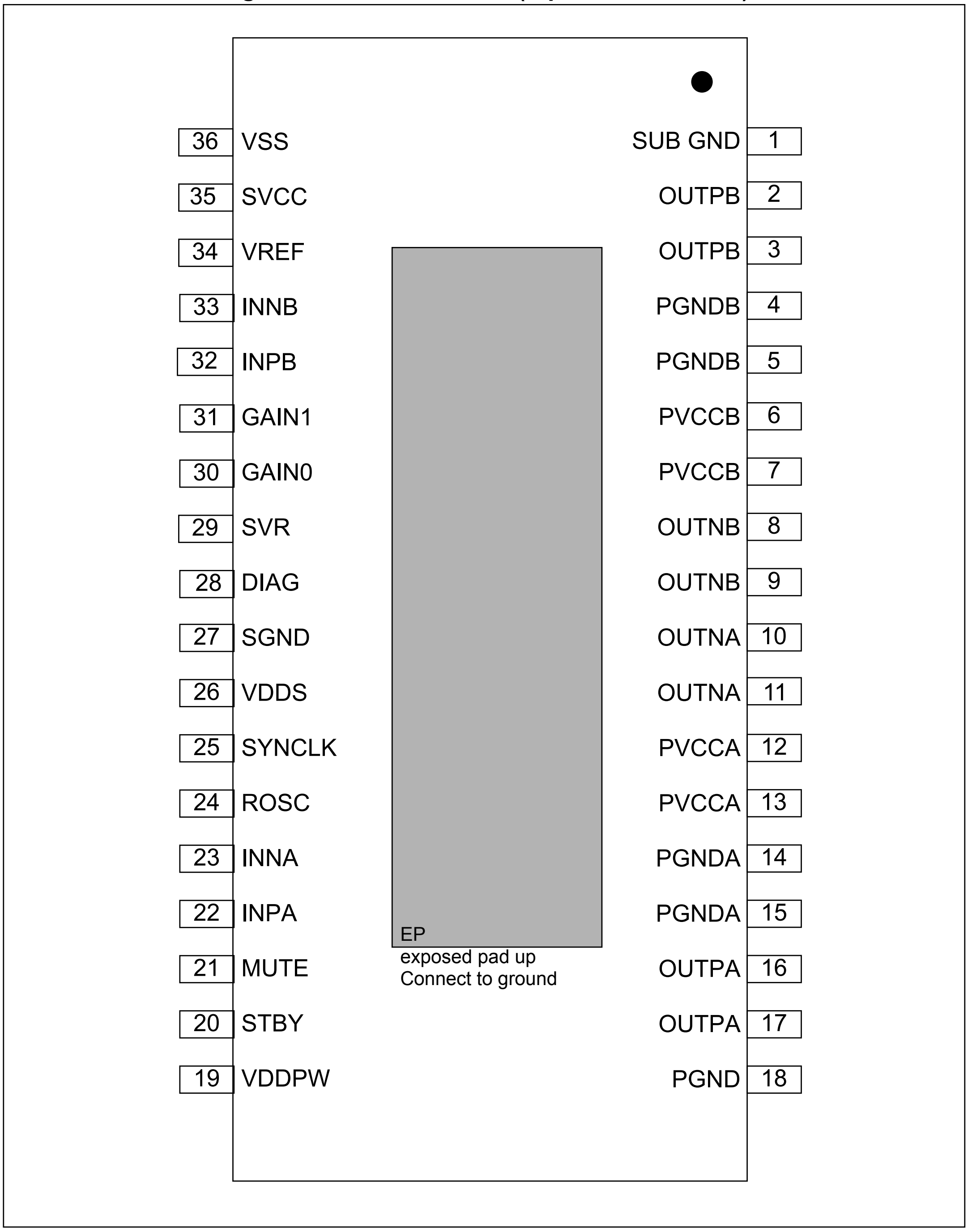
Figure 1. Internal block diagram (showing one channel only)



2 Pin description

2.1 Pinout

Figure 2. Pin connections (top view, PCB view)



2.2 Pin list

Table 2. Pin description list

Number	Name	Type	Description
1	SUB_GND	PWR	Connect to the frame
2,3	OUTPB	O	Positive PWM for right channel
4,5	PGNDB	PWR	Power stage ground for right channel
6,7	PVCCB	PWR	Power supply for right channel
8,9	OUTNB	O	Negative PWM output for right channel
10,11	OUTNA	O	Negative PWM output for left channel
12,13	PVCCA	PWR	Power supply for left channel
14,15	PGNDA	PWR	Power stage ground for left channel
16,17	OUTPA	O	Positive PWM output for left channel
18	PGND	PWR	Power stage ground
19	VDDPW	O	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	I	Standby mode control
21	MUTE	I	Mute mode control
22	INPA	I	Positive differential input of left channel
23	INNA	I	Negative differential input of left channel
24	ROSC	O	Master oscillator frequency-setting pin
25	SYNCLK	I/O	Clock in/out for external oscillator
26	VDDS	O	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	PWR	Signal ground
28	DIAG	O	Open-drain diagnostic output
29	SVR	O	Supply voltage rejection
30	GAIN0	I	Gain setting input 1
31	GAIN1	I	Gain setting input 2
32	INPB	I	Positive differential input of right channel
33	INNB	I	Negative differential input of right channel
34	VREF	O	Half VDDS (nominal) referred to ground
35	SVCC	PWR	Signal power supply
36	VSS	O	3.3-V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for heatsink, to be connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage for pins PVCCA, PVCCB, SVCC	30	V
VI	Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN0, GAIN1	-0.3 - 3.6	V
T_{op}	Operating temperature	-40 to +85	°C
T_j	Junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction to case	-	2	3	°C/W

3.3 Electrical specifications

Unless otherwise stated, the results in *Table 5* below are given for the conditions: V_{CC} = 25 V, R_L (load) = 8 Ω, R_{OSC} = R3 = 39 kΩ, C8 = 100 nF, f = 1 kHz, G_V = 21.6 dB and Tamb = 25 °C.

Table 5. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage for pins PVCCA, PVCCB, SVCC	-	8	-	26	V
I_q	Total quiescent current	Without LC	-	26	35	mA
I_{qSTBY}	Quiescent current in standby	-	-	2.5	5.0	µA
V_{OS}	Output offset voltage	Play mode	-	-	±100	mV
		Mute mode	-	-	±60	
I_{OCP}	Overcurrent protection threshold	R_L = 0 Ω	4.8	6.0	-	A
T_j	Junction temperature at thermal shutdown	-	-	150	-	°C
R_i	Input resistance	Differential input	48	60	-	kΩ
V_{OVP}	Overvoltage protection threshold	-	28	29	-	V

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{UVP}	Undervoltage protection threshold	-	-	-	7	V
R_{dsON}	Power transistor on resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
P_o	Output power	THD = 10%	-	40	-	W
		THD = 1%	-	32	-	
P_o	Output power	R_L = 6 Ω, THD = 10%, V_{CC} = 25V	-	50	-	W
		R_L = 6 Ω, THD = 1% V_{CC} = 25V	-	40	-	
P_D	Dissipated power	P_o =40W +40 W, THD = 10%	-	8.0	-	W
η	Efficiency	P_o = 40 W + 40W	80	90	-	%
THD	Total harmonic distortion	P_o = 1 W	-	0.1	0.4	%
G_V	Closed-loop gain	GAIN0 = L, GAIN1 = L	20.6	21.6	22.6	dB
		GAIN0 = L, GAIN1 = H	26.6	27.6	28.6	
		GAIN0 = H, GAIN1 = L	30.1	31.1	32.1	
		GAIN0 = H, GAIN1 = H	32.6	33.6	34.6	
ΔG_V	Gain matching	-	-	-	±1	dB
CT	Cross talk	f = 1 kHz	-	50	-	dB
eN	Total input noise	A Curve, G_V = 20 dB	-	20	-	µV
		f = 22 Hz to 22 kHz	-	25	35	
SVRR	Supply voltage rejection ratio	fr = 100 Hz, Vr = 0.5 V, C_{SVR} = 10 µF	40	50	-	dB
T_r, T_f	Rise and fall times	-	-	50	-	ns
f_{SW}	Switching frequency	Internal oscillator	290	310	330	kHz
f_{SWR}	Output switching frequency Range	With internal oscillator (1)	250	-	400	kHz
		With external oscillator (2)	250	-	400	
V_{inH}	Digital input high (H)	-	2.3	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
A_{MUTE}	Mute attenuation	V_{MUTE} = 1 V	60	80	-	dB

1. $f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4)$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ with R3 = 39 kΩ (see *Figure 28.*).
2. $f_{SW} = f_{SYNCLK} / 2$ with the frequency of the external oscillator.

4 Characterization curves

The general test conditions used for producing the characterization curves can be summarized as follows:

Test board: SZ LAB TDA7492 slug-up demo board

Test frequency: 1 kHz (also 100 Hz for THD vs. output power only)

Output power: 1 W

- For 6-Ω loads
  - test voltage: 25 V
  - LC filter: L = 22 µH and C = 220 nF
- For 8-Ω loads
  - test voltage: 25 V
  - LC filter: L = 33 µH and C = 220 nF
- For 4-Ω loads
  - test voltage: 20 V
  - LC filter: L = 15 µH and C = 470 nF.

Figure 28 on page 22 shows the circuit with which the characterization curves, shown in the next sections, were measured. *Figure 27 on page 21* shows the PCB layout.

4.1 Characterizations for 6-Ω loads

Figure 3. Output power vs. supply voltage

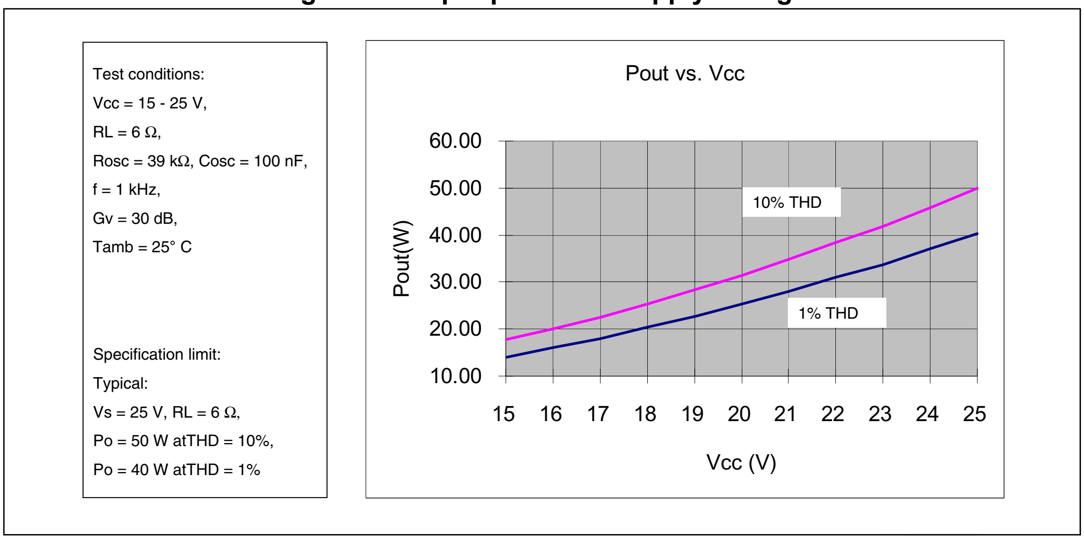


Figure 4. THD vs. output power (1 kHz)

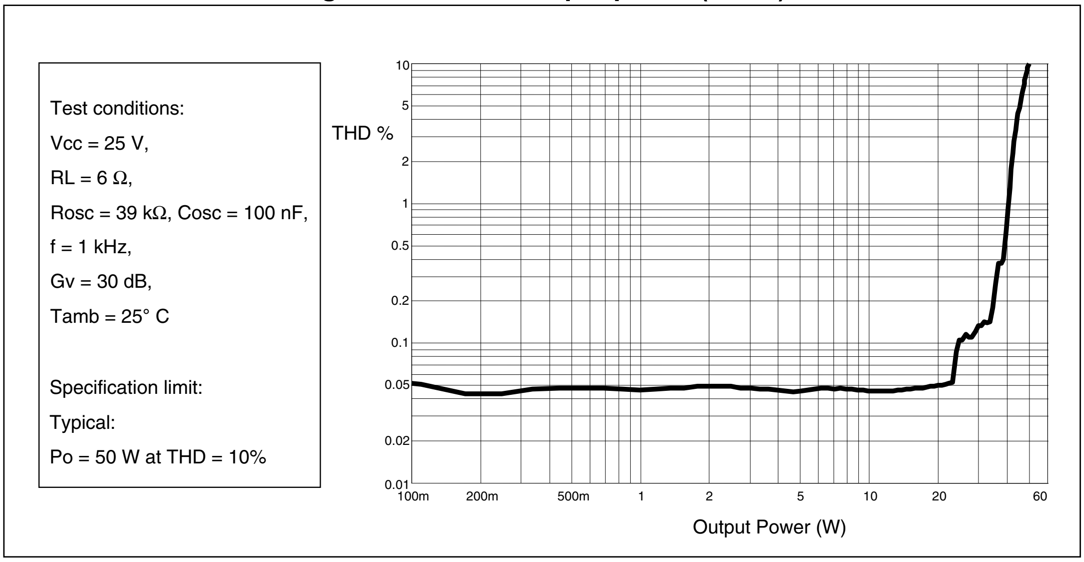


Figure 5. THD vs. output power (100 Hz)

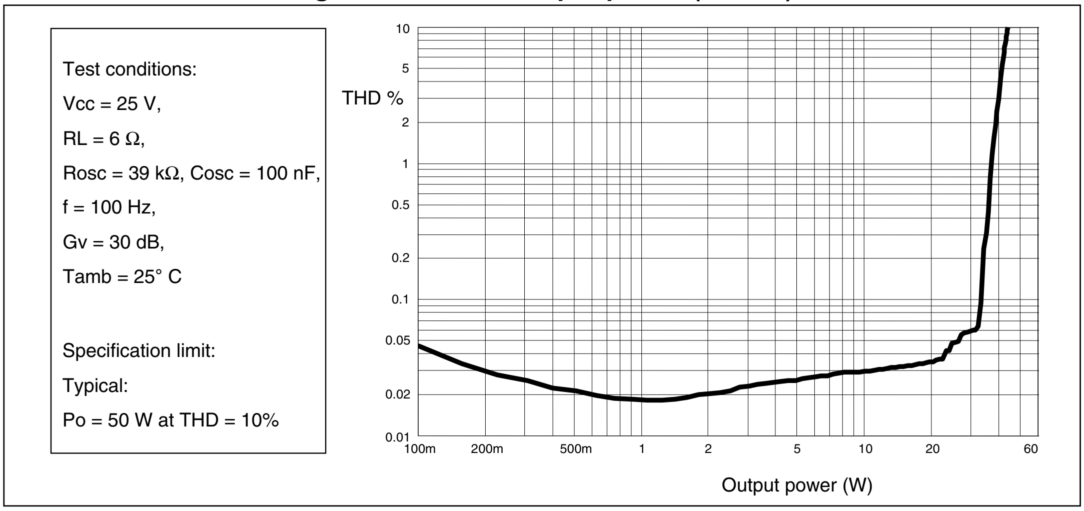


Figure 6. THD vs. frequency

Test conditions:

Vcc = 25 V,

RL = 6 Ω,

Rosc = 39 kΩ, Cosc = 100 nF,

f = 1 kHz,

Gv = 30 dB,

Po = 1 W,

Tamb = 25° C

Specification limit:

Typical: THD < 0.4%

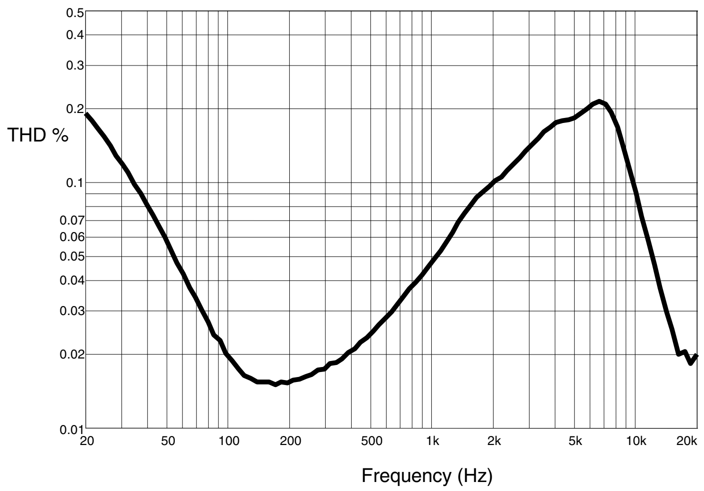


Figure 7. Frequency response

Test conditions:

Vcc = 25 V,

RL = 6 Ω,

Rosc = 39 kΩ, Cosc = 100 nF,

f = 1 kHz,

Gv = 30 dB,

Po = 1 W,

Tamb = 25° C

Specification limit:

Max: +/-3 dB (20 Hz to 20 kHz)

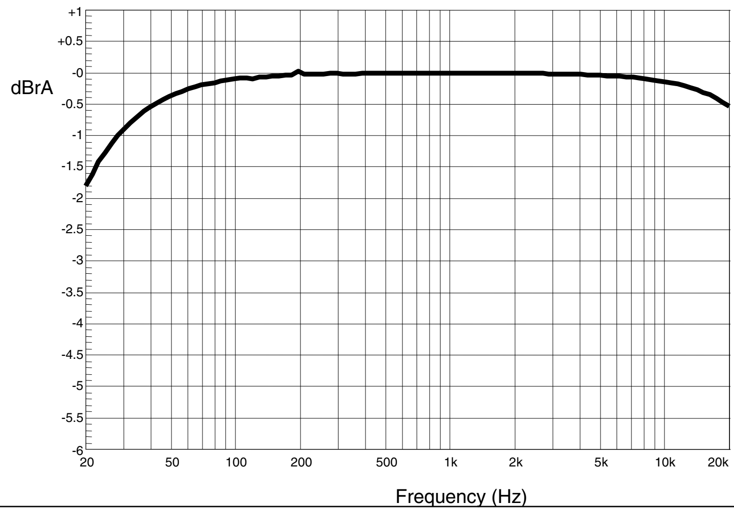


Figure 8. Crosstalk

Test conditions:

Vcc = 25 V,

RL = 6 Ω,

Rosc = 39 kΩ, Cosc = 100 nF,

f = 1 kHz,

Gv = 30 dB,

Po = 1 W

Tamb = 25° C

Specification limit:

Typical: > 50 dB (at f = 1 kHz)

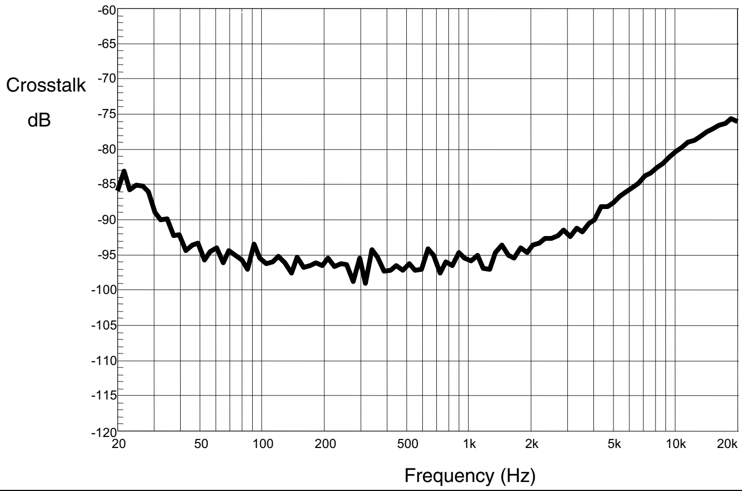


Figure 9. FFT performance (0 dB)

Test conditions:
Vcc = 25 V,
RL = 6 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical: > 60 dB
for the harmonic frequency

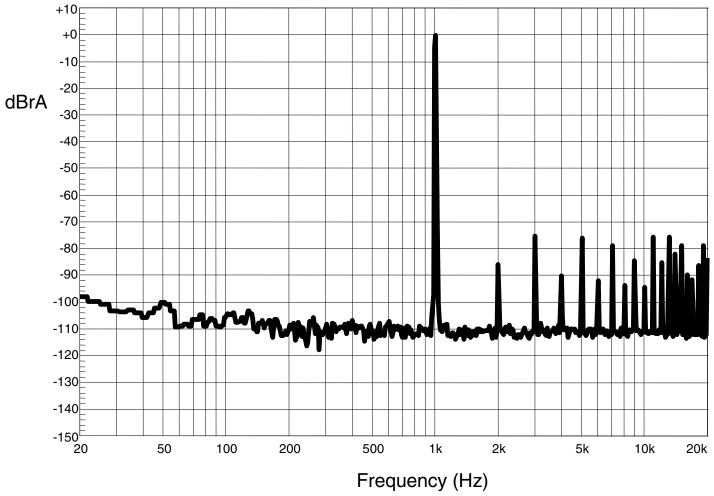
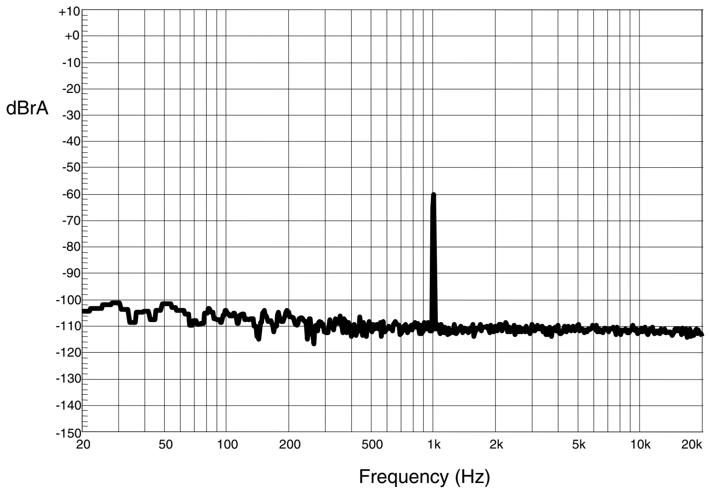


Figure 10. FFT performance (-60 dB)

Test conditions:
Vcc = 25 V,
RL = 6 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Po = -60 dB (at 1 W = 0 dB)
Tamb = 25° C

Specification limit:
Typical: > 90 dB
for the harmonic frequency



4.2 Characterizations for 8-Ω loads

Figure 11. Output power vs. supply voltage

Test conditions:
Vcc = 5 - 25 V,
RL = 8 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Tamb = 25° C

Specification limit:
Typical:
Vs = 25 V, RL = 8 Ω,
Po = 40 W at THD = 10%,
Po = 32 W at THD = 1%

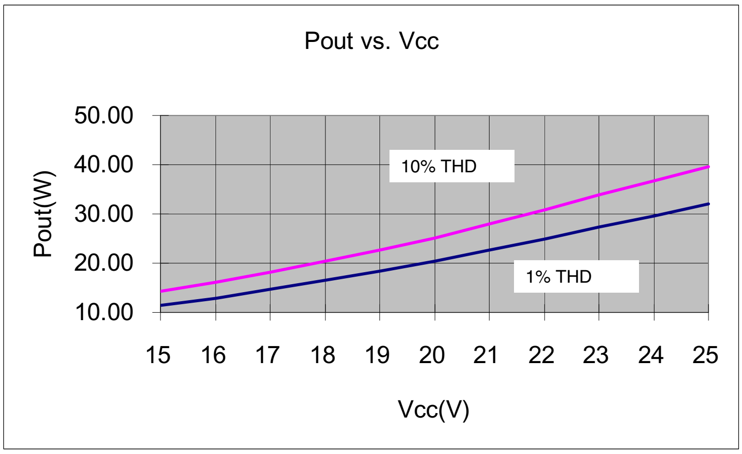


Figure 12. THD vs. output power (1 kHz)

Test conditions:
Vcc = 25 V,
RL = 8 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Tamb = 25° C

Specification limit:
Typical:
Po = 40 W at THD = 10%

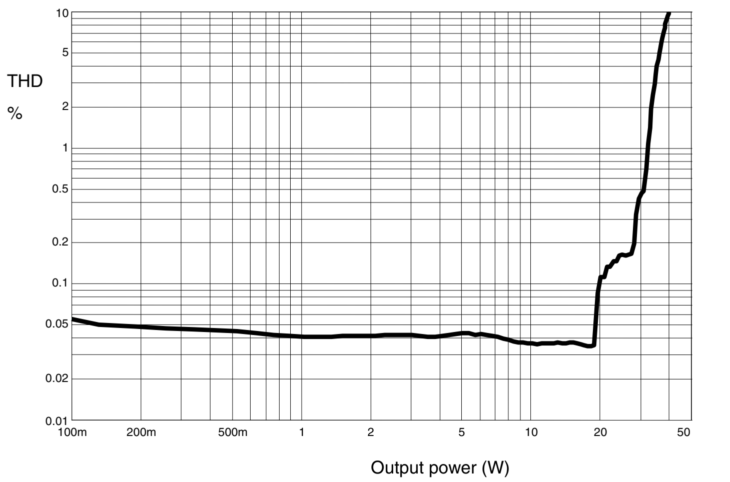


Figure 13. THD vs. output (100 Hz)

Test conditions:
Vcc = 25 V,
RL = 8 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 100 Hz,
Gv = 30 dB,
Tamb = 25° C

Specification limit:
Typical:
Po = 40 W at THD = 10%

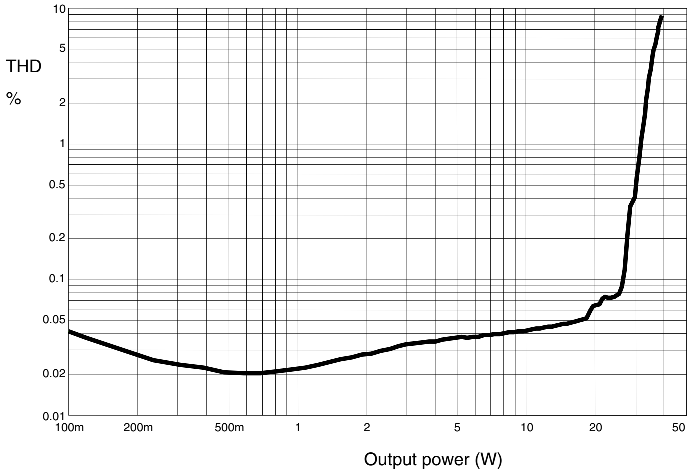


Figure 14. THD vs. frequency

Test conditions:
Vcc = 25 V,
RL = 8 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical: THD < 0.4%

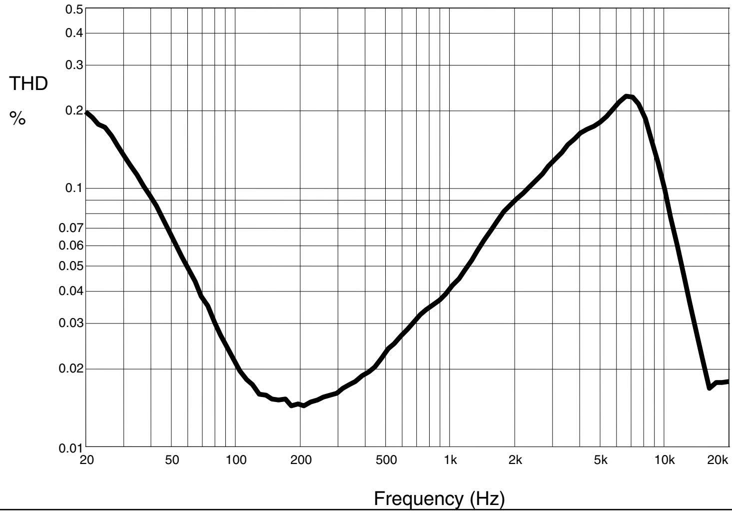


Figure 15. Frequency response

Test conditions:
Vcc = 25 V,
RL = 8 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Po = 1 W,
Tamb = 25° C

Specification limit:
Max: +/-3 dB (20 Hz to 20 kHz)

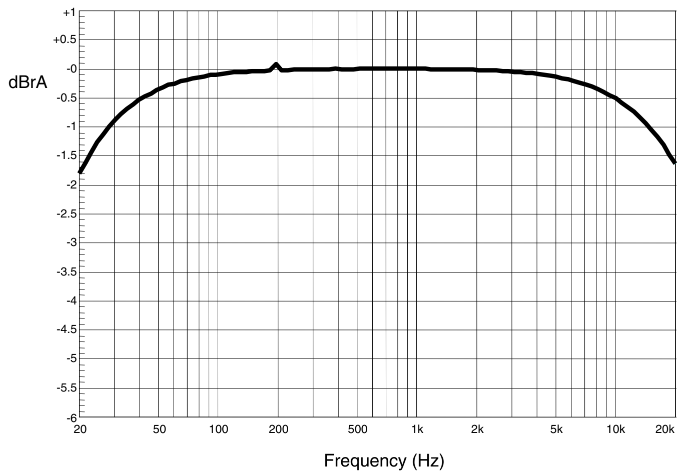


Figure 16. Crosstalk

Test conditions:
Vcc = 25 V,
RL = 8 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical: > 50 dB (at f = 1 kHz)

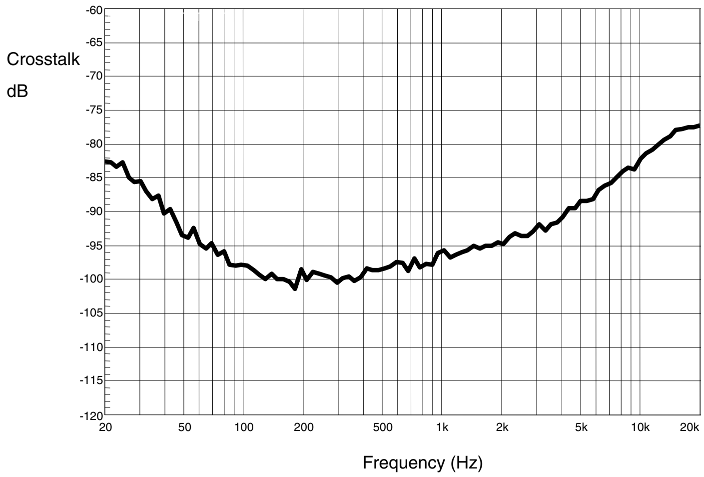


Figure 17. FFT performance (0 dB)

Test conditions:
Vcc = 25 V,
RL = 8 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical: > 60 dB
for the harmonic frequency

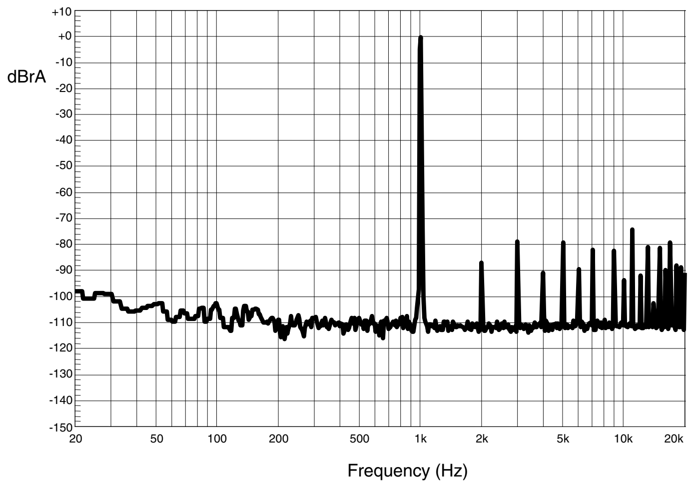
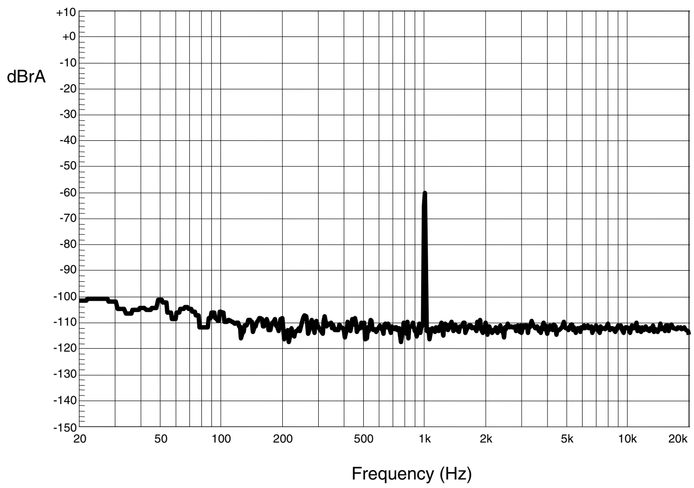


Figure 18. FFT performance (-60 dB)

Test conditions:
Vcc = 25 V,
RL = 8 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 30 dB,
Po = -60 dB (at 1 W = 0 dB)
Tamb = 25° C

Specification limit:
Typical: > 90 dB
for the harmonic frequency



4.3 Characterizations for 4-Ω loads

Figure 19. Output power vs. supply voltage

Test conditions:
Vcc = 15 - 22 V,
RL = 4 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 20 dB,
Tamb = 25° C

Specification limit:
Typical:
Vs = 20 V, RL = 4 Ω,
Po = 47 W at THD = 10%,
Po = 38 W at THD = 1%

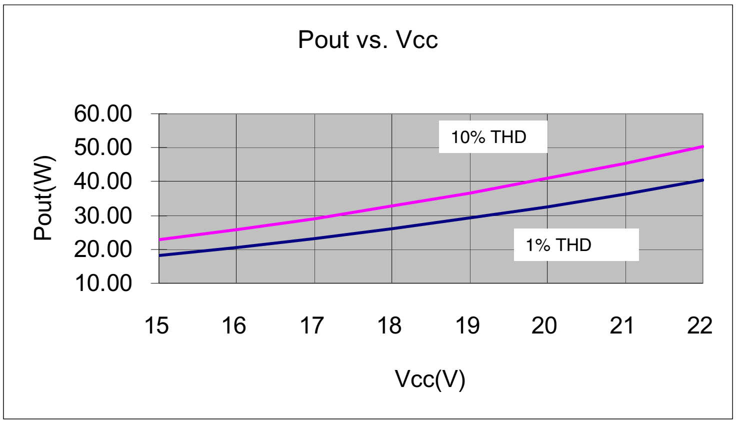


Figure 20. THD vs. output power (1 kHz)

Test conditions:
Vcc = 20 V,
RL = 4 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 20 dB,
Tamb = 25° C

Specification limit:
Typical:
Po = 38 W at THD = 1%

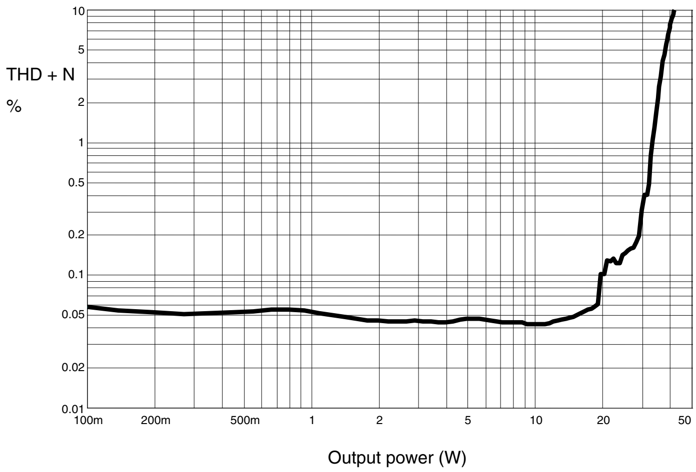


Figure 21. THD vs. output (100 Hz)

Test conditions:
Vcc = 20 V,
RL = 4 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 100 Hz,
Gv = 20 dB,
Tamb = 25° C

Specification limit:
Typical:
Po = 38 W at THD = 1%

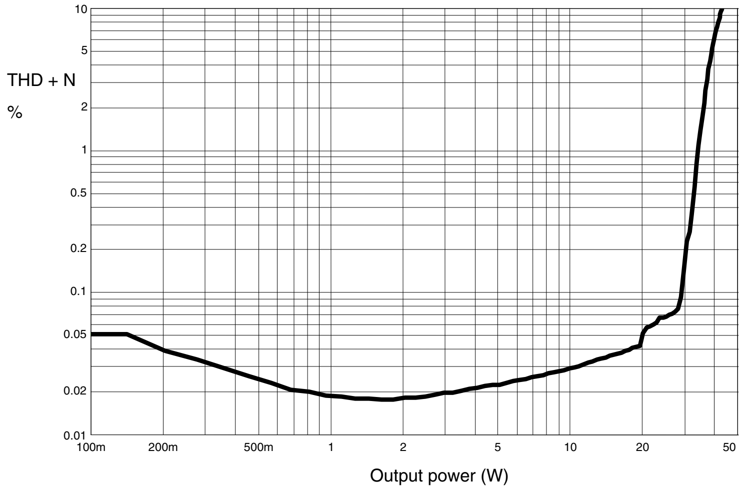


Figure 22. THD vs. frequency

Test conditions:
Vcc = 20 V,
RL = 4 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 20 dB,
0 dB at f = 1 kHz,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical: THD < 0.4%

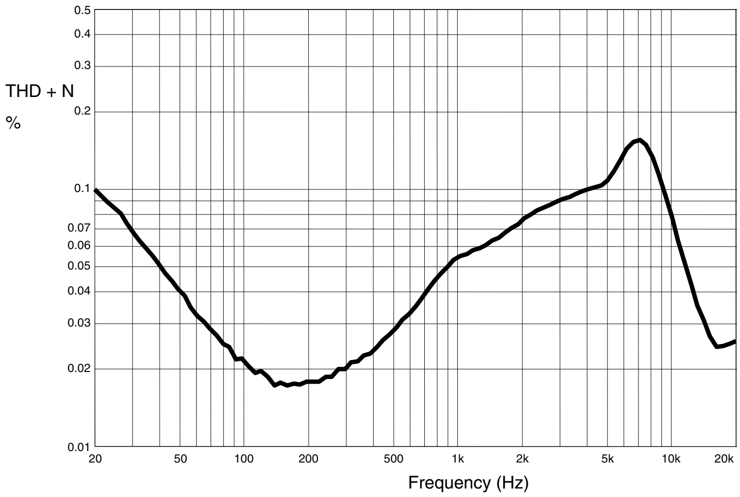


Figure 23. Frequency response

Test conditions:
Vcc = 20 V,
RL = 4 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 20 dB,
0 dB at f = 1 kHz,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical:
Max: +/-3 dB (20 Hz to 20 kHz)

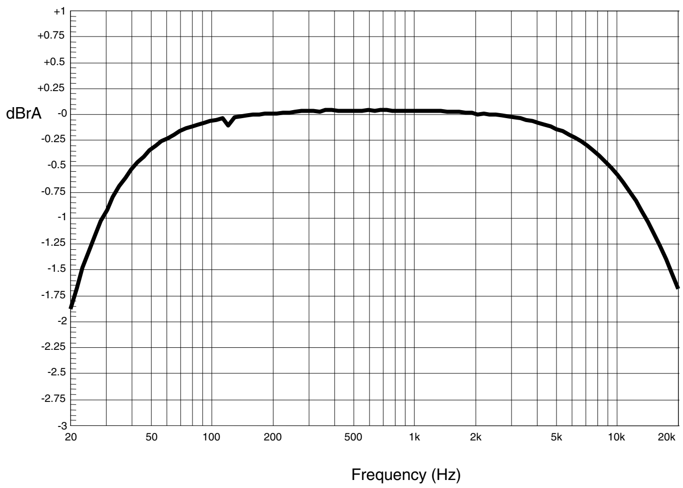


Figure 24. Crosstalk

Test conditions:
Vcc = 20 V,
RL = 4 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 20 dB,
0 dB at f = 1 kHz,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical: > 50 dB (at f = 1 kHz)

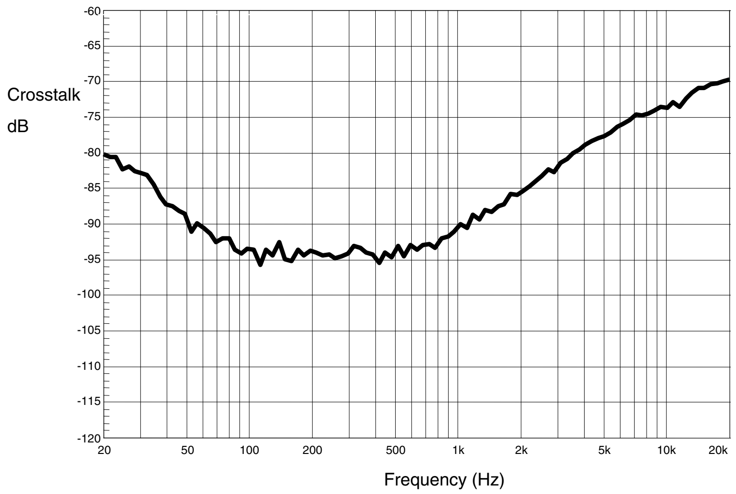


Figure 25. FFT performance (0 dB)

Test conditions:
Vcc = 20 V,
RL = 4 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 20 dB,
0 dB at f = 1 kHz,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical: > 60 dB
for the harmonic frequency

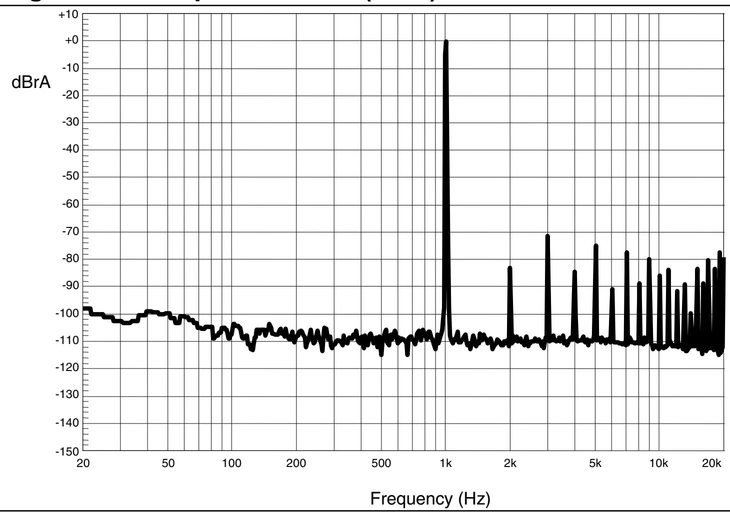
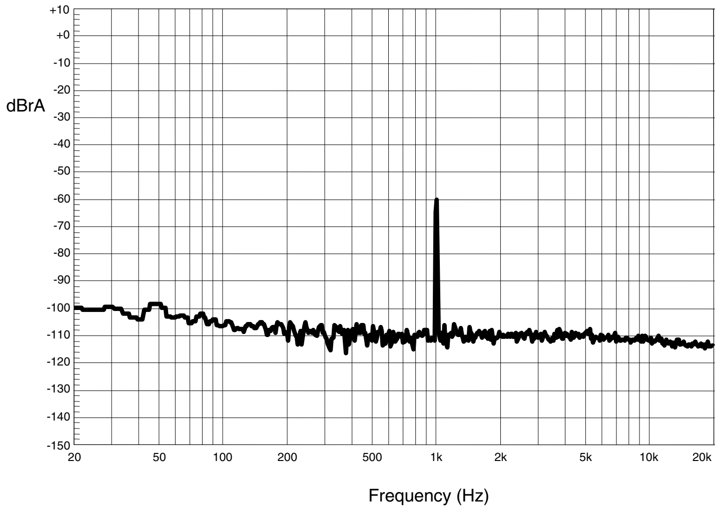


Figure 26. FFT performance (-60 dB)

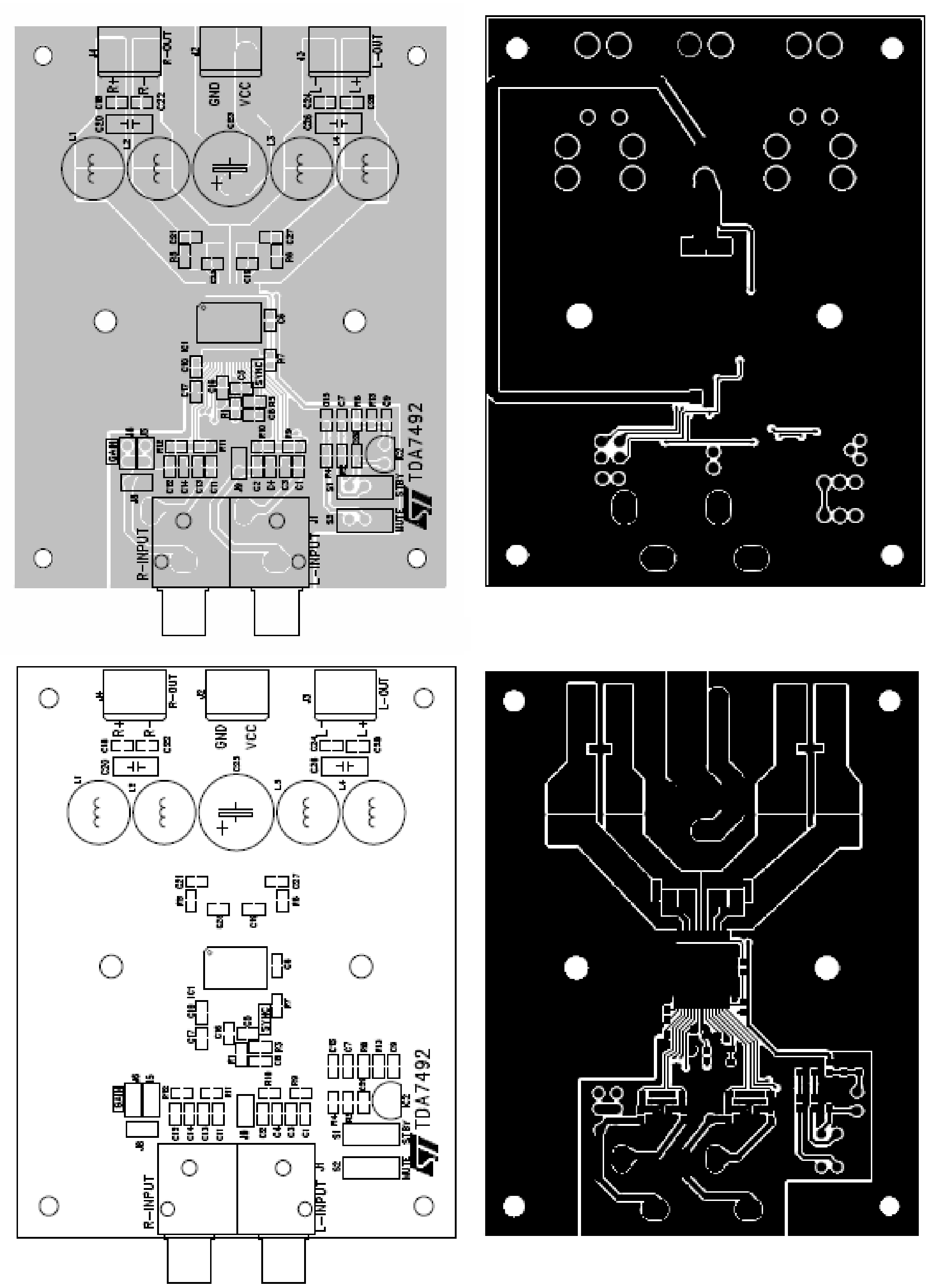
Test conditions:
Vcc = 20 V,
RL = 4 Ω,
Rosc = 39 kΩ, Cosc = 100 nF,
f = 1 kHz,
Gv = 20 dB,
0 dB at f = 1 kHz,
Po = 1 W,
Tamb = 25° C

Specification limit:
Typical: > 90 dB
for the harmonic frequency



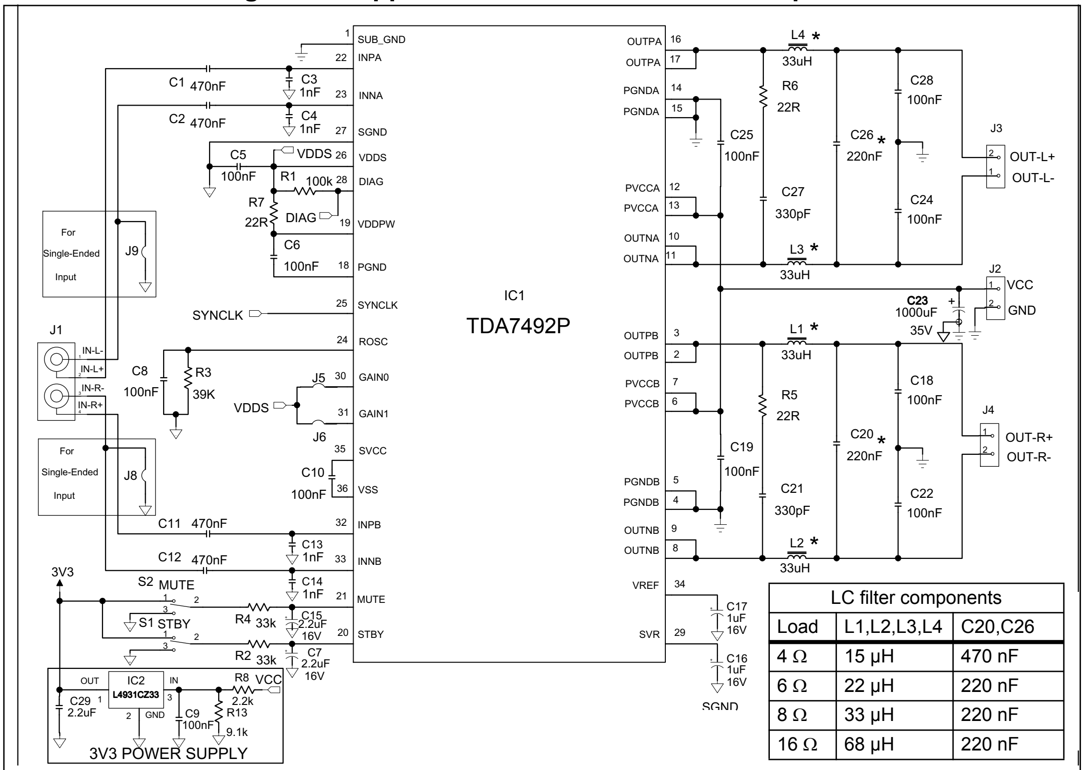
4.4 Test board

Figure 27. Test board layout



5 Applications circuit

Figure 28. Applications circuit for class-D amplifier



LC filter components		
Load	L1,L2,L3,L4	C20,C26
4 Ω	15 µH	470 nF
6 Ω	22 µH	220 nF
8 Ω	33 µH	220 nF
16 Ω	68 µH	220 nF

Input settings for standby, mute and play:

STBY : MUTE	Mode
0 V : 0 V	Standby
0 V : 3.3 V	Standby
3.3 V : 0 V	Mute
3.3 V : 3.3 V	Play

Input settings for gain:

GAIN0 : GAIN1	Nominal gain
0 V : 0 V	21.6 dB
0 V : 3.3 V	27.6 dB
3.3 V : 0 V	31.1 dB
3.3 V : 3.3 V	33.6 dB

6 Applications information

6.1 Mode selection

The three operating modes of the TDA7492 are set by the two inputs, STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

The protection functions of the TDA7492 are enabled by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 29*. The input current of the corresponding pins must be limited to 200 µA.

Table 6. Mode settings

Mode	STBY	MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Drive levels defined in *Table 5: Electrical specifications on page 9*

Figure 29. Standby and mute circuits

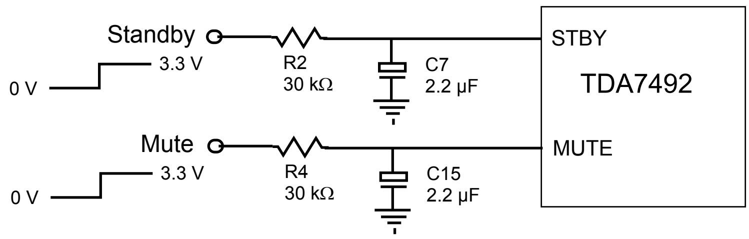
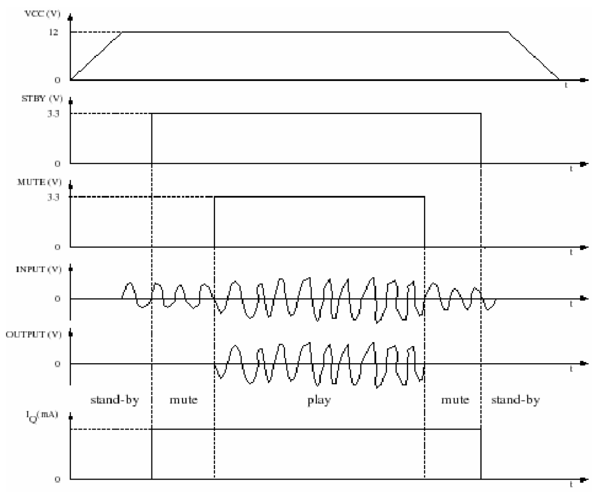


Figure 30. Turn on/off sequence for minimizing speaker "pop"



6.2 Gain setting

The gain of the TDA7492 is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin31). Internally, the gain is set by changing the feedback resistors of the amplifier.

Table 7. Gain settings

GAIN0	GAIN1	Nominal gain, G_v (dB)
0	0	21.6
0	1	27.6
1	0	31.1
1	1	33.6

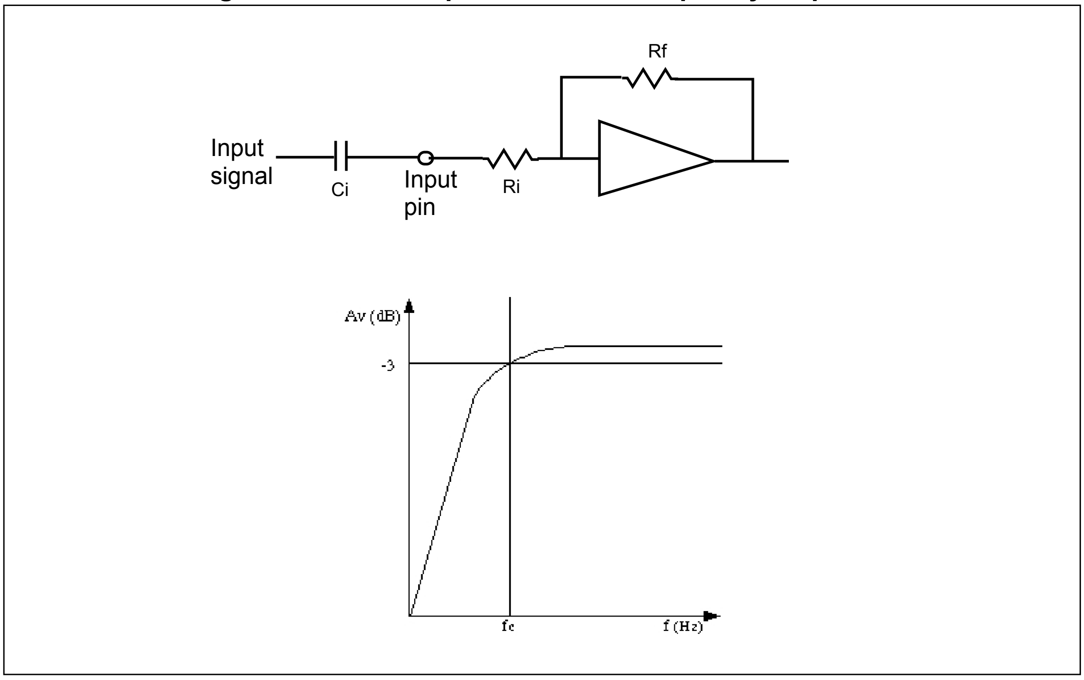
6.3 Input resistance and capacitance

The input impedance is set by an internal resistor Ri = 60 kΩ (typical). An input capacitor (Ci) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in *Figure 31*. For Ci = 470 nF the high-pass filter cutoff frequency is below 20 Hz:

$$fc = 1 / (2 * \pi * Ri * Ci)$$

Figure 31. Device input circuit and frequency response



6.4 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7492 as master clock, while the other devices are in slave mode, that is, externally clocked. The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

6.4.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency, f_{SW}, is controlled by the resistor, R_{OSC}, connected to pin ROSC:

$$f_{SW} = 10^6 / ((R_{OSC} * 16 + 182) * 4) \text{ kHz}$$

where R_{OSC} is in kΩ.

In master mode, pin SYNCLK is used as a clock output pin whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly, then resistor R_{OSC} must be less than 60 kΩ as given below in *Table 8*.

6.4.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in *Table 8*.

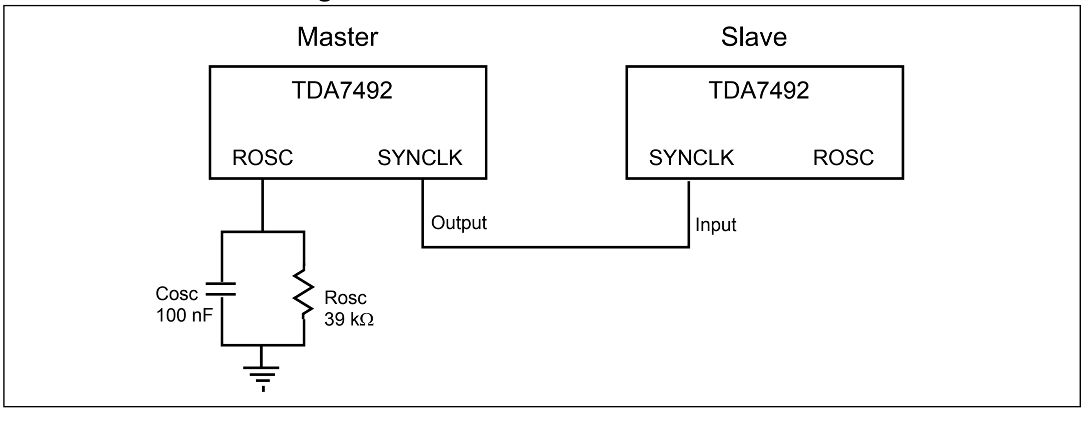
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 8. How to set up SYNCLK

Mode	ROSC	SYNCLK
Master	R_{OSC} < 60 kΩ	Output
Slave	Floating (not connected)	Input

Figure 32. Master and slave connection



6.5 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cutoff frequency of 27 kHz, are shown in *Figure 33* and *Figure 34* below.

Figure 33. Typical LC filter for a 8-Ω speaker

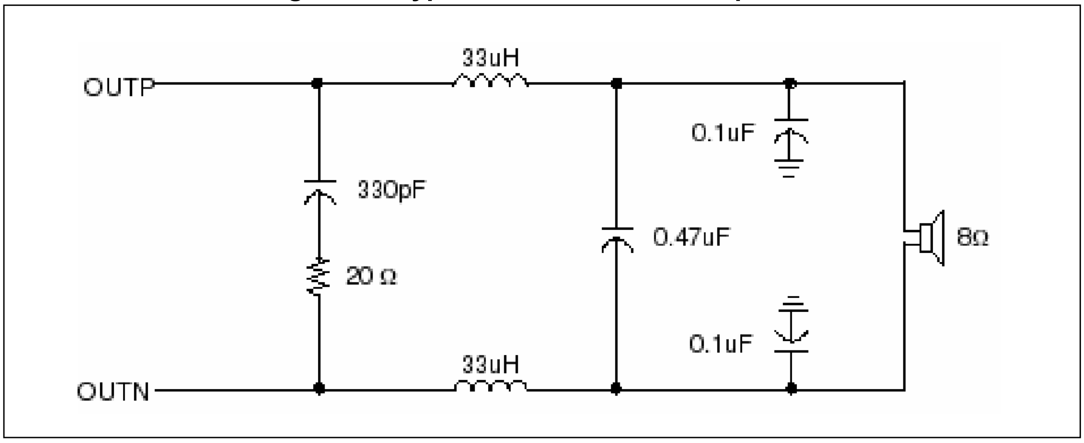
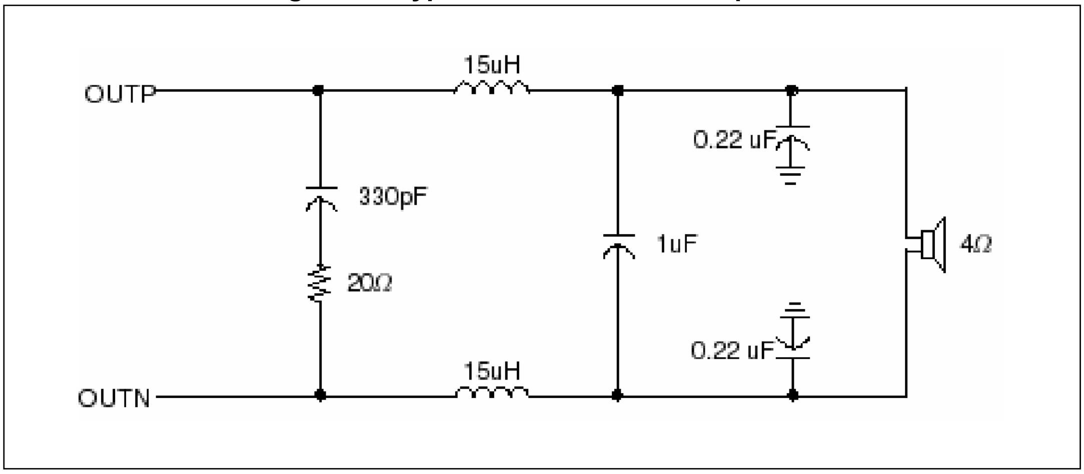


Figure 34. Typical LC filter for a 4-Ω speaker



6.6 Protection functions

The TDA7492 is fully protected against overvoltages, undervoltages, overcurrents and thermal overloads as explained here.

Overvoltage protection (OVP)

If the supply voltage exceeds the value for V_{OVP} given in *Table 5: Electrical specifications on page 9* the overvoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage drops to below the threshold value the device restarts.

Undervoltage protection (UVP)

If the supply voltage drops below the value for V_{UVP} given in *Table 5: Electrical specifications on page 9* the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

Overcurrent protection (OCP)

If the output current exceeds the value for I_{OCP} given in *Table 5: Electrical specifications on page 9* the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time, T_{OC}, is determined by the R-C components connected to pin STBY.

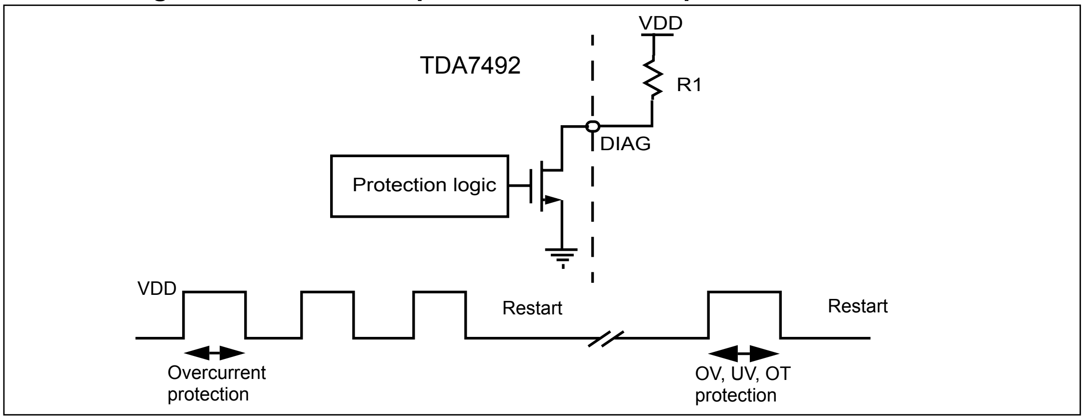
Thermal protection (OTP)

If the junction temperature, T_j, reaches 145 °C (nominally), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for T_j given in *Table 5: Electrical specifications on page 9* the device shuts down and the output is forced to the high-impedance state. When the device cools sufficiently the device restarts.

6.7 Diagnostic output

The output pin DIAG is an open drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (<26 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 μA) of the pin.

Figure 35. Behavior of pin DIAG for various protection conditions



6.8 Heatsink requirements

As with most amplifiers, the power dissipated within the device depends primarily on the supply voltage, the load impedance and the output modulation level.

The maximum estimated power dissipation for the TDA7492 is around 7 W. At 25 °C ambient a heatsink having Rth =15 °C/W is sufficient for sine-wave testing at maximum power. A musical program, however, dissipates about 40% less power than this and a heatsink with Rth = 25 °C/W is thus recommended. Even at the maximum recommended ambient temperature for consumer applications of 50 °C there is still a clear safety margin before the maximum junction temperature (150 °C) is reached.

7 Package mechanical data

The TDA7492 comes in a 36-pin PowerSSO package with exposed pad up (EPU). *Figure 36* shows the package outline and *Table 9* gives the dimensions.

Figure 36. PowerSSO-36 EPU outline drawing

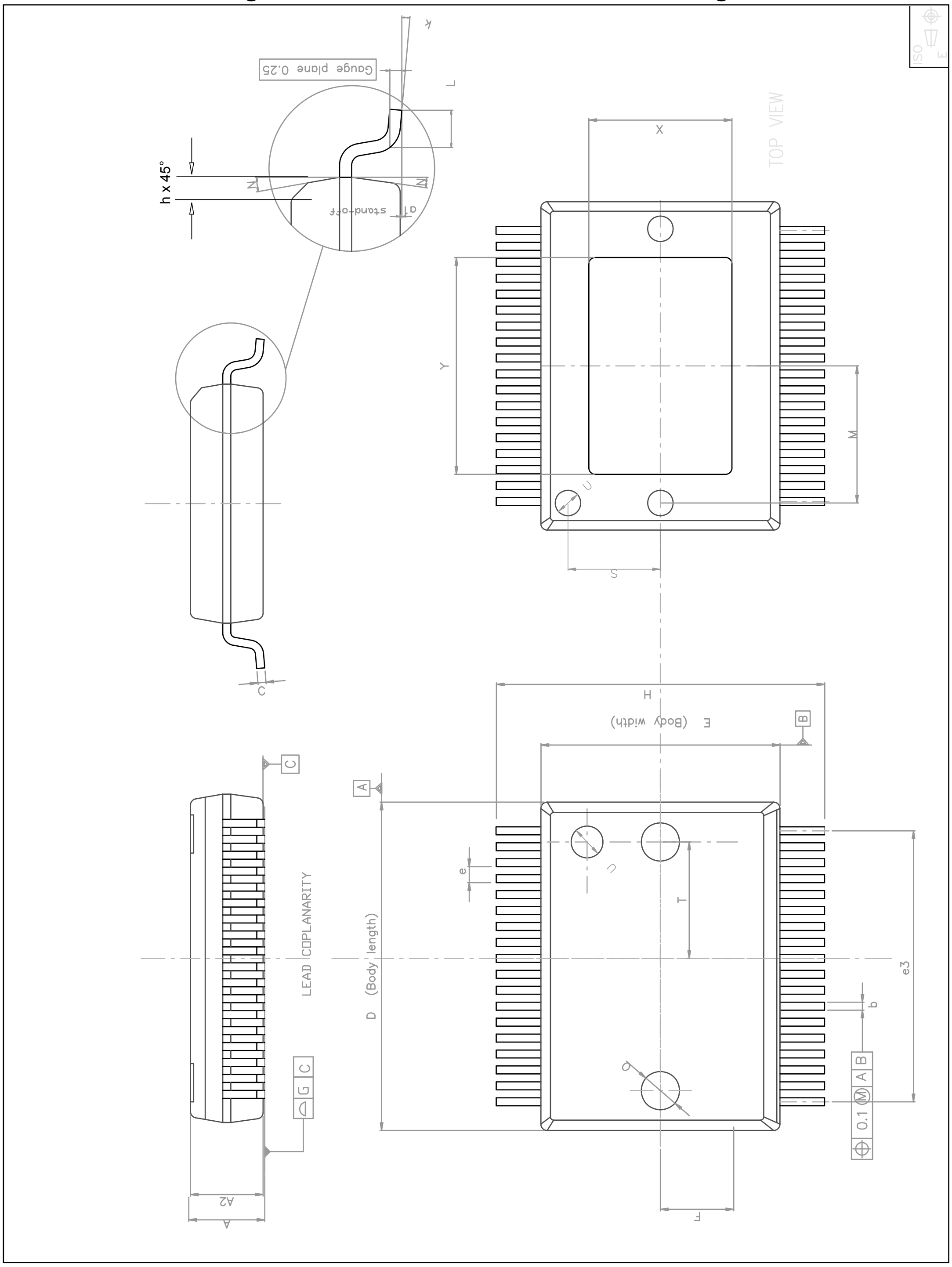


Table 9. PowerSSO-36 EPU dimensions

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.45	0.085	-	0.096
A2	2.15	-	2.35	0.085	-	0.093
a1	0	-	0.10	0	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	-	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	6.50	-	7.10	0.256	-	0.280

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8 Revision history

Table 10. Document revision history

Date	Revision	Changes
30-Jul-2008	1	Initial release.
4-Nov-2008	2	Updated V_{OS} details in *Table 5* Updated *Chapter 4: Characterization curves on page 11*.
15-Apr-2009	3	Updated supply operating range to 8 V - 26 V *on page 1* Changed C1 to C8 at beginning of *Section 3.3 on page 9* Updated *Table 5: Electrical specifications on page 9* for V_{CC} min, Iq condition, V_{OS} min/max, I_{OC}, and added new parameter V_{UV} Updated *Figure 3: Test circuit for characterizations on page 10* Updated *Figure 28: Applications circuit for class-D amplifier on page 22* Inserted brackets in equation in *Table 5*, footnote and in *Section 6.4.1 on page 25* Updated values in UVP and OCP in *Section 6.6 on page 27* Updated package presentation in *Chapter 7 on page 29* and max vaules for A and A2 in *Table 9: PowerSSO-36 EPU dimensions on page 30*.
03-Sep-2009	4	Added text for exposed pad in *Figure 2 on page 7* Added text for exposed pad in *Table 2 on page 8* Removed *Figure 3: Test circuit for characterizations* since it is identical to apps circuit in *Figure 28 on page 22* Moved section *Test board on page 21* to end of chapter Updated package Y (Min) dimension in *Table 9 on page 30*
12-Sep-2011	5	Updated OUTNA in *Table 2: Pin description list*
22-Jan-2015	6	Updated operative temperature range to -40 to +85 °C in *Table 1: Device summary* and *Table 3: Absolute maximum ratings* Updated Y dimension in *Table 9: PowerSSO-36 EPU dimensions*