

PIC16(L)F1826/1827 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1826/1827 family devices that you have received conform functionally to the current Device Data Sheet (DS41391D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC16(L)F1826/1827 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICKit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICKit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1826/1827 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾			
		A2	A3	A4	A5
PIC16F1826	10 0111 100x xxxx	2	3	4	5
PIC16LF1826	10 1000 100x xxxx	2	3	4	5
PIC16F1827	10 0111 101x xxxx	2	3	4	5
PIC16LF1827	10 1000 101x xxxx	2	3	4	5

- Note 1:** The Device ID is located in the last configuration memory space.
- Note 2:** Refer to the "PIC16F/LF182X/PIC12F/LF1822 Memory Programming Specification" (DS41390) for detailed information on Device and Revision IDs for your specific device.

PIC16(L)F1826/1827

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾			
				A2	A3	A4	A5
Data EE Memory	Memory Endurance	1.1	Erase/Write endurance limited.	X	X		
Program Flash Memory (PFM)	Endurance	2.1	Erase/Write endurance limited.	X	X		
Timer1	Timer0 Gate Source	3.1	Toggle mode works improperly.	X	X		
Oscillator	HS mode	4.1	Frequency/Voltage range.	X	X	X	X
ADC	ADC Conversion	5.1	ADC Conversion may not complete.	X	X		
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	6.1	PWM 0% duty cycle direction change.	X	X		
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	6.2	PWM 0% duty cycle port steering.	X	X		
Resets	Power-on Reset (POR)	7.1	Reset under low-power conditions.		X		
Timer1	T1 Gate Toggle mode	8.1	T1 gate flip-flop does not clear.	X	X		
BOR	Wake-up from Sleep	9.1	Device resets on wake-up from Sleep (LF devices only).	X	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A5).

1. Module: Data EE Memory

1.1 Data EE Memory Endurance

The typical write/erase endurance of the Data EE Memory is limited to 10k cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

2. Module: Program Flash Memory (PFM)

2.1 Program Flash Memory Endurance

The typical write/erase endurance of the PFM is limited to 1k cycles when VDD is above 3.0 volts.

Work around

Use an error correction method that stores data in multiple locations.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

3. Module: Timer1

3.1 Timer1 Gate Toggle Mode with Timer0 as Gate Source

Timer1 Gate Toggle mode provides unexpected results when Timer0 overflow is selected as the Timer1 gate source. We do not recommend using Timer0 overflow as the Timer1 gate source while in Timer1 Gate Toggle mode or when Toggle mode is used in conjunction with Timer1 Gate Single-Pulse mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

PIC16(L)F1826/1827

4. Module: Oscillator

4.1 HS Oscillator Frequency

The Standard Operating Conditions for the HS Oscillator are as follows:

Characteristic	Min.	Typ†	Max.	Units	Conditions	Operating Temperature
Oscillator Frequency	1	—	20	MHz	HS Oscillator mode, VDD > 2.3V	-40°C ≤ TA ≤ +85°C
Oscillator Frequency	1	—	20	MHz	HS Oscillator mode, VDD ≥ 2.8V	-40°C ≤ TA ≤ +125°C

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

5. Module: ADC

5.1 Analog-to-Digital Conversion

An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and it is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (any FOSC frequency).

When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

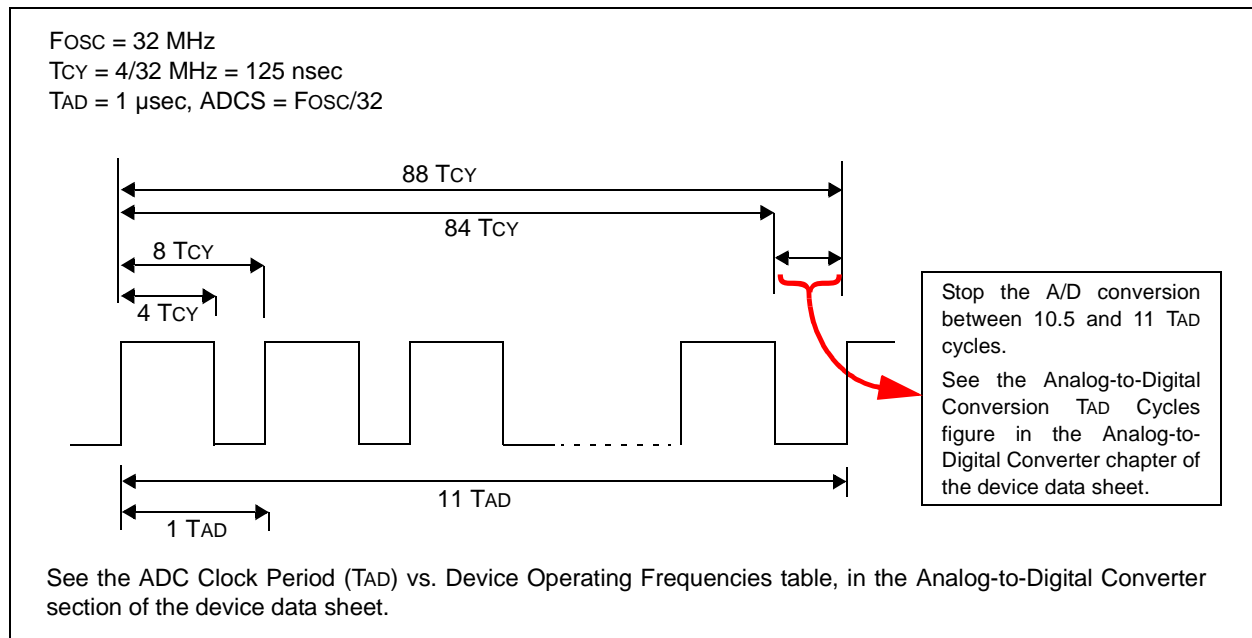
Work around

Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Method 3: This method is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to [Figure 1](#) for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE



In [Figure 1](#), 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

PIC16(L)F1826/1827

Note: The exact delay time will depend on the TAD divisor (ADCS) selection. The Tcy counts shown in the timing diagram above apply to this example only. Refer to [Table 3](#) for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, ADGO    ; Start ADC conversion
                        ; Provide 86
                        ; instruction cycle
                        ; delay here
BCF    ADCON0, ADGO    ; Terminate the
                        ; conversion manually
MOVF   ADRESH, W      ; Read conversion
                        ; result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to [Table 3](#).

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS BY TAD SELECTION

TAD	Instruction Cycle Delay Counts
Fosc/64	172
Fosc/32	86
Fosc/16	43

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

6. Module: Enhanced Capture Compare PWM (ECCP)

6.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the Pxm<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

6.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

7. Module: Resets

7.1 Reset under Low-Power Conditions

This issue pertains only to the F product version, PIC16F1826/1827. The LF product version, PIC16LF1826/1827, is not affected by this issue in any way.

When employing any one of the low-power oscillators (ECL mode, LP mode, LFINTOSC, or Timer1 Oscillator as alternate system clock source) at temperatures of -20°C or colder while, at the same time, the source voltage supplied to the VDD pin drops below 2.7 volts, the device may experience a Power-on Reset (POR). Also, when the source voltage supplied to the VDD pin is below 2.7 volts, at temperatures of -20°C or colder, and a SLEEP instruction is executed, the device may experience a Power-on Reset (POR) upon entering Sleep mode, regardless of the type of clock source being used or which power-managed mode is being employed.

Work around

There are three separate work-arounds and one recommendation available to avoid this Reset condition. Employing any one of these will avoid this reset condition.

1. Enabling the Brown-out Reset (BOR) circuitry.
2. Enabling the Fixed Voltage Reference (FVR) module.
3. Maintaining a source voltage (VDD) to the device above 2.7 volts when operating at temperatures of -20°C or colder.
4. Use the LF product version (PIC16LF1826/1827) when the VDD required is between 1.8V and 3.6V.

The 'Affected Silicon Revisions' below refers only to the F product version, PIC16F1826/1827.

Affected Silicon Revisions

A2	A3	A4	A5				
	X						

8. Module: Timer1

8.1 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

PIC16(L)F1826/1827

9. Module: BOR

9.1 BOR Reset

This issue affects only the PIC16LF1826/1827 devices. The device may undergo a BOR Reset when waking-up from Sleep and BOR is re-enabled. A BOR Reset may also occur the moment the software BOR is enabled.

Under certain voltage and temperature conditions and when either SBODEN or BOR_NSLEEP is selected, the devices may occasionally reset when waking-up from Sleep or BOR is enabled.

Work around

- Method 1: In applications where BOR use is not critical, turn off the BOR in the Configuration Word.
- Method 2: Set the FVREN bit of the FVRCON register. Maintain this bit on at all times.
- Method 3: When BOR module is needed only during run-time, use the software-enabled BOR by setting the SBODEN option on the Configuration Word. BOR should be turned off by software before Sleep, then follow the below sequence for turning BOR on after Wake-up:
- Wake-up event occurs;
 - Turn on FVR (FVREN bit of the FVRCON register);
 - Wait until FVRRDY bit is set;
 - Wait 15 μ s after the FVR Ready bit is set;
 - Manually turn on the BOR.
- Method 4: Use the software-enabled BOR as described in Method 3, but use the following sequence:
- Switch to internal 32 kHz oscillator immediately before Sleep;
 - Upon wake-up, turn on FVR (FVREN bit of the FVRCON register);
 - Manually turn on the BOR;
 - Switch the clock back to the preferred clock source.

Note: When using the software BOR follow the steps in Methods 3 or 4 above when enabling BOR for the first time during program execution.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41391D):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Temperature Indicator

In Register 14-1: FVRCON: Fixed Voltage Reference Control Register, the TSEN and TSRNG bits that enable and select the range for the temperature indicator module are missing. The corrected register table is shown below.

REGISTER 14-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVREN	FVRRDY ⁽¹⁾	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	FVREN: Fixed Voltage Reference Enable bit 0 = Fixed Voltage Reference is disabled 1 = Fixed Voltage Reference is enabled
bit 6	FVRRDY: Fixed Voltage Reference Ready Flag bit ⁽¹⁾ 0 = Fixed Voltage Reference output is not ready or not enabled 1 = Fixed Voltage Reference output is ready for use
bit 5	TSEN: Temperature Indicator Enable bit ⁽³⁾ 0 = Temperature Indicator is disabled 1 = Temperature Indicator is enabled
bit 4	TSRNG: Temperature Indicator Range Selection bit ⁽³⁾ 0 = VOUT = VDD - 2VT (Low Range) 1 = VOUT = VDD - 4VT (High Range)
bit 3-2	CDAFVR<1:0>: Comparator and DAC Fixed Voltage Reference Selection bit 00 = Comparator and DAC Fixed Voltage Reference Peripheral output is off. 01 = Comparator and DAC Fixed Voltage Reference Peripheral output is 1x (1.024V) 10 = Comparator and DAC Fixed Voltage Reference Peripheral output is 2x (2.048V) ⁽²⁾ 11 = Comparator and DAC Fixed Voltage Reference Peripheral output is 4x (4.096V) ⁽²⁾
bit 1-0	ADFVR<1:0>: ADC Fixed Voltage Reference Selection bit 00 = ADC Fixed Voltage Reference Peripheral output is off. 01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V) 10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V) ⁽²⁾ 11 = ADC Fixed Voltage Reference Peripheral output is 4x (4.096V) ⁽²⁾

- Note 1:** FVRRDY is always '1' on devices with LDO (PIC16F1826/27).
Note 2: Fixed Voltage Reference output cannot exceed VDD.
Note 3: See Section 15.0, "Temperature Indicator Module", for additional information.

PIC16(L)F1826/1827

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2009)

Initial release of this document.

Rev B Document (02/2010)

Added PIC16F1826 and PIC16F1827 to this errata;
Added Rev. A3 for PIC16F/LF1826/1827.

Data Sheet Clarifications: Added Modules 1 thru 5.

Rev C Document (05/2010)

Added Modules 5, 6 and 7.

Rev D Document (06/2010)

Removed Module 6 (Oscillator); Added Modules 7
(Resets) and 8 (Timer1).

Data Sheet Clarifications: Removed Modules 1 to 5.

Rev E Document (07/2010)

Revised Module 5.1; Other minor corrections.

Rev F Document (09/2010)

Added Silicon Revision A4.

Rev G Document (02/2011)

Added Module 9.

Rev H Document (05/2011)

Added Silicon Revision A5.

Data Sheet Clarifications: Added Module 1.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICTail, REAL ICE, rLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009-2011, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-61341-194-0

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==**



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3180
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-213-7830
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

05/02/11