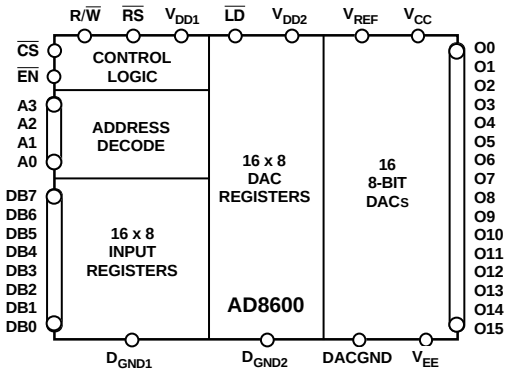
16-Channel, 8-Bit Multiplying DAC

AD8600

FEATURES
16 Independently Addressable Voltage Outputs
Full-Scale Set by External Reference
2 μs Settling Time
Double Buffered 8-Bit Parallel Input
High Speed Data Load Rate
Data Readback
Operates from Single +5 V
Optional ±6 V Supply Extends Output Range

APPLICATIONS
Phased Array Ultrasound & Sonar
Power Level Setting
Receiver Gain Setting
Automatic Test Equipment
LCD Clock Level Setting

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8600 contains 16 independent voltage output digital-to-analog converters that share a common external reference input voltage. Each DAC has its own DAC register and input register to allow double buffering. An 8-bit parallel data input, four address pins, a $\overline{CS}$ select, a $\overline{LD}$, $\overline{EN}$, R/$\overline{W}$, and $\overline{RS}$ provide the digital interface.

The AD8600 is constructed in a monolithic CBCMOS process which optimizes use of CMOS for logic and bipolar for speed and precision. The digital-to-analog converter design uses voltage mode operation ideally suited to single supply operation. The internal DAC voltage range is fixed at DACGND to V_{REF}. The voltage buffers provide an output voltage range that approaches ground and extends to 1.0 V below V_{CC}. Changes in reference voltage values and digital inputs will settle within ±1 LSB in 2 μs.

Data is preloaded into the input registers one at a time after the internal address decoder selects the input register. In the write mode (R/$\overline{W}$ low) data is latched into the input register during the positive edge of the $\overline{EN}$ pulse. Pulses as short as 40 ns can be used to load the data. After changes have been submitted to the input registers, the DAC registers are simultaneously updated by a common load $\overline{EN} \times \overline{LD}$ strobe. The new analog output voltages simultaneously appear on all 16 outputs.

At system power up or during fault recovery the reset ($\overline{RS}$) pin forces all DAC registers into the zero state which places zero volts at all DAC outputs.

The AD8600 is offered in the PLCC-44 package. The device is designed and tested for operation over the extended industrial temperature range of –40°C to +85°C.

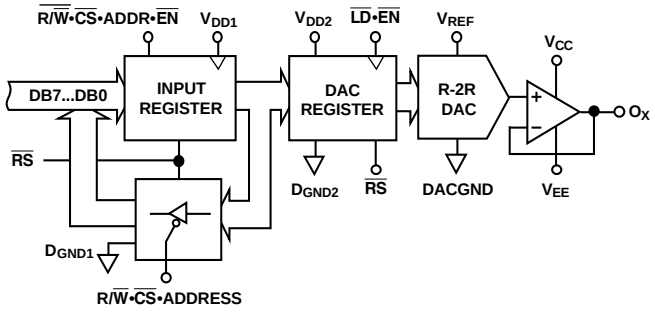


Figure 1. Equivalent DAC Channel

REV. 0

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AD8600–SPECIFICATIONS

SINGLE SUPPLY (@ $V_{DD1} = V_{DD2} = V_{CC} = +5$ V ± 5%, $V_{EE} = 0$ V, $V_{REF} = +2.500$ V, $-40°C \le T_A \le +85°C$, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE[1]						
Resolution	N		8			Bits
Relative Accuracy[2]	INL		–1	±1/2	+1	LSB
Differential Nonlinearity[2]	DNL	Guaranteed Monotonic	–1	±1/4	+1	LSB
Full-Scale Voltage	V_{FS}	Data = FF_H	2.480	2.490	2.500	V
Full-Scale Tempco	TCV_{FS}	Data = FF_H		±20		ppm/°C
Zero Scale Error	V_{ZSE}	Data = 00_H, $\overline{RS}$ = "0," T_A = +25°C			+3.5	LSB
	V_{ZSE}	Data = 00_H, $\overline{RS}$ = "0"			+5	LSB
Reference Input Resistance	R_{REF}	Data = AB_H	1.2	2		kΩ
ANALOG OUTPUT						
Output Voltage Range[2]	OVR_{SS}	V_{REF} = +2.5 V	0.000		2.500	V
Output Current	I_{OUT}	Data = 80_H		±2		mA
Capacitive Load	C_L	No Oscillation		50		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Logic Input Current	I_{IL}				10	µA
Logic Input Capacitance[3]	C_{IL}				10	pF
LOGIC OUTPUTS						
Logic Out High Voltage	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Out Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
AC CHARACTERISTICS[3]						
Slew Rate	SR	For ΔV_{REF} or FS Code Change	4	7		V/µs
Voltage Output Settling Time[2]	t_{S1}	±1 LSB of Final Value, Full-Scale Data Change		2		µs
Voltage Output Settling Time[2]	t_{S2}	±1 LSB of Final Value, ΔV_{REF} = 1 V, Data = FF_H		2		µs
POWER SUPPLIES						
Positive Supply Current	I_{CC}	V_{IH} = 5 V, V_{IL} = 0 V, No Load		24	35	mA
Logic Supply Currents	$I_{DD1\&2}$	V_{IH} = 5 V, V_{IL} = 0 V, No Load			0.1	mA
Power Dissipation	P_{DISS}	V_{IH} = 5 V, V_{IL} = 0 V, No Load		120	175	mW
Power Supply Sensitivity	PSS	ΔV_{CC} = ±5%			0.007	%/%
Logic Power Supply Range	V_{DDR}		4.75		5.25	V
Positive Power Supply Range[3]	V_{CCR}		V_{DD}		7.0	V

NOTES

[1]When V_{REF} = 2.500 V, 1 LSB = 9.76 mV.

[2]Single supply operation does not include the final 2 LSBs near analog ground. If this performance is critical, use a negative supply (V_{EE}) pin of at least –0.7 V to –5.25 V. Note that for the INL measurement zero-scale voltage is extrapolated using codes 7_{10} to 80_{10}.

[3]Guaranteed by design not subject to production test.

Specifications subject to change without notice.

DUAL SUPPLY (@ $V_{DD1} = V_{DD2} = V_{CC} = +5\ V \pm 5\%$, $V_{EE} = -5\ V \pm 5\%$, $V_{REF} = +3.500\ V$, $-40°C \le T_A \le +85°C$, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE[1]						
Resolution	N		8			Bits
Total Unadjusted Error	TUE	All Other DACs Loaded with Data = 55_H	–1	±3/4	+1	LSB
Relative Accuracy	INL		–1	±1/2	+1	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic	–1	±1/4	+1	LSB
Full-Scale Voltage	V_{FS}	Data = FF_H, V_{REF} = +3.5 V	3.473	3.486	3.500	V
Full-Scale Voltage Error	V_{FSE}	Data = FF_H, V_{REF} = +3.5 V	–1		+1	LSB
Full-Scale Tempco	TCV_{FS}	Data = FF_H, V_{REF} = +3.5 V		±20		ppm/°C
Zero Scale Error	V_{ZSE}	Data = 00_H, $\overline{RS}$ = "0," T_A = +25°C	–2	±1	+2	mV
Zero Scale Error	V_{ZSE}	Data = 00_H, All Other DACs Data = 00_H	–1		+1	LSB
Zero Scale Error	V_{ZSE}	Data = 00_H, All Other DACs Data = 55_H		±1/2		LSB
Zero Scale Tempco	TCV_{ZS}	Data = 00_H, V_{CC} = +5 V, V_{EE} = –5 V		±10		µV/°C
Reference Input Resistance	R_{REF}	Data = AB_H	1.2	2		kΩ
Reference Input Capacitance[2]	C_{REF}	Data = AB_H			240	pF
ANALOG OUTPUT						
Output Voltage Range	OVR_1	V_{REF} = +3.5 V	0.000		3.500	V
Output Voltage Range[2]	OVR_2	$V_{CC} = V_{DD2}$ = +7 V, V_{EE} = –0.7 V, V_{REF} = 5 V	0.000		5.000	V
Output Current	I_{OUT}	Data = 80_H		±2		mA
Capacitive Load[2]	C_L	No Oscillation		50		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Logic Input Current	I_{IL}				10	µA
Logic Input Capacitance[2]	C_{IL}				10	pF
LOGIC OUTPUTS						
Logic Out High Voltage	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Out Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
AC CHARACTERISTICS[2]						
Reference In Bandwidth	BW	–3 dB Frequency, $V_{REF} = 2.5\ V_{DC} + 0.1\ V_{AC}$	500			kHz
Slew Rate	SR	For ΔV_{REF} or FS Code Change	4	7		V/µs
Voltage Noise Density	e_N	f = 1 kHz, V_{REF} = 0 V		46		nV/√Hz
Digital Feedthrough	FT	Digital Inputs to DAC Outputs		10		nVs
Voltage Output Settling Time[3]	t_{S1}	±1 LSB of Final Value, FS Data Change		1	2	µs
Voltage Output Settling Time[3]	t_{S2}	±1 LSB of Final Value, ΔV_{REF} = 1 V, Data = FF_H		1	2	µs
POWER SUPPLIES						
Positive Supply Current	I_{CC}	V_{IH} = 5 V, V_{IL} = 0 V, V_{EE} = –5 V, No Load		22	35	mA
Negative Supply Current	I_{EE}	V_{IH} = 5 V, V_{IL} = 0 V, V_{EE} = –5 V, No Load		22	35	mA
Logic Supply Currents	$I_{DD1\&2}$	V_{IH} = 5 V, V_{IL} = 0 V, V_{EE} = –5 V, No Load			0.1	mA
Power Dissipation[4]	P_{DISS}	V_{IH} = 5 V, V_{IL} = 0 V, V_{EE} = –5 V, No Load		225	350	mW
Power Supply Sensitivity	PSS	ΔV_{CC} & ΔV_{EE} = ±5%			0.007	%/%
Logic Power Supply Range	V_{DDR}		4.75		5.25	V
Pos Power Supply Range[2]	V_{CCR}		V_{DD}		7.0	V
Neg Power Supply Range[2]	V_{EER}		–5.25		0.0	V

NOTES
[1]When V_{REF} = +3.500 V, 1 LSB = 13.67 mV.
[2]Guaranteed by design not subject to production test.
[3]Settling time test is performed using R_L = 50 kΩ and C_L = 35 pF.
[4]Power Dissipation is calculated using $5\ V \times (I_{DD} + |I_{SS}| + I_{DD1} + I_{DD2})$.
Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_{DD1} = V_{DD2} = V_{CC} = +5\ V \pm 5\%$, $V_{EE} = -5\ V$, $V_{REF} = +3.500\ V$, $-40°C \le T_A \le +85°C$, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INTERFACE TIMING[1, 2]						
Clock ($\overline{EN}$) Frequency	f_{CLK}	Data Loading			12.5	MHz
Clock ($\overline{EN}$) High Pulse Width	t_{CH}		40			ns
Clock ($\overline{EN}$) LowPulse Width	t_{CL}		40			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		10			ns
Address Setup Time	t_{AS}		0			ns
Address Hold Time	t_{AH}		0			ns
Valid Address to Data Valid	t_{AD}				160	ns
Load Enable Setup Time	t_{LS}		0			ns
Load Enable Hold Time	t_{LH}		0			ns
Read/Write to Clock ($\overline{EN}$)	t_{RWC}		30			ns
Read/Write to DataBus Hi-Z	t_{RWZ}				120	ns
Read/Write to DataBus Active	t_{RWD}				120	ns
Clock ($\overline{EN}$) to Read/Write	t_{TWH}		0			ns
Clock ($\overline{EN}$) to Chip Select	t_{TCH}		0			ns
Chip Select to Clock ($\overline{EN}$)	t_{CSC}		30			ns
Chip Select to Data Valid	t_{CSD}				120	ns
Chip Select to DataBus Hi-Z	t_{CSZ}				150	ns
Reset Pulse Width	t_{RS}		25			ns

NOTES
[1]Guaranteed by design not subject to production test.
[2]All logic input signals have maximum rise and fall times of 2 ns.
Specifications subject to change without notice.

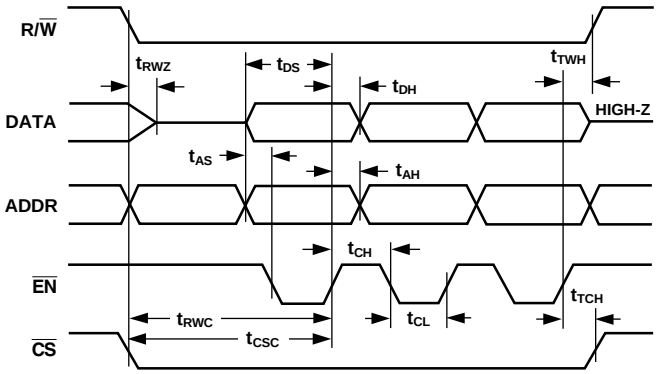


Figure 2. Write Timing

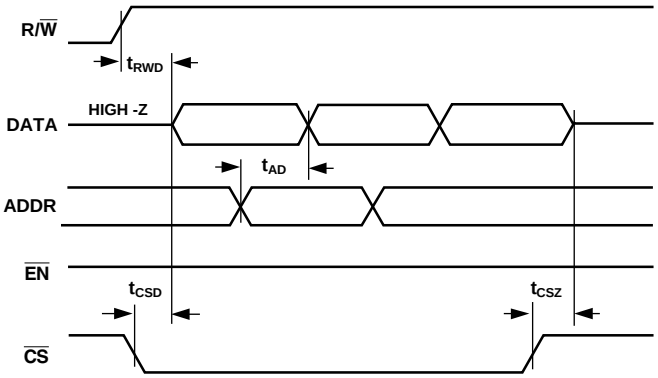


Figure 3. Readback Timing

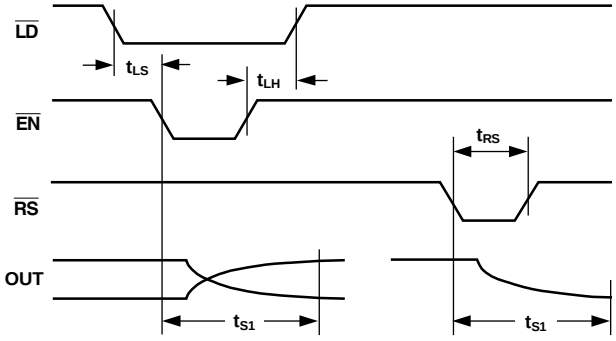


Figure 4. Write to DAC Register & Voltage Output Settling Timing ($\overline{CS}$= High, Prevents Input Register Changes)

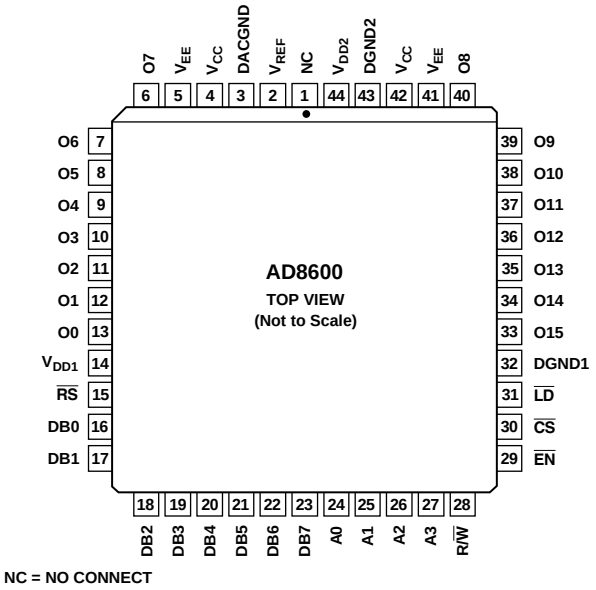
ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD1} (Digital Supply) to GND . . . . . –0.3 V, +7 V
V_{DD2} (DAC Buffer/Driver Supply) . . . . . –0.3 V, +7 V
V_{CC} (Analog Supply) to GND . . . . . –0.3 V, +7 V
V_{EE} (Analog Supply) to GND . . . . . +0.3 V, –7 V
V_{REF} to GND . . . . . –0.3 V, V_{CC} + 0.3 V
V_{DD2} to V_{REF} . . . . . –0.3 V
V_{OUT} to GND . . . . . V_{CC}
Short Circuit Duration
  V_{OUT} to GND or Power Supplies[1] . . . . . Continuous
Digital Input/Output Voltage to GND . . . –0.3 V, V_{DD} + 0.3 V
Thermal Resistance–Theta Junction-to-Ambient (θ_{JA})
  PLCC-44 . . . . . 47°C/W
Package Power Dissipation . . . . . $(T_J - T_A)/\theta_{JA}$
Maximum Junction Temperature T_J max . . . . . 150°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

NOTE
[1]No more than four outputs may be shorted to power or GND simultaneously.

PIN CONFIGURATION



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature	Package Description	Package Option
AD8600AP	–40°C to +85°C	44-Lead PLCC	P-44A
AD8600Chips	+25°C	Die*	

*For die specifications contact your local Analog Devices sales office.
The AD8600 contains 5782 transistors.

PIN DESCRIPTION

Pin No.	Name	Description
1	NC	No Connection
2	V_{REF}	Reference input voltage common to all DACs.
3	DACGND	DAC Analog Ground Return. Sets analog zero-scale voltage.
4	V_{CC}	Output Amplifier Positive Supply
5	V_{EE}	Output Amplifier Negative Supply
6	O7	DAC Channel Output No. 7
7	O6	DAC Channel Output No. 6
8	O5	DAC Channel Output No. 5
9	O4	DAC Channel Output No. 4
10	O3	DAC Channel Output No. 3
11	O2	DAC Channel Output No. 2
12	O1	DAC Channel Output No. 1
13	O0	DAC Channel Output No. 0
14	V_{DD1}	Digital Logic Power Supply
15	$\overline{RS}$	Active Low Reset Input Pin
16	DB0	Data Bit Zero I/O (LSB)
17	DB1	Data Bit I/O
18	DB2	Data Bit I/O
19	DB3	Data Bit I/O
20	DB4	Data Bit I/O
21	DB5	Data Bit I/O
22	DB6	Data Bit I/O
23	DB7	Most Significant Data Bit I/O (MSB)
24	A0	Address Bit Zero (LSB)
25	A1	Address Bit
26	A2	Address Bit
27	A3	Most Significant Addr Bit (MSB)
28	R/$\overline{W}$	Read/Write Select Control Input
29	$\overline{EN}$	Active Low Enable Clock Strobe
30	$\overline{CS}$	Chip Select Input
31	$\overline{LD}$	DAC Register Load Strobe
32	DGND1	Digital Ground Input No. 1
33	O15	DAC Channel Output No. 15
34	O14	DAC Channel Output No. 14
35	O13	DAC Channel Output No. 13
36	O12	DAC Channel Output No. 12
37	O11	DAC Channel Output No. 11
38	O10	DAC Channel Output No. 10
39	O9	DAC Channel Output No. 9
40	O8	DAC Channel Output No. 8
41	V_{EE}	Output Amplifier Negative Supply
42	V_{CC}	Output Amplifier Positive Supply
43	DGND2	Digital Ground Input No. 2
44	V_{DD2}	DAC Analog Supply Voltage

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8600 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TRANSFER EQUATIONS

Output Voltage

$$O_i = D \times \frac{V_{REF}}{256}$$

where *i* is the DAC channel number and *D* is the decimal value of the DAC register data.

Table I. Truth Table

$\overline{EN}$	R/$\overline{W}$	$\overline{CS}$	$\overline{LD}$	$\overline{RS}$	Operation
					Write to DAC Register
–	X	H	L	H	Update DAC Register
L	X	H	–	H	Update DAC Register
+	X	H	L	H	Latches DAC Register
L	X	H	+	H	Latches DAC Register
L	L	L	L	H	DAC Register Transparent
					Write to Input Register
L	L	L	H	H	Load Data to Input Register at Decoded Address
+	L	L	H	H	Latches Data in Input Register at Decoded Address
L	L	+	H	H	Latches Data in Input Register at Decoded Address
					Readback Input Registers
X	H	L	H	H	Input Register Readback (Data Access)
X	H	+	H	H	Hi-Z Readback Disconnects from Bus
X	X	H	X	X	Hi-Z on Data Bus
					Reset
X	X	X	X	L	Clear All Registers to Zero, V_{OUT} = 0 V
X	X	H	H	+	Latches All Registers to Zero
L	X	L	H	+	$\overline{CS}$ = Low; Input Register Ready for R/$\overline{W}$, DAC Register Latched to Zero

NOTES
[1]+ symbol means positive edge of control input line.
[2]– symbol means negative edge of control input line.

Decoded DAC Register

$$O_i = A$$

where *A* is the decimal value of the decoded address bits A3, A2, A1, A0 (LSB).

Address, $\overline{CS}$, R/$\overline{W}$ and data inputs should be stable prior to activation of the active low $\overline{EN}$ input. Input registers are transparent when $\overline{EN}$ is low. When $\overline{EN}$ returns high, data is latched into the decoded input register. When the load strobe $\overline{LD}$ and $\overline{EN}$ pins are active low, all input register data is transferred to the DAC registers. The DAC registers are transparent while they are enabled.

Table II. Address Decode Table

A3 (MSB)	A2	A1	A0 (LSB)	Addr Code (Hex)	DAC Updated
(Binary)					
0	0	0	0	0	O0
0	0	0	1	1	O1
0	0	1	0	2	O2
0	0	1	1	3	O3
0	1	0	0	4	O4
0	1	0	1	5	O5
0	1	1	0	6	O6
0	1	1	1	7	O7
1	0	0	0	8	O8
1	0	0	1	9	O9
1	0	1	0	A	O10
1	0	1	1	B	O11
1	1	0	0	C	O12
1	1	0	1	D	O13
1	1	1	0	E	O14
1	1	1	1	F	O15

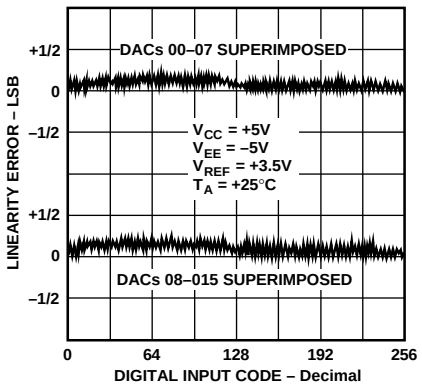


Figure 5. Linearity Error vs. Digital Code

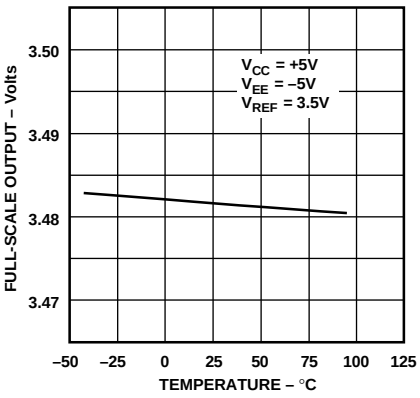


Figure 6. Full-Scale Voltage vs. Temperature

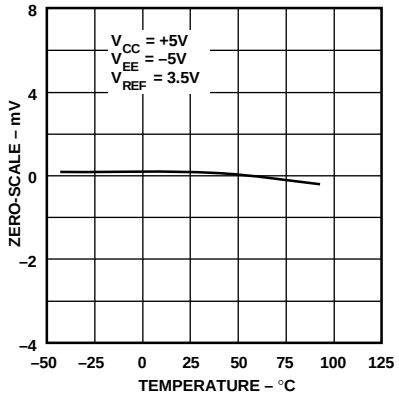


Figure 7. Zero-Scale Voltage vs. Temperature

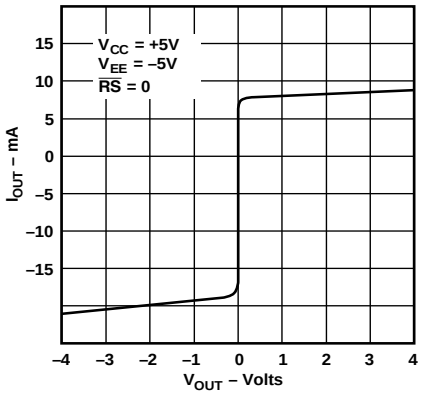


Figure 8. Output Current vs. Voltage

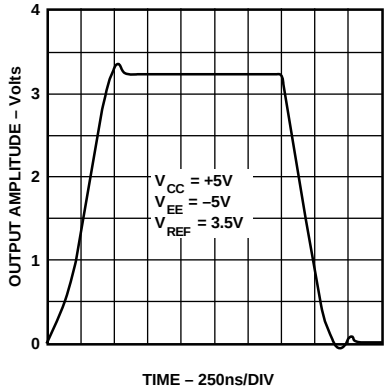


Figure 9. Full-Scale Settling Time

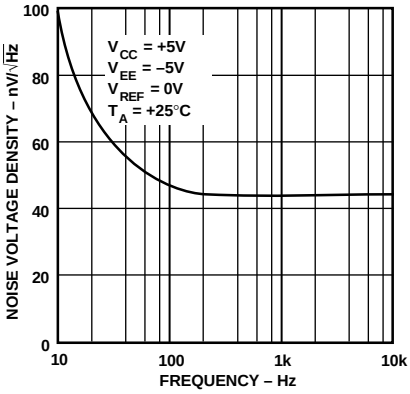


Figure 10. Voltage Noise Density vs. Frequency

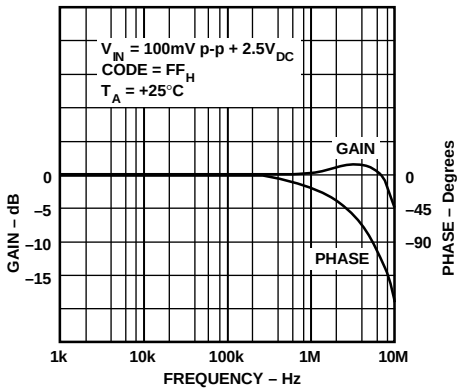


Figure 11. Gain & Phase vs. Frequency

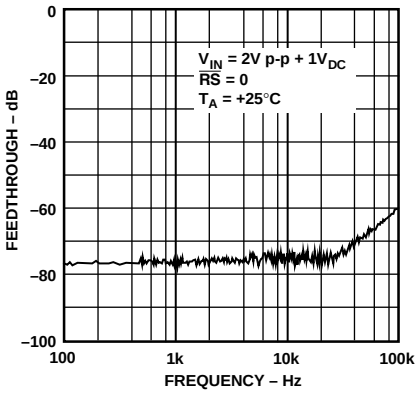


Figure 12. AC Feedthrough vs. Frequency

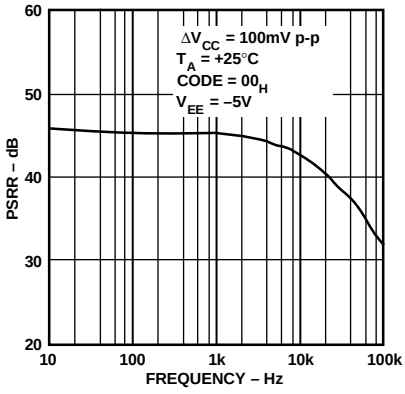


Figure 13. PSRR vs. Frequency

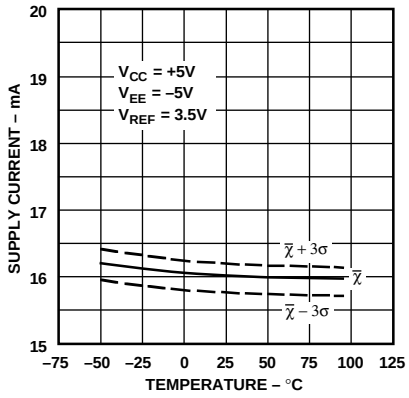


Figure 14. Supply Current vs. Temperature

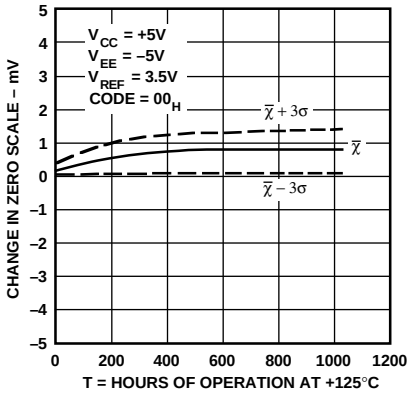


Figure 15. Output Voltage Drift Accelerated by Burn-In

Operation

The AD8600 is a 16-channel voltage output, 8-bit digital to analog converter. The AD8600 operates from a single +5 V supply, or for a wider output swing range, the part can operate from dual supplies of ±5 V or ±6 V or a single supply of +7 V. The DACs are based upon a unique R-2R ladder structure* that removes the possibility of current injection from the reference to ground during code switching. Each of the 8-bit DACs has an output amplifier to provide 16 low impedance outputs. With a single external reference, 16 independent dc output levels can be programmed through a parallel digital interface. The interface includes 4 bits of address (A0–A3), 8 bits of data (DB0–DB7), a read/write select pin (R/$\overline{W}$), an enable clock strobe ($\overline{EN}$), a DAC register load strobe ($\overline{LD}$), and a chip select pin ($\overline{CS}$). Additionally a reset pin ($\overline{RS}$) is provided to asynchronously reset all 16 DACs to 0 V output.

D/A Converter Section

The internal DAC is an 8-bit voltage mode device with an output that swings from DACGND to the external reference voltage, V_{REF}. The equivalent schematic of one of the DACs is shown in Figure 16. The DAC uses an R-2R ladder to ensure accuracy and linearity over the full temperature range of the part. The switches shown are actually N and P-channel MOSFETs to allow maximum flexibility and range in the choice of reference

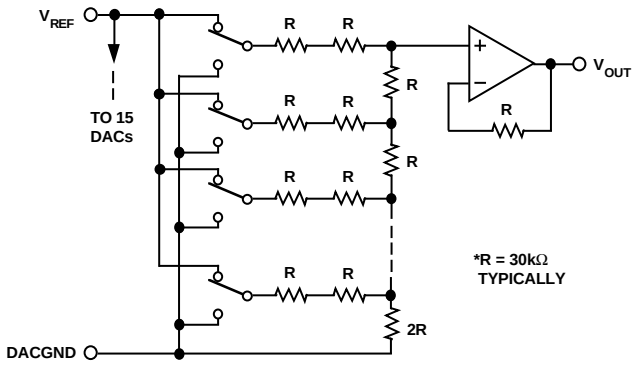


Figure 16. Equivalent Schematic of Analog Channel

voltage. The switches' low ON resistance and matching is important in maintaining the accuracy of the R-2R ladder.

Amplifier Section

The output of the DAC ladder is buffered by a rail-to-rail output amplifier. This amplifier is configured as a unity gain follower as shown in Figure 16. The input stage of the amplifier contains a PNP differential pair to provide low offset drift and noise. The output stage is shown in Figure 17. It employs complementary bipolar transistors with their collectors connected to the output to provide rail-to-rail operation. The NPN transistor enters into saturation as the output approaches the negative rail. Thus, in single supply, the output low voltage is limited by the saturation voltage of the transistor. For the transistors used in the AD8600, this is approximately 40 mV. The AD8600 was not designed to swing to the positive rail in contrast to some of ADI's other DACs (for example, the AD8582). The output stage of the amplifier is actually capable of swinging to the positive rail, but the input stage limits this swing to approximately 1.0 V below V_{CC}.

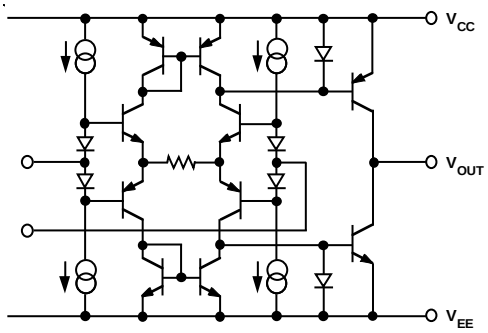


Figure 17. Equivalent Analog Output Circuit

During normal operation, the output stage can typically source and sink ±1 mA of current. However, the actual short circuit current is much higher. In fact, each DAC is capable of sourcing 20 mA and sinking 8 mA during a short condition. The absolute maximum ratings state that, at most, four DACs can be shorted simultaneously. This restriction is due to current densities in the metal traces. If the current density is too high, voltage drops in the traces will cause a loss in linearity performance for the other DACs in the package. Thus to ensure long-term reliability, no more than four DACs should be shorted simultaneously.

*Patent Pending.

Power Supply and Grounding Considerations

The low power consumption of the AD8600 is a direct result of circuit design optimizing using a CBCMOS process. The overall power dissipation of 120 mW translates to a total supply current of only 24 mA for 16 DACs. Thus, each DAC consumes only 1.5 mA. Because the digital interface is comprised entirely of CMOS logic, the power dissipation is dependent upon the logic input levels. As expected for CMOS, the lowest power dissipation is achieved when the input level is either close to ground or +5 V. Thus, to minimize the power consumption, CMOS logic should be used to interface to the AD8600.

The AD8600 has multiple supply pins. V_{CC} (Pins 4 and 42) is the output amplifiers' positive supply, and V_{EE} (Pins 5 and 41) the amplifiers' negative supply. The digital input circuitry is powered by V_{DD1} (Pin 14), and finally the DAC register and R-2R ladder switches are powered by V_{DD2} (Pin 44). To minimize noise feedthrough from the supplies, each supply pin should be decoupled with a 0.1 µF ceramic capacitor close to the pin. When applying power to the device, it is important for the digital supply, V_{DD2}, to power on before the reference voltage and for V_{REF} to remain less than 0.3 V above V_{DD2} during normal operation. Otherwise, an inherent diode will energize, and it could damage the AD8600.

In order to improve ESD resistance, the AD8600 has several ESD protection diodes on its various pins. These diodes shunt ESD energy to the power supplies and protect the sensitive active circuitry. During normal operation, all the ESD diodes are reversed biased and do not affect the part. However, if overvoltages occur on the various inputs, these diodes will energize. If the overvoltage is due to ESD, the electrical spike is typically short enough so that the part is not damaged. However, if the overvoltage is continuous and has sufficient current, the part could be damaged. To protect the part, it is important not to forward bias any of the ESD protection diodes during normal operation or during power up. Figure 18 shows the location of these diodes. For example, the digital inputs have diodes connected to V_{CC} and from DGND1. Thus, the voltage on any digital input should never exceed the analog supply or drop below ground, which is also indicated in the absolute maximum ratings.

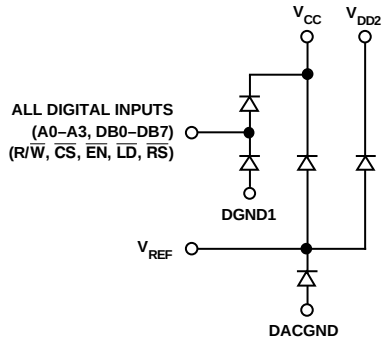


Figure 18. ESD Protection Diode Locations

Attention should be paid to the ground pins of the AD8600 to ensure that noise is not introduced to the output. The pin labeled DACGND (Pin 3) is actually the ground for the R-2R ladder, and because of this, it is important to connect this pin to a high quality analog ground. Ideally, the analog ground should be an actual ground plane. This helps create a low impedance, low noise ground to maintain accuracy in the analog circuitry.

The digital ground pins (DGND1 at Pin 32 and DGND2 at Pin 43) provide the ground reference for the internal digital circuitry and latches. The first thought may be to connect both of these pins to the system digital ground. However, this is not the best choice because of the high noise typically found on a system's digital ground. This noise can feed through to the output through the DAC's ground pins. Instead, DGND1 and DGND2 should be connected to the analog ground plane. The actual switching current in these pins is small and should not degrade the analog ground.

5 V Output Swing

The output swing is limited to 1.0 V below the positive supply. This gives a maximum output of +4.0 V on a +5 V supply. To increase the output range, the analog supply, V_{CC}, and the DAC ladder supply, V_{DD2}, can be increased to +7 V. This allows an output of +5 V with a 5 V reference. V_{DD1} should remain at +5 V to ensure that the input logic levels do not change.

Reference Input Considerations

The AD8600 is designed for one reference to drive all 16 DACs. The reference pin (V_{REF}) is connected directly to the R-2R ladders of each DAC. With 16 DACs in parallel, the input impedance is typically 2 kΩ and a minimum of 1.2 kΩ. The input resistance is code dependent. Thus, the chosen reference device must be able to drive this load. Some examples of +2.5 V references that easily interface to the AD8600 are the REF43, AD680, and AD780. The unique architecture ensures that the reference does not have to supply "shoot through" current, which is a condition in some voltage mode DACs where the reference is momentarily connected to ground through the CMOS switches. By eliminating this possibility, all 16 DACs in the AD8600 can easily be driven from a single reference.

Interface Timing and Control

The AD8600 employs a double buffered DAC structure with each DAC channel having a unique input register and DAC register as shown in the diagram entitled "Equivalent DAC Channel" on the first page of the data sheet. This structure allows maximum flexibility in loading the DACs. For example, each DAC can be updated independently, or, if desired, all 16 input registers can be loaded, followed by a single $\overline{LD}$ strobe to update all 16 DACs simultaneously. An additional feature is the ability to read back from the input register to verify the DAC's data.

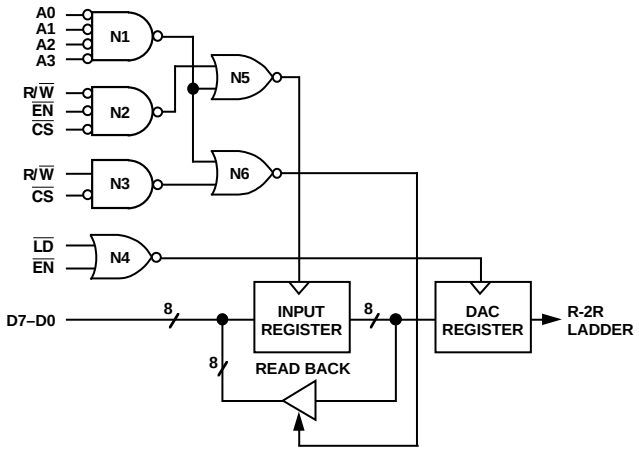


Figure 19. Logic Interface Circuit for DAC Channel 0

The interface logic for a single DAC channel is shown in Figure 19. This figure specifically shows the logic for Channel 0; however, by changing the address input configuration to gate N1, the other 15 channels are achieved. All of the logic for the AD8600 is level sensitive and not edge triggered. For example, if all the control inputs ($\overline{CS}$, R/$\overline{W}$, $\overline{EN}$, $\overline{LD}$) are low, the input and DAC registers are transparent and any change in the digital inputs will immediately change the DAC's R-2R ladder.

Table I details the different logic combinations and their effects. Chip Select ($\overline{CS}$), Enable ($\overline{EN}$) and R/$\overline{W}$ must be low to write the input register. During this time that all three are low, any data on DB7–DB0 changes the contents of the input register. This data is not latched until either $\overline{EN}$ or $\overline{CS}$ returns high. The data setup and hold times shown in the timing diagrams must be observed to ensure that the proper data is latched into the input register.

To load multiple input registers in the fastest time possible, both R/$\overline{W}$ and $\overline{CS}$ should remain low, and the $\overline{EN}$ line be used to "clock" in the data. As the write timing diagram shows, the address should be updated at the same time as $\overline{EN}$ goes low. Before $\overline{EN}$ returns high, valid data must be present for a time equal to the data setup time (t_{DS}), and after $\overline{EN}$ returns high, the data Hold Time (t_{DH}) must be maintained. If these minimum times are violated, invalid data may be latched into the input register. This cycle can be repeated 16 times to load all of the DACs. The fastest interface time is equal to the sum of the low and high times (t_{CL} and t_{CH}) for the $\overline{EN}$ input, which gives a minimum of 80 ns. Because the $\overline{EN}$ input is used to clock in the data, it is often referred to as the clock input, and the timing specifications give a maximum clock frequency of 12.5 MHz, which is just the reciprocal of 80 ns.

After all the input registers have been loaded, a single load strobe will transfer the contents of the input registers to the DAC registers. $\overline{EN}$ must also be low during this time. If the address or data on the inputs could change, then $\overline{CS}$ should be high during this time to ensure that new data is not loaded into an input register. Alternatively, a single DAC can be updated by first loading its input register and then transferring that to the DAC register without loading the other 15 input registers.

The final interface option is to read data from the DAC's input registers, which is accomplished by setting R/$\overline{W}$ high and bringing $\overline{CS}$ low. Read back allows the microprocessor to verify that correct data has been loaded into the DACs. During this time $\overline{EN}$ and $\overline{LD}$ should be high. After a delay equal to t_{RWD}, the data bus becomes active and the contents of the input register are read back to the data pins, DB0–DB7. The address can be changed to look at the contents of all the input registers. Note that after an address change, the valid data is not available for a time equal to t_{AD}. The delay time is due to the internal readback buffers needing to charge up the data bus (measured with a 35 pF load). These buffers are low power and do not have high current to charge the bus quickly. When $\overline{CS}$ returns high, the data pins assume a high impedance state and control of the data lines or bus passes back to the microprocessor.

Unipolar Output Operation

The AD8600 is configured to give unipolar operation. The full-scale output voltage is equivalent to the reference input voltage minus 1 LSB. The output is dependent upon the digital code and follows Table III. The actual numbers given for the analog output are calculated assuming a +2.5 V reference.

Table III. Unipolar Code Table

DAC Binary Input MSB LSB	Analog Output
1 1 1 1 1 1 1 1	$+V_{REF}$ (255/256) = +2.49 V
1 0 0 0 0 0 0 1	$+V_{REF}$ (129/256) = +1.26 V
1 0 0 0 0 0 0 0	$+V_{REF}$ (128/256) = +1.25 V
0 1 1 1 1 1 1 1	$+V_{REF}$ (127/256) = +1.24 V
0 0 0 0 0 0 0 1	$+V_{REF}$ (001/256) = +0.01 V
0 0 0 0 0 0 0 0	$+V_{REF}$ (000/256) = +0.00 V

Bipolar Output Operation

The AD8600 can be configured for bipolar operation with the addition of an op amp for each output as shown in Figure 20. The output will now have a swing of $\pm V_{REF}$, as detailed in Table IV. This modification is only needed on those channels that require bipolar outputs. For channels which only require unipolar output, no external amplifier is needed. The OP495 quad amplifier is chosen for the external amplifier because of its low power, rail-to-rail output swing, and DC accuracy. Again, the values calculated for the analog output are based upon an assumed +2.5 V reference.

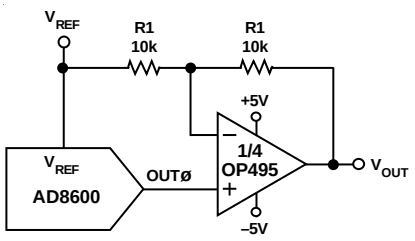


Figure 20. Circuit for Bipolar Output Operation

Table IV. Bipolar Code Table

DAC Binary Input MSB LSB	Analog Output
1 1 1 1 1 1 1 1	+2 V_{REF} (255/256) – V_{REF} = +2.49 V
1 0 0 0 0 0 0 1	+2 V_{REF} (129/256) – V_{REF} = +0.02 V
1 0 0 0 0 0 0 0	+2 V_{REF} (128/256) – V_{REF} = +0.00 V
0 1 1 1 1 1 1 1	+2 V_{REF} (127/256) – V_{REF} = –0.02 V
0 0 0 0 0 0 0 1	+2 V_{REF} (001/256) – V_{REF} = –2.48 V
0 0 0 0 0 0 0 0	+2 V_{REF} (000/256) – V_{REF} = –2.50 V

Interfacing to the 68HC11 Microcontroller

The 68HC11 is a popular microcontroller from Motorola, which is easily interfaced to the AD8600. The connections between the two components are shown in Figure 21. Port C of the 68HC11 is used as a bidirectional input/output data port to write to and read from the AD8600. Port B is used for addressing and control information. The bottom 4 LSBs of Port B are the address, and the top 4 MSBs are the control lines ($\overline{LD}$, $\overline{CS}$, $\overline{EN}$, and R/$\overline{W}$). The microcode for the 68 HC11 is shown in Figure 22. The comments in the program explain the function of each step. Three routines are included in this listing: read from the AD8600, write to the AD8600, and a continuous loop that generates a saw-tooth waveform. This loop is used in the application below.

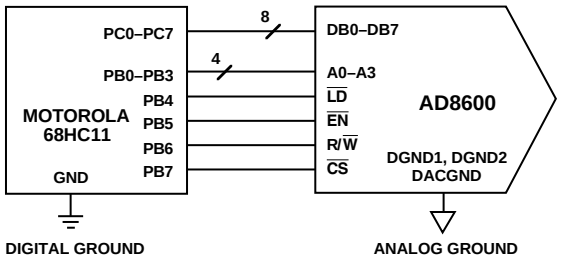


Figure 21. Interfacing the 68HC11 to the AD8600

```
* This program contains subroutines to read and write
* to the AD8600 from the 68HC11.  Additionally, a ramp
* program has been included, to continuously ramp the
* output giving a triangle wave output.
*
* The following connections need to be made:
*   68HC11       AD8600
*    GND          DGND1,2
*    PC0-PC7      DB0–DB7 respectively, data port
*    PB0-PB3      A0–A3 respectively, address port
*    PB4          LD
*    PB5          EN
*    PB6          R/W
*    PB7          CS
*
portc  equ   $1003    define port addresses
portb  equ   $1004
ddrc   equ   $1007
*
       org   $C000
read   lds   #$CFFF   subroutine to read from AD8600
*
       ldaa  #$00     initialize port c to 00000000
       staa  ddrc     configures PC0-PC7 as inputs.
*
       ldx   #$00     points to DAC address in 68HC11 memory
       ldaa  0,x      put the address in the accumulator
       adda  #$70     add the control bits to the address
*                     R/W, LD, EN are high,  CS is low.
       staa  portb    output control and address on port b.
*
       inx            points to memory location to store the data
       ldaa  portc    read data from DAC
       staa  0,x      Store this data in memory at address “x”
*
       ldy   #$1000
       bset  portb,y $f0    Set CS, LD, EN high
       jmp   $e000    Return to BUFFALO
*
*
write  lds   #$cfff   routine to write to AD8600
       ldaa  #$ff     initialize port c to 11111111
       staa  ddrc     configures PC0-PC7 as outputs.
*
       ldx   #$00     points to DAC address in 68HC11 mem
       ldaa  0,x      puts the address in the accumulator
       adda  #$30     set CS, R/W low and LD, EN high
       staa  portb    output to portb for control and address
*
       inx            points to memory location to store the data
       ldaa  0,x      load the data into the accumulator
       staa  portc    write the data to the DAC
*
       ldy   #$1000
       bclr  portb,y $30   Set LD, EN low to latch data
       bset  portb,y $b0   Bring LD, EN, CS high, write is complete
*
       jmp   $e000    Return to BUFFALO
*
*
ramp   lds   #$cfff   routine to generate a triangle wave
       ldaa  #$ff     configure port c as outputs
```

```
        staa  ddrc
*
        ldx   #$00      set x to point to the DAC address
        ldaa  0,x       load the address from 68HC11 mem
        staa  portb     set the address on portb
*                       LD, CS, EN, R/W are all low for
*                       transparent DAC loading
        ldab  #$ff      set accumulator b to 255
*
loop    ldaa  #$00      start the triangle wave at zero
        staa  portc     write the data to the AD8600
*
load    inca            increase the data by one
        staa  portc     send the new data to the AD8600
        cba             compare a to b
        bne   load      we haven't reached 255 yet
        jmp   loop      we have reached 255, so start over
```

Figure 22. 68HC11 Microcode to Interface to the AD8600.

Time Dependent Variable Gain Amplifier Using the AD600

The AD8600 is ideal for generating a control signal to set the gain of the AD600, a wideband, low noise variable gain amplifier. The AD600 (and similar parts such as the AD602 and AD603) is often used in ultrasound applications, which require the gain to vary with time. When a burst of ultrasound is applied, the reflections from near objects are much stronger than from far objects. To accurately resolve the far objects, the gain must be greater than for the near objects. Additionally, the signals take longer to reach the ultrasound sensor when reflected from a distant object. Thus, the gain must increase as the time increases.

The AD600 requires a dc voltage to adjust its gain over a 40 dB range. Since it is a dual, the two variable gain amplifiers can be cascaded to achieve 80 dB of gain. The AD8600 is used to generate a ramped output to control the gain of the AD600. The slope of the ramp should correspond to the time delay of the ultrasound signal. Since ultrasound applications often require multiple channels, the AD8600 is ideal for this application.

The circuit to achieve a time dependent variable gain amp is shown in Figure 23. The AD600's gain is controlled by differential inputs, C1LO and C1HI, with a gain constant of 32 dB/V. Thus for 40 dB of gain, the differential control input needs to be 1.25 V. In this application, the C1LO input is set at the midscale voltage of 0.625 V, which is generated by a simple voltage divider from the REF43. The AD8600's output is divided in half, generating a 0 V to 1.25 V ramp, and then applied to C1HI. This ramp sweeps the gain from 0 dB to 40 dB.

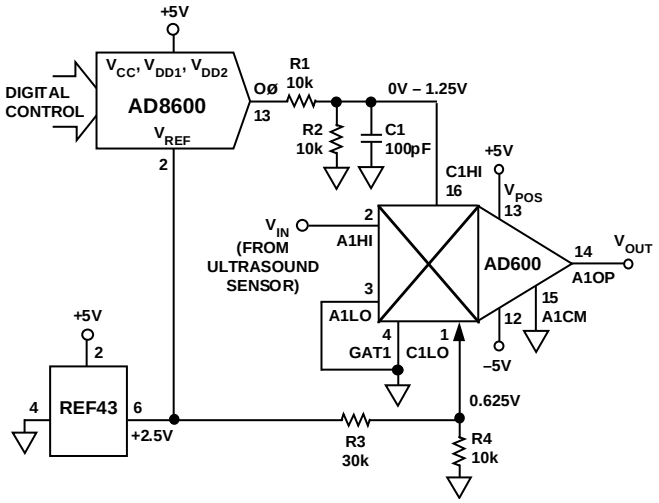


Figure 23. Ultrasound Amplifier with Digitally Controlled Variable Gain

The functionality of this circuit is shown in the scope photo in Figure 24 The top trace is the control ramp, which goes from 0 V to 1.25 V. The bottom trace is the output of the AD600. The input is actually a 12 mV p-p, 10 kHz sine wave. Thus, the bottom trace shows the envelop of this waveform to illustrate the increase in gain as time progresses. This ramp was generated under control of the 68HC11 using the "ramp" subroutine as mentioned above. The slope of the ramp can easily be lengthened by adding some delay in the loop, or the slope can be increased by stepping by 2 or more LSBs instead of the current 1 LSB changes.

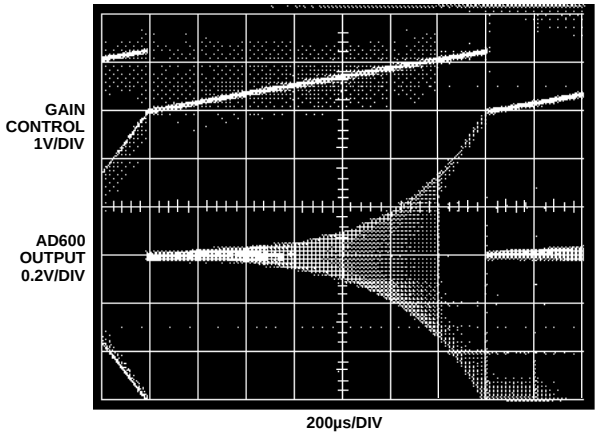


Figure 24. Time Dependent Gain of the AD600

Glitch Impulse

A specification of interest in many DAC applications is the glitch impulse. This is the amount of energy contained in any overshoot when a DAC changes at its major carry transition, in other words, when the DAC switches from code 01111111 to code 10000000. This point is the most demanding because all of the R-2R ladder switches are changing state. The AD8600's glitch impulse is shown in Figure 25. Calculating the value of the glitch is accomplished by calculating the area of the pulse, which for the AD8600 is: Glitch Impulse = (1/2) × (100 mV) × (200 ns) = 10 nV sec.

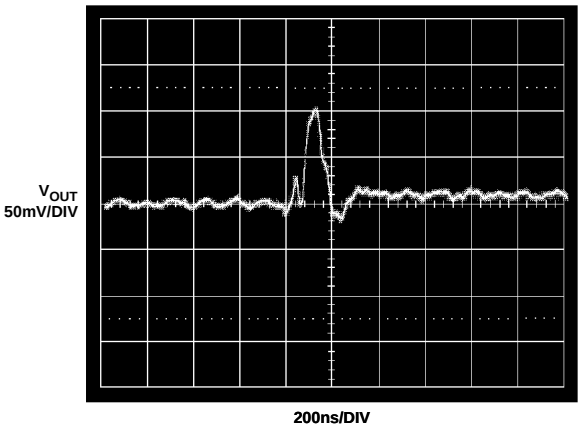
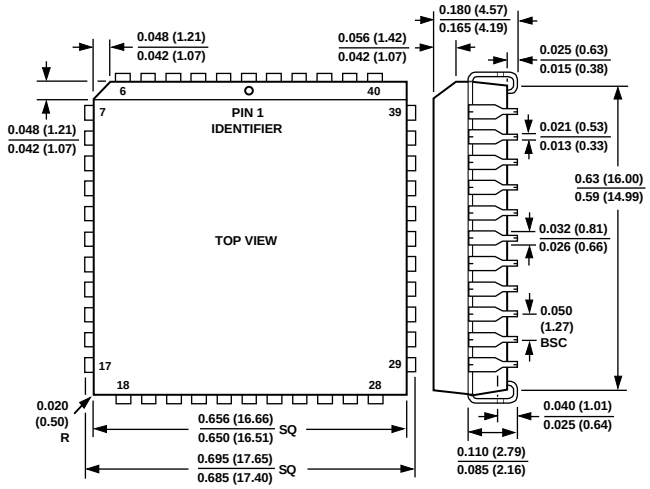


Figure 25. Glitch Impulse

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Plastic Lead Chip Carrier (PLCC) Package (P-44A)



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