

# FAN7380

## Half-Bridge Gate Driver (SOURCING/SINKING : 90mA/180mA)

### Features

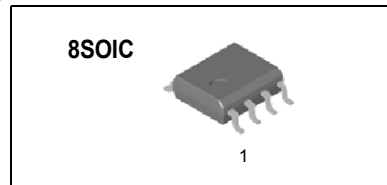
- Floating Channel Designed For Bootstrapping Operation To +600V
- Typically 90mA/180mA Sourcing/Sinking Current Driving Capability For Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative VS Swing To -9.8V For Signal Propagation @ VCC=VBS=15V
- VCC & VBS Supply Range From 10V To 20V
- UVLO Functions For Both Channels
- TTL Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50nsec
- Built-in 100nsec Dead-Time Control Function
- Output In-Phase With Input

### Typical Applications

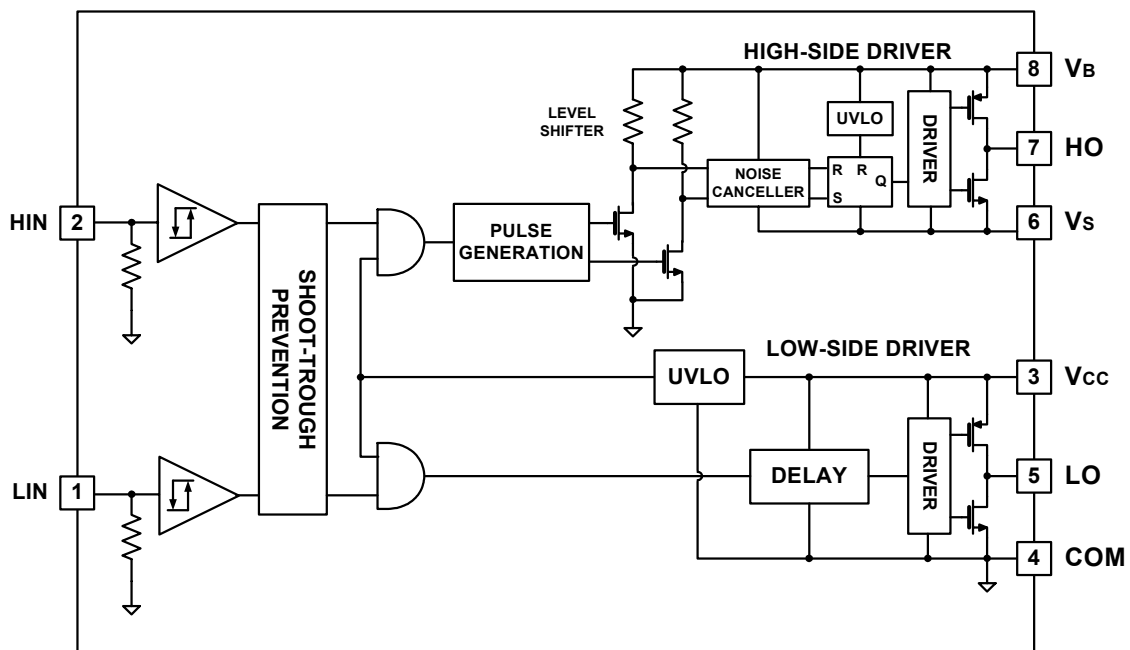
- Fluorescent Lamp Ballast
- Compact Fluorescent Lamp Ballast

### Description

The FAN7380 is a monolithic half-bridge gate driver IC for MOSFETs and IGBTs, which operate up to +600V. Fairchild's high voltage process and common-mode noise canceling technique give stable operation of high-side driver under high dv/dt noise circumstances. Advanced level shift circuit allows high-side gate driver operation up to  $V_S = -9.8V$  (typ.) for  $V_{BS} = 15V$ . The input logic level is compatible with standard TTL series logic gates. The internal shoot-through protection circuit provides 100nsec dead-time to prevent output switching devices from both conduction during transition periods. UVLO circuits for both channels prevent malfunction when VCC and VBS are lower than the specified threshold voltage. Output drivers typically source/sink 90mA/180mA, respectively, which is suitable for the applications such as fluorescent/compact fluorescent lamp ballast applications and the systems that require low di/dt noise.

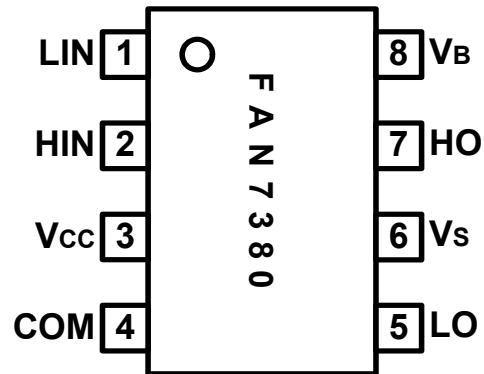


### Internal Block Diagram



Rev. 1.0.0

## Pin Assignments



## Pin Descriptions

Pin No	Symbol	I/O	Description
1	LIN		Logic Input for Low Side Gate Driver Output
2	HIN		Logic Input for High Side Gate Driver Output
3	VCC		Low Side Supply Voltage
4	COM		Logic Ground and Low Side Driver Return
5	LO		Low Side Driver Output
6	VS		High Voltage Floating Supply Return
7	HO		High Side Driver Output
8	VB		High Side Floating Supply

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
High side offset Voltage	V <sub>S</sub>	V <sub>B</sub> -25	-	V <sub>B</sub> +0.3	V
High side floating supply voltage	V <sub>B</sub>	-0.3		625	
High side floating output voltage HO	V <sub>HO</sub>	V <sub>S</sub> -0.3		V <sub>B</sub> +0.3	
Low side and logic fixed supply voltage	V <sub>CC</sub>	-0.3		25	
Low side output voltage LO	V <sub>LO</sub>	-0.3		V <sub>CC</sub> +0.3	
Logic input voltage(HIN, LIN)	V <sub>IN</sub>	-0.3		V <sub>CC</sub> +0.3	
Logic Ground	COM	V <sub>CC</sub> -25		V <sub>CC</sub> +0.3	
Allowable offset voltage SLEW RATE	dV <sub>S</sub> /dt			50	V/ns
Power Dissipation	PD			0.625	W
Thermal resistance, junction to ambient	R <sub>thja</sub>			200	°C/W
Junction Temperature	T <sub>J</sub>			150	°C
Storage Temperature	T <sub>S</sub>	-50		150	°C

Note : Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltage referenced to COM, all currents are defined positive into any lead.

## Recommended Operating Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
High side floating supply voltage	V <sub>B</sub>	V <sub>S</sub> +10	-	V <sub>S</sub> +20	V
High side floating supply offset voltage	V <sub>S</sub>	6-V <sub>CC</sub>		600	
High side(HO) output voltage	V <sub>HO</sub>	V <sub>S</sub>		V <sub>B</sub>	
Low side(LO) output voltage	V <sub>LO</sub>	COM		V <sub>CC</sub>	
Logic input voltage(HIN, LIN)	V <sub>IN</sub>	COM		V <sub>CC</sub>	
Low side supply voltage	V <sub>CC</sub>	10		20	
Ambient Temperature	T <sub>A</sub>	-40		125	°C

## ESD Level

Parameter	Pins	Conditions	Level	Unit
Human Body Model(HBM)	HIN, LIN, VCC, COM, VB, HO	R=1.5kΩ, C=100pF	±1500	V
	LO, VS		±1000	
Machine Model(MM)	All Pins	C=200pF	±300	
Charged Device Model(CDM)	All Pins		±500	

## Static Electrical Characteristics

( $V_{BIAS}(V_{CC}, V_{BS})=15.0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_S$  is applicable to HO and LO.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VCC & VBS supply under voltage positive going threshold	$V_{CCUV+}$ $V_{BSUV+}$		8.2	9.2	10.0	V
VCC & VBS supply under voltage negative going threshold	$V_{CCUV-}$ $V_{BSUV-}$		7.6	8.7	9.6	
VCC supply under voltage lockout hysteresis	$V_{CCUVH}$ $V_{BSUVH}$		-	0.5	-	
Offset supply leakage current	$I_{LK}$	$V_B=V_S=600V$	-	-	50	$\mu A$
Quiescent VBS supply current	$I_{QBS}$	$V_{IN}=0V$ or 5V	-	44	100	
Quiescent VCC supply current	$I_{QCC}$	$V_{IN}=0V$ or 5V	-	70	180	
Operating VBS supply current	$I_{PBS}$	$f_{in}=20kHz$ , rms value	-	-	600	$\mu A$
Operating VCC supply current	$I_{PCC}$	$f_{in}=20kHz$ , rms value	-	-	610	
Logic "1" input voltage	$V_{IH}$		2.5	-	-	V
Logic "0" input voltage	$V_{IL}$		-	-	0.8	
High level output voltage, $V_{BIAS}-V_O$	$V_{OH}$	$I_O=20mA$	-	-	2.8	V
Low level output voltage, $V_O$	$V_{OL}$		-	-	1.2	
Logic "1" input bias current	$I_{IN+}$	$V_{IN}=5V$	-	5	40	$\mu A$
Logic "0" input bias current	$I_{IN-}$	$V_{IN}=0V$	-	1.0	2.0	
Output high short circuit pulse current	$I_{O+}$	$V_O=0V$ $PW \leq 10\mu s$	60	90	-	mA
Output low short circuit pulsed current	$I_{O-}$		130	180	-	
Allowable negative $V_S$ pin voltage for HIN signal propagation to HO	$V_S$		-	-9.8	-7	V

## Dynamic Electrical Characteristics

( $V_{BIAS}(V_{CC}, V_{BS})=15.0V$ ,  $V_S=COM$ ,  $C_L=1000pF$  and  $T_A = 25^\circ C$ , unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Turn-on propagation delay	$t_{on}$	$V_S=0V$	70	135	200	ns
Turn-off propagation delay	$t_{off}$	$V_S=0V$ or 600V	60	130	190	
Turn-on rise time	$t_r$		160	230	290	
Turn-off fall time	$t_f$		20	90	160	
Dead time	DT		80	100	190	
Delay matching, HS & LS turn-on/off	MT		-	-	50	

## Typical Characteristics

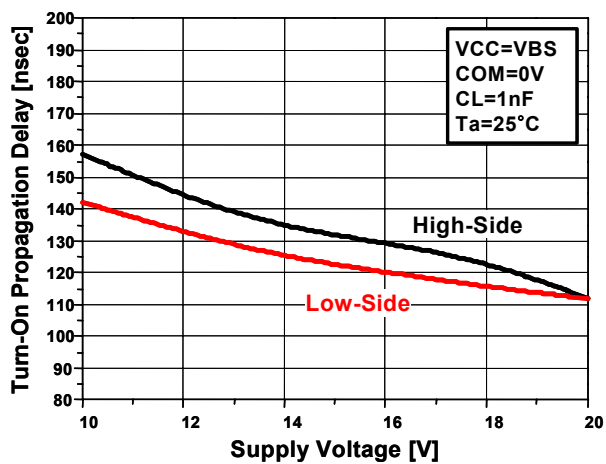


Fig. 1 Turn-On Propagation Delay vs. Supply Voltage

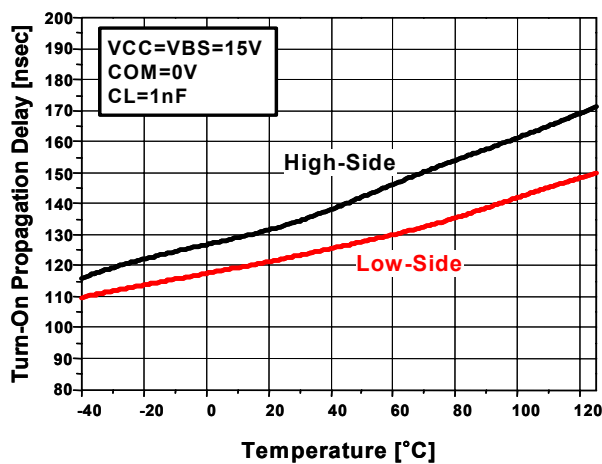


Fig. 2 Turn-On Propagation Delay vs. Temperature

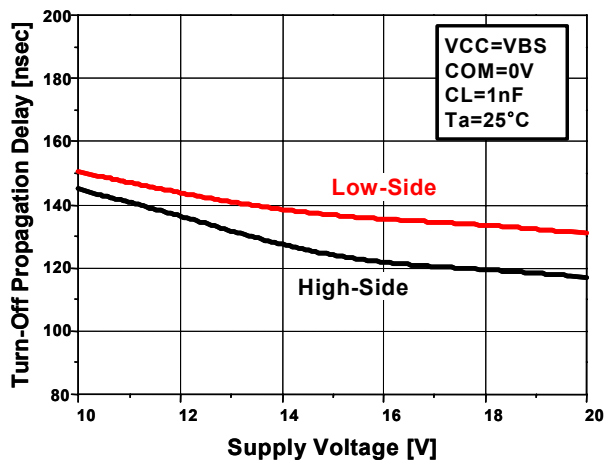


Fig. 3 Turn-Off Propagation Delay vs. Supply Voltage

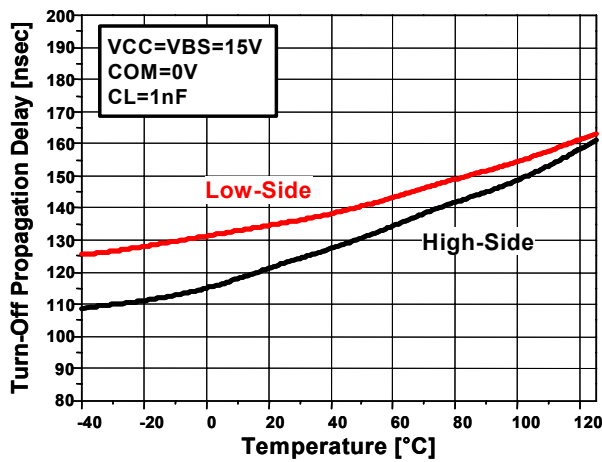


Fig. 4 Turn-Off Propagation Delay vs. Temperature

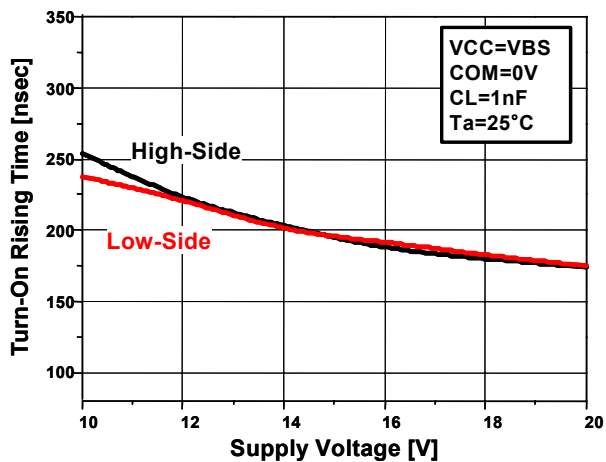


Fig. 5 Turn-On Rising Time vs. Supply Voltage

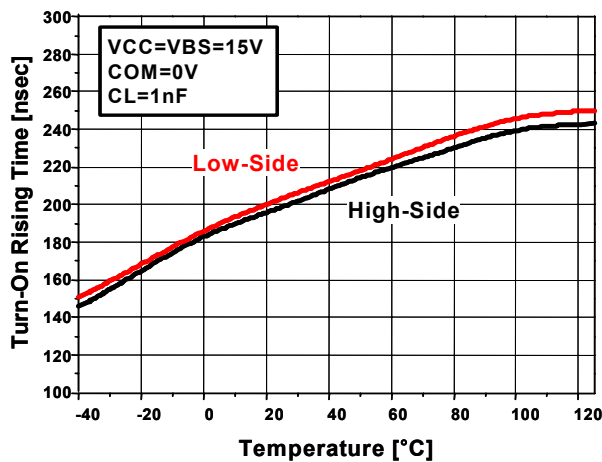


Fig. 6 Turn-On Rising Time vs. Temperature

## Typical Characteristics

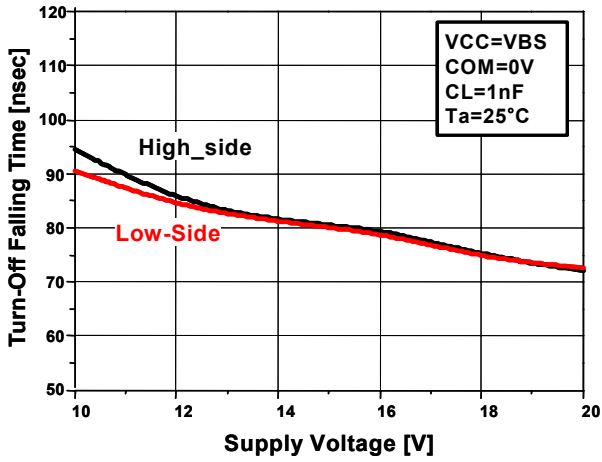


Fig. 7 Turn-Off Falling Time vs. Supply Voltage

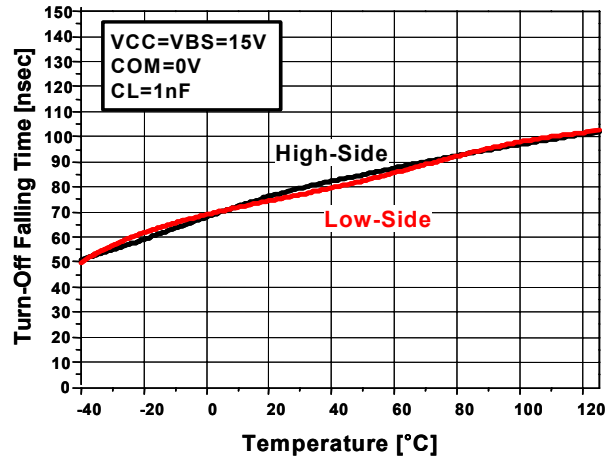


Fig. 8 Turn-Off Falling Time vs. Temperature

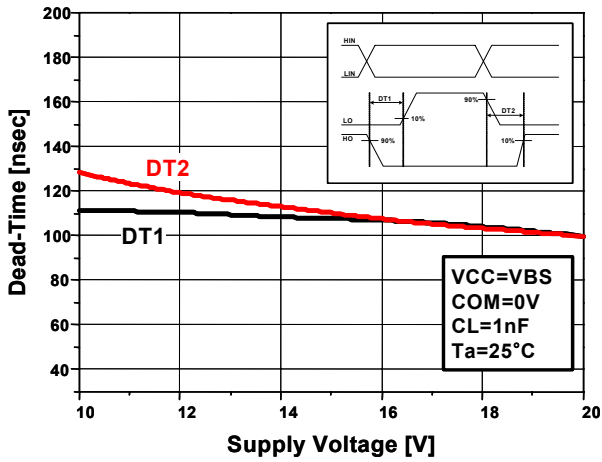


Fig. 9 Dead Time vs. Supply Voltage

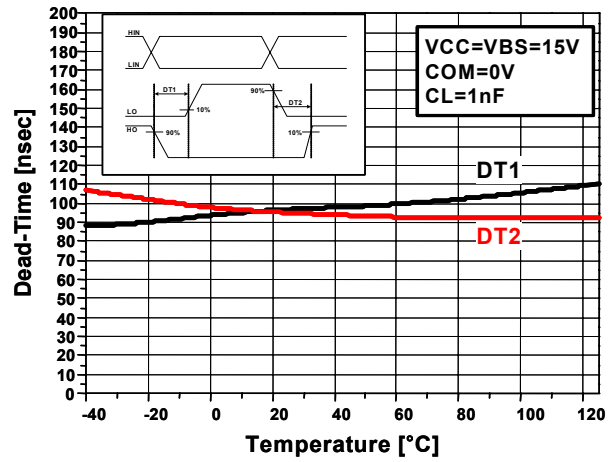


Fig. 10 Dead Time vs. Temperature

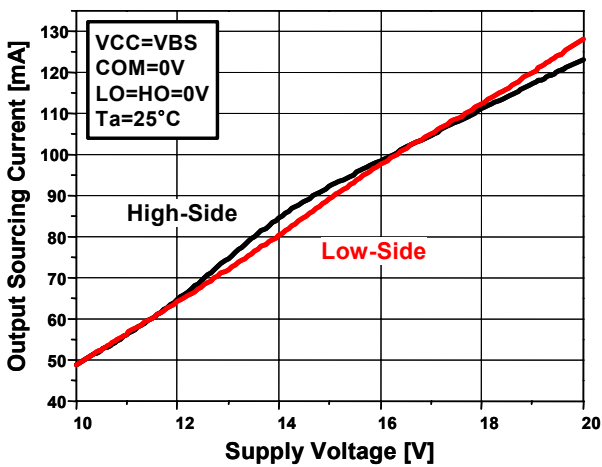


Fig. 11 Output Sourcing Current vs. Supply Voltage

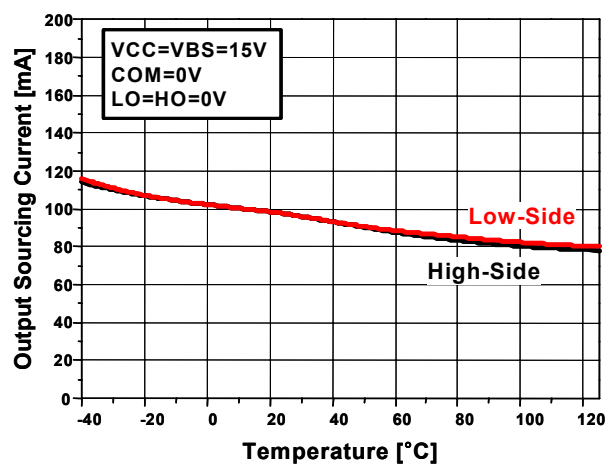


Fig. 12 Output Sourcing Current vs. Temperature

## Typical Characteristics

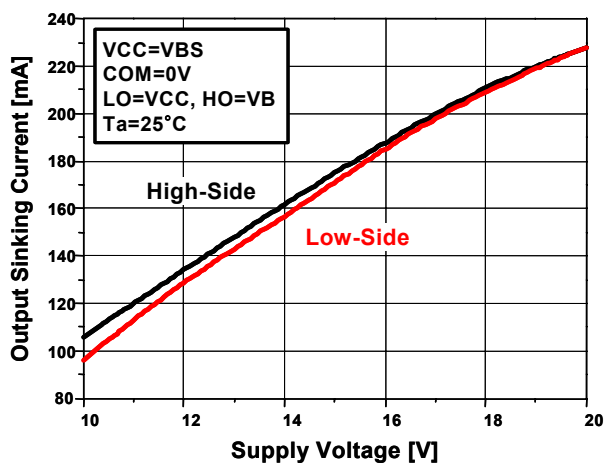


Fig. 13 Output Sinking Current vs. Supply Voltage

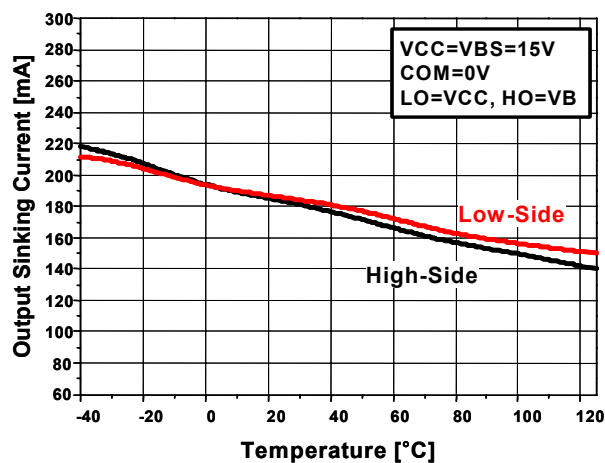


Fig. 14 Output Sinking Current vs. Temperature

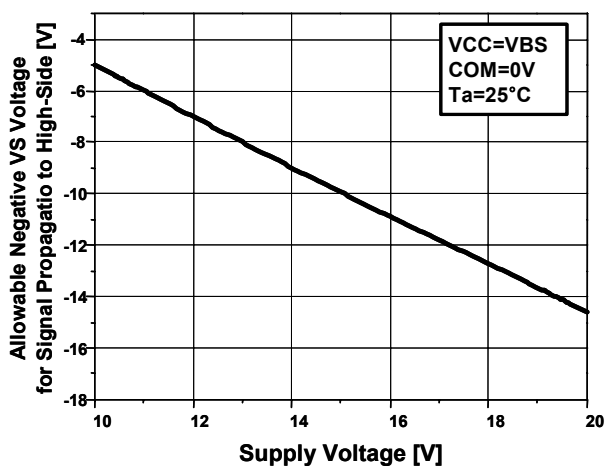


Fig. 15 Allowable Negative VS Voltage for Signal Propagation to High Side vs. Supply Voltage

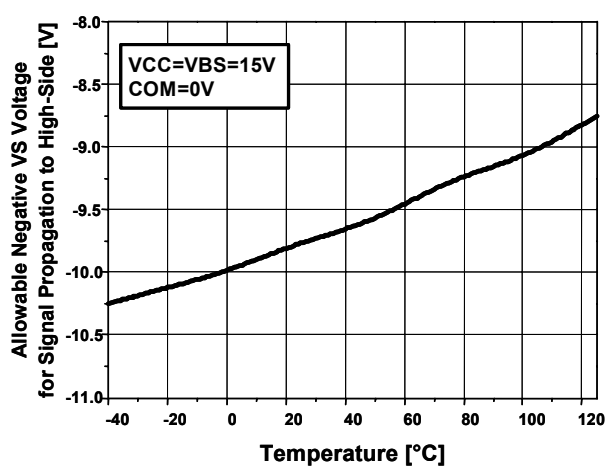


Fig. 16 Allowable Negative VS Voltage for Signal Propagation to High Side vs. Temperature

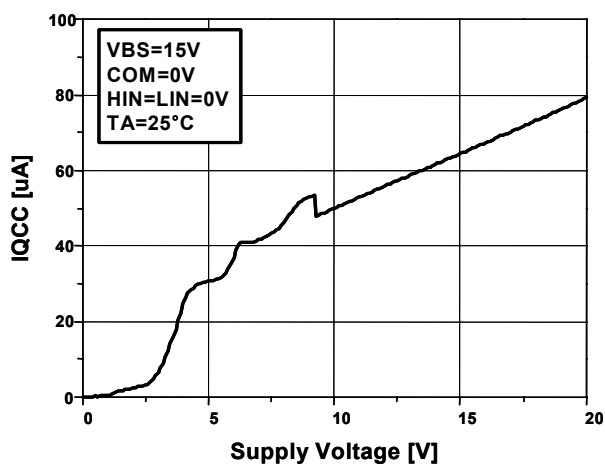


Fig. 17 IQCC vs. Supply Voltage

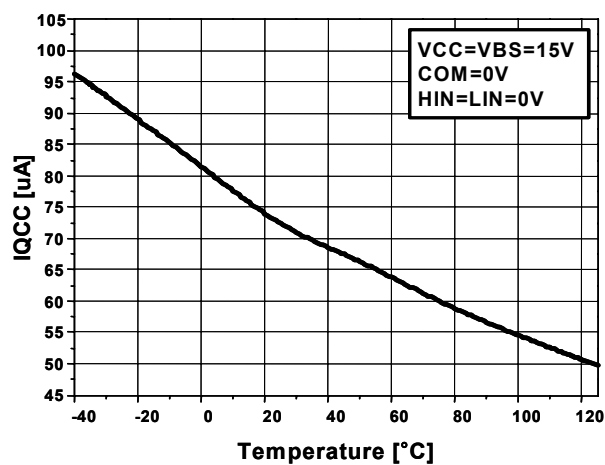


Fig. 18 IQCC vs. Temperature

## Typical Characteristics

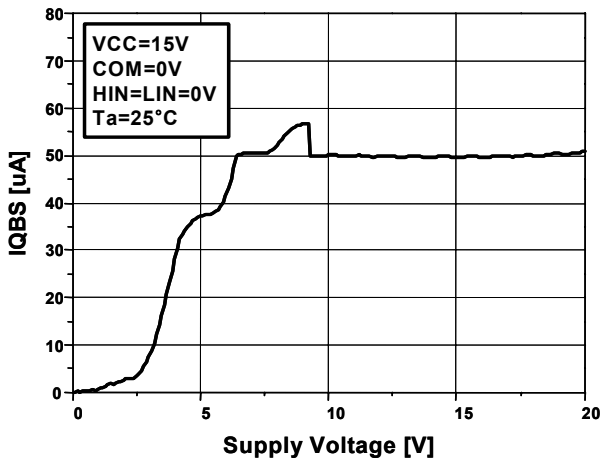


Fig. 19 IQBS vs. Supply Voltage

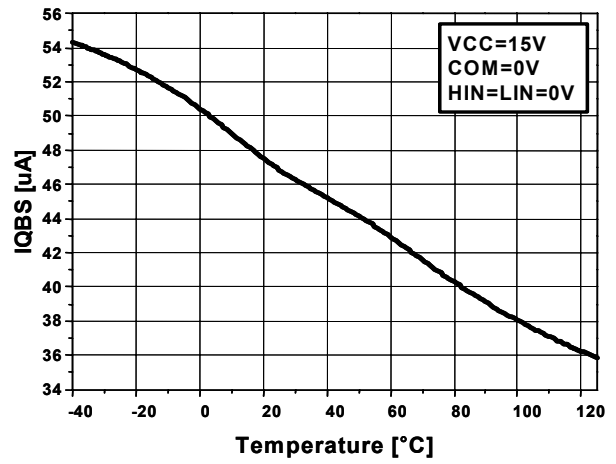


Fig. 20 IQBS vs. Temperature

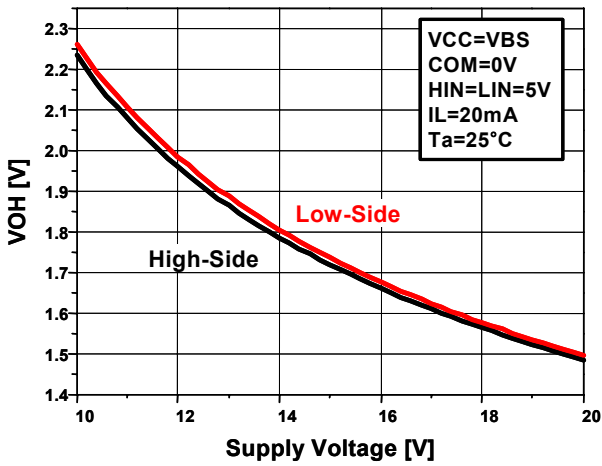


Fig. 21 High Level Output Voltage vs. Supply Voltage

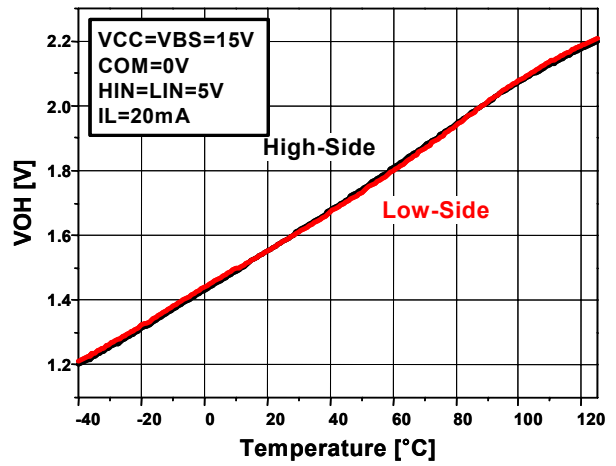


Fig. 22 High Level Output Voltage vs. Temperature

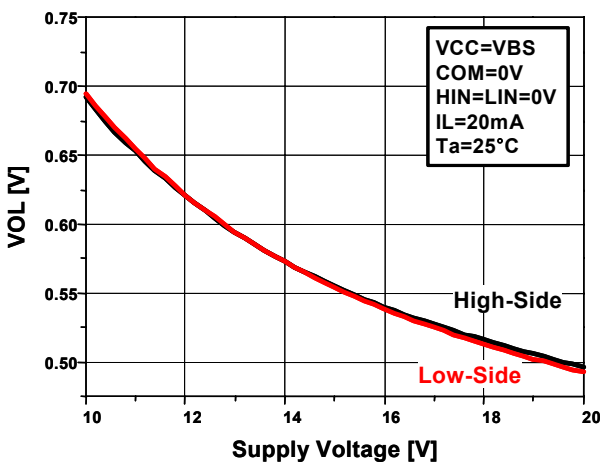


Fig. 23 Low Level Output Voltage vs. Supply Voltage

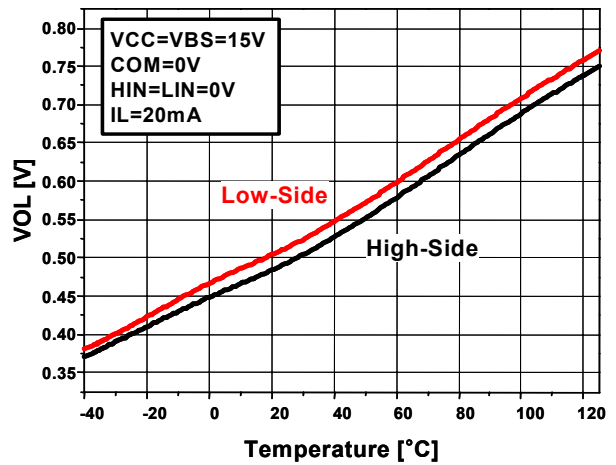


Fig. 24 Low Level Output Voltage vs. Temperature



## Typical Characteristics

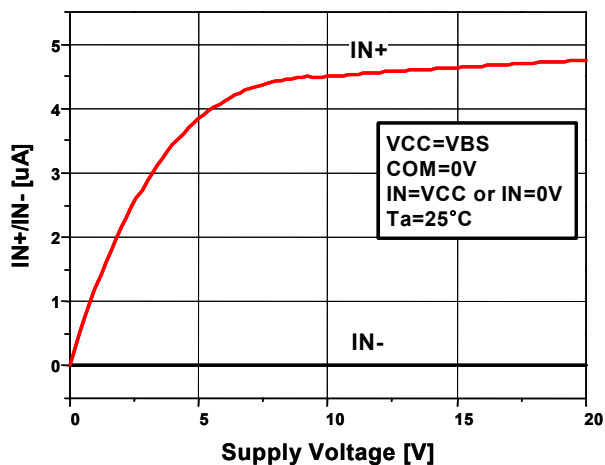


Fig. 25 Input Bias Current vs. Supply Voltage

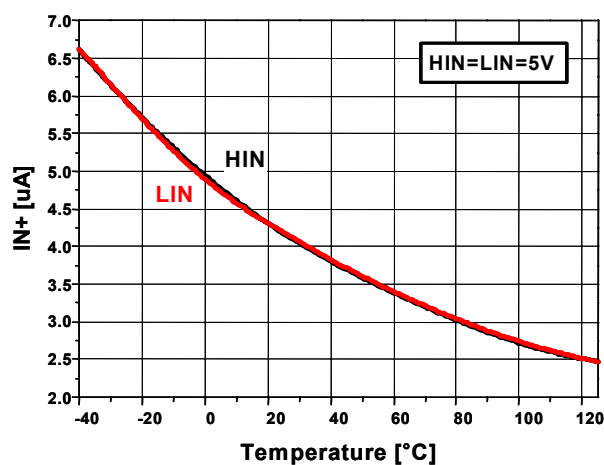


Fig. 26 Input Bias Current vs. Temperature

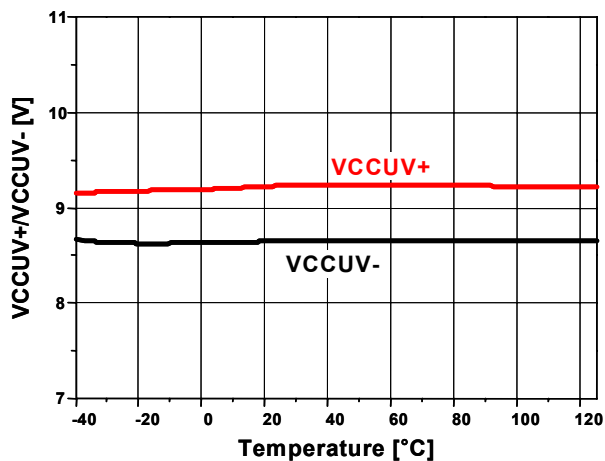


Fig. 27 VCC UVLO Threshold Voltage vs. Temperature

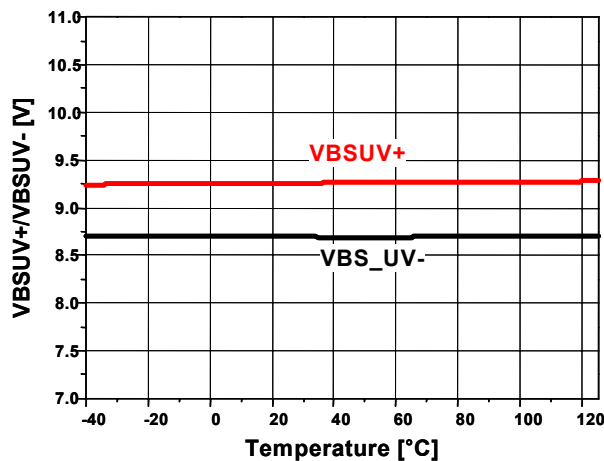


Fig. 28 VBS UVLO Threshold Voltage vs. Temperature

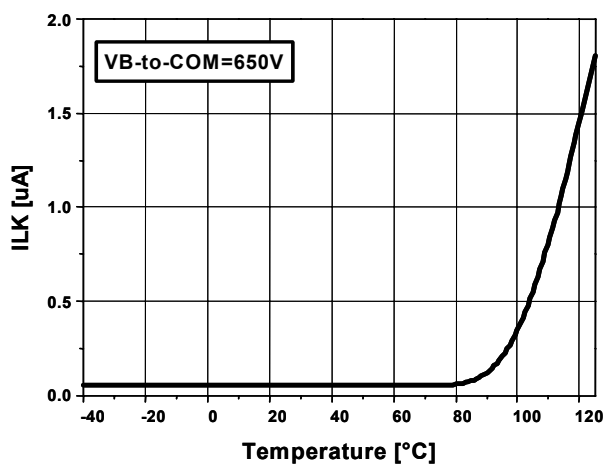


Fig. 29 VB to COM Leakage Current vs. Temperature

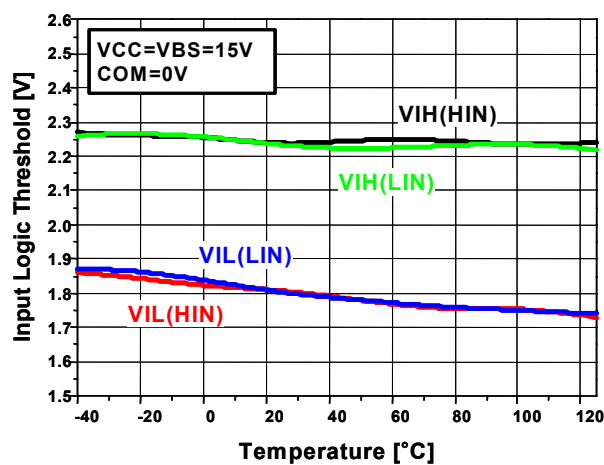
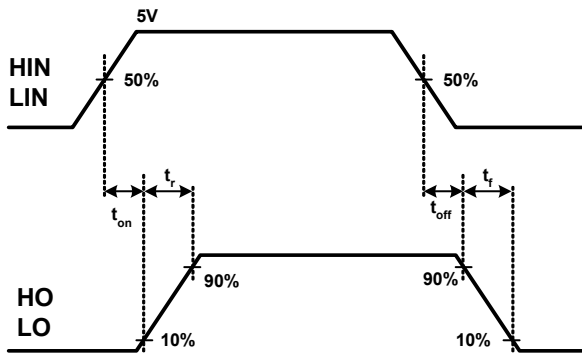
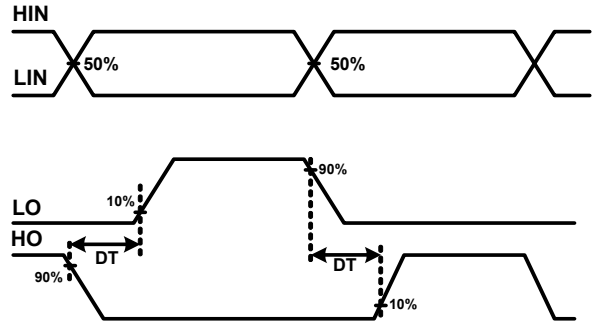


Fig. 30 Input Logic Threshold vs. Temperature

## Switching Time Definitions

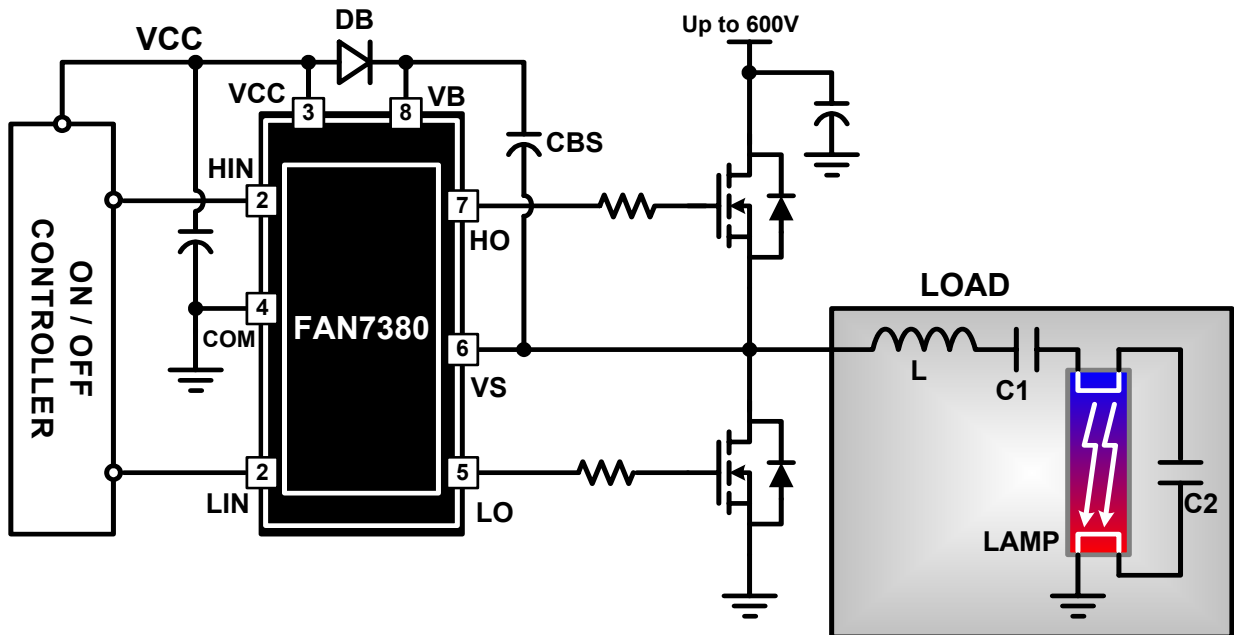


Switching Time Waveforms



Internal Deadtime Timing

## Typical Application Circuit



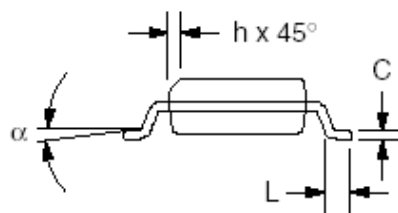
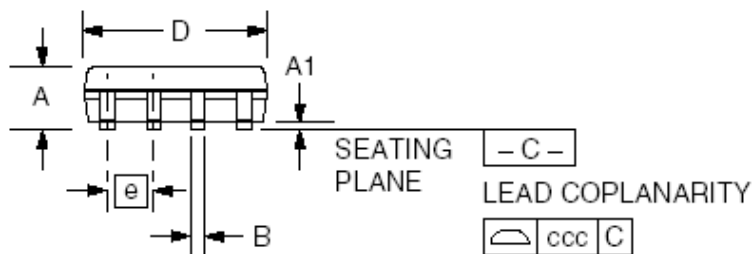
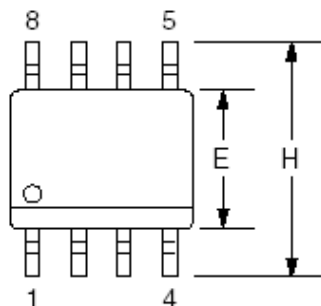
# Mechanical Dimensions

## Package

Dimensions in millimeters

### 8-SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.0075	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
$\alpha$	0°	8°	0°	8°	
ccc	—	.004	—	0.10	



**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.

---

## Ordering Information

Device	Package	Operating Temperature	Packing
FAN7380M	8SOIC	-40°C ~ +125°C	Tube
FAN7380MX			Tape & Reel

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.