

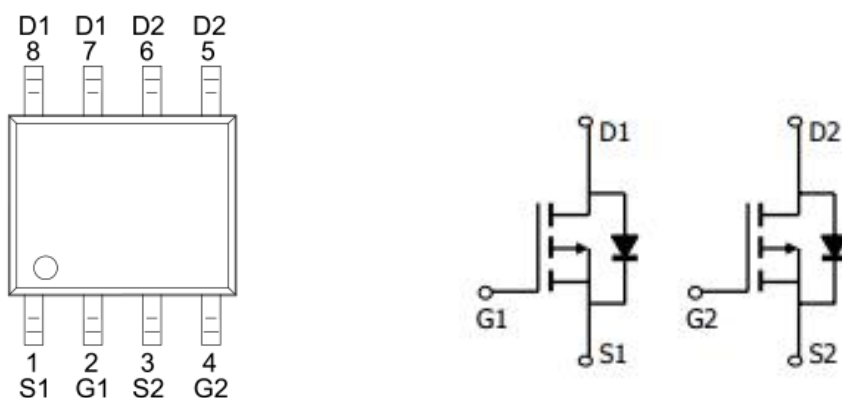
1. Features

- n $R_{DS(on)}=42m\Omega$ (typ) @ $V_{GS}=10\text{ V}$
- n Green device available
- n Super low gate charge
- n Excellent Cdv/dt effect decline
- n Advanced high cell density trench technology

2. Description

The KPE4403A2 is the high cell density trenched Dual P-channel MOSFET, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KNE4403A2 meet the RoHS and Green product requirement.

3. Symbol



4. Absolute maximum ratings

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current $V_{GS}@-10V^1$	I_D	$T_C=25^\circ C$	-5.0
		$T_C=70^\circ C$	-3.9
Pulsed drain current ²	I_{DM}	-25	A
Single pulse avalanche energy ³	EAS	18.1	mJ
Avalanche current	I_{AS}	-19	A
Total power dissipation ⁴	P_D	1.5	W
Junction and storage temperature range	T_J, T_{STG}	-55 to 150	$^\circ C$
Thermal resistance-junction to ambient ¹	$R_{\theta JA}$	85	$^\circ C/W$
Thermal resistance-junction to case ¹	$R_{\theta JC}$	25	$^\circ C/W$

5. Electrical characteristics

(T_J=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-30	-	-	V
BV _{DSS} Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25 °C, I _D =-1mA	-	-0.023	-	V/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	-	-	1	μA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	-	-	5	
Gate-source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.2	-	-2.5	V
V _{GS(th)} Temperature coefficient	ΔV _{GS(th)}		-	4	-	MV/°C
Static drain-source on- resistance ²	R _{DS(on)}	V _{GS} =-10V, I _D =-4A	-	42	55	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	64	78	
Forward transconductance	g _{FS}	V _{DS} =-5V, I _D =-4A	-	10	-	S
Total gate charge	Q _g	V _{DS} =-15V, V _{GS} =-4.5V I _D =-4A	-	6.5	-	nC
Gate-source charge	Q _{gs}		-	2.2	-	
Gate-drain charge	Q _{gd}		-	2	-	
Turn-on delay time	t _{d(on)}	V _{DD} =-15V, R _G =3.3Ω, V _{GS} =-10V I _D =-4A	-	2.7	-	ns
Rise time	t _r		-	8.6	-	
Turn-off delay time	t _{d(off)}		-	40	-	
Fall time	t _f		-	5	-	
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-15V F=1.0MHZ	-	580	-	pF
Output capacitance	C _{oss}		-	95	-	
Reverse transfer capacitance	C _{rss}		-	80	-	
Diode characteristics						
Continuous source current ^{1,5}	I _S	V _G =V _D =0V, Force current	-	-	-5.0	A
Pulsed source current ^{2,5}	I _{SM}		-	-	-25	A
Diode forward voltage ²	V _{SD}	V _{GS} =0V, I _S =-1A, T _J =25°C	-	-	-1.3	V
Reverse recovery time	t _{rr}	I _F =-4A, di/dt=100A/us, T _J =25°C	-	7.5	-	nS
Reverse recovery charge	Q _{rr}		-	2.6	-	nC

Note:1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2. The data tested by pulsed, pulse width ≤300us, duty cycle ≤2%.

3. The EAS data shows Max.rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH. I_{AS}=-19A.

4. The power dissipation is limited by 150 °C junction temperature.

5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

6. Test circuits and waveforms

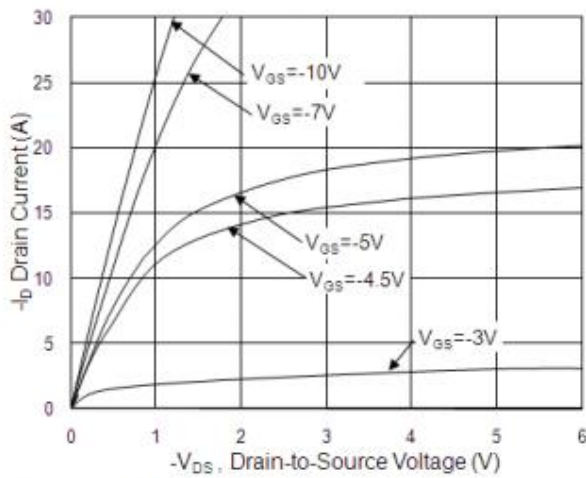


Fig.1 Typical Output Characteristics

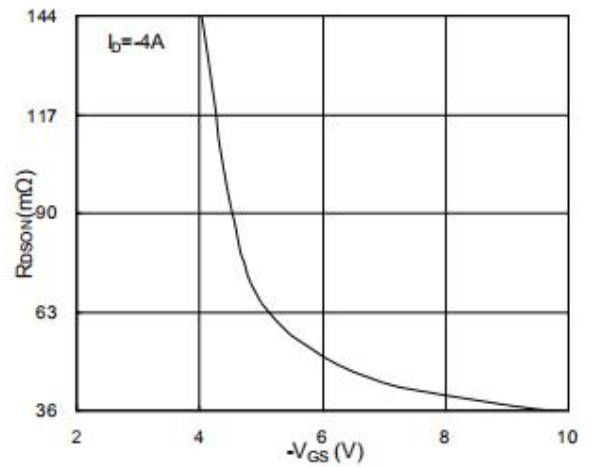


Fig.2 On-Resistance vs. Gate-Source

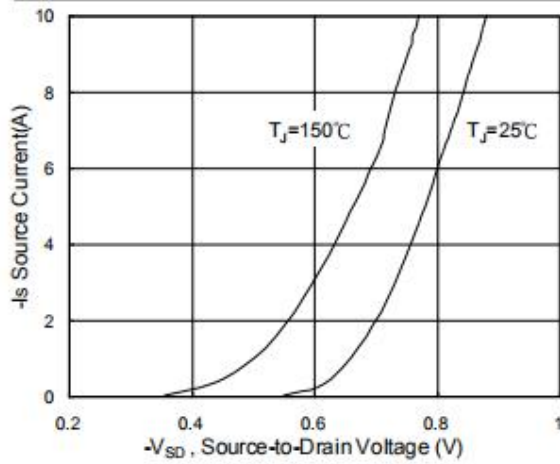


Fig.3 Forward Characteristics of Reverse

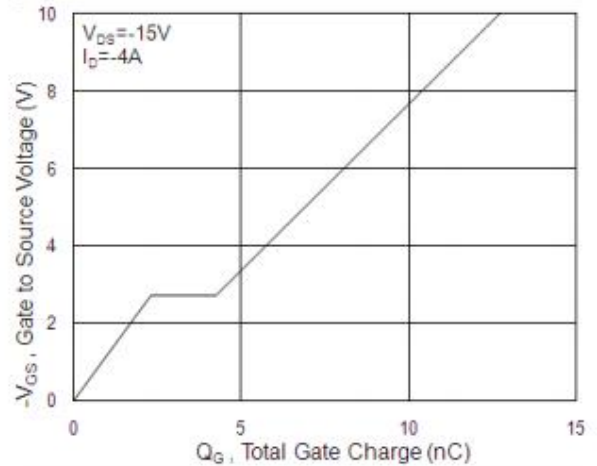


Fig.4 Gate-Charge Characteristics

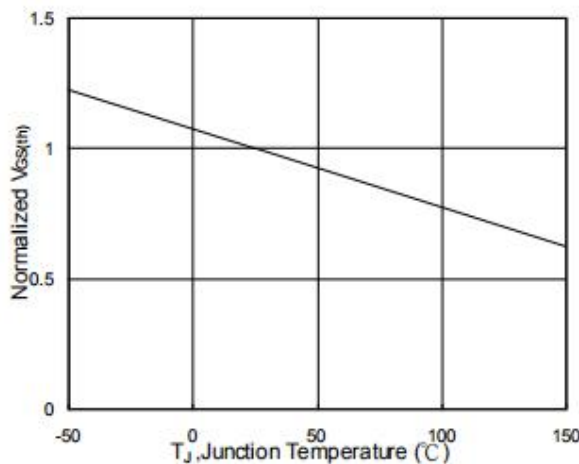


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

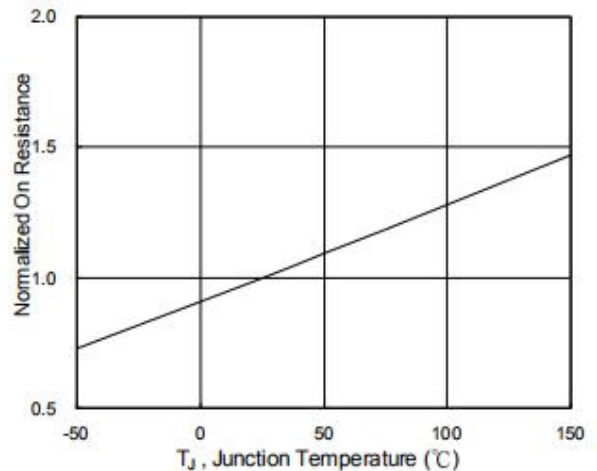


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

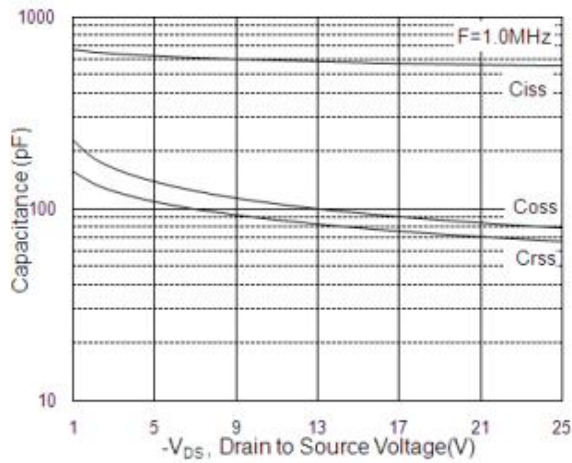


Fig.7 Capacitance

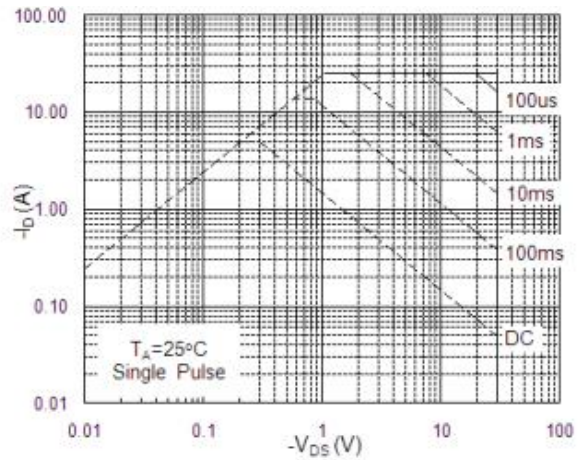


Fig.8 Safe Operating Area

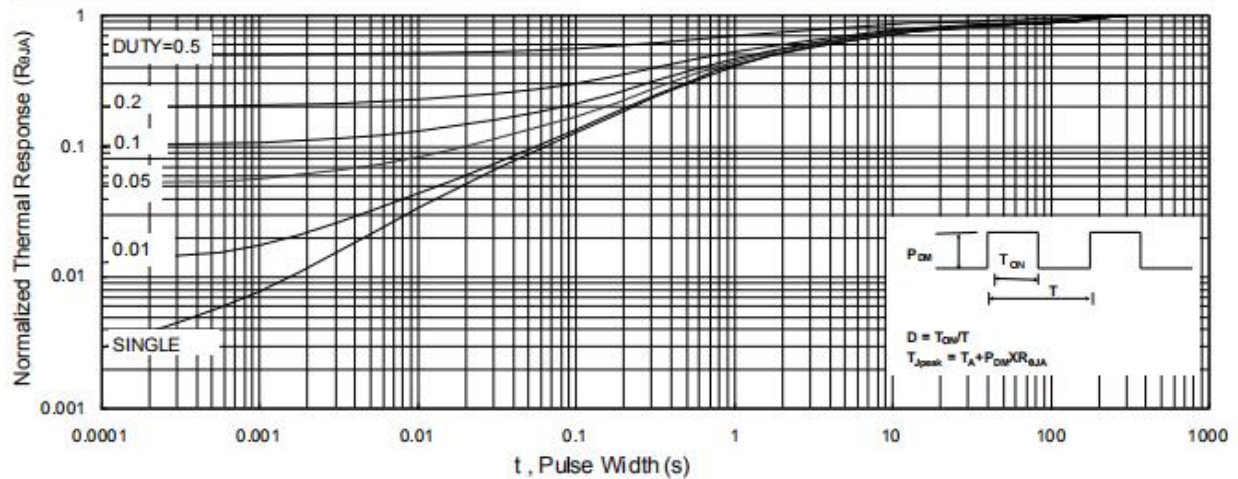


Fig.9 Normalized Maximum Transient Thermal Impedance

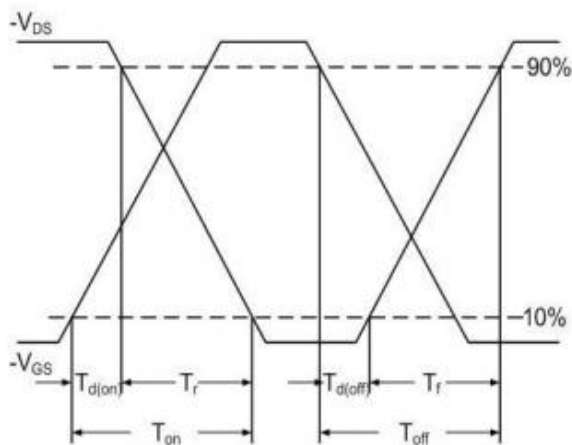


Fig.10 Switching Time Waveform

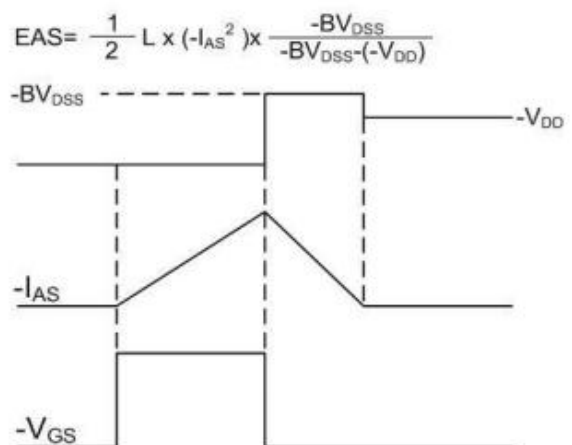


Fig.11 Unclamped Inductive Switching Waveform

$$EAS = \frac{1}{2} L \times (-I_{AS}^2) \times \frac{-BV_{DSS}}{-BV_{DSS} - (-V_{DD})}$$