NCP81166, NCP81166A

Synchronous Buck MOSFET Drivers

The NCP81166/A is a high performance dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. 2mm x 2mm DFN8 package allows for space−optimized board layout.

Zero current detect feature allows for a high−efficiency solution even at light load conditions. Pre−OVP feature aids in protecting the load in the event of a short across the high−side FET. V_{CC} UVLO ensures the MOSFETs are off when supply voltages are low. A bi−directional Enable pin provides a fault signal to the controller when a pre−OVP or UVLO fault is detected.

Features

- Space−Efficient 2 mm x 2mm DFN8 Thermally−Enhanced Package
- V_{CC} Range of 4.5 V to 13.2 V
- Integrated Bootstrap Diode
- Pre−OVP Function Protects Load during HS FET Short
  - NCP81166: 2.25 V SW Trip Threshold
  - NCP81166A: 1.8 V SW Trip Threshold
- Zero Current Detect Function Provides Power Saving Operation during Light Load Conditions
- Bi−directional Enable Feature pulls Enable pin low during pre−OVP and UVLO Faults
- 5 V tri−state PWM Logic
- Adaptive Anti−Cross−Conduction Circuit Protects against Cross−Conduction during FET turn−on and turn−off
- Output Disable Control turns off both MOSFETs via Enable pin
- VCC Undervoltage Lockout
- Direct interface to ASP1252, ASP1400 and other compatible PWM Controllers
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Solutions for Desktop Systems

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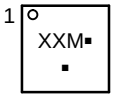
DFN8
MN SUFFIX
CASE 506CN

MARKING DIAGRAM



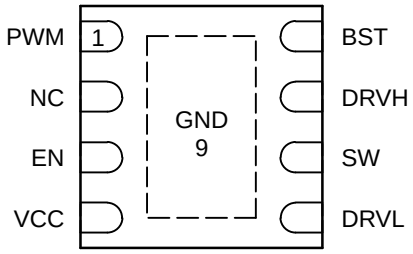
XX = Specific Device Code
CE for NCP81166
CH for NCP81166A
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81166MNTBG	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP81166AMNTBG	DFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



(Top View)

Figure 1. Pin Diagram

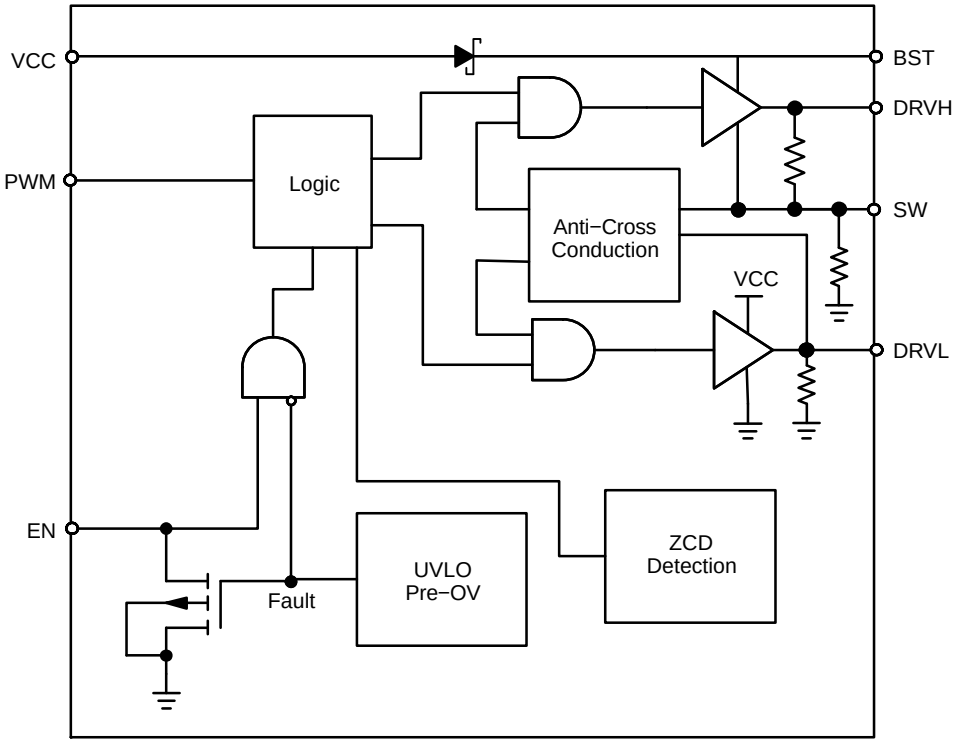


Figure 2. Block Diagram

Table 1. Pin Descriptions

Pin No.	Symbol	Description
1	PWM	Control input. The PWM signal has three distinctive states: Low = Low Side FET Enabled, Mid = Diode Emulation Enabled, High = High Side FET Enabled.
2	NC	No connect. There is no electrical connection from this pin to the die. Externally connecting this pin to ground will not affect the functionality of the part.
3	EN	Logic input. A logic high to enable the part and a logic low to disable the part. Pin is internally pulled low during pre−OVP and UVLO faults.
4	VCC	Power supply input. Connect a bypass capacitor (1 μF) from this pin to ground.
5	DRVL	Low side gate drive output. Connect to the gate of low side MOSFET.
6	SW	Switch node. Connect this pin to the source of the high side MOSFET and drain of the low side MOSFET.
7	DRVH	High side gate drive output. Connect to the gate of high side MOSFET.
8	BST	Floating bootstrap supply pin for high side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.
9	GND	Bias and reference ground. All signals are referenced to this node.

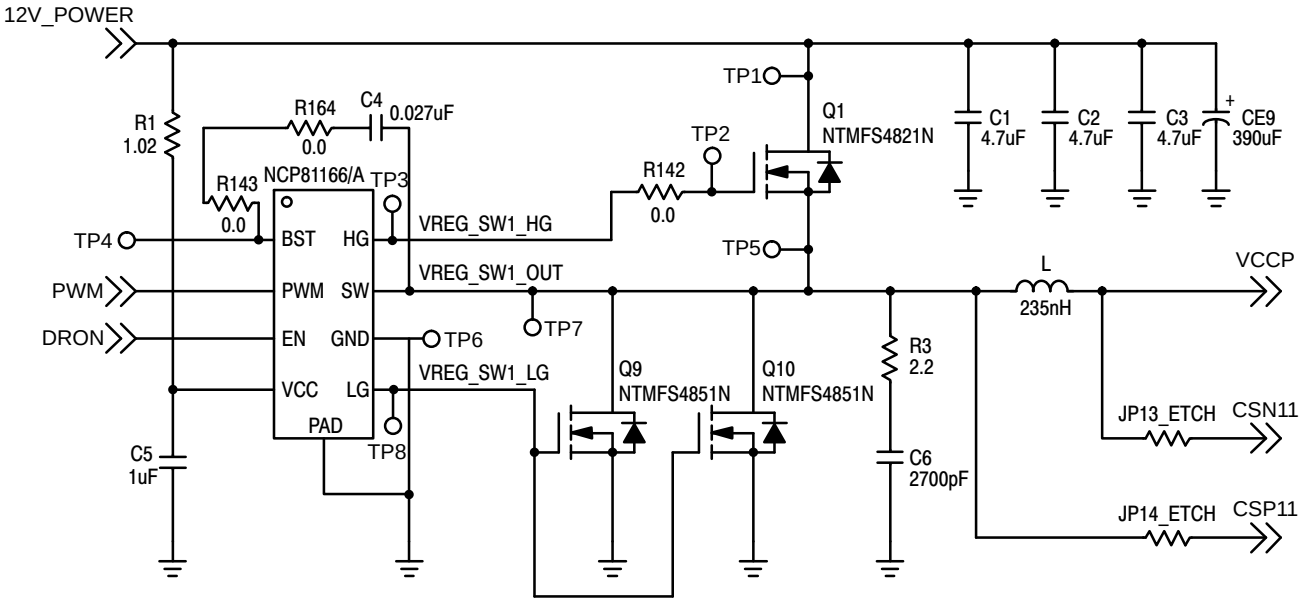


Figure 3. Application Circuit

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
VCC	Main Supply Voltage Input	15 V	−0.3 V
BST	Bootstrap Supply Voltage	35 V wrt/ GND 40 V ≤ 50 ns wrt/ GND 15 V wrt/ SW	−0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	35 V 40 V ≤ 50 ns	−5 V −10 V (200 ns)
DRVH	High Side Driver Output	BST+0.3 V	−0.3 V wrt/SW −2 V (<200 ns) wrt/SW
DRVL	Low Side Driver Output	VCC+0.3 V	−0.3 V DC −5 V (<200 ns)
PWM	DRVH and DRVL Control Input	6.5 V	−0.3 V
EN	Enable Pin	6.5 V	−0.3 V
GND	Ground	0 V	0 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. THERMAL INFORMATION (All signals referenced to AGND unless noted otherwise)

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Characteristic (Note 1)	74	°C/W
T_J	Operating Junction Temperature Range* (Note 2)	−40 to 150	°C
T_A	Operating Ambient Temperature Range*	−10 to +125	°C
T_{STG}	Maximum Storage Temperature Range	−55 to +150	°C
MSL	Moisture Sensitivity Level	1	

* The maximum package power dissipation must be observed.
1. I in^2 Cu, 1 oz thickness.
2. Operation at −40°C to −10°C guaranteed by design, not production tested.

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −10°C < T_A < +125°C; 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST−SWN < 13.2 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY VOLTAGE					
VCC Operation Voltage		4.5		13.2	V
Pre−OVP Threshold			2.75	3.2	V
UNDERVOLTAGE LOCKOUT					
VCC Start Threshold		3.8	4.35	4.5	V
VCC UVLO Hysteresis		150	200	250	mV
Output Overvoltage Trip Threshold at Startup	VCC > Pre−OVP Threshold NCP81166 NCP81166A	2.1 1.65	2.25 1.80	2.4 1.95	V
SUPPLY CURRENT					
Normal Mode	Icc + Ibst, EN = 5 V, PWM = OSC, Fsw = 100 KHz, Cload = 3 nF for DRVH, 3 nF for DRVL		10		mA
Standby Current	Icc + Ibst, EN = GND		0.5	1.4	mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = LOW, No loading on DRVH & DRVL		2.0		mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = HIGH, No loading on DRVH & DRVL		2.0		mA
BOOTSTRAP DIODE					
Forward Voltage	V_{CC} = 12 V, forward bias current = 2 mA	0.1	0.4	0.6	V
PWM INPUT					
PWM Input High		3.4			V
PWM Mid−State		1.3		2.7	V
PWM Input Low				0.7	V
ZCD Blanking Timer			250		ns
HIGH SIDE DRIVER (VCC = 12 V)					
Output Impedance, Sourcing Current	VBST − VSW = 12 V		1.9	3.0	Ω
Output Impedance, Sinking Current	VBST − VSW = 12 V		1.0	1.7	Ω
DRVH Rise Time tr_{DRVH}	V_{VCC} = 12 V, 3 nF load, VBST−VSW = 12 V		16	30	ns
DRVH Fall Time tf_{DRVH}	V_{VCC} = 12 V, 3 nF load, VBST−VSW = 12 V		11	25	ns
DRVH Turn−Off Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF	8.0		30	ns
DRVH Turn−On Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF			30	ns
SW Pull Down Resistance	SW to PGND		45		kΩ
DRVH Pull Down Resistance	DRVH to SW, BST−SW = 0 V		45		kΩ
HIGH SIDE DRIVER (VCC = 5 V)					
Output Impedance, Sourcing Current	VBST − VSW = 5 V		2.5		Ω
Output Impedance, Sinking Current	VBST − VSW = 5 V		1.6		Ω
DRVH Rise Time tr_{DRVH}	V_{VCC} = 5 V, 3 nF load, VBST − VSW = 5 V		30		ns
DRVH Fall Time tf_{DRVH}	V_{VCC} = 5 V, 3 nF load, VBST − VSW = 5 V		27		ns
DRVH Turn−Off Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF		20		ns
DRVH Turn−On Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF		27		ns
SW Pull Down Resistance	SW to PGND		45		kΩ

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −10°C < T_A < +125°C; 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST−SWN < 13.2 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
HIGH SIDE DRIVER (VCC = 5 V)					
DRVH Pull Down Resistance	DRVH to SW, BST−SW = 0 V		45		kΩ
LOW SIDE DRIVER (VCC = 12 V)					
Output Impedance, Sourcing Current			2.0	3.0	Ω
Output Impedance, Sinking Current			0.7	1.5	Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		16	35	ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		11	20	ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF			35	ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF	8.0		30	ns
DRVL Pull Down Resistance	DRVL to PGND, VCC = PGND		45		kΩ
LOW SIDE DRIVER (VCC = 5 V)					
Output Impedance, Sourcing Current			2.5		Ω
Output Impedance, Sinking Current			1.0		Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		30		ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		22		ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF		27		ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF		12		ns
DRVL Pull Down Resistance	DRVL to PGND, VCC = PGND		45		kΩ
EN INPUT					
Input Voltage High		2.0			V
Input Voltage Low				1.0	V
Hysteresis			500		mV
Normal Mode Bias Current		−1		1	μA
Enable Pin Sink Current		4		30	mA
Propagation Delay Time			20	40	ns
SW Node					
SW Node Leakage Current				20	μA
Zero Cross Detection Threshold Voltage	SW to −20 mV, ramp slowly until BG goes off (Start in DCM mode) (Note 3)		−6		mV

Table 5. DECODER TRUTH TABLE

PWM INPUT	ZCD	DRVL	DRVH
PWM High	ZCD Reset	Low	High
PWM Mid	Positive current through the inductor	High	Low
PWM Mid	Zero current through the inductor	Low	Low
PWM Low	ZCD Reset	High	Low

3. Guaranteed by design; not production tested.

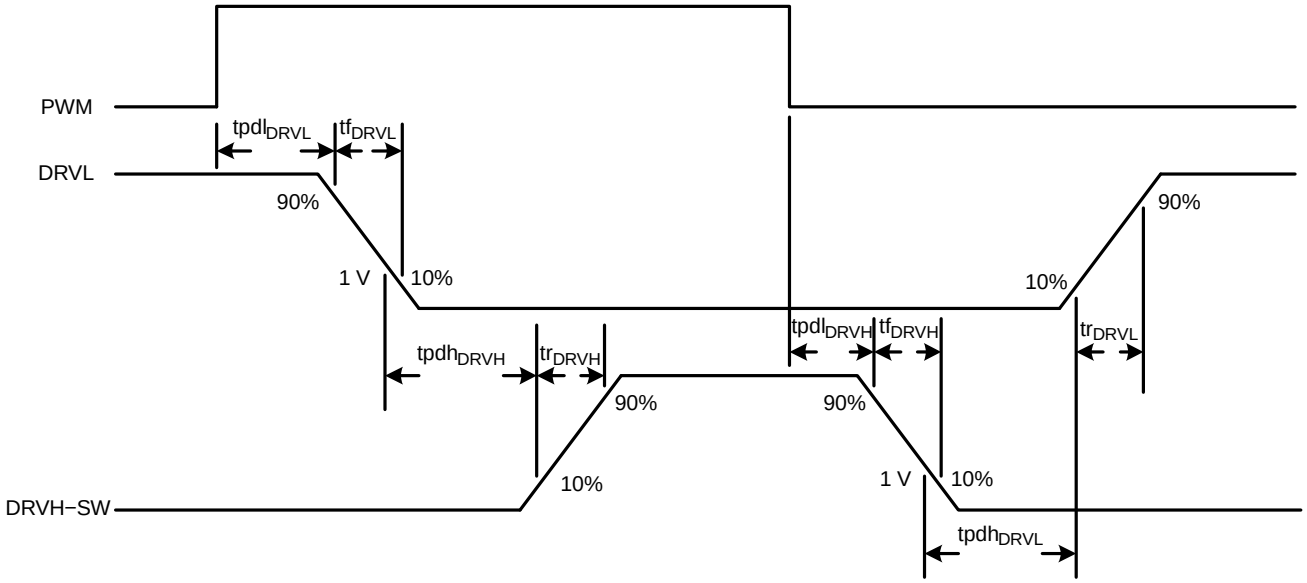


Figure 4. Timing Diagram

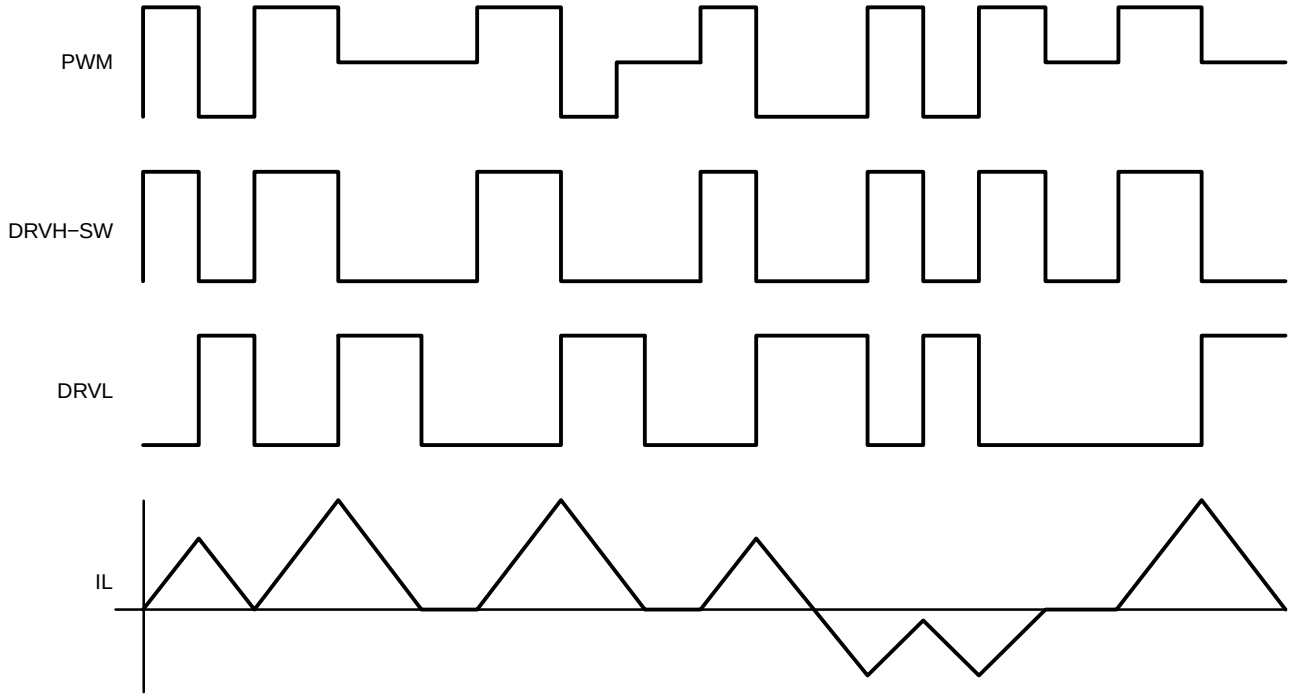


Figure 5. Logic Diagram

APPLICATIONS INFORMATION

Description

The NCP81166/A gate driver is a single phase MOSFET driver designed for driving N−channel MOSFETs in a synchronous buck converter topology. The NCP81166 is designed to work with the ON Semiconductor's ASP1252 controller and the NCP81166A is designed to work with ON Semiconductor's ASP1400 controller.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low−$R_{DS(on)}$ N−channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCC and GND pins. There is a 45 kΩ pull−down resistor connected between DRVL and GND.

High−Side Driver

The high−side driver is designed to drive a floating low−$R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the SW pin. There is a 45 kΩ pull−down resistor connected between DRVH and SW.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor. When the NCP81166/A is starting up, the SW pin is held at ground, allowing the bootstrap capacitor to charge up to VCC (minus the diode forward voltage) through the bootstrap diode. When the PWM input is driven high, the high−side driver will turn on the high−side MOSFET, using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the SW pin rises. When the high−side MOSFET is fully turned on, SW will settle to VIN and BST will settle to VIN + VCC (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the high−side driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used for C_{BST}.

Power Supply Decoupling

The NCP81166/A can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage, a low−ESR capacitor should be placed near the VCC and GND pins. A MLCC between 1 μF and 4.7 μF is typically used.

Undervoltage Lockout

DRVH and DRVL are low until VCC reaches the VCC UVLO threshold, typically 4.35 V. Once VCC reaches this threshold, the PWM signal will control DRVH and DRVL. There is a 200 mV hysteresis on VCC UVLO. There are pull−down resistors on DRVH, DRVL and SW to prevent the gates of the MOSFETs from accumulating enough charge to turn on when the driver is powered off.

Pre−Overvoltage Protection

The pre−Overvoltage Protection (pre−OVP) feature is used to protect the load if there is a short across the high−side FET. When VCC is greater than 2.75 V, the voltage on SW is monitored. During startup, if SW is determined to be greater than Output Overvoltage Trip Threshold, DRVL will be latched high to turn on the synchronous FET and provide a path from VIN to ground. This also pulls the EN pin low. To exit this behavior, power to the driver must be turned off (VCC less than $UVLO_{RISING}$ minus UVLO hysteresis) and then VCC powered back on. When VCC rises above $UVLO_{RISING}$ and EN is above EN_{HI}, the gate driver enters normal PWM operation (DRVH and DRVL respond to the PWM signal) and the pre−OVP function is disabled.

Bi − Directional EN Signal

The Enable pin (EN) is used to disable the DRVH and DRVL outputs to prevent power transfer. When EN is above the EN_{HI} threshold, DRVH and DRVL change their states according to the PWM input. Fault modes, such as pre−OVP and UVLO, turn on an internal MOSFET that pulls the EN pin towards ground. By connecting EN to the DRON pin of a controller, the controller is alerted when the driver encounters a fault condition.

PWM Input and Zero Cross Detect (ZCD)

Switching PWM between logic−high and logic−low states will allow the driver to operate in continuous conduction mode as long as VCC is greater than the UVLO threshold and EN is high. The threshold limits are specified in the electrical characteristics table in this datasheet.

When PWM is set above PWM_{HI}, DRVL will first turn off after a propagation delay of $tpdl_{DRVL}$. To ensure non−overlap between DRVL and DRVH, there is a delay of $tpdh_{DRVH}$ from the time DRVL falls to 1 V, before DRVH is allowed to turn on.

When PWM falls below PWM_{LO}, DRVH will first turn off after a propagation delay of $tpdl_{DRVH}$. To ensure non−overlap between DRVH and DRVL, there is a delay of $tpdh_{DRVL}$ from the time DRVH – SW falls to 1 V, before DRVL is allowed to turn on.

When PWM enters the mid−state voltage range, PWM_{MID}, DRVL goes high after the non−overlap delay, and stays high for the duration of the ZCD blanking timer and an 80 ns de−bounce timer. Once these timers expire, SW is monitored for zero current detection and pulls DRVL low once zero current is detected.

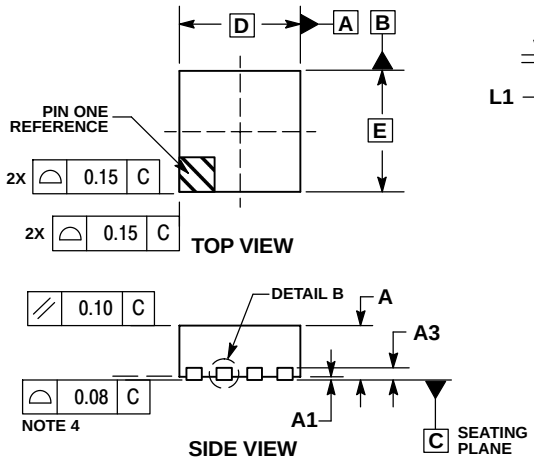
Layout Guidelines

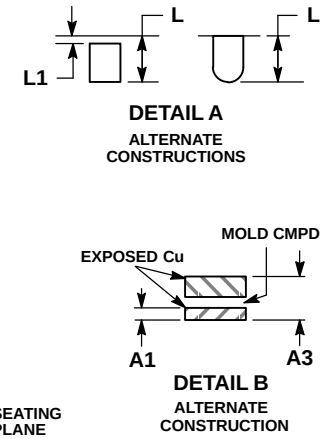
Layout for DC−DC converter is very important. The bootstrap and VCC bypass capacitors should be placed as close as to the driver IC as possible.

Connect the GND flag to local ground plane. The ground plane can provide a good return path for gate drives and reduce the ground noise. This connection also allows for good heat dissipation. To minimize the ground loop for the low−side MOSFET, the GND flag should be close to the low−side FET source pin. The gate drive trace should be routed to minimize the length, the minimum recommended width is 20 mils.

PACKAGE DIMENSIONS

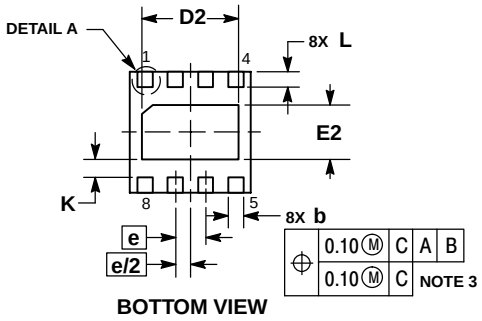
DFN8 2x2, 0.5P
CASE 506CN
ISSUE O



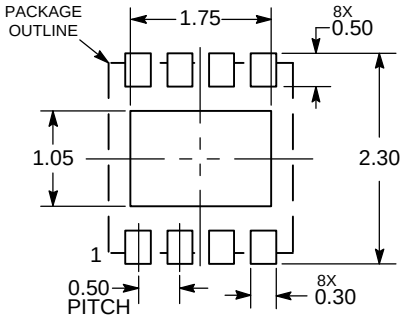


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
K	0.27 REF	
L	0.17	0.38
L1	−−−	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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