

# 3.3 V ECL ÷2, ÷4, ÷8 Clock Generation Chip

## MC100LVEL34

### Description

The MC100LVEL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple LVEL34s in a system.

### Features

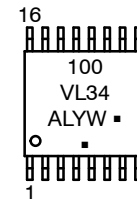
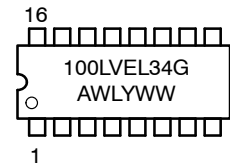
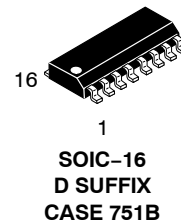
- 50 ps Typical Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 1.5 GHz Toggle Frequency
- The 100 Series Contains Temperature Compensation.
- PECL Mode Operating Range:  
 $V_{CC} = 3.0 \text{ V to } 3.8 \text{ V with } V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0 \text{ V with } V_{EE} = -3.0 \text{ V to } -3.8 \text{ V}$
- Open Input Default State
- LVDS Input Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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### MARKING DIAGRAMS\*



A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

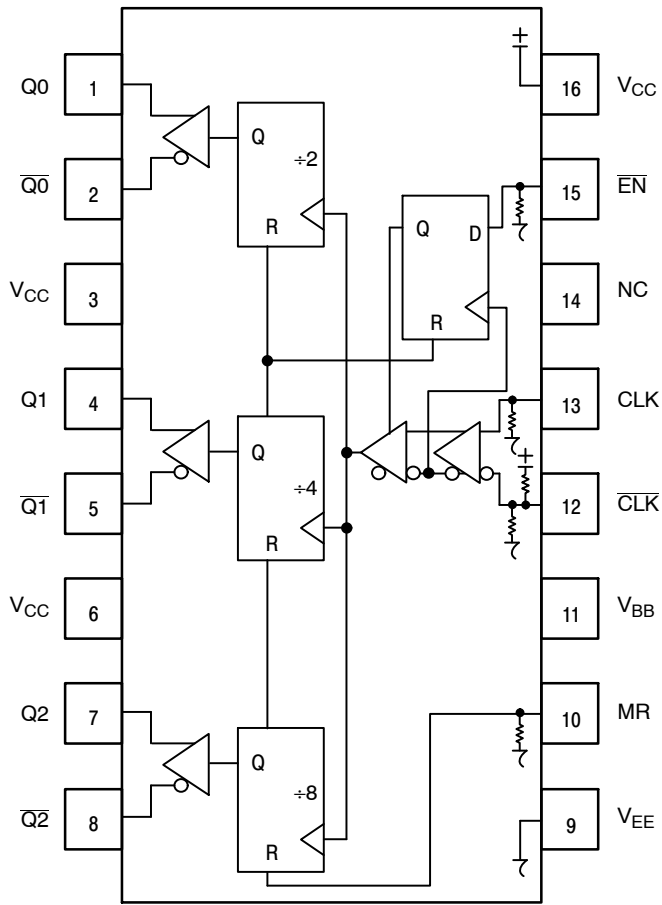
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

# MC100LEVEL34



Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 16-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

| PIN                         | FUNCTION                 |
|-----------------------------|--------------------------|
| CLK*, $\overline{CLK}^{**}$ | ECL Diff Clock Inputs    |
| EN*                         | ECL Sync Enable          |
| MR*                         | ECL Master Reset         |
| Q0, $\overline{Q0}$         | ECL Diff ÷2 Outputs      |
| Q1, $\overline{Q1}$         | ECL Diff ÷4 Outputs      |
| Q2, $\overline{Q2}$         | ECL Diff ÷8 Outputs      |
| $V_{BB}$                    | Reference Voltage Output |
| $V_{CC}$                    | Positive Supply          |
| $V_{EE}$                    | Negative Supply          |
| NC                          | No Connect               |

\* Pins will default LOW when left open.

\*\*Pins will default to  $V_{CC}/2$  when left open.

Table 2. FUNCTION TABLE

| CLK | EN | MR | FUNCTION        |
|-----|----|----|-----------------|
| Z   | L  | L  | Divide          |
| ZZ  | H  | L  | Hold $Q_{0-3}$  |
| X   | X  | H  | Reset $Q_{0-3}$ |

Z = Low-to-High Transition

ZZ = High-to-Low Transition

Table 3. ATTRIBUTES

| Characteristics   | Value                       |
|---|-----------------------------|
| Internal Input Pulldown Resistor  | 75 k $\Omega$               |
| Internal Input Pullup Resistor  | 37.5 k $\Omega$             |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)               | Pb-Free Pkg                 |
| SOIC-16<br>TSSOP-16   | Level 1<br>Level 1          |
| Flammability Rating<br>Oxygen Index: 28 to 34                               | UL 94 V-0 @ 0.125 in        |
| Transistor Count  | 210 Devices                 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                      |                             |

1. For additional information, see Application Note [AND8003/D](#).

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**Table 4. MAXIMUM RATINGS**

| Symbol        | Parameter                                | Condition 1           | Condition 2       | Rating      | Unit                        |
|---------------|--|-----------------------|-------------------|-------------|-----------------------------|
| $V_{CC}$      | PECL Mode Power Supply                   | $V_{EE} = 0\text{ V}$ |                   | 6           | V                           |
| $V_{EE}$      | NECL Mode Power Supply                   | $V_{CC} = 0\text{ V}$ |                   | -6          | V                           |
| $V_I$         | PECL Mode Input Voltage                  | $V_{EE} = 0\text{ V}$ | $V_I \leq V_{CC}$ | 6           | V                           |
|               | NECL Mode Input Voltage                  | $V_{CC} = 0\text{ V}$ | $V_I \geq V_{EE}$ | -6          | V                           |
| $I_{out}$     | Output Current                           | Continuous<br>Surge   |                   | 50          | mA                          |
|               |  |                       |                   | 100         | mA                          |
| $I_{BB}$      | $V_{BB}$ Sink/Source                     |                       |                   | $\pm 0.5$   | mA                          |
| $T_A$         | Operating Temperature Range              |                       |                   | -40 to +85  | $^{\circ}\text{C}$          |
| $T_{stg}$     | Storage Temperature Range                |                       |                   | -65 to +150 | $^{\circ}\text{C}$          |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm                | SOIC-16           | 100         | $^{\circ}\text{C}/\text{W}$ |
|               |  | 500 lfpm              | SOIC-16           | 60          | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)    | Standard Board        | SOIC-16           | 33 to 36    | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm                | TSSOP-16          | 138         | $^{\circ}\text{C}/\text{W}$ |
|               |  | 500 lfpm              | TSSOP-16          | 108         | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)    | Standard Board        | TSSOP-16          | 33 to 36    | $^{\circ}\text{C}/\text{W}$ |
| $T_{sol}$     | Wave Solder                              |                       |                   | 265         | $^{\circ}\text{C}$          |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 5. 100LVEL DC CHARACTERISTICS, PECL ( $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2))**

| Symbol      | Characteristic   | -40 $^{\circ}\text{C}$ |      |      | 25 $^{\circ}\text{C}$ |      |      | 85 $^{\circ}\text{C}$ |      |      | Unit          |
|-------------|--|------------------------|------|------|-----------------------|------|------|-----------------------|------|------|---------------|
|             |  | Min                    | Typ  | Max  | Min                   | Typ  | Max  | Min                   | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current   | 40                     | 50   | 60   | 40                    | 50   | 60   | 42                    | 52   | 62   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 3)   | 2155                   | 2280 | 2405 | 2155                  | 2280 | 2405 | 2155                  | 2280 | 2405 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 3)  | 1305                   | 1570 | 1725 | 1305                  | 1570 | 1725 | 1305                  | 1570 | 1725 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | 2075                   |      | 2420 | 2075                  |      | 2420 | 2075                  |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | 1305                   |      | 1675 | 1305                  |      | 1675 | 1305                  |      | 1675 | mV            |
| $V_{BB}$    | Output Voltage Reference   | 1775                   | 1875 | 1975 | 1775                  | 1875 | 1975 | 1775                  | 1875 | 1975 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.2                    |      | 3.3  | 1.2                   |      | 3.3  | 1.2                   |      | 3.3  | V             |
| $I_{IH}$    | Input HIGH Current   |                        |      | 150  |                       |      | 150  |                       |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | D                      |      |      | 0.5                   |      |      | 0.5                   |      |      | $\mu\text{A}$ |
|             |  | $\bar{D}$              | 0.5  |      |                       | -150 |      |                       | -150 |      |               |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925 V to -0.5 V.
- All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 6. 100LEVEL DC CHARACTERISTICS, NECL** ( $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -3.8\text{ V}$  to  $-3.0\text{ V}$  (Note 5))

| Symbol      | Characteristic   | -40°C          |       |       | 25°C           |       |       | 85°C           |       |       | Unit          |
|-------------|--|----------------|-------|-------|----------------|-------|-------|----------------|-------|-------|---------------|
|             |  | Min            | Typ   | Max   | Min            | Typ   | Max   | Min            | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current   | 23             | 30    | 40    | 23             | 30    | 40    | 23             | 30    | 40    | mA            |
| $I_{EE}$    | Power Supply Current   | 40             | 50    | 60    | 40             | 50    | 60    | 42             | 52    | 62    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 6)   | -1145          | -1020 | -895  | -1145          | -1020 | -895  | -1145          | -1020 | -895  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 6)  | -1995          | -1700 | -1575 | -1995          | -1700 | -1575 | -1995          | -1700 | -1575 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | -1225          |       | -880  | -1225          |       | -880  | -1225          |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | -1995          |       | -1625 | -1995          |       | -1625 | -1995          |       | -1625 | mV            |
| $V_{BB}$    | Output Voltage Reference   | -1525          | -1425 | -1325 | -1525          | -1425 | -1325 | -1525          | -1425 | -1325 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | $V_{EE} + 1.2$ |       | 0.0   | $V_{EE} + 1.2$ |       | 0.0   | $V_{EE} + 1.2$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current   |                |       | 150   |                |       | 150   |                |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>D<br>D  | 0.5<br>-150    |       |       | 0.5<br>-150    |       |       | 0.5<br>-150    |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .

6. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 7. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 8)

| Symbol                 | Characteristic  | -40°C      |            |              | 25°C       |            |              | 85°C       |            |              | Unit |
|------------------------|---|------------|------------|--------------|------------|------------|--------------|------------|------------|--------------|------|
|                        |   | Min        | Typ        | Max          | Min        | Typ        | Max          | Min        | Typ        | Max          |      |
| $f_{max}$              | Maximum Toggle Frequency (Figure 4)                         | 1.5        |            |              | 1.5        |            |              | 1.5        |            |              | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>CLK to Q0, Q1, Q2<br>MR to Q | 550<br>500 | 650<br>600 | 1000<br>1000 | 600<br>550 | 700<br>650 | 1000<br>1000 | 650<br>600 | 750<br>700 | 1000<br>1000 | ps   |
| $t_{JITTER}$           | Cycle-to-Cycle Jitter (Figure 4)                            |            | < 1        |              |            | < 1        |              |            | < 1        |              | ps   |
| $t_S$                  | Setup Time $\overline{EN}$                                  | 150        | 50         |              | 150        | 50         |              | 150        | 50         |              | ps   |
| $t_H$                  | Hold Time $\overline{EN}$                                   | 200        | 100        |              | 200        | 100        |              | 200        | 100        |              | ps   |
| $t_{RR}$               | Set/Reset Recovery  | 300        | 200        |              | 300        | 200        |              | 300        | 200        |              | ps   |
| $V_{PP}$               | Input Swing (Note 9)  | 150        |            | 1000         | 150        |            | 1000         | 150        |            | 1000         | mV   |
| $t_r$<br>$t_f$         | Output Rise/Fall Times Q (20% – 80%)                        | 120        | 170        | 400          | 140        | 180        | 400          | 160        | 200        | 400          | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

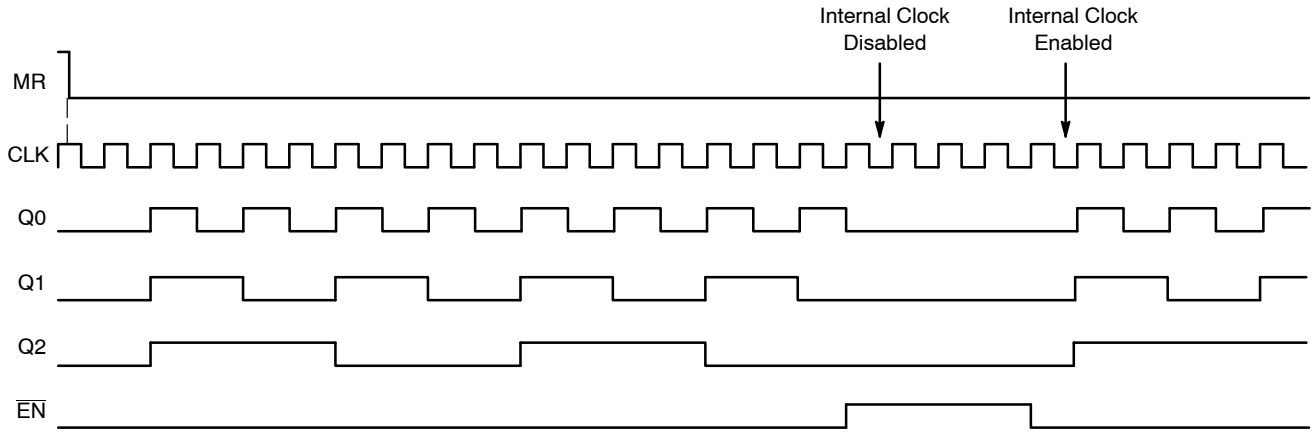
8. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

9.  $V_{PP}(\text{min})$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

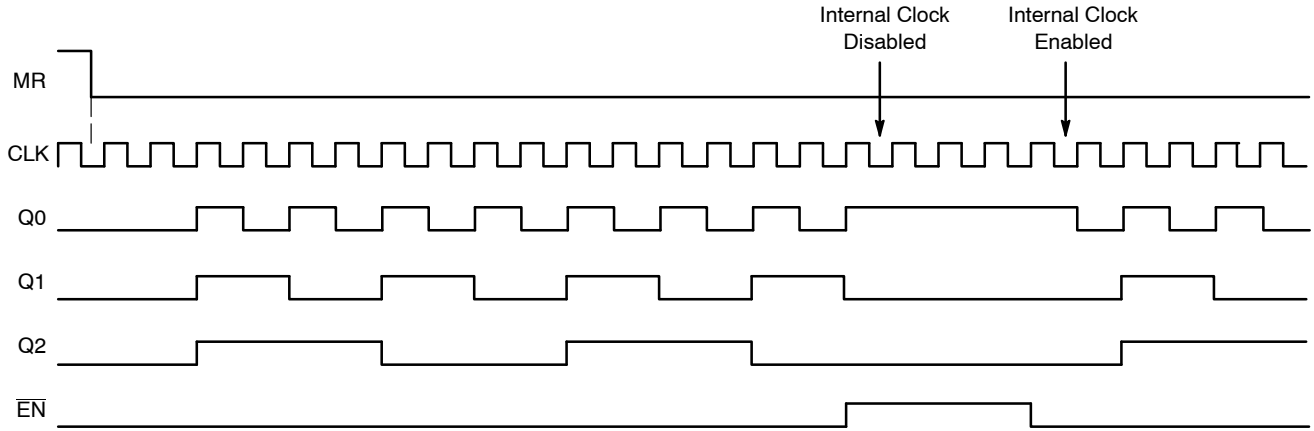
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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There are two distinct functional relationships between the Master Reset and Clock:



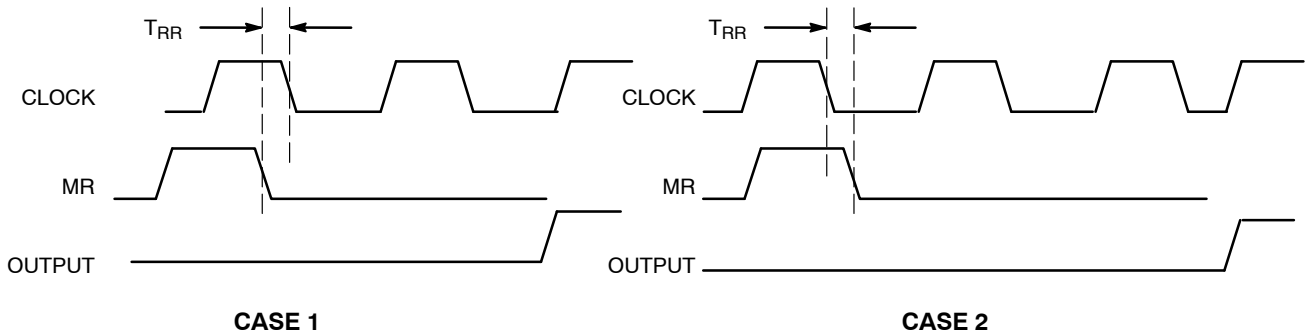
**CASE 1: If the MR is Deasserted (H-L), while the Clock is Still High, the Outputs will Follow the Second Ensuing Clock Rising Edge**



**CASE 2: If the MR is Deasserted (H-L), after the Clock has Transitioned Low, the Outputs will Follow the Third Ensuing Clock Rising Edge**

**Figure 2. Timing Diagrams**

The  $\overline{EN}$  signal will “freeze” the internal divider flip-flops on the first falling edge of CLK after its assertion. The internal divider flip-flops will maintain their state during the freeze. When  $\overline{EN}$  is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip-flops will “unfreeze” and continue to their next state count with proper phase relationships.



**Figure 3. Reset Recovery Time**

# MC100LVEL34

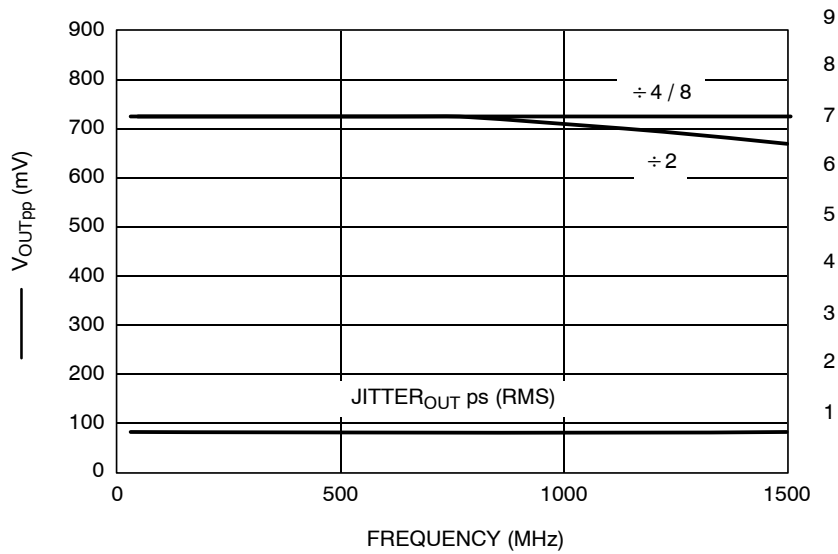


Figure 4.  $F_{max}/Jitter$

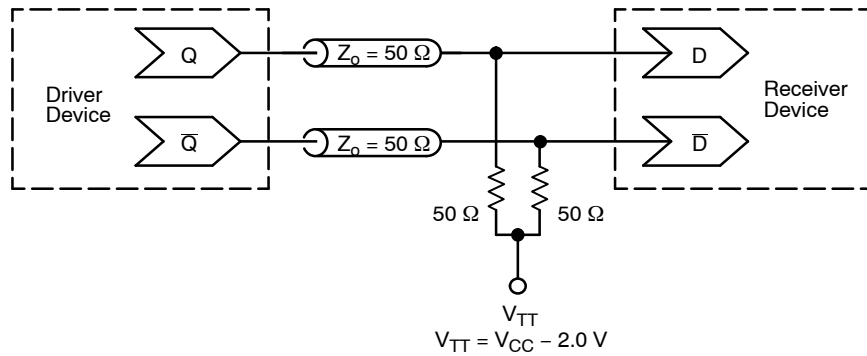


Figure 5. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

# MC100LVEL34

## ORDERING INFORMATION

| Device           | Package               | Shipping <sup>†</sup> |
|------------------|-----------------------|-----------------------|
| MC100LVEL34DR2G  | SOIC-16<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC100LVEL34DTG   | TSSOP-16<br>(Pb-Free) | 96 Units / Rail       |
| MC100LVEL34DTR2G | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

### SOLDERING FOOTPRINT



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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

|                  |             |  |
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