

CD405xB-Q1 CMOS Single 8-Channel Analog Multiplexer/Demultiplexer with Logic-Level Conversion

1 Features

- AEC-Q100 Qualified for Automotive Applications
 - Temperature Grade 1: -45°C To $+125^{\circ}\text{C}$, T_A
- Wide Range of Digital and Analog Signal Levels
 - Digital: 3 V to 20 V
 - Analog: $\leq 20 V_{P-P}$
- Low ON Resistance, 125 Ω (Typical) Over 15 V_{P-P} Signal Input Range for $V_{DD} - V_{EE} = 18 V$
- High OFF Resistance, Channel Leakage of $\pm 100 \text{ pA}$ (Typical) at $V_{DD} - V_{EE} = 18 V$
- Logic-Level Conversion for Digital Addressing Signals of 3 V to 20 V ($V_{DD} - V_{SS} = 3 V$ to 20 V) to Switch Analog Signals to 20 V_{P-P} ($V_{DD} - V_{EE} = 20 V$) Matched Switch Characteristics, $r_{ON} = 5 \Omega$ (Typical) for $V_{DD} - V_{EE} = 15 V$ Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2 μW (Typical) at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10 V$
- Binary Address Decoding on Chip
- 5 V, 10 V, and 15 V Parametric Ratings
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 μA at 18 V Over Full Package Temperature Range, 100 nA at 18 V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

2 Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating
- Factory Automation
- Televisions
- Appliances
- Consumer Audio
- Programmable Logic Circuits
- Sensors

3 Description

The CD405xB-Q1 analog multiplexers and demultiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------------|-------------------|
| CD405xB | SOIC (D) (16) | 9.90 mm x 3.91 mm |
| | TSSOP (PW) (16) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagrams of CD405xB-Q1

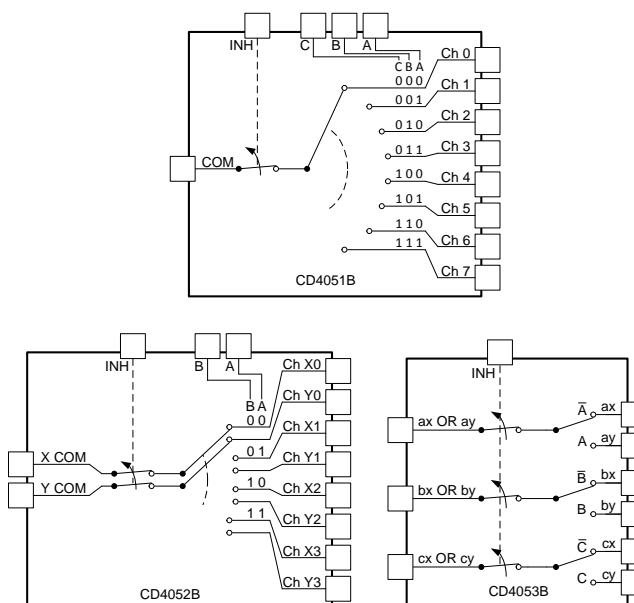


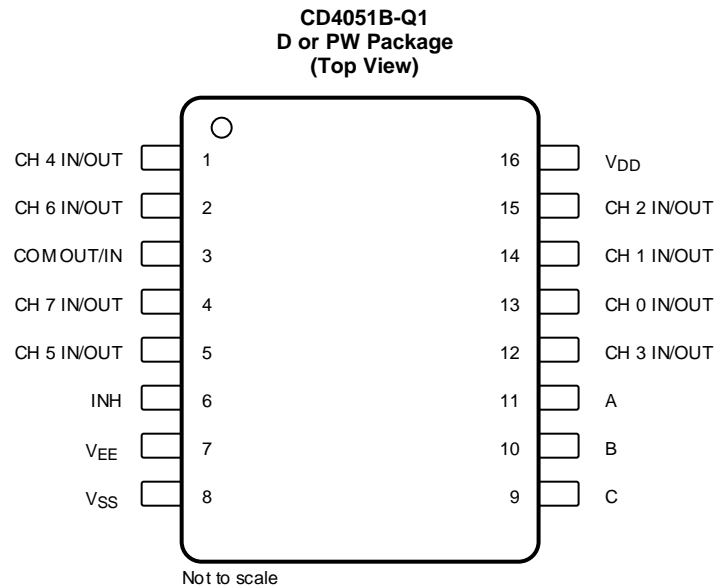
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4 Revision History

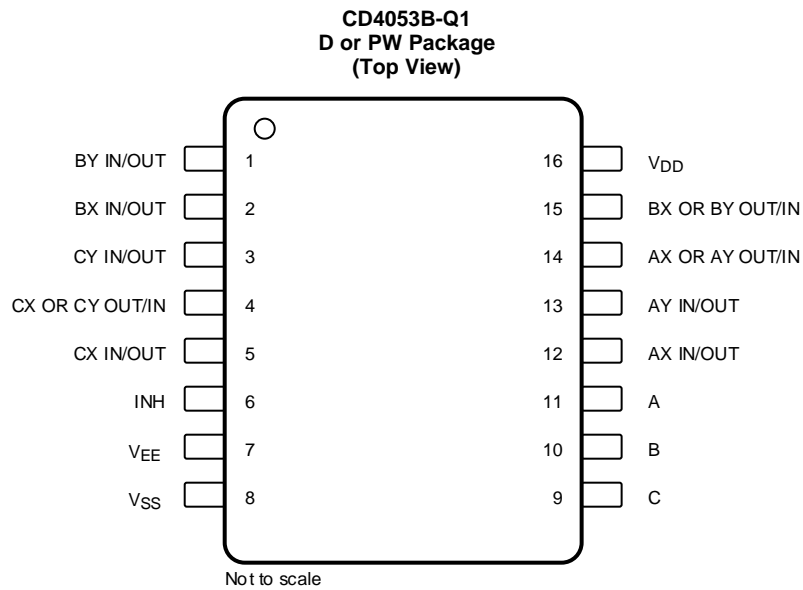
| Changes from Revision A (January 2008) to Revision B | Page |
|--|-------------|
| • Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted part number CD4052B-Q1 from the data sheets | 1 |

5 Pin Configuration and Functions



Pin Functions CD4051B-Q1

| PIN | | I/O | DESCRIPTION |
|-----|-----------------|-----|--|
| NO. | NAME | | |
| 1 | CH 4 IN/OUT | I/O | Channel 4 in/out |
| 2 | CH 6 IN/OUT | I/O | Channel 6 in/out |
| 3 | COM OUT/IN | I/O | Common out/in |
| 4 | CH 7 IN/OUT | I/O | Channel 7 in/out |
| 5 | CH 5 IN/OUT | I/O | Channel 5 in/out |
| 6 | INH | I | Disables all channels. See Table 1 . |
| 7 | V _{EE} | — | Negative power input |
| 8 | V _{SS} | — | Ground |
| 9 | C | I | Channel select C. See Table 1 . |
| 10 | B | I | Channel select B. See . |
| 11 | A | I | Channel select A. See Table 1 . |
| 12 | CH 3 IN/OUT | I/O | Channel 3 in/out |
| 13 | CH 0 IN/OUT | I/O | Channel 0 in/out |
| 14 | CH 1 IN/OUT | I/O | Channel 1 in/out |
| 15 | CH 2 IN/OUT | I/O | Channel 2 in/out |
| 16 | V _{DD} | — | Positive power input |


Pin Functions CD4053B-Q1

| PIN | | I/O | DESCRIPTION |
|-----|--------------------|-----|--|
| NO. | NAME | | |
| 1 | BY IN/OUT | I/O | B channel Y in/out |
| 2 | BX IN/OUT | I/O | B channel X in/out |
| 3 | CY IN/OUT | I/O | C channel Y in/out |
| 4 | CX OR CY OUT/IN | I/O | C common out/in |
| 5 | CX IN/OUT | I/O | C channel X in/out |
| 6 | INH | I | Disables all channels. See Table 1 . |
| 7 | V _{EE} | — | Negative power input |
| 8 | V _{SS} | — | Ground |
| 9 | C | I | Channel select C. See Table 1 . |
| 10 | B | I | Channel select B. See Table 1 . |
| 11 | A | I | Channel select A. See Table 1 . |
| 12 | AX IN/OUT | I/O | A channel X in/out |
| 13 | AY IN/OUT | I/O | A channel Y in/out |
| 14 | AX OR AY OUT/IN | I/O | A common out/in |
| 15 | BX OR BY OUT/IN | I/O | B common out/in |
| 16 | V _{DD} | — | Positive power input |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------------|---|------|-----------------------|------|
| Supply Voltage | V+ to V-, Voltages Referenced to V _{SS} Terminal | -0.5 | 20 | V |
| DC Input Voltage | | -0.5 | V _{DD} + 0.5 | V |
| DC Input Current | Any One Input | -10 | 10 | mA |
| T _{JMAX1} | Maximum junction temperature, ceramic package | | 175 | °C |
| T _{JMAX2} | Maximum junction temperature, plastic package | | 150 | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | VALUE | UNIT |
|---|-------------------------|---|------|
| CD4051B-Q1 in PDIP, CDIP, SOIC, SOP, TSSOP Packages | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2 | V |
| | | Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6 | |
| CD4053B-Q1 in PDIP, CDIP, SOP and TSSOP Packages | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2 | V |
| | | Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|-------------------|-----|-----|------|
| Temperature Range | -55 | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | CD405xB-Q1 | | UNIT | |
|-------------------------------|--|---------|------|------|
| | D | PW | | |
| | 16 Pins | 16 Pins | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 86.7 | 108 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 47.3 | | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 45.3 | | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 12.1 | | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 44.9 | | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

 over operating free-air temperature range, $V_{\text{SUPPLY}} = \pm 5 \text{ V}$, and $R_L = 100 \Omega$, (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT | |
|---|-------------------------|---------------------|---------------------|---------------------|-------|------------|------------------|----------|---------------|------|
| | V_{IS} (V) | V_{EE} (V) | V_{SS} (V) | V_{DD} (V) | TEMP | | | | | |
| SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS}) | | | | | | | | | | |
| Quiescent Device Current, I_{DD} Max | 5 | | | | -55°C | | | 5 | μA | |
| | | | | | -40°C | | | 5 | | |
| | | | | | 25°C | 0.04 | | 5 | | |
| | | | | | 85°C | | | 150 | | |
| | | | | | 125°C | | | 150 | | |
| | 10 | | | | | -55°C | | | | 10 |
| | | | | | | -40°C | | | | 10 |
| | | | | | | 25°C | 0.04 | | | 10 |
| | | | | | | 85°C | | | | 300 |
| | | | | | | 125°C | | | | 300 |
| | 15 | | | | | -55°C | | | | 20 |
| | | | | | | -40°C | | | | 20 |
| | | | | | | 25°C | 0.04 | | | 20 |
| | | | | | | 85°C | | | | 600 |
| | | | | | | 125°C | | | | 600 |
| | 20 | | | | | -55°C | | | | 100 |
| | | | | | | -40°C | | | | 100 |
| | | | | | | 25°C | 0.08 | | | 100 |
| | | | | | | 85°C | | | | 3000 |
| | | | | | | 125°C | | | | 3000 |
| Drain to Source ON Resistance r_{ON} Max $0 \leq V_{\text{IS}} \leq V_{\text{DD}}$ | 5 | 0 | 0 | 0 | -55°C | | | 800 | Ω | |
| | | | | | -40°C | | | 850 | | |
| | | | | | 25°C | 470 | | 1050 | | |
| | | | | | 85°C | | | 1200 | | |
| | | | | | 125°C | | | 1300 | | |
| | 10 | 0 | 0 | 0 | 0 | -55°C | | | | 310 |
| | | | | | | -40°C | | | | 300 |
| | | | | | | 25°C | 180 | | | 400 |
| | | | | | | 85°C | | | | 520 |
| | 15 | 0 | 0 | 0 | 0 | -55°C | | | | 200 |
| | | | | | | -40°C | | | | 210 |
| | | | | | | 25°C | 125 | | | 240 |
| 85°C | | | | | | | | 300 | | |
| Change in ON Resistance (Between Any Two Channels), Δr_{ON} | 5 | 0 | 0 | 0 | 25°C | | 15 | Ω | | |
| | | | | | | 10 | 10 | | | |
| | | | | | | 15 | 5 | | | |
| OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max) | 18 | 0 | 0 | 0 | -55°C | | ± 100 | nA | | |
| | | | | | -40°C | | | | | |
| | | | | | 25°C | ± 0.01 | $\pm 100^{(2)}$ | | | |
| | | | | | 85°C | | $\pm 1000^{(2)}$ | | | |
| | | | | | 125°C | | | | | |
| ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (Common OUT/IN) (Max) | 5 or 0 | -5 | 0 | 10.5 | 85°C | | $\pm 300^{(3)}$ | nA | | |
| | 5 | 0 | 0 | 18 | 85°C | | $\pm 300^{(3)}$ | | | |
| Capacitance | Input, C_{IS} | -5 | -5 | -5 | 25°C | | 5 | pF | | |
| | Output, C_{OS} | CD4051B-Q1 | | | 25°C | | 30 | | | |
| | | CD4053B-Q1 | | | | 9 | | | | |
| Feed through, C_{IOS} | | | | | | | 0.2 | | | |


 (1) Peak-to-Peak voltage symmetrical about $(V_{\text{DD}} - V_{\text{EE}}) / 2$.

(2) Determined by minimum feasible leakage measurement for automatic testing.

(3) Does not apply to Hi-Rel CD4051BF and CD4051BFA3 devices.

Electrical Characteristics (continued)

over operating free-air temperature range, $V_{\text{SUPPLY}} = \pm 5 \text{ V}$, and $R_L = 100 \Omega$, (unless otherwise noted)⁽¹⁾

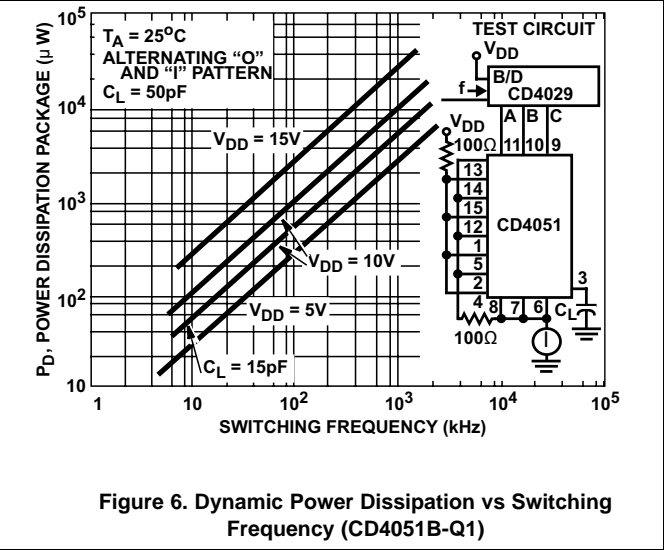
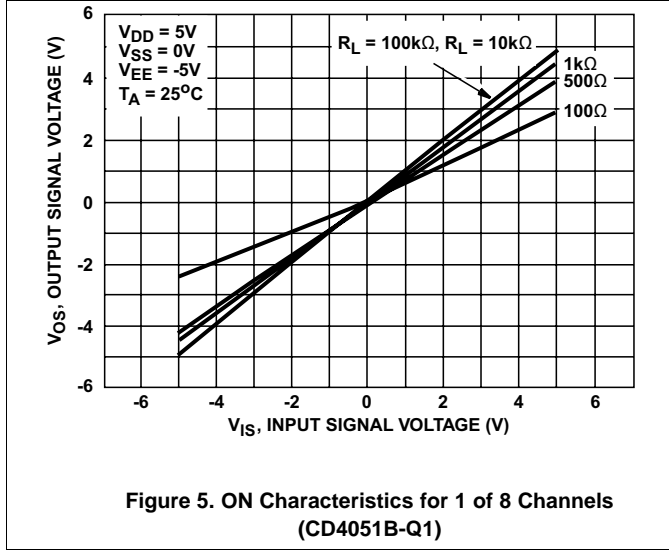
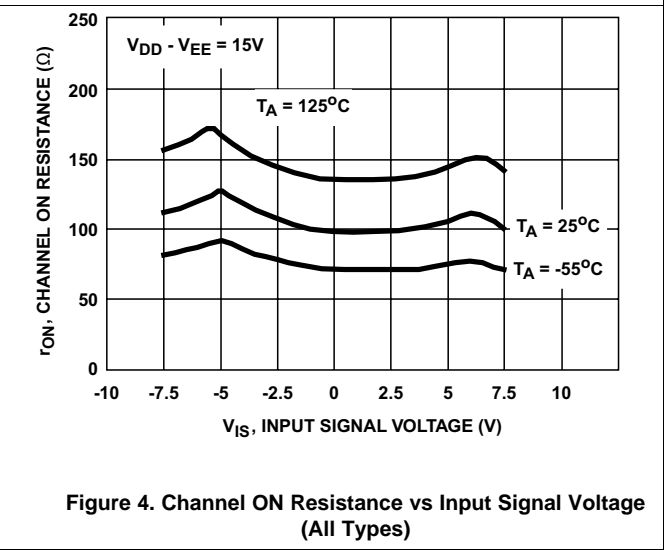
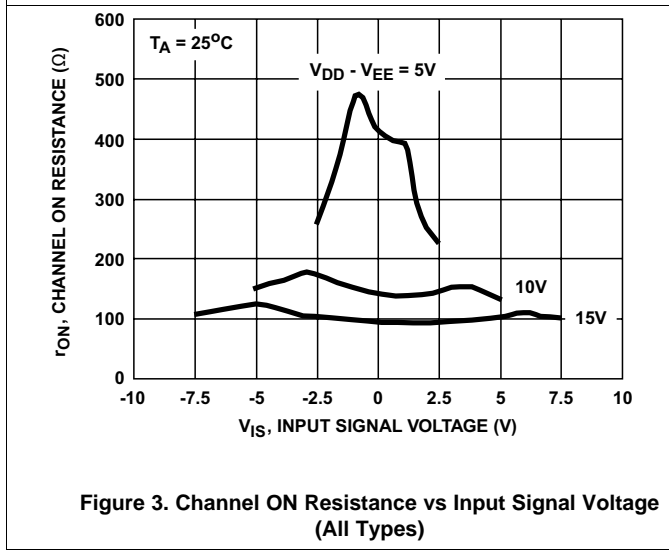
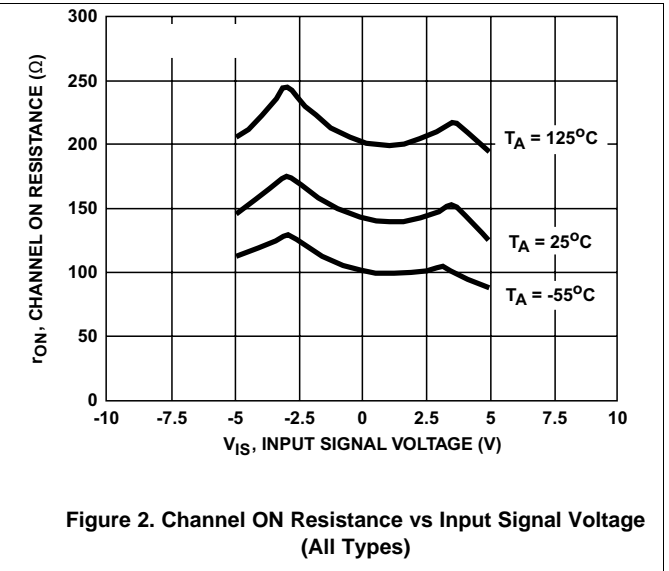
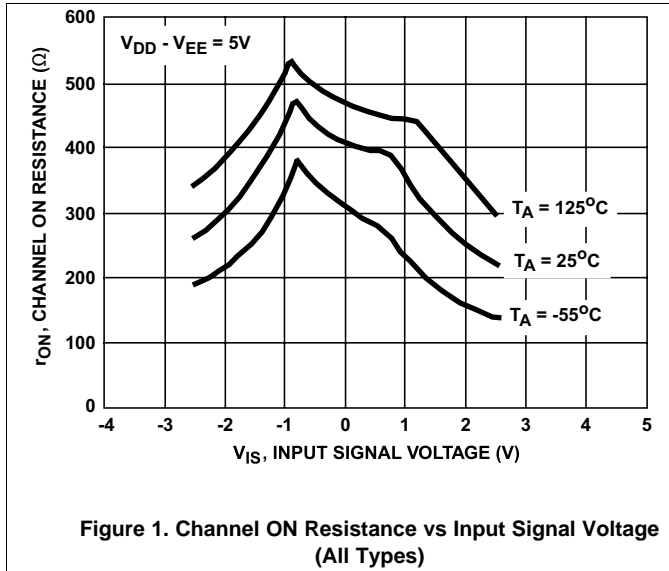
| PARAMETER | | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT | | | | | |
|---|---|--|---|---------------------|---------------------|------|-----|-----|-----|---------------|-------|---------------|-----------|-----|-----|
| | | V_{IS} (V) | V_{EE} (V) | V_{SS} (V) | V_{DD} (V) | TEMP | | | | | | | | | |
| Propagation Delay Time (Signal Input to Output) |  | V_{DD} | $R_L = 200 \text{ k}\Omega$, | | 5 | 25°C | 30 | 60 | ns | | | | | | |
| | | | $C_L = 50 \text{ pF}$, | | 10 | | 15 | 30 | | | | | | | |
| | | $t_r, t_f = 20 \text{ ns}$ | | 15 | 10 | 20 | | | | | | | | | |
| CONTROL (ADDRESS OR INHIBIT), V_C | | | | | | | | | | | | | | | |
| Input Low Voltage, V_{IL} , Max | | $V_{\text{IL}} = V_{\text{DD}}$ through 1 k Ω ; $V_{\text{IH}} = V_{\text{DD}}$ through 1 k Ω | $V_{\text{EE}} = V_{\text{SS}}$, $R_L = 1 \text{ k}\Omega$ to V_{SS} , $I_{\text{IS}} < 2 \mu\text{A}$ on All OFF Channels | | | | | | | V | | | | | |
| | | | | | | | | | | | 5 | -55°C | 1.5 | | |
| | | | | | | | | | | | | -40°C | 1.5 | | |
| | | | | | | | | | | | | 25°C | | 1.5 | |
| | | | | | | | | | | | | 85°C | 1.5 | | |
| | | | | | | | | | | | | 125°C | 1.5 | | |
| | | | | | | | | | | | 10 | -55°C | 3 | | |
| | | | | | | | | | | | | -40°C | 3 | | |
| | | | | | | | | | | | | 25°C | | 3 | |
| | | | | | | | | | | | | 85°C | 3 | | |
| | | | | | | | | | | | | 125°C | 3 | | |
| | | | | | | | | | | | 15 | -55°C | 4 | | |
| | | | | | | | | | | | | -40°C | 4 | | |
| | | | | | | | | | | | | 25°C | | 4 | |
| | | | | | | | | | | | | 85°C | 4 | | |
| 125°C | 4 | | | | | | | | | | | | | | |
| Input High Voltage, V_{IH} , Min | | $V_{\text{IL}} = V_{\text{DD}}$ through 1 k Ω ; $V_{\text{IH}} = V_{\text{DD}}$ through 1 k Ω | $V_{\text{EE}} = V_{\text{SS}}$, $R_L = 1 \text{ k}\Omega$ to V_{SS} , $I_{\text{IS}} < 2 \mu\text{A}$ on All OFF Channels | | | | | | | V | | | | | |
| | | | | | | | | | | | 5 | -55°C | 3.5 | | |
| | | | | | | | | | | | | -40°C | 3.5 | | |
| | | | | | | | | | | | | 25°C | 3.5 | | |
| | | | | | | | | | | | | 85°C | 3.5 | | |
| | | | | | | | | | | | | 125°C | 3.5 | | |
| | | | | | | | | | | | 10 | -55°C | 7 | | |
| | | | | | | | | | | | | -40°C | 7 | | |
| | | | | | | | | | | | | 25°C | 7 | | |
| | | | | | | | | | | | | 85°C | 7 | | |
| | | | | | | | | | | | | 125°C | 7 | | |
| | | | | | | | | | | | 15 | -55°C | 11 | | |
| | | | | | | | | | | | | -40°C | 11 | | |
| | | | | | | | | | | | | 25°C | 11 | | |
| | | | | | | | | | | | | 85°C | 11 | | |
| 125°C | 11 | | | | | | | | | | | | | | |
| Input Current, I_{IN} (Max) | | | $V_{\text{IN}} = 0, 18$ | | | 18 | | | | μA | | | | | |
| | | | | | | | | | | | -55°C | ± 0.1 | | | |
| | | | | | | | | | | | -40°C | ± 0.1 | | | |
| | | | | | | | | | | | 25°C | $\pm 10^{-5}$ | ± 0.1 | | |
| | | | | | | | | | | | 85°C | ± 1 | | | |
| Propagation Delay Time | Address-to-Signal OUT (Channels ON or OFF) (See Figure 9, Figure 10, and Figure 14) | $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 10 \text{ k}\Omega$ | | | | | | | | ns | | | | | |
| | | | | | | | | | | | 0 | 0 | 5 | 450 | 720 |
| | | | | | | | | | | | 0 | 0 | 10 | 160 | 320 |
| | | | | | | | | | | | 0 | 0 | 15 | 120 | 240 |
| Propagation Delay Time | Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 10) | $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 1 \text{ k}\Omega$ | | | | | | | | ns | | | | | |
| | | | | | | | | | | | 0 | 0 | 5 | 400 | 720 |
| | | | | | | | | | | | 0 | 0 | 10 | 160 | 320 |
| | | | | | | | | | | | 0 | 0 | 15 | 120 | 240 |
| Propagation Delay Time | Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 16) | $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 10 \text{ k}\Omega$ | | | | | | | | ns | | | | | |
| | | | | | | | | | | | -10 | 0 | 5 | 200 | 400 |
| | | | | | | | | | | | 0 | 0 | 5 | 200 | 450 |
| | | | | | | | | | | | 0 | 0 | 10 | 90 | 210 |
| Input Capacitance, C_{IN} (Any Address or Inhibit Input) | | | | | | | | | | pF | | | | | |
| | | | | | | | | | | | 0 | 0 | 15 | 70 | 160 |
| | | | | | | | | | | | -10 | 0 | 5 | 130 | 300 |
| | | | | | | | 5 | 7.5 | | | | | | | |

6.6 AC Performance Characteristics

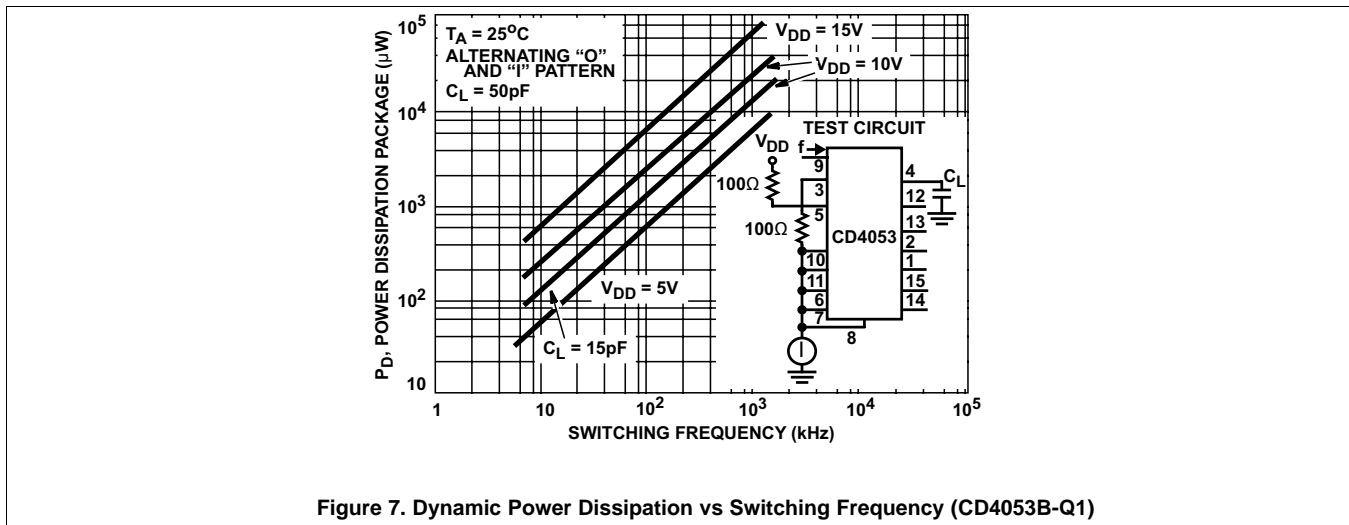
| PARAMETER | TEST CONDITIONS | | | | TYP | UNIT | |
|---|---|---------------------|---------------------|--|-------------------------|-------|--------------------|
| | V _{IS} (V) | V _{DD} (V) | R _L (kΩ) | | | | |
| Cutoff (–3dB) Frequency Channel ON (Sine Wave Input) | 5 ⁽¹⁾ | 10 | 1 | V _{OS} at Common OUT/IN | CD4053B-Q1 | 30 | MHz |
| | | | | | CD4051B-Q1 | 20 | |
| | $V_{EE} = V_{SS},$ $20 \text{Log} \frac{V_{OS}}{V_{IS}} = -3 \text{ dB}$ | | | V _{OS} at Any Channel | | 60 | |
| Total Harmonic Distortion, THD | 2 ⁽¹⁾ | 5 | 10 | | | 0.3% | |
| | 3 ⁽¹⁾ | 10 | | | | 0.2% | |
| | 5 ⁽¹⁾ | 15 | | | | 0.12% | |
| | $V_{EE} = V_{SS}, f_{IS} = 1 \text{ kHz Sine Wave}$ | | | | | | |
| –40dB Feedthrough Frequency (All Channels OFF) | 5 ⁽¹⁾ | 10 | 1 | V _{OS} at Common OUT/IN | CD4053B-Q1 | 8 | MHz |
| | | | | | CD4051B-Q1 | 12 | |
| | $V_{EE} = V_{SS},$ $20 \text{Log} \frac{V_{OS}}{V_{IS}} = -40 \text{ dB}$ | | | V _{OS} at Any Channel | | 8 | |
| –40dB Signal Crosstalk Frequency | 5 ⁽¹⁾ | 10 | 1 | Between Any two Channels | | 3 | MHz |
| | $V_{EE} = V_{SS},$ $20 \text{Log} \frac{V_{OS}}{V_{IS}} = -40 \text{ dB}$ | | | Between Sections, CD4052 Only | Measured on Common | 6 | |
| | | | | | Measured on Any Channel | 10 | |
| | | | | Between Any Two Sections, CD4053 Only | In Pin 2, Out Pin 14 | 2.5 | |
| | | | | | In Pin 15, Out Pin 14 | 6 | |
| Address-or-Inhibit-to- Signal Crosstalk | | 10 | 10 ⁽²⁾ | | | 65 | mV _{PEAK} |
| | $V_{EE} = 0, V_{SS} = 0, t_r, t_f = 20 \text{ ns},$ $V_{CC} = V_{DD} - V_{SS} \text{ (Square Wave)}$ | | | | | 65 | |

- (1) Peak-to-Peak voltage symmetrical about $(V_{DD} - V_{EE}) / 2$.
 (2) Both ends of channel.

6.7 Typical Characteristics



Typical Characteristics (continued)



7 Parameter Measurement Information

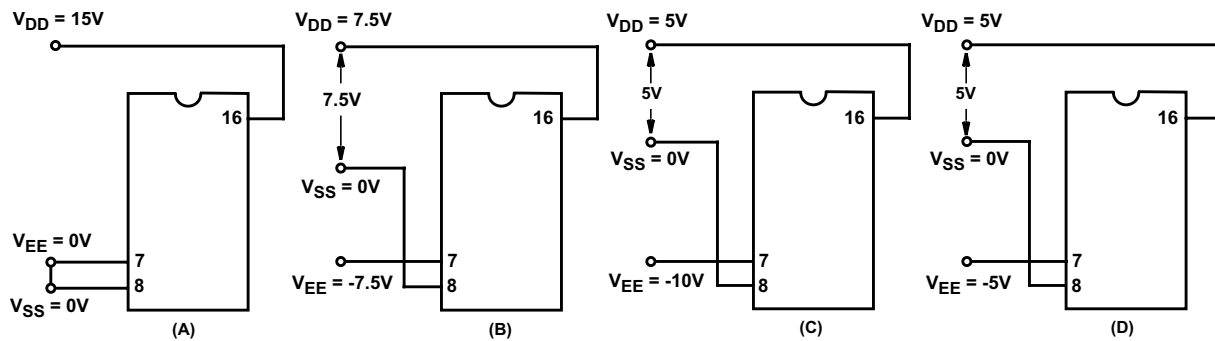


Figure 8. Typical Bias Voltages

NOTE

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: 0 = V_{SS} and 1 = V_{DD} . The analog signal (through the TG) may swing from V_{EE} to V_{DD} .

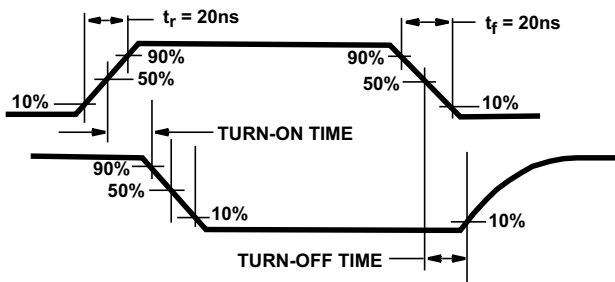


Figure 9. Waveforms, Channel Being Turned ON ($R_L = 1\text{ k}\Omega$)

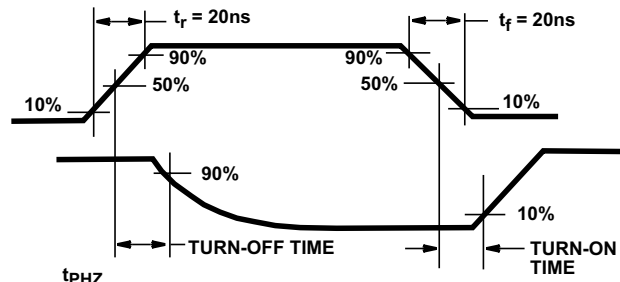


Figure 10. Waveforms, Channel Being Turned OFF ($R_L = 1\text{ k}\Omega$)

Parameter Measurement Information (continued)

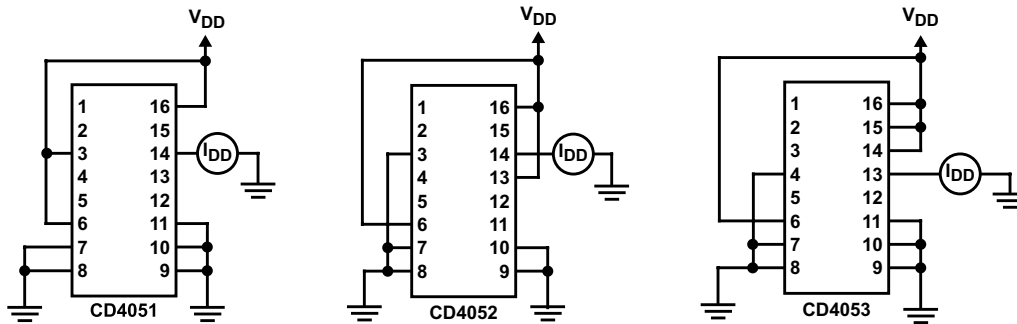
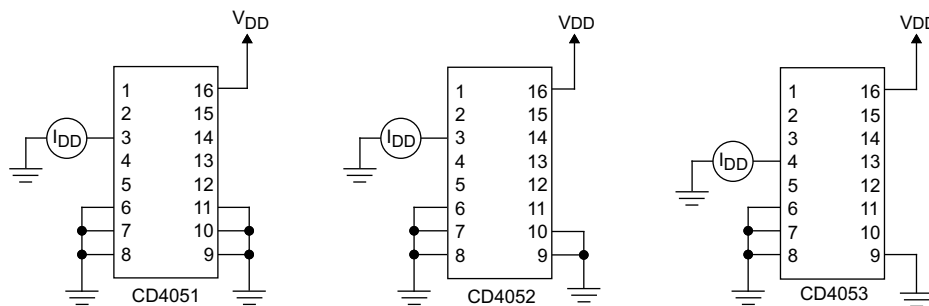


Figure 11. OFF Channel Leakage Current - Any Channel OFF



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Figure 12. On Channel Leakage Current - Any Channel On

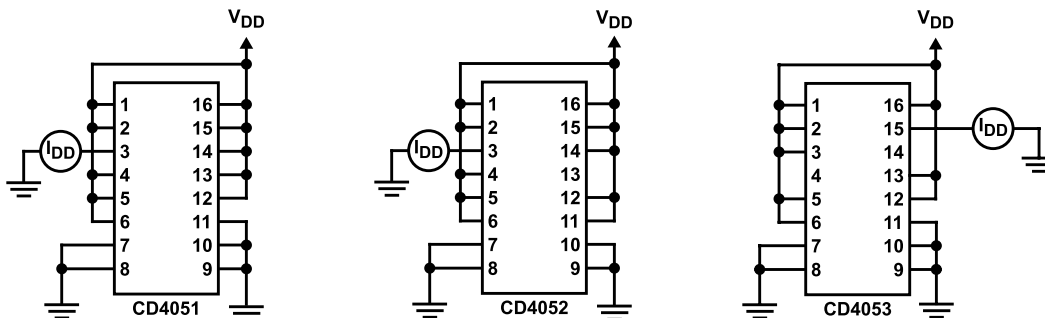


Figure 13. OFF Channel Leakage Current - All Channels OFF

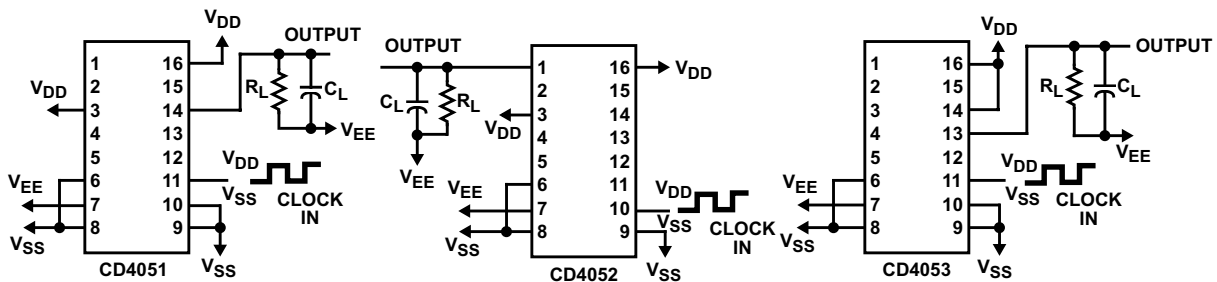


Figure 14. Propagation Delay - Address Input to Signal Output

Parameter Measurement Information (continued)

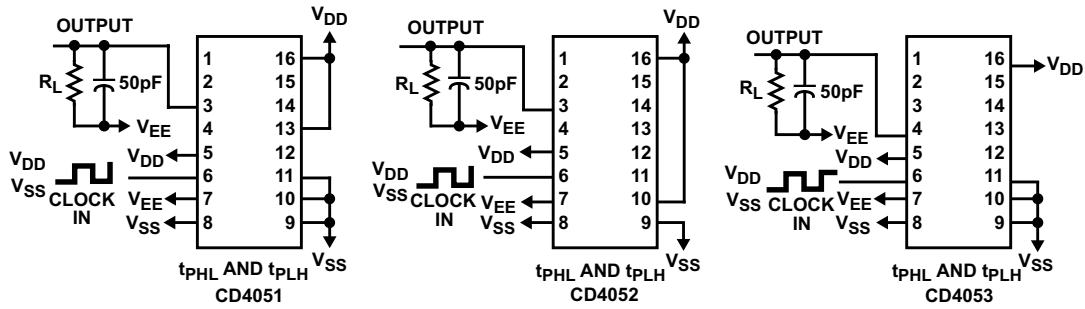


Figure 15. Propagation Delay - Inhibit Input to Signal Output

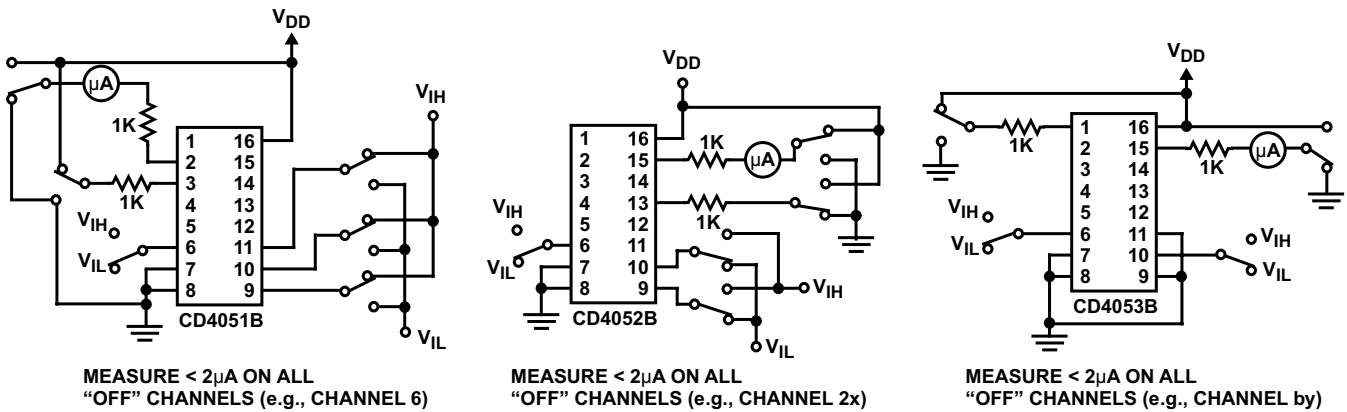


Figure 16. Input Voltage Test Circuits (Noise Immunity)

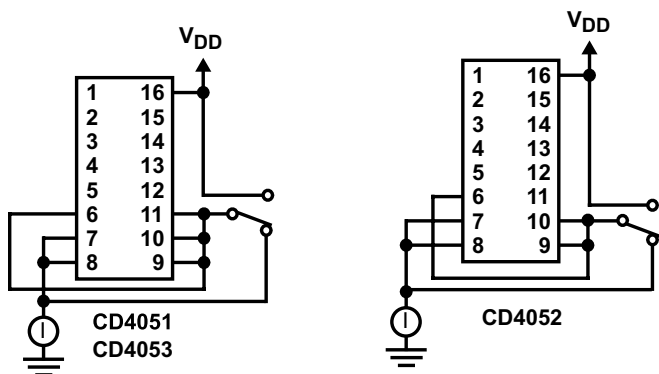


Figure 17. Quiescent Device Current

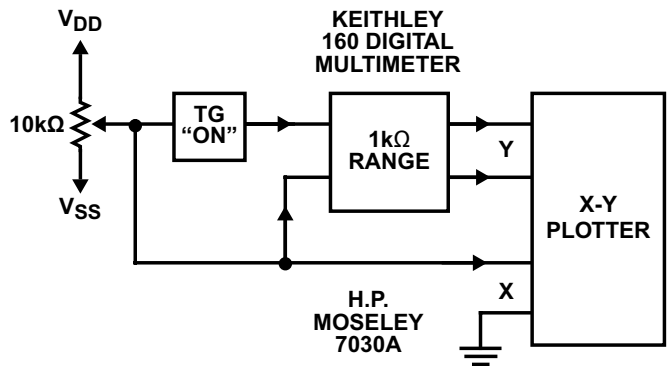


Figure 18. Channel ON Resistance Measurement Circuit

Parameter Measurement Information (continued)

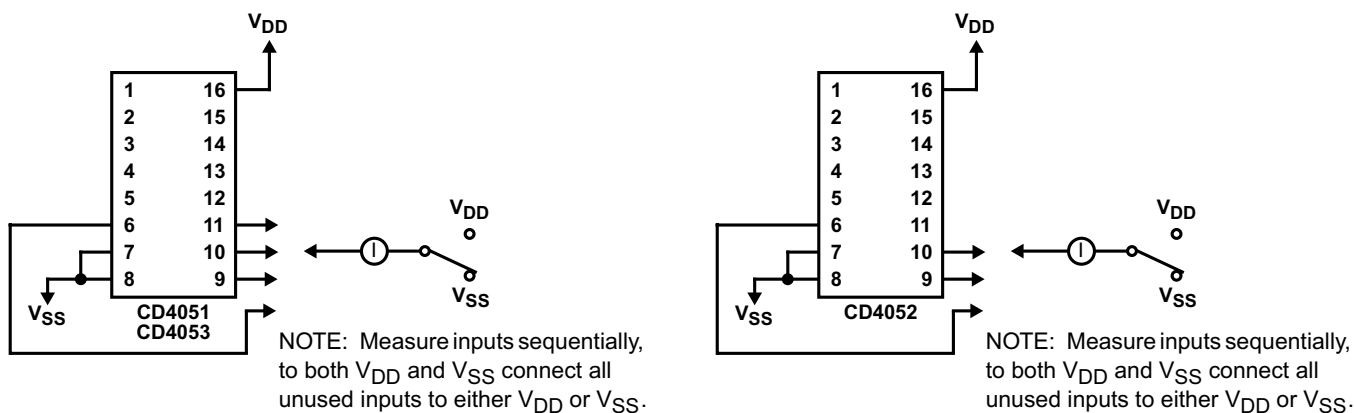


Figure 19. Input Current

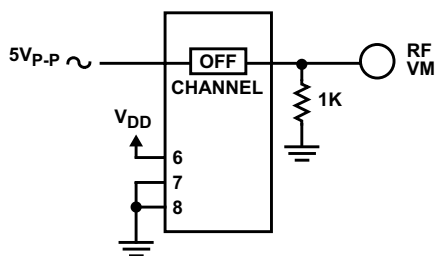


Figure 20. Feedthrough (All Types)

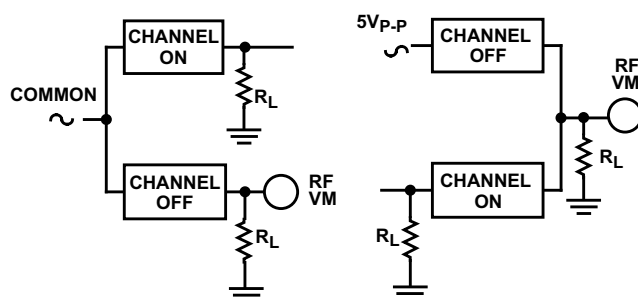


Figure 21. Crosstalk Between Any Two Channels (All Types)

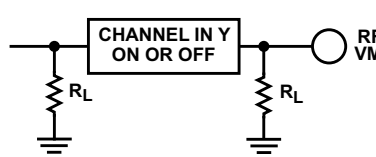
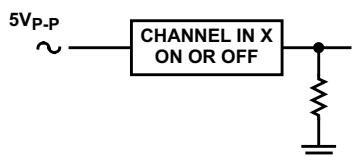


Figure 22. Crosstalk Between Duals or Triplets (CD4053B-Q1)

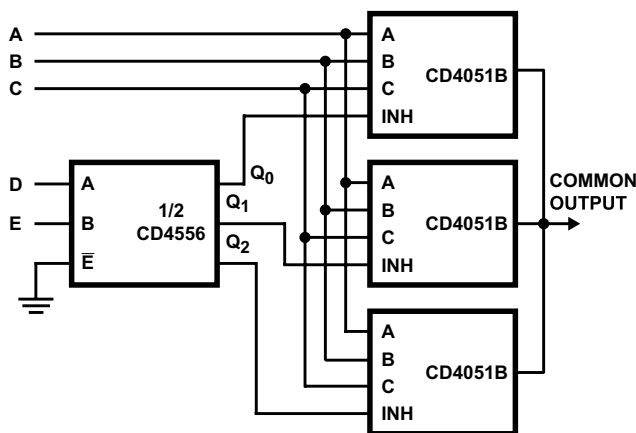


Figure 23. 24-to-1 MUX Addressing

8 Detailed Description

8.1 Overview

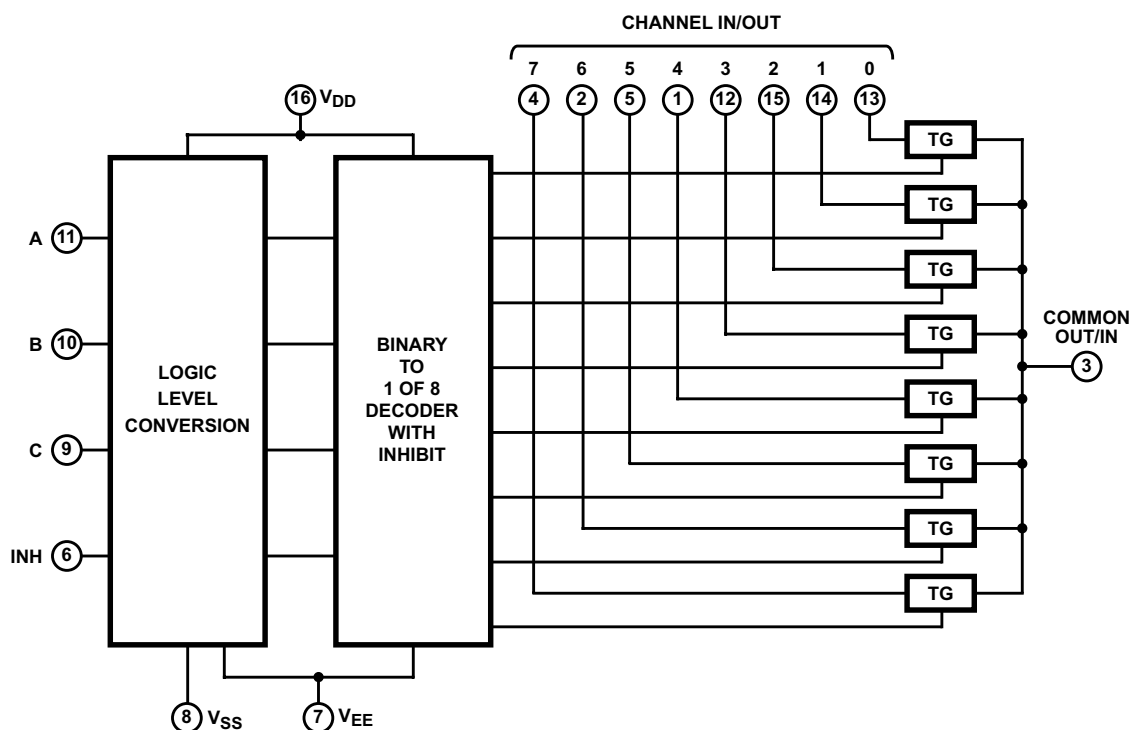
The CD4051B-Q1 and CD4053B-Q1 analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V_{P-P} can be achieved by digital signal amplitudes of 4.5 V to 20 V (if $V_{DD} - V_{SS} = 3$ V, a $V_{DD} - V_{EE}$ of up to 13 V can be controlled; for $V_{DD} - V_{EE}$ level differences above 13 V, a $V_{DD} - V_{SS}$ of at least 4.5 V is required). For example, if $V_{DD} = +4.5$ V, $V_{SS} = 0$ V, and $V_{EE} = -13.5$ V, analog signals from -13.5 V to $+4.5$ V can be controlled by digital inputs of 0 V to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic 1 is present at the inhibit input terminal, all channels are off.

The CD4051B-Q1 device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4053B-Q1 device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

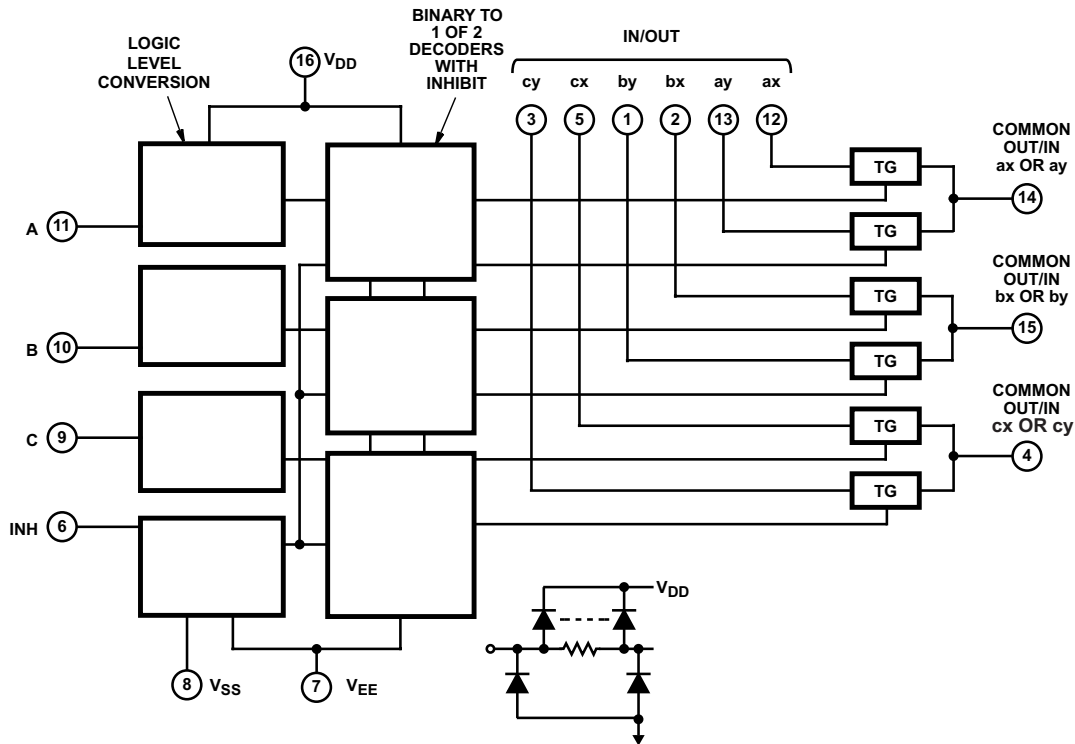
8.2 Functional Block Diagrams



All inputs are protected by standard CMOS protection network.

Figure 24. Functional Block Diagram, CD4051B-Q1

Functional Block Diagrams (continued)



All inputs are protected by standard CMOS protection network.

Figure 25. Functional Block Diagram, CD4053B-Q1

8.3 Feature Description

The CD405xB-Q1 line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3 V to 20 V, and analog signals are accepted at levels ≤ 20 V. They have low ON resistance, typically 125 Ω over 15 V_{P-P} signal input range for $V_{DD} - V_{EE} = 18$ V. This allows for very little signal loss through the switch. Matched switch characteristics are typically $r_{ON} = 5 \Omega$ for $V_{DD} - V_{EE} = 15$ V.

The CD405xB-Q1 devices also have high OFF resistance, which keeps from wasting power when the switch is in the OFF position, with typical channel leakage of ± 100 pA at $V_{DD} - V_{EE} = 18$ V. Very low quiescent power dissipation under all digital-control input and supply conditions, typically 0.2 μW at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10$ V keeps power consumption total very low. All devices have been 100% tested for quiescent current at 20 V with maximum input current of 1 μA at 18 V over the full package temperature range, and only 100 nA at 18 V and 25°C.

Logic-level conversion for digital addressing signals of 3 V to 20 V ($V_{DD} - V_{SS} = 3$ V to 20 V) to switch analog signals to 20 V_{P-P} ($V_{DD} - V_{EE} = 20$ V). Binary address decoding on chip makes channel selection easy. When channels are changed, a break-before-make system eliminates channel overlap.

8.4 Device Functional Modes

Table 1. Truth Table⁽¹⁾

| INPUT STATES | | | | ON CHANNEL(S) |
|-------------------|---|---|---|----------------|
| INHIBIT | C | B | A | |
| CD4051B-Q1 | | | | |
| L | L | L | L | 0 |
| L | L | L | H | 1 |
| L | L | H | L | 2 |
| L | L | H | H | 3 |
| L | H | L | L | 4 |
| L | H | L | H | 5 |
| L | H | H | L | 6 |
| L | H | H | H | 7 |
| H | X | X | X | None |
| CD4053B | | | | |
| L | L | L | L | ay or by or cy |
| L | H | H | H | ay or by or cy |
| H | X | X | X | None |

(1) X = Don't Care

Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - For switch time specifications, see propagation delay times in [Electrical Characteristics](#).
 - Inputs should not be pushed more than 0.5 V above V_{DD} or below V_{EE} .
 - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in [Electrical Characteristics](#).
2. Recommended Output Conditions
 - Outputs should not be pulled above V_{DD} or below V_{EE} .
3. Input/output current consideration: The CD405xB-Q1 series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

9.2.3 Application Curve

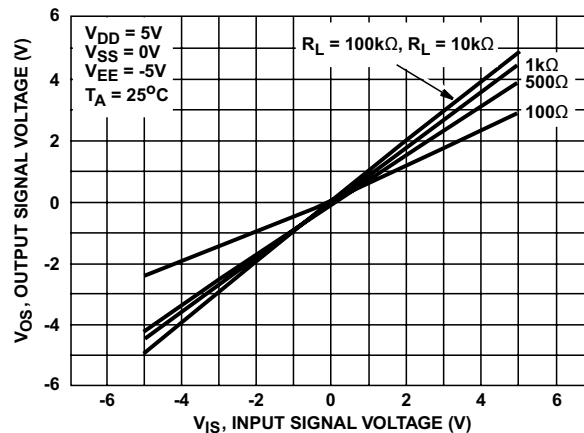


Figure 27. ON Characteristics for 1 of 8 Channels (CD4051B-Q1)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Electrical Characteristics](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. [Figure 28](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

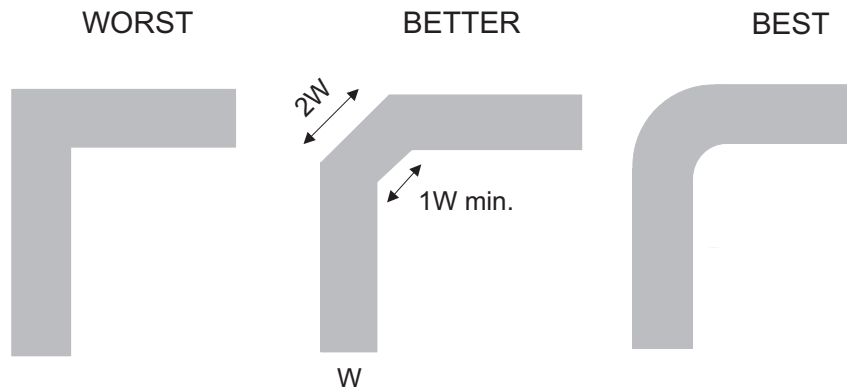


Figure 28. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD4051B-Q1 | Click here | Click here | Click here | Click here | Click here |
| CD4053B-Q1 | Click here | Click here | Click here | Click here | Click here |

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD4051BQPWRG4Q1 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CM051BQ | Samples |
| CD4051BQPWRQ1 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CM051BQ | Samples |
| CD4053BQM96G4Q1 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CD4053Q | Samples |
| CD4053BQM96Q1 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CD4053Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4051B-Q1, CD4053B-Q1 :

- Catalog: [CD4051B](#), [CD4053B](#)
- Military: [CD4051B-MIL](#), [CD4053B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4051BQPWRG4Q1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD4051BQPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

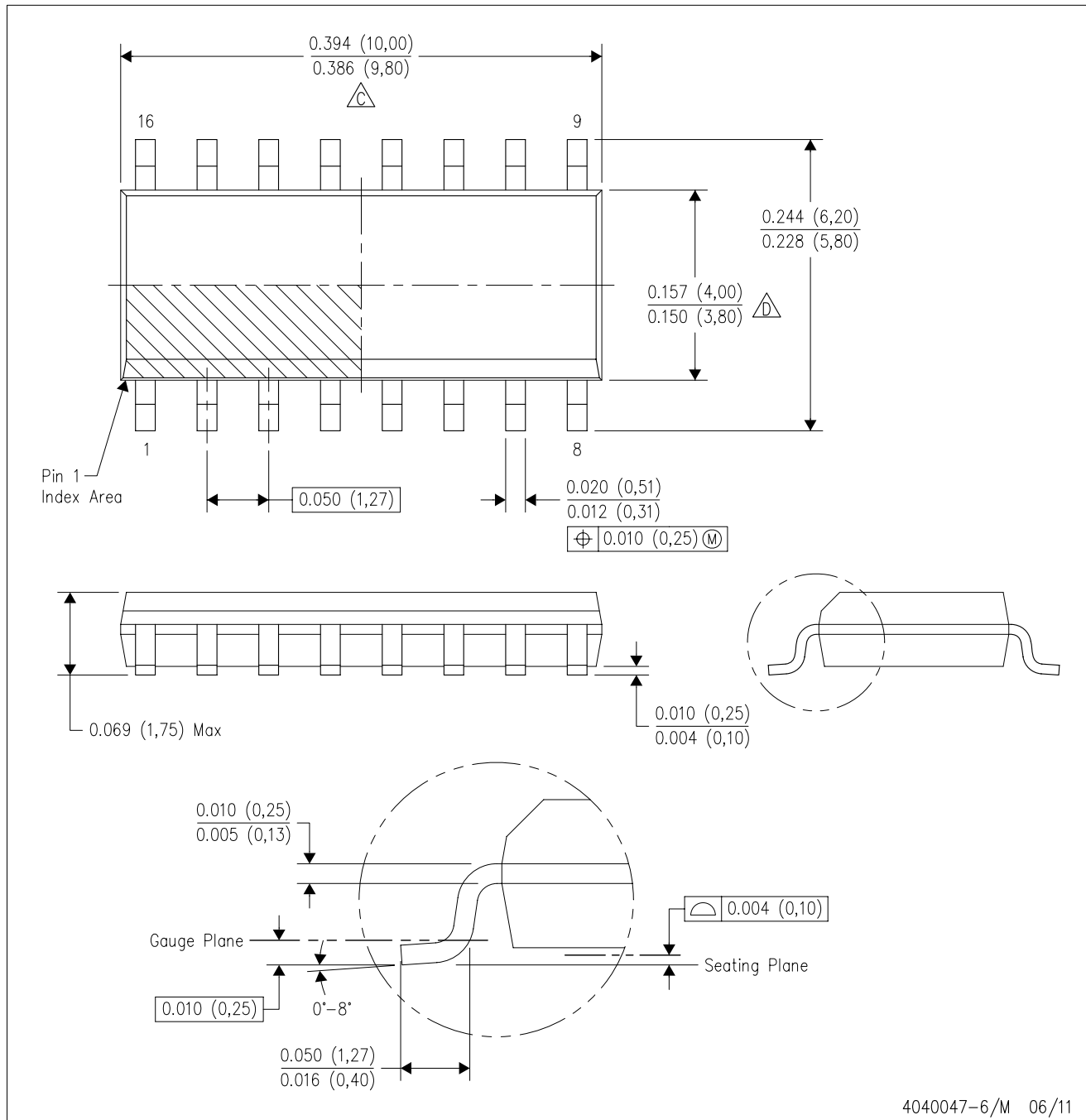
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4051BQPWRG4Q1 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| CD4051BQPWRQ1 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

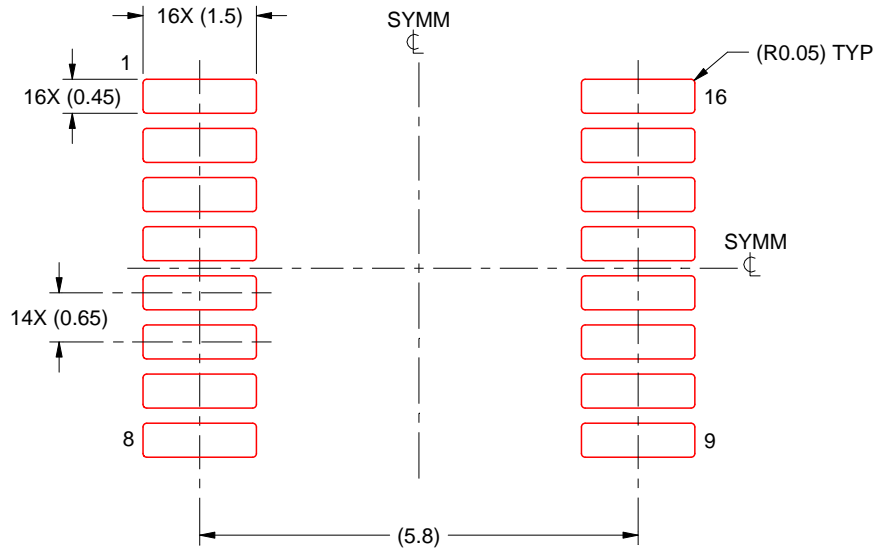
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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