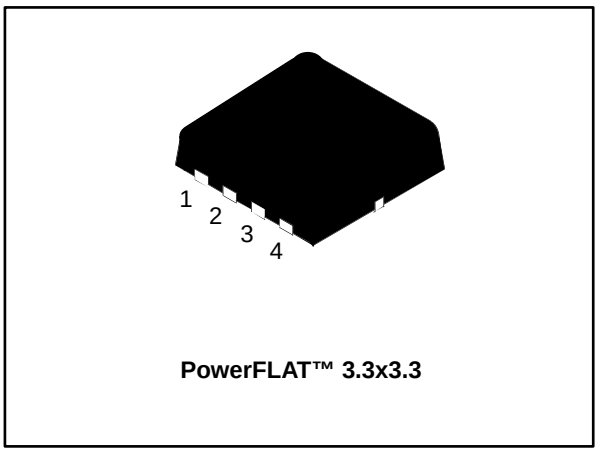
STL8P4LLF6

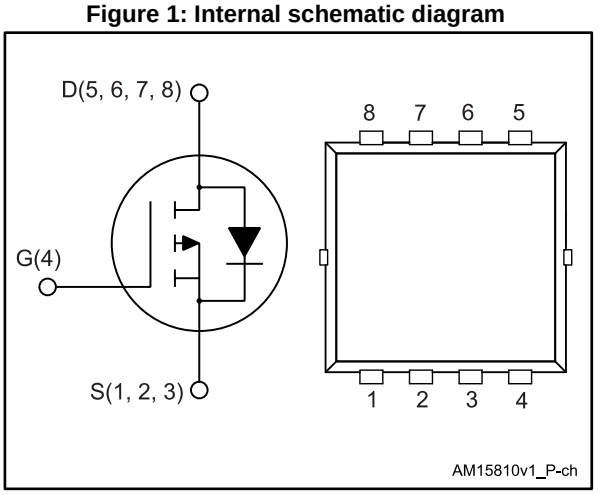
P-channel 40 V, 0.0175 Ω typ.,8 A, STripFET™ F6 Power MOSFET in a PowerFLAT™ 3.3 x 3.3 package

Datasheet - production data



PowerFLAT™ 3.3x3.3

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL8P4LLF6	40 V	0.0205 Ω	8 A	2.9 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL8P4LLF6	8P4F6	PowerFLAT™ 3.3 x 3.3	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_{pcb} = 25 °C	8	A
I_D (1)	Drain current (continuous) at T_{pcb} = 100 °C	5	A
I_{DM} (1)(2)	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at T_{pcb} = 25 °C	2.9	W
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Maximum junction temperature	150	°C

Notes:

(1)this value is related to $R_{thj\text{-}pcb}$

(2)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.50	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max.	42.8	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t ≤ 10 s

For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
		V_{GS} = 0 V, V_{DS} = 40 V, T_C = 125 °C			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		0.0175	0.0205	Ω
		V_{GS} = 4.5 V, I_D= 4 A		0.021	0.029	

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2850	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Reverse transfer capacitance		-	180	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 8 A, V_{GS} = 4.5 V (see *Figure 14: "Gate charge test circuit"*)	-	22	-	nC
Q_{gs}	Gate-source charge		-	9.4	-	nC
Q_{gd}	Gate-drain charge		-	7.3	-	nC
R_G	Gate input resistance	I_D = 0 A, gate DC bias = 0 V, f = 1 MHz, magnitude of alternative signal = 20 mV	-	1.4	-	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 4 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Switching times test circuit for resistive load"*)	-	43	-	ns
t_r	Rise time		-	47	-	ns
$t_{d(off)}$	Turn-off-delay time		-	148	-	ns
t_f	Fall time		-	19	-	ns

For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 8 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 32 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	26		ns
Q_{rr}	Reverse recovery charge		-	21		nC
I_{RRM}	Reverse recovery current		-	1.7		A

Notes:

(1)Pulse test: pulse duration = 300 µs, duty cycle 1.5%

For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

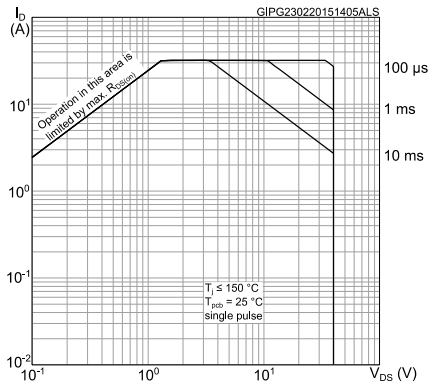


Figure 3: Thermal impedance

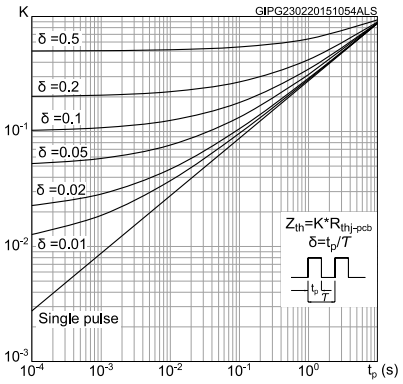


Figure 4: Output characteristics

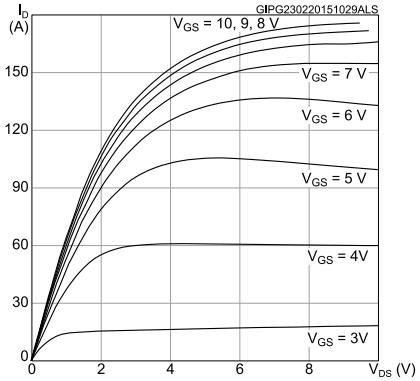


Figure 5: Transfer characteristics

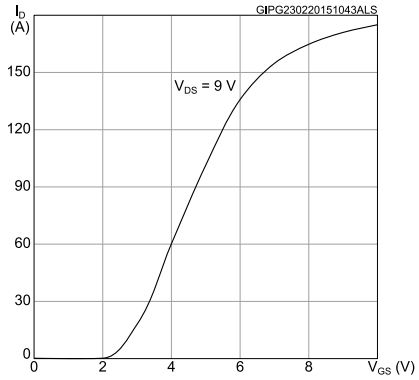


Figure 6: Normalized gate threshold voltage vs temperature

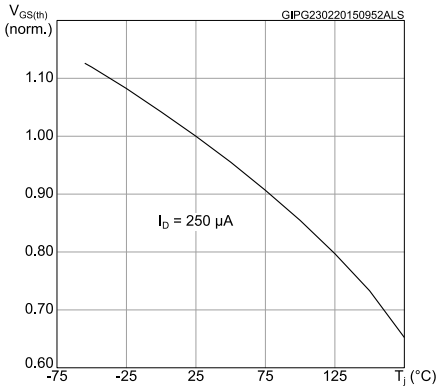


Figure 7: Normalized V(BR)DSS vs temperature

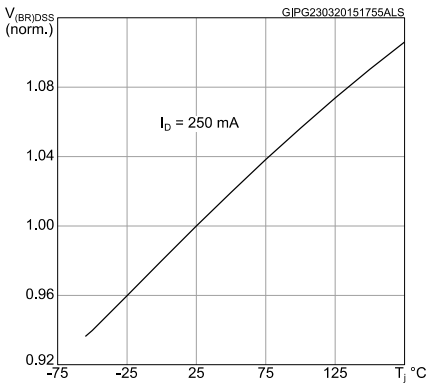


Figure 8: Static drain-source on-resistance

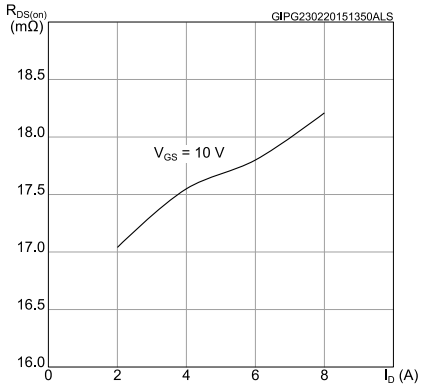


Figure 9: Normalized on-resistance vs. temperature

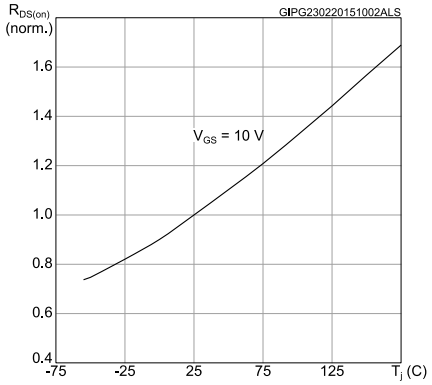


Figure 10: Gate charge vs gate-source voltage

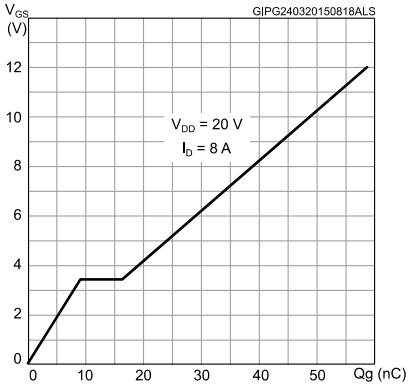


Figure 11: Capacitance variations voltage

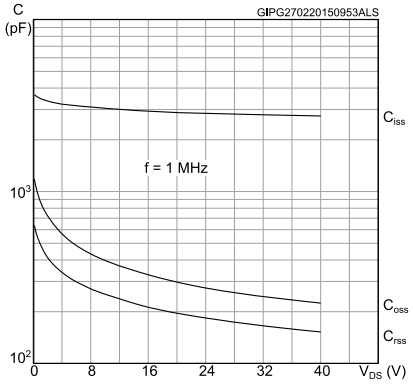
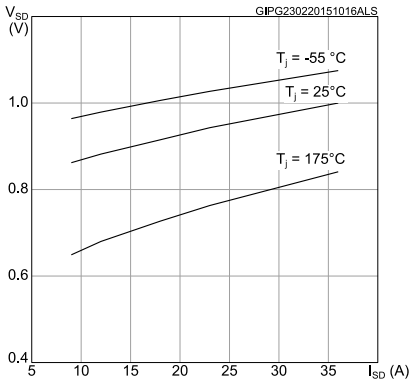


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

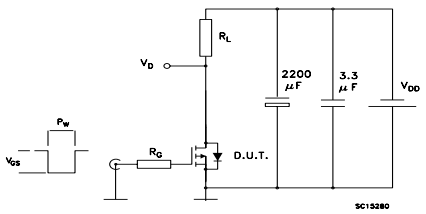


Figure 14: Gate charge test circuit

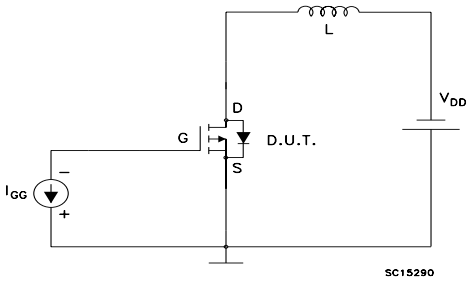
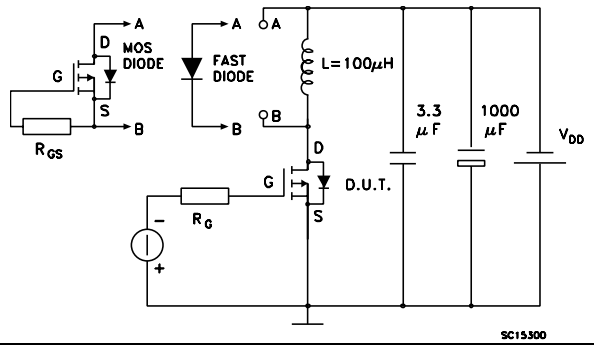


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 3.3x3.3 package information

Figure 16: PowerFLAT™ 3.3x3.3 package outline

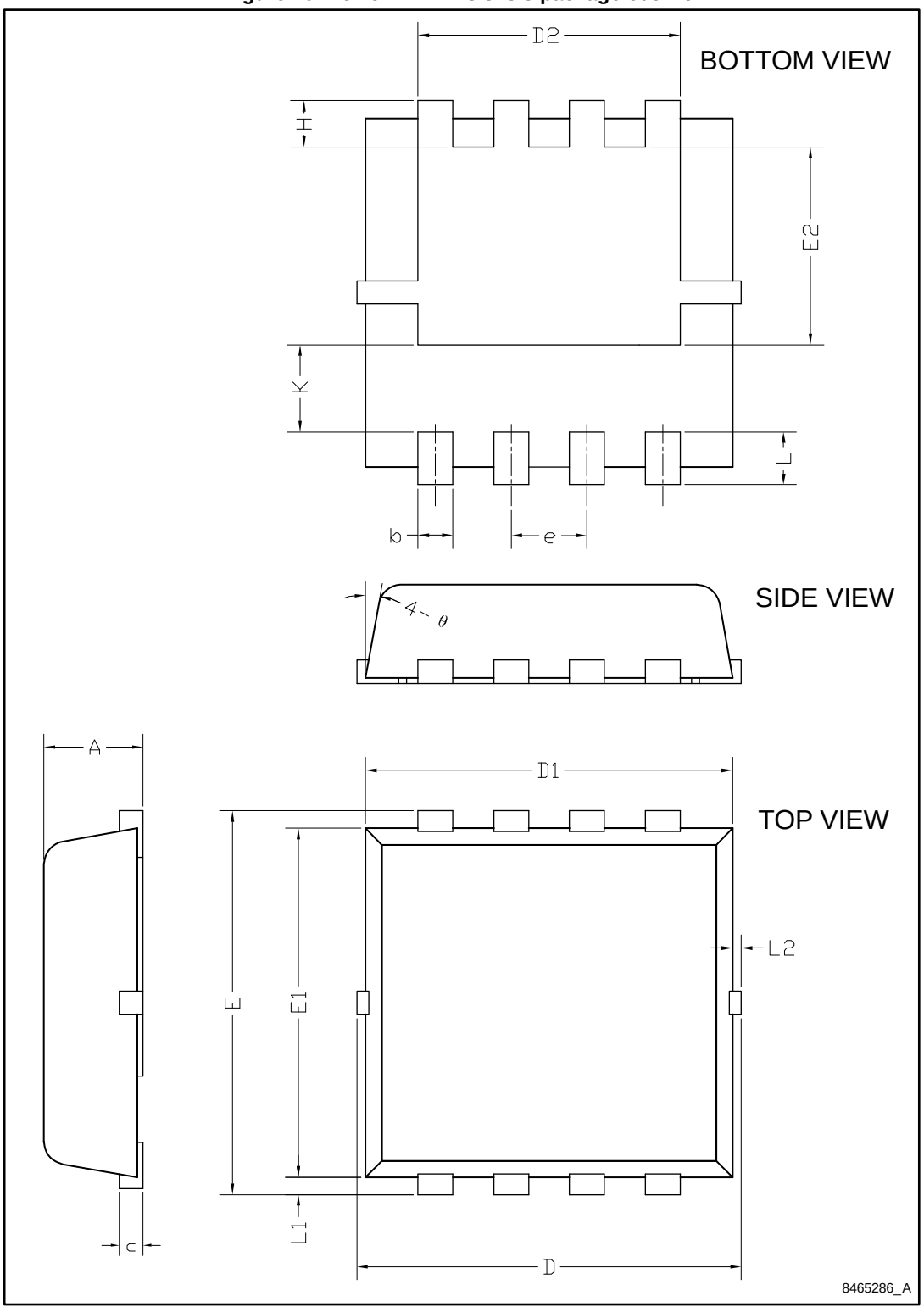
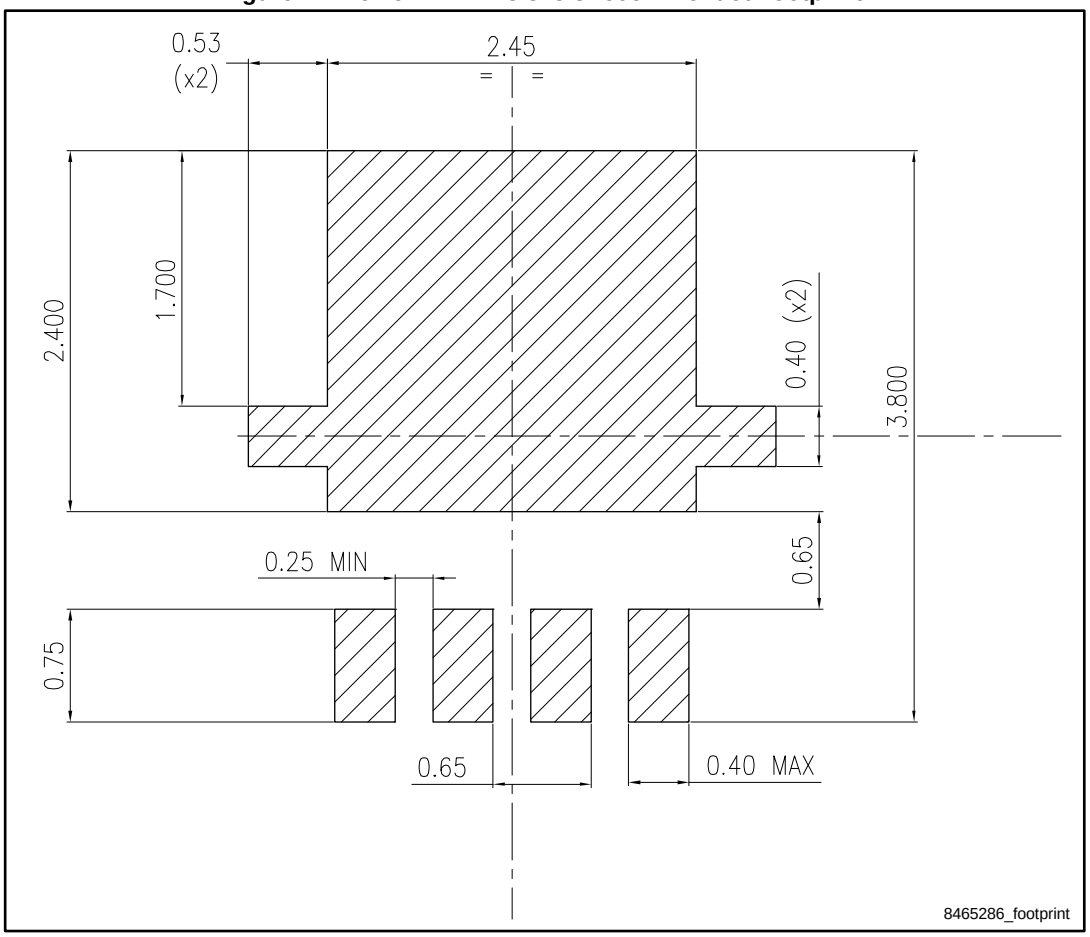


Table 8: PowerFLAT™ 3.3x3.3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	030	0.45	0.60
L1	0.05	0.15	0.25
L2			0.5
ϑ	8°	10°	12°

Figure 17: PowerFLAT™ 3.3x3.3 recommended footprint



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
28-Jan-2014	1	Initial release.
24-Mar-2015	2	Text edits throughout document On cover page, updated title, description and features table Updated Table 4: Static Updated Table 5: Dynamic Updated Table 6: Switching times Updated Table 7: Source-drain diode Added Section 2.1: Electrical characteristics (curves) Renamed and updated Section 4.1 PowerFLAT™ 3.3 x 3.3 package information

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

STMicroelectronics:

STL8P4LLF6