±60 V Fault Protection and Detection, 11 Ω R_{ON}, Dual SPST Switch

Data Sheet **ADG5421F**

FEATURES

- Overvoltage fault protection up to ±60 V on S1 and S2 pins
- Power-off protection up to ±60 V on S1 and S2 pins
- Known state without digital inputs present
- Low on resistance of 11 Ω typical
- Ultraflat, on resistance
- Latch-up immune under any circumstance
- 3.5 kV human body model (HBM) ESD rating
- V_{SS} to V_{DD} −2 V signal range
  - Fully specified at ±15 V, ±20 V, +12 V, and +36 V
  - ±5 V to ±22 V dual-supply operation
  - 8 V to 44 V single-supply operation
- 10-lead, 3 mm × 2 mm, LFCSP

APPLICATIONS

- Analog input and output modules
- Process control and distributed control systems
- Data acquisition
- Instrumentation
- Avionics
- Automatic test equipment
- Communication systems
- Relay replacement

GENERAL DESCRIPTION

The ADG5421F is a dual SPST, low on resistance switch that features overvoltage protection, power-off protection, and overvoltage detection on the source pins.

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. When powered, if the analog input signal levels on either of the Sx pins exceed V_{DD} or V_{SS} by the threshold voltage, V_T, both switches turn off together, and the open-drain fault flag (FF) pin pulls to a logic low. Input signal levels up to +60 V or −60 V relative to ground are blocked in both the powered and unpowered condition.

The switches turn on with a Logic 1 input and conduct equally well in both directions. The digital input is compatible with 1.8 V logic inputs over the full operating supply range.

FUNCTIONAL BLOCK DIAGRAM

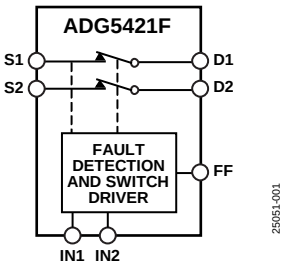

Figure 1.

COMPANION PRODUCTS

Precision 24-Bit ADC: AD7768-1
Precision 16-Bit, 2 MSPS SAR ADC: AD4000

PRODUCT HIGHLIGHTS

1. Source pins are protected against voltages greater than the supply rails, up to −60 V and +60 V in both powered and unpowered state.
2. Overvoltage detection with digital output indicates operating state of switches.
3. Trench isolation guards against latch-up.
4. The ADG5421F can operate from a dual supply of ±5 V up to ±22 V or a single power supply of +8 V up to +44 V.
5. Negative channel metal oxide semiconductor (NMOS) only architecture requires 2 V headroom towards V_{DD} and provides low R_{ON} and low R_{ON} flatness across the signal range of V_{SS} to V_{DD} − 2 V.

Rev. 0 Document Feedback

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REVISION HISTORY

10/2020—Revision 0: Initial Version

SPECIFICATIONS

Table 1. Operating Supply Voltages

Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGE				
Dual	±5		±22	V
Single	8		44	V

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +13.5 V, V_{SS} = −13.5 V
Analog Signal Range	V_{SS} to V_{DD} − 2			V	
On Resistance, R_{ON}	11.5			Ω typ	Source voltage (V_S) = V_{SS} to 10 V, source current (I_S) = 10 mA, see Figure 31
	14	17.5	20.5	Ω max	V_S = V_{SS} to 10 V, I_S = 10 mA
	11			Ω typ	V_S = V_{SS} to 9 V, I_S = 10 mA
	13.5	17	20	Ω max	V_S = V_{SS} to 9 V, I_S = 10 mA
On-Resistance Flatness, $R_{FLAT (ON)}$	0.3			Ω typ	V_S = V_{SS} to 10 V, I_S = 10 mA
	0.7	0.8	0.9	Ω max	V_S = V_{SS} to 10 V, I_S = 10 mA
	0.02			Ω typ	V_S = V_{SS} to 9 V, I_S = 10 mA
	0.06	0.1	0.1	Ω max	V_S = V_{SS} to 9 V, I_S = 10 mA
On-Resistance Matching, $R_{MATCH (ON)}$	0.02			Ω typ	V_S = V_{SS} to 10 V, I_S = 10 mA
	0.2	0.35	0.45	Ω max	V_S = V_{SS} to 10 V, I_S = 10 mA
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±10 V, drain voltage (V_D) = ∓ 10 V, see Figure 32
	±0.2	±2.5	±22	nA max	V_S = ±10 V, drain voltage (V_D) = ∓ 10 V
			±8	nA max	V_S = ±10 V, drain voltage (V_D) = ∓ 10 V, −40°C to +105°C
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓ 10 V, see Figure 32
	±0.2	±2.5	±22	nA max	V_S = ±10 V, V_D = ∓ 10 V
			±8	nA max	V_S = ±10 V, V_D = ∓ 10 V, −40°C to +105°C
Channel On Leakage, I_D (On), I_S (On)	±0.05			nA typ	V_S = ±10 V, V_D = ±10 V, see Figure 33
	±0.3	±3.5	±30	nA max	V_S = ±10 V, V_D = ±10 V
			±14	nA max	V_S = ±10 V, V_D = ±10 V, −40°C to +105°C
FAULT					
Threshold Voltage, V_T	0.7			V	See Figure 25
Source Leakage Current, I_S					
With Overvoltage			±30	µA typ	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±60 V, see Figure 34
Power Supplies Grounded or Floating			±5.5	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, IN = 0 V or floating, V_S = ±60 V, see Figure 35

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Drain Leakage Current, I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±60 V, see Figure 34
	±0.2	±2	±20	nA max	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V, see Figure 35
	±0.2	±2	±20	nA max	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V
Power Supplies Floating			±0.1	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, IN = 0 V, see Figure 35
DIGITAL INPUTS AND OUTPUTS					
Input Voltage High, V_{INH}			1.3	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Low or High Current, I_{INL} or I_{INH}	0.7			µA typ	Input voltage (V_{IN}) = 0 V or 5 V
			1	µA max	V_{IN} = 0 V or 5 V
Digital Input Capacitance, C_{IN}	5			pF typ	
Output Voltage Low, V_{OL}	0.4			V max	Fault flag current (I_{FF}) = 2 mA
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	11.2			µs typ	Load resistance (R_L) = 300 Ω, load capacitance (C_L) = 35 pF, V_S = 10 V, see Figure 45
	14.1	14.1	14.1	µs max	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
Off Time, t_{OFF}	140			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see Figure 45
	170	170	170	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
Break-Before-Make Time Delay, t_D	10			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
	7.7	7.6	7.6	µs min	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
Overvoltage Response Time, $t_{RESPONSE}$					
Positive	160			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 40
	180	190	190	ns max	R_L = 1 kΩ, C_L = 5 pF
Negative	420			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 41
	510	540	570	ns max	R_L = 1 kΩ, C_L = 5 pF
Overvoltage Recovery Time, $t_{RECOVERY}$	9.8			µs typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 42
	12.8	12.8	12.8	µs max	R_L = 1 kΩ, C_L = 5 pF
Interrupt Flag Response Time, $t_{DIGRESP}$	110			ns typ	Pull-up resistor (R_{PULLUP}) = 1 kΩ, C_L = 12 pF, pull-up voltage (V_{PULL_UP}) = 5 V, see Figure 43
	130	140	140	ns max	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
Interrupt Flag Recovery Time, t_{DIGREC}	1.8			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V, see Figure 44
	2.4	2.6	2.6	µs max	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
Charge Injection, Q_{INJ}	−135			pC typ	V_S = 0 V, source resistor (R_S) = 0 Ω, C_L = 1 nF, see Figure 46
Off Isolation	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency (f) = 1 MHz, see Figure 36
Channel to Channel Crosstalk	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 10 V p-p, f = 20 Hz to 20 kHz, see Figure 39

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
−3 dB Bandwidth	630			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 38
Insertion Loss	−0.95			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
Source Off Capacitance, C_S (Off)	7			pF typ	V_S = 0 V, f = 1 MHz
Drain Off Capacitance, C_D (Off)	5			pF typ	V_S = 0 V, f = 1 MHz
Drain On Capacitance and Source On Capacitance, C_D (On) and C_S (On)	11			pF typ	V_S = 0 V, f = 1 MHz
Drain On Capacitance and Source On Capacitance Flatness, C_{DFLAT} (On) and C_{SFLAT} (On)	2.5			pF typ	V_S = V_{SS} to V_{DD} − 2 V, f = 1 MHz
Capacitance Matching, C_{MATCH} (On)	0.3			pF typ	V_S = V_{SS} to V_{DD} − 2 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, digital inputs = 0 V or +5 V
Normal Mode					
Positive Supply Current, I_{DD}	130			µA typ	
	205		205	µA max	
GND Current, I_{GND}	55			µA typ	
	90		90	µA max	
Negative Supply Current, I_{SS}	75			µA typ	
	115		115	µA max	
Fault Mode					V_S = ±60 V
I_{DD}	185			µA typ	
	270		270	µA max	
I_{GND}	155			µA typ	
	210		210	µA max	
I_{SS}	55			µA typ	
	90		90	µA max	

±20 V DUAL SUPPLY

V_{DD} = 20 V ± 10%, V_{SS} = −20 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +18 V, V_{SS} = −18 V
Analog Signal Range	V_{SS} to V_{DD} − 2			V	
R_{ON}	11.5			Ω typ	V_S = V_{SS} to 15 V, I_S = 10 mA, see Figure 31
	14	17.5	20.5	Ω max	V_S = V_{SS} to 15 V, I_S = 10 mA
	11			Ω typ	V_S = V_{SS} to 13.5 V, I_S = 10 mA
	13.5	17	20	Ω max	V_S = V_{SS} to 13.5 V, I_S = 10 mA
$R_{FLAT (ON)}$	0.6			Ω typ	V_S = V_{SS} to 15 V, I_S = 10 mA
	0.7	0.8	0.9	Ω max	V_S = V_{SS} to 15 V, I_S = 10 mA
	0.02			Ω typ	V_S = V_{SS} to 13.5 V, I_S = 10 mA
	0.06	0.1	0.1	Ω max	V_S = V_{SS} to 13.5 V, I_S = 10 mA
$R_{MATCH (ON)}$	0.02			Ω typ	V_S = V_{SS} to 15 V, I_S = 10 mA
	0.2	0.35	0.45	Ω max	V_S = V_{SS} to 15 V, I_S = 10 mA

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_S (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 32
	±0.2	±2.5	±22	nA max	V_S = ±15 V, V_D = ∓15 V
			±8	nA max	V_S = ±15 V, V_D = ∓15 V, −40°C to +105°C
I_D (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 32
	±0.2	±2.5	±22	nA max	V_S = ±15 V, V_D = ∓15 V
			±8	nA max	V_S = ±15 V, V_D = ∓15 V, −40°C to +105°C
I_D (On), I_S (On)	±0.05			nA typ	V_S = ±15 V, V_D = ±15 V, see Figure 33
	±0.3	±3.5	±30	nA max	V_S = ±15 V, V_D = ±15 V
			±14	nA max	V_S = ±15 V, V_D = ±15 V, −40°C to +105°C
FAULT					
V_T	0.7			V typ	See Figure 25
I_S					
With Overvoltage			±30	µA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±60 V, see Figure 34
Power Supplies Grounded or Floating			±5.5	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, IN = 0 V or floating, V_S = ±60 V, see Figure 35
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±60 V, see Figure 34
	±0.2	±2	±20	nA max	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V, see Figure 35
	±0.2	±2	±20	nA max	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V
Power Supplies Floating			±0.1	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, IN = 0 V, see Figure 35
DIGITAL INPUTS AND OUTPUTS					
V_{INH}			1.3	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = 0 V or 5 V
			1	µA max	V_{IN} = 0 V or 5 V
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA
DYNAMIC CHARACTERISTICS					
t_{ON}	12.6			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see Figure 45
	15.9	15.9	15.9	µs max	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
t_{OFF}	140			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V, see Figure 45
	160	160	160	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
t_D	11.5			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
	8.9	8.8	8.8	µs min	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
$t_{RESPONSE}$					
Positive	160			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 40
	190	190	190	ns max	R_L = 1 kΩ, C_L = 5 pF
Negative	360			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 41
	440	460	490	ns max	R_L = 1 kΩ, C_L = 5 pF
$t_{RECOVERY}$	11.7			µs typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 42
	14.8	14.8	14.9	µs max	R_L = 1 kΩ, C_L = 5 pF
$t_{DIGRESP}$	120			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V, see Figure 43
	140	140	140	ns max	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
t_{DIGREC}	2.2			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V, see Figure 44
	2.8	3	3	µs max	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
Q_{INJ}	−150			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 46
Off Isolation	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Channel to Channel Crosstalk	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 10 V p-p, f = 20 Hz to 20 kHz, see Figure 39
−3 dB Bandwidth	630			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 38
Insertion Loss	−0.95			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
C_S (Off)	6			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	5			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	11			pF typ	V_S = 0 V, f = 1 MHz
C_{DFLAT} (On), C_{SFLAT} (On)	2.5			pF typ	V_S = V_{SS} to V_{DD} − 2 V, f = 1 MHz
C_{MATCH} (On)	0.3			pF typ	V_S = V_{SS} to V_{DD} − 2 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, digital inputs = 0 V or +5 V
Normal Mode					
I_{DD}	130			µA typ	
	205		205	µA max	
I_{GND}	55			µA typ	
	90		90	µA max	
I_{SS}	75			µA typ	
	115		115	µA max	
Fault Mode					V_S = ±60 V
I_{DD}	185			µA typ	
	270		270	µA max	
I_{GND}	155			µA typ	
	210		210	µA max	
I_{SS}	55			µA typ	
	90		90	µA max	

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V, V_{SS} = 0 V
Analog Signal Range	V_{SS} to V_{DD} − 2			V	
R_{ON}	11.5			Ω typ	V_S = 0 V to 7.5 V, I_S = 10 mA, see Figure 31
	14.5	18	21.5	Ω max	V_S = 0 V to 7.5 V, I_S = 10 mA
	11			Ω typ	V_S = 0 V to 6 V, I_S = 10 mA
	13.5	17	20	Ω max	V_S = 0 V to 6 V, I_S = 10 mA
$R_{FLAT (ON)}$	0.7			Ω typ	V_S = 0 V to 7.5 V, I_S = 10 mA
	1.25	1.3	1.35	Ω max	V_S = 0 V to 7.5 V, I_S = 10 mA
	0.01			Ω typ	V_S = 0 V to 6 V, I_S = 10 mA
	0.04	0.06	0.06	Ω max	V_S = 0 V to 6 V, I_S = 10 mA
$R_{MATCH (ON)}$	0.02			Ω typ	V_S = 0 V to 7.5 V, I_S = 10 mA
	0.2	0.35	0.45	Ω max	V_S = 0 V to 7.5 V, I_S = 10 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
I_S (Off)	±0.05			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V, see Figure 32
	±0.2	±2.5	±22	nA max	V_S = 1 V to 10 V, V_D = 10 V to 1 V
			±8	nA max	V_S = 1 V to 10 V, V_D = 10 V to 1 V, −40°C to +105°C
I_D (Off)	±0.05			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V, see Figure 32
	±0.2	±2.5	±22	nA max	V_S = 1 V to 10 V, V_D = 10 V to 1 V
			±8	nA max	V_S = 1 V to 10 V, V_D = 10 V to 1 V, −40°C to +105°C
I_D (On), I_S (On)	±0.05			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V, see Figure 33
	±0.3	±3.5	±30	nA max	V_S = 1 V to 10 V, V_D = 10 V to 1 V
			±14	nA max	V_S = 1 V to 10 V, V_D = 10 V to 1 V, −40°C to +105°C
FAULT					
V_T	0.7			V typ	See Figure 25
I_S					
With Overvoltage			±30	µA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, see Figure 34
Power Supplies Grounded or Floating			±5.5	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, IN = 0 V or floating, V_S = ±60 V, see Figure 35
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = +13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, see Figure 34
	±0.2	±2	±20	nA max	V_{DD} = +13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V, see Figure 35
	±0.2	±2	±20	nA max	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V
Power Supplies Floating			±0.1	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, IN = 0 V, see Figure 35

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS AND OUTPUTS					
V_{INH}			1.3	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = 0 V or 5 V
			1	µA max	V_{IN} = 0 V or 5 V
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA
DYNAMIC CHARACTERISTICS					
t_{ON}	5.3			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see Figure 45
	6.3	6.3	6.3	µs max	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V
t_{OFF}	200			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V, see Figure 45
	240	240	240	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V
t_D	4.5			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V
	3.5	3.4	3.4	µs min	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V
$t_{RESPONSE}$					
Positive	210			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 40
	250	250	250	ns max	R_L = 1 kΩ, C_L = 5 pF
Negative	600			ns typ	R_{PULLUP} = 1 kΩ, C_L = 5 pF, see Figure 41
	700	700	700	ns max	R_{PULLUP} = 1 kΩ, C_L = 5 pF
$t_{RECOVERY}$	5.3			µs typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 42
	6.2	6.5	6.6	µs max	R_L = 1 kΩ, C_L = 5 pF
$t_{DIGRESP}$	110			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V, see Figure 43
	130	130	130	ns max	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
t_{DIGREC}	1.6			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V, see Figure 44
	2.1	2.4	2.4	µs max	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
Q_{INJ}	−75			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 46
Off Isolation	−69			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Channel to Channel Crosstalk	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
THD + N	0.0018			% typ	R_L = 10 kΩ, V_S = 6 V p-p, f = 20 Hz to 20 kHz, see Figure 39
−3 dB Bandwidth	570			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 38
Insertion Loss	−0.95			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
C_S (Off)	8			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	7			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	11			pF typ	V_S = 6 V, f = 1 MHz
C_{DFLAT} (On), C_{SFLAT} (On)	2			pF typ	V_S = V_{SS} to V_{DD} − 2 V, f = 1 MHz
C_{MATCH} (On)	0.4			pF typ	V_S = V_{SS} to V_{DD} − 2 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, digital inputs = 0 V or 5 V
Normal Mode					
I_{DD}	125			µA typ	
	200		200	µA max	
I_{GND}	45			µA typ	
	80		80	µA max	
I_{SS}	80			µA typ	
	120		120	µA max	
Fault Mode					V_S = ±60 V
I_{DD}	185			µA typ	
	270		270	µA max	
I_{GND}	155			µA typ	
	210		210	µA max	
I_{SS}	55			µA typ	
	90		90	µA max	

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 5.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 32.4 V, V_{SS} = 0 V
Analog Signal Range	V_{SS} to V_{DD} − 2			V	
R_{ON}	12			Ω typ	V_S = 0 V to 29.5 V, I_S = 10 mA, see Figure 31
	14.5	18	21.5	Ω max	V_S = 0 V to 29.5 V, I_S = 10 mA
	11			Ω typ	V_S = 0 V to 27 V, I_S = 10 mA
	13.5	17	20	Ω max	V_S = 0 V to 27 V, I_S = 10 mA
$R_{FLAT (ON)}$	1.1			Ω typ	V_S = 0 V to 29.5 V, I_S = 10 mA
	1.25	1.3	1.35	Ω max	V_S = 0 V to 29.5 V, I_S = 10 mA
	0.01			Ω typ	V_S = 0 V to 27 V, I_S = 10 mA
	0.04	0.06	0.06	Ω max	V_S = 0 V to 27 V, I_S = 10 mA
$R_{MATCH (ON)}$	0.02			Ω typ	V_S = 0 V to 29.5 V, I_S = 10 mA
	0.2	0.35	0.45	Ω max	V_S = 0 V to 29.5 V, I_S = 10 mA
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
I_S (Off)	±0.05			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V, see Figure 32
	±0.2	±2.5	±22	nA max	V_S = 1 V to 30 V, V_D = 30 V to 1 V
			±8	nA max	V_S = 1 V to 30 V, V_D = 30 V to 1 V, −40°C to +105°C
I_D (Off)	±0.05			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V, see Figure 32
	±0.2	±2.5	±22	nA max	V_S = 1 V to 30 V, V_D = 30 V to 1 V
			±8	nA max	V_S = 1 V to 30 V, V_D = 30 V to 1 V, −40°C to +105°C
I_D (On), I_S (On)	±0.05			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V, see Figure 33
	±0.3	±3.5	±30	nA max	V_S = 1 V to 30 V, V_D = 30 V to 1 V
			±14	nA max	V_S = 1 V to 30 V, V_D = 30 V to 1 V, −40°C to +105°C
FAULT					
V_T	0.7			V typ	See Figure 25
I_S					
With Overvoltage			±30	µA typ	V_{DD} = +39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +60 V, and V_S = −40 V, see Figure 34
Power Supplies Grounded or Floating			±5.5	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, IN = 0 V or floating, V_S = ±60 V, see Figure 35
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = +39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +60 V and V_S = −40 V, see Figure 34
	±0.2	±2	±20	nA max	V_{DD} = +39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +60 V and V_S = −40 V
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V, see Figure 35
	±0.2	±2	±20	nA max	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, IN = 0 V
Power Supplies Floating			±0.1	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, IN = 0 V, see Figure 35

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS AND OUTPUTS					
V_{INH}			1.3	V min	
V_{INL}			0.8	V max	
I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = 0 V or 5 V
			1	µA max	V_{IN} = 0 V or 5 V
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA
DYNAMIC CHARACTERISTICS					
t_{ON}	7.2			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V, see Figure 45
	8.7	8.7	8.7	µs max	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V
t_{OFF}	200			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V, see Figure 45
	240	250	250	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V
t_D	6			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V
	4.7	4.6	4.6	µs min	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V
$t_{RESPONSE}$					
Positive	240			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 40
	290	290	290	ns max	R_L = 1 kΩ, C_L = 5 pF
Negative	600			ns typ	R_{PULLUP} = 1 kΩ, C_L = 5 pF, see Figure 41
	700	700	700	ns max	R_{PULLUP} = 1 kΩ, C_L = 5 pF
$t_{RECOVERY}$	6.6			µs typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 42
	10.7	10.8	11.3	µs max	R_L = 1 kΩ, C_L = 5 pF
$t_{DIGRESP}$	120			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V, see Figure 43
	150	150	150	ns max	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
t_{DIGREC}	4.1			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V, see Figure 44
	7.8	8	8.5	µs max	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
Q_{INJ}	−115			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF, see Figure 46
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 36
Channel to Channel Crosstalk	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
THD + N	0.0008			% typ	R_L = 10 kΩ, V_S = 18 V p-p, f = 20 Hz to 20 kHz, see Figure 39
−3 dB Bandwidth	630			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 38
Insertion Loss	−0.95			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
C_S (Off)	6			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	5			pF typ	V_S = 18 V, f = 1 MHz
CD (On), C_S (On)	10			pF typ	V_S = 18 V, f = 1 MHz
C_{DFLAT} (On), C_{SFLAT} (On)	3.3			pF typ	V_S = V_{SS} to V_{DD} − 2 V, f = 1 MHz
C_{MATCH} (On)	0.3			pF typ	V_S = V_{SS} to V_{DD} − 2 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, digital inputs = 0 V or 5 V
Normal Mode					
I_{DD}	125			µA typ	
	200		200	µA max	
I_{GND}	45			µA typ	
	80		80	µA max	
I_{SS}	80			µA typ	
	120		120	µA max	
Fault Mode					V_S = +60 V and V_S = −40 V
I_{DD}	185			µA typ	
	270		270	µA max	
I_{GND}	155			µA typ	
	210		210	µA max	
I_{SS}	55			µA typ	
	90		90	µA max	

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 6.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, S OR D					
θ_{JA} = 170°C/W	88	61	41	mA max	$V_S = V_{SS}$ to V_{DD} − 5 V
	81	57	39	mA max	$V_S = V_{SS}$ to V_{DD} − 2 V

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Value
V_{DD} to V_{SS}	60 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	−28 V to +0.3 V
Sx Pins	−60 V to +60 V
Sx to V_{DD}	80 V
Sx to V_{SS}	80 V
V_S to V_D	80 V
Dx Pins[1]	V_{SS} − 0.7 V to V_{DD} + 0.7 V or 30 mA, whichever occurs first
Digital Inputs	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	278 mA (pulsed at 1 ms, 10% duty cycle maximum)
Digital Output	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-Free	As per JEDEC J-STD-020

[1] Overvoltages at the Dx pins are clamped by the internal diodes. Limit current to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-10-16	170	58.2	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADG5421F

Table 9. ADG5421F, 10-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM[1]	3.5	2

[1] This is the HBM for the input and output port to supplies, the input and output port to the input and output port, and for all other pins.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

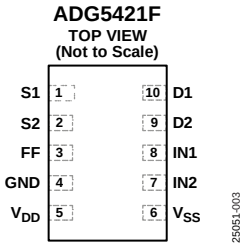

Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1	Overvoltage Protected Source Terminal. S1 can be an input or an output.
2	S2	Overvoltage Protected Source Terminal. S2 can be an input or an output.
3	FF	Fault Flag Digital Output. The FF pin is an open-drain output that requires an external pull-up resistor. This digital output pulls low when a fault condition occurs on either of the Sx inputs.
4	GND	Ground (0 V) Reference.
5	V_{DD}	Most Positive Power Supply Potential.
6	V_{SS}	Most Negative Power Supply Potential.
7	IN2	Logic Control Input.
8	IN1	Logic Control Input.
9	D2	Drain Terminal. D1 can be an input or an output.
10	D1	Drain Terminal. D2 can be an input or an output.

TYPICAL PERFORMANCE CHARACTERISTICS

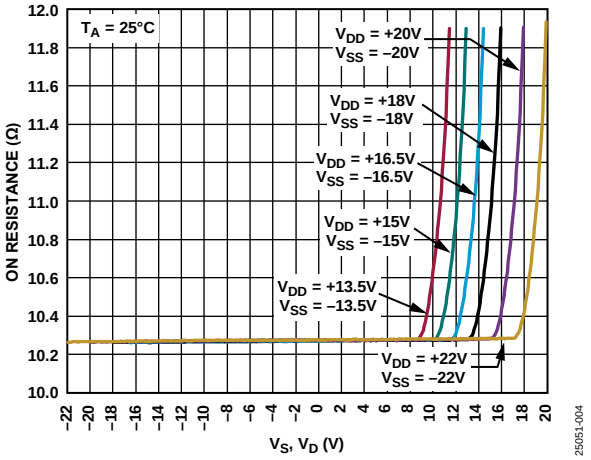

Figure 3. On Resistance as a Function of V_S, V_D (Dual Supply)

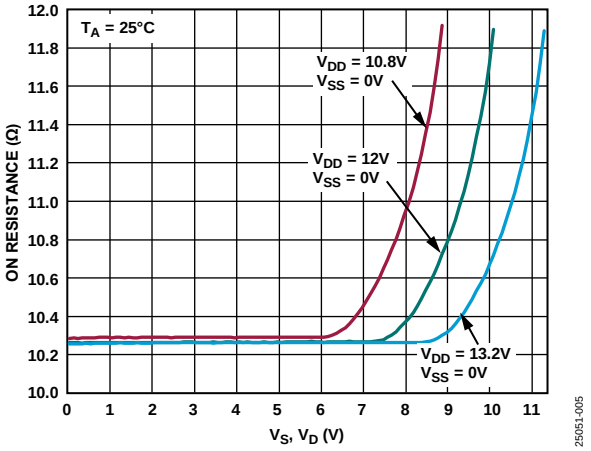

Figure 4. On Resistance as a Function of V_S, V_D (12 V Single Supply)

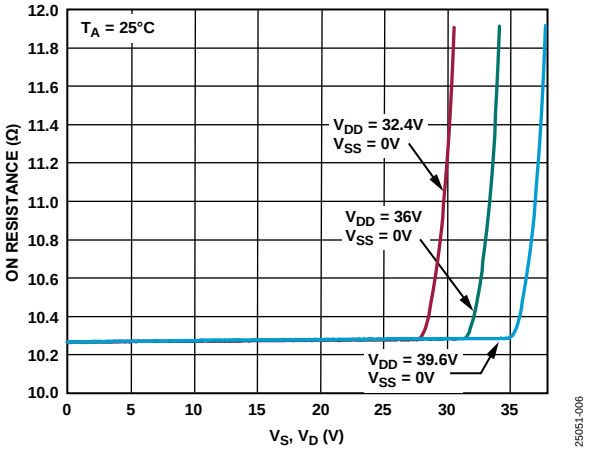

Figure 5. On Resistance as a Function of V_S, V_D (36 V Single Supply)

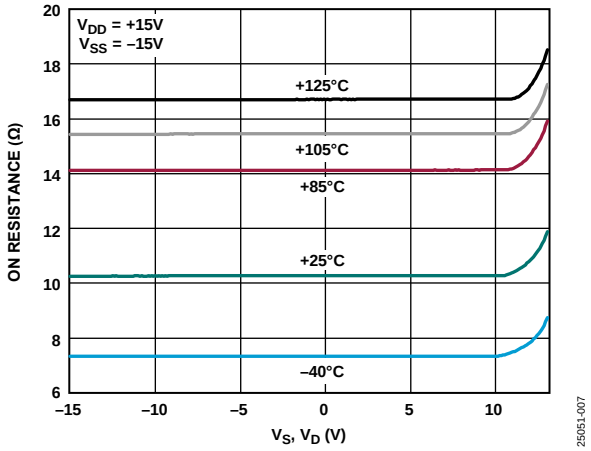

Figure 6. On Resistance as a Function of V_S, V_D for Different Temperatures, ±15 V Dual Supply

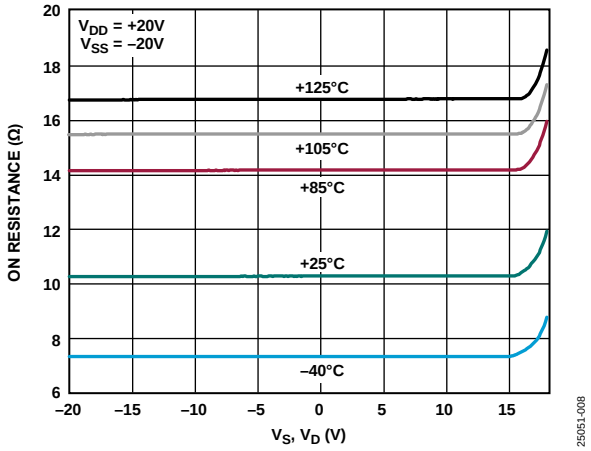

Figure 7. On Resistance as a Function of V_S, V_D for Different Temperatures, ±20 V Dual Supply

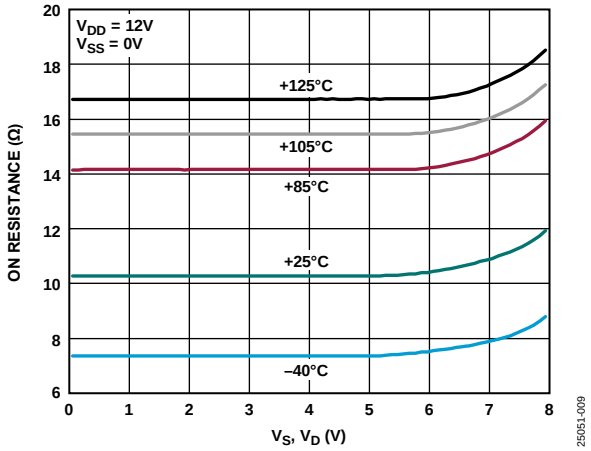

Figure 8. On Resistance as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

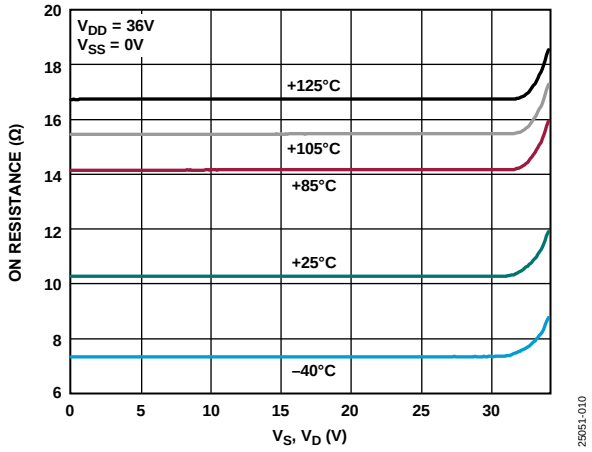

Figure 9. On Resistance as a Function of V_S, V_D for Different Temperatures, 36 V Single Supply

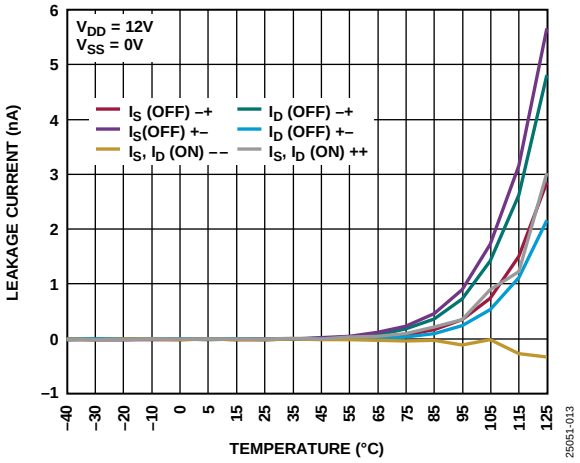

Figure 12. Leakage Current vs. Temperature, 12 V Single Supply

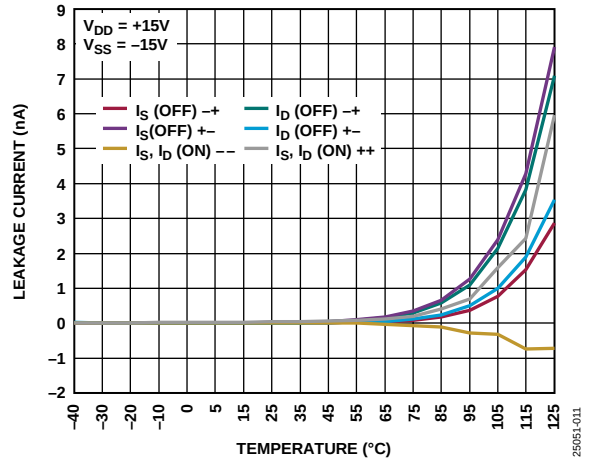

Figure 10. Leakage Current vs. Temperature, ±15 V Dual Supply

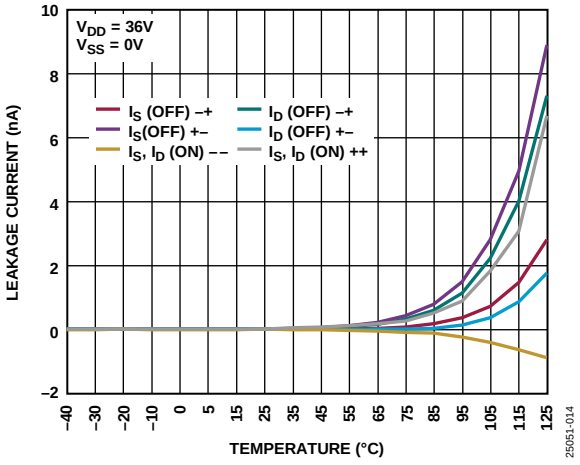

Figure 13. Leakage Current vs. Temperature, 36 V Single Supply

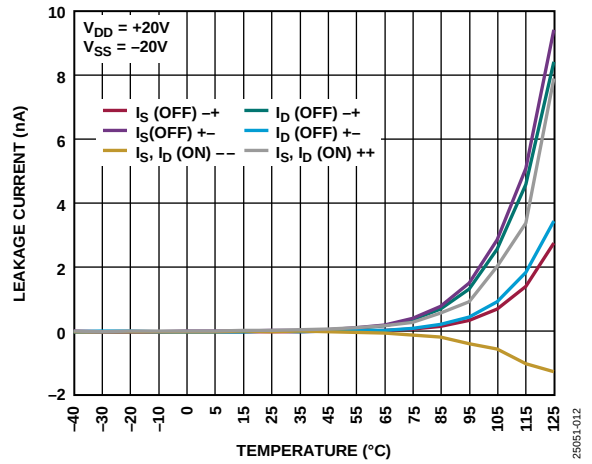

Figure 11. Leakage Current vs. Temperature, ±20 V Dual Supply

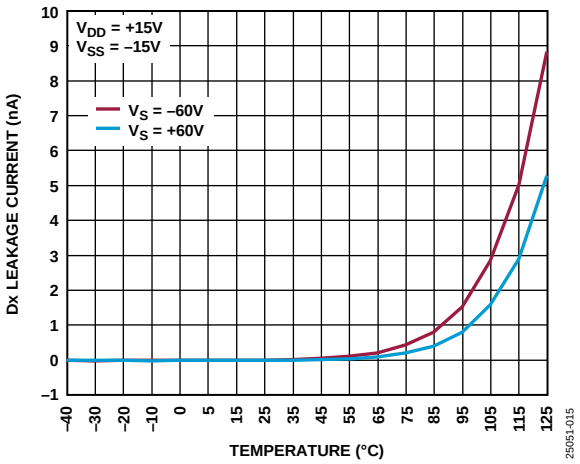

Figure 14. Dx Leakage Current vs. Temperature During Overvoltage, ±15 V Dual Supply

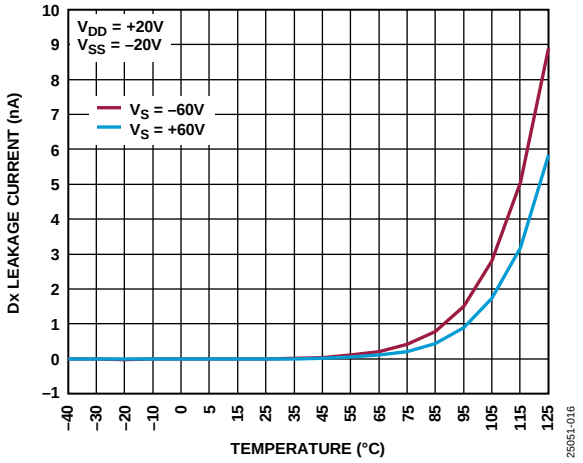

Figure 15. Dx Leakage Current vs. Temperature During Overvoltage, ±20 V Dual Supply

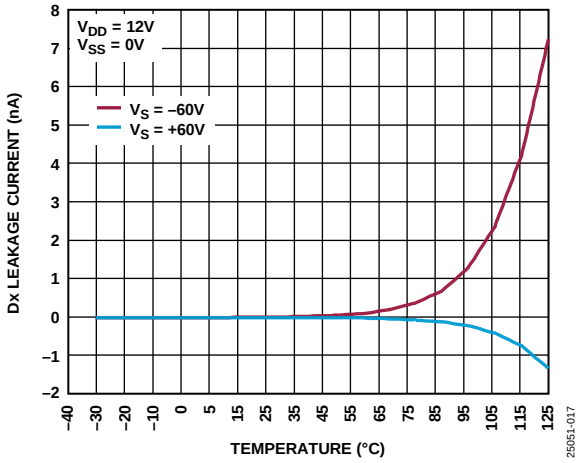

Figure 16. Dx Leakage Current vs. Temperature During Overvoltage, 12 V Single Supply

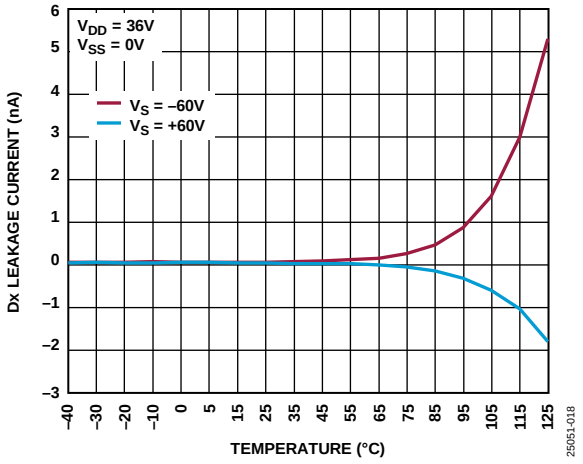

Figure 17. Dx Leakage Current vs. Temperature During Overvoltage, 36 V Single Supply

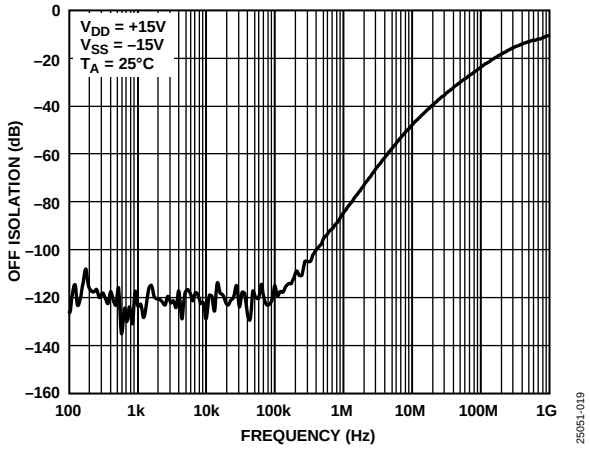

Figure 18. Off Isolation vs. Frequency, ±15 V Dual Supply

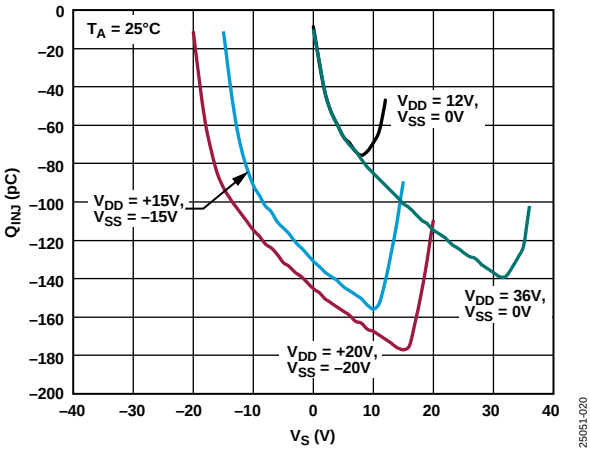

Figure 19. Q_{INJ} vs. V_S

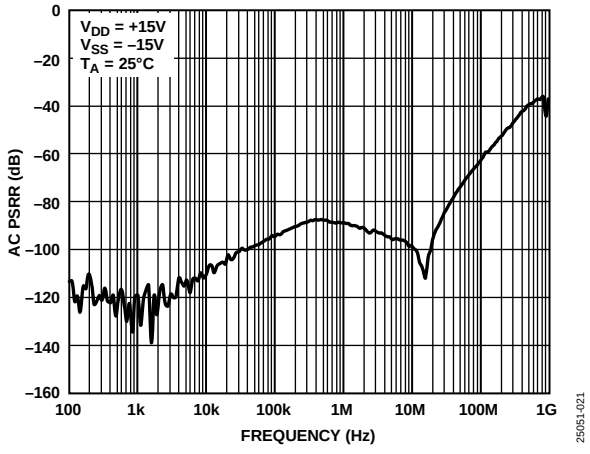

Figure 20. AC Power Supply Rejection Ratio (PSRR) vs. Frequency, ±15 V Dual Supply

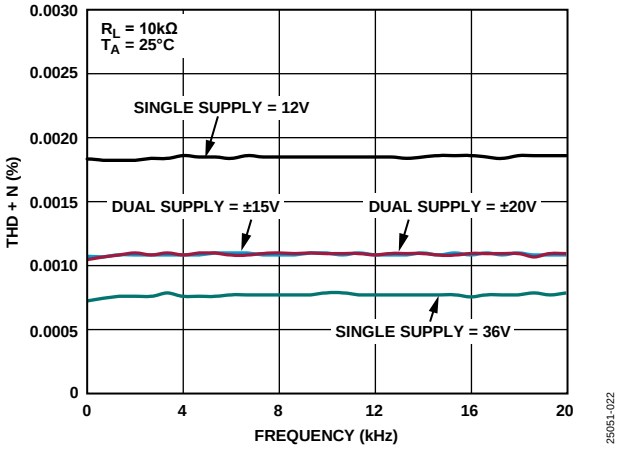

Figure 21. THD + N vs. Frequency

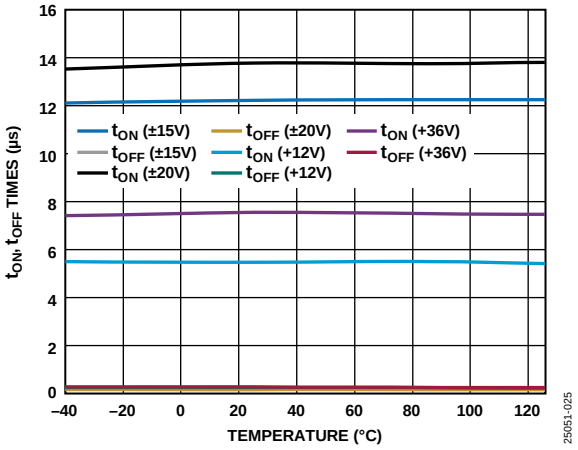

Figure 24. t_{ON}, t_{OFF} Times vs. Temperature for Various Supplies

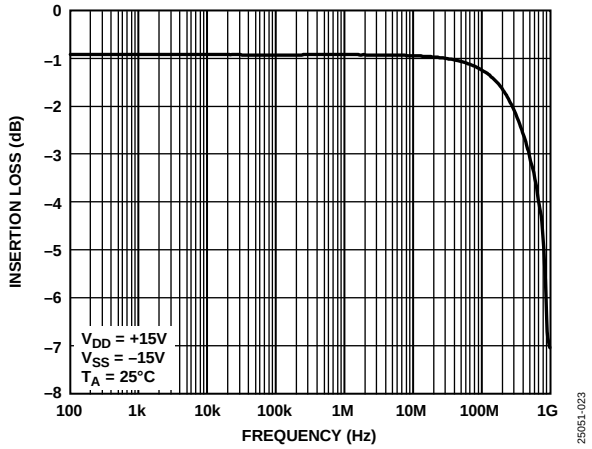

Figure 22. Insertion Loss vs. Frequency, ±15 V Dual Supply

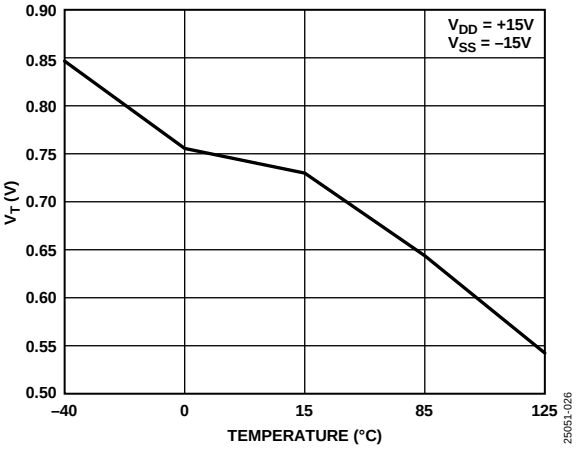

Figure 25. V_T vs. Temperature, ±15 V Dual Supply

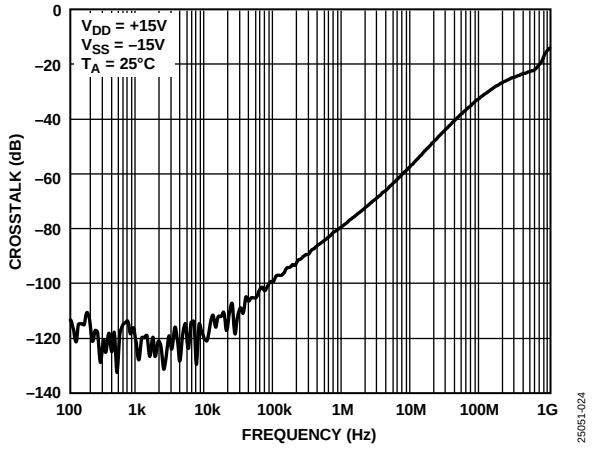

Figure 23. Crosstalk vs. Frequency, ±15 V Dual Supply

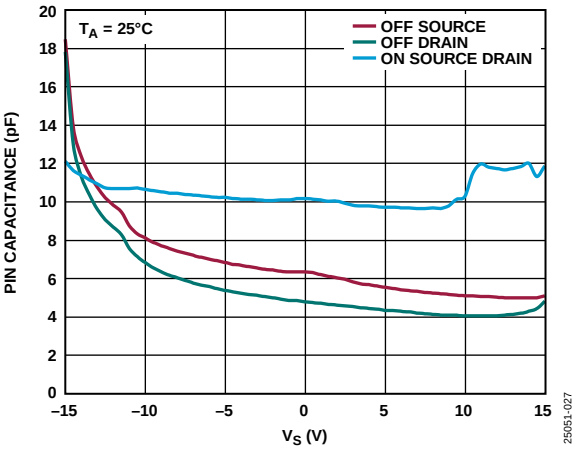

Figure 26. Pin Capacitance vs. V_S

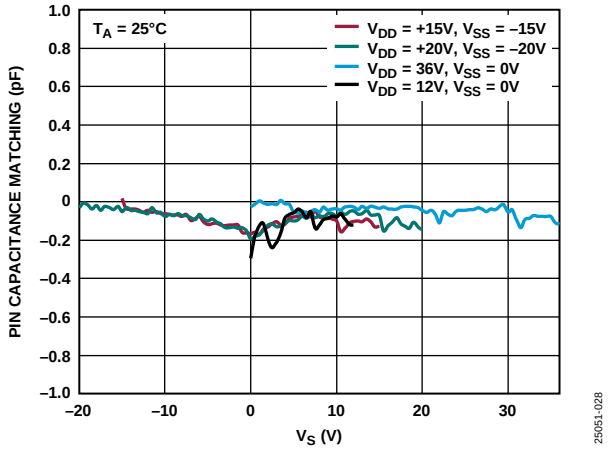

Figure 27. Pin Capacitance Matching vs. V_S

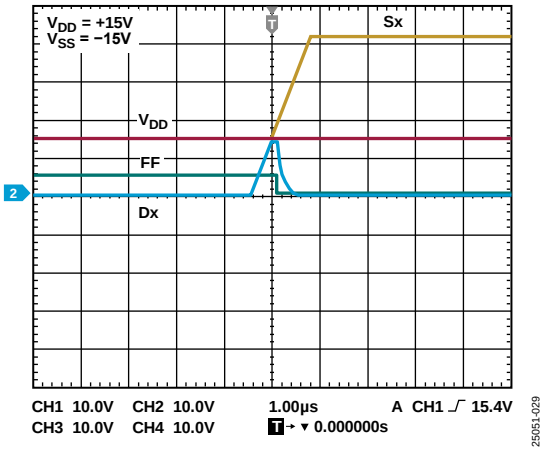

Figure 28. Drain Output Response to Positive Overvoltage

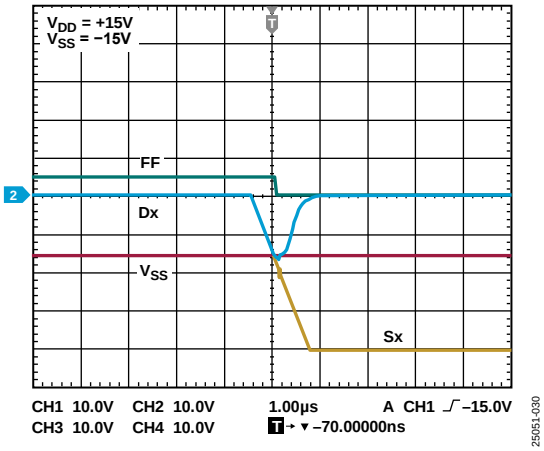

Figure 29. Drain Output Response to Negative Overvoltage

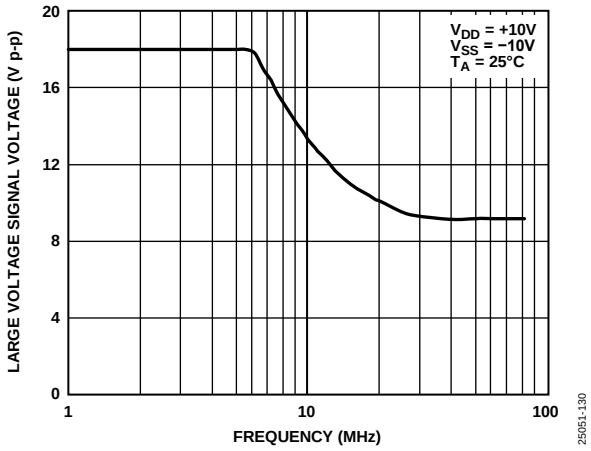

Figure 30. Large Voltage Signal Voltage vs. Frequency

TEST CIRCUITS

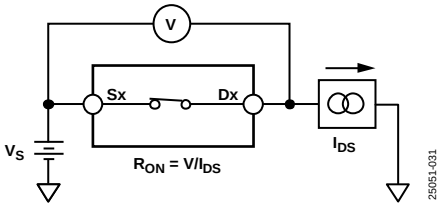

Figure 31. On Resistance (I_{DS} Is the Drain to Source Current.)

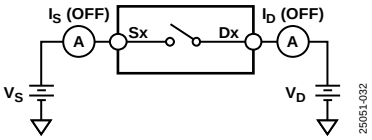

Figure 32. Off Leakage

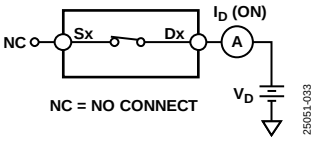

Figure 33. On Leakage

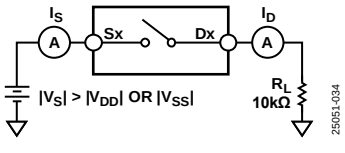

Figure 34. Switch Overvoltage Leakage

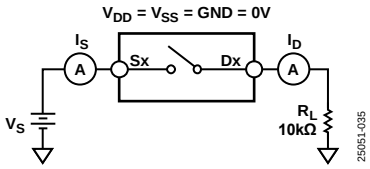

Figure 35. Switch Unpowered Leakage

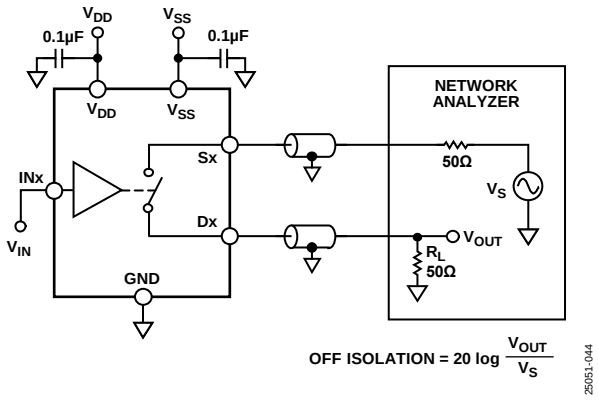

Figure 36. Off Isolation (V_{OUT} Is the Output Voltage)

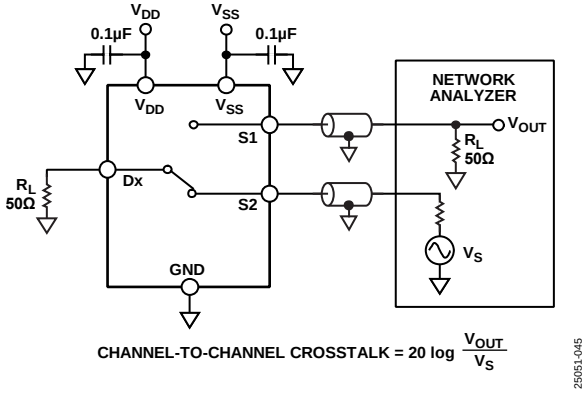

Figure 37. Channel to Channel Crosstalk

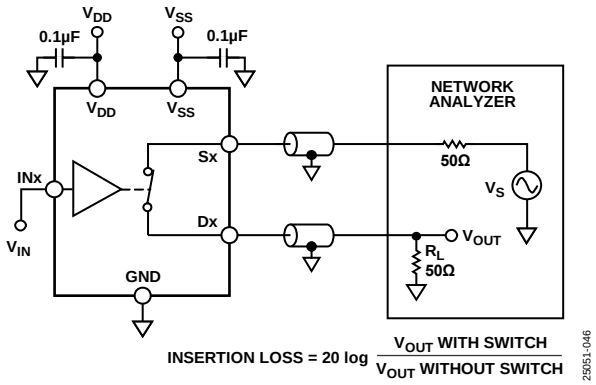

Figure 38. Bandwidth

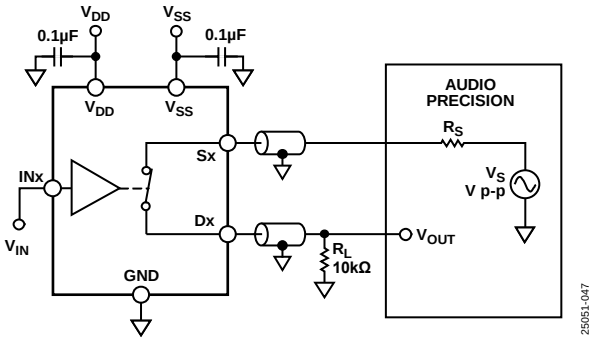

Figure 39. THD + N

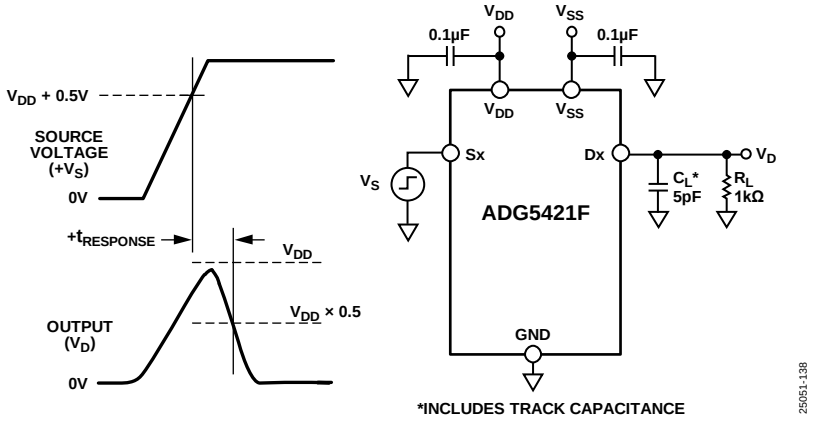

Figure 40. Positive Overvoltage Response Time, $t_{RESPONSE}$

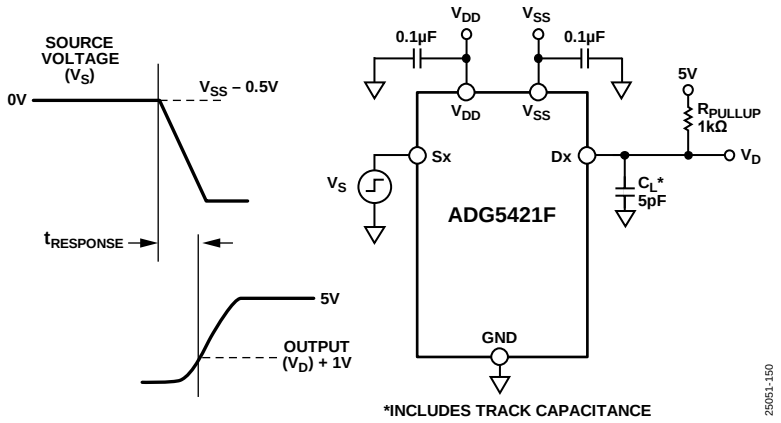

Figure 41. Negative Overvoltage Response Time, Single-Supply, $t_{RESPONSE}$

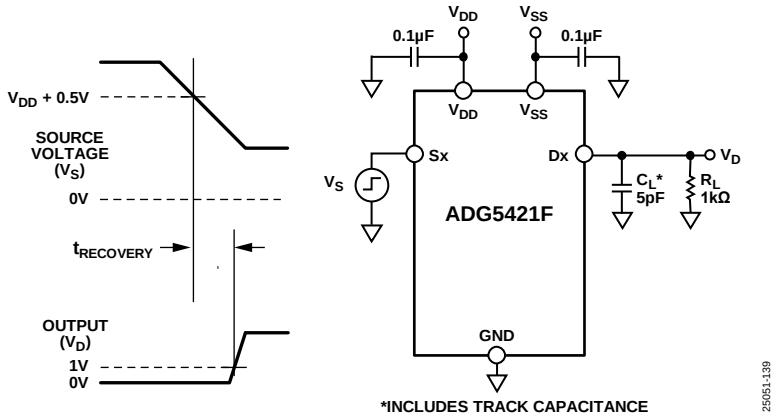

Figure 42. Overvoltage Recovery Time, $t_{RECOVERY}$

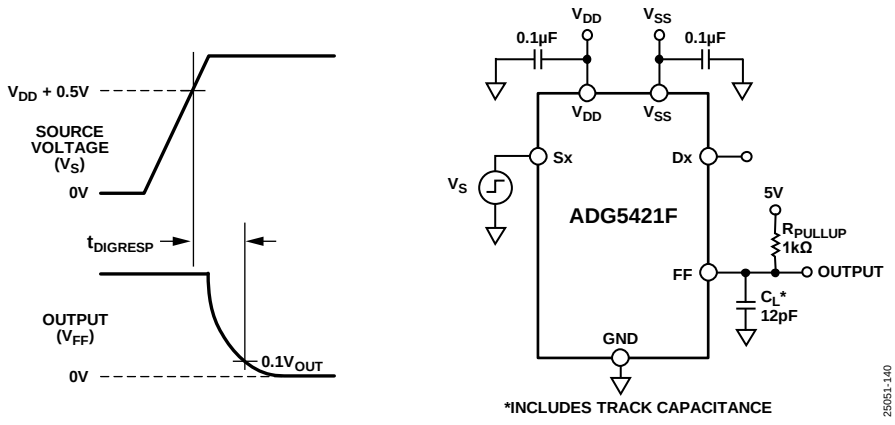

Figure 43. Interrupt Flag Response Time, $t_{DIGRESP}$ (V_{FF} Is the Fault Flag Voltage)

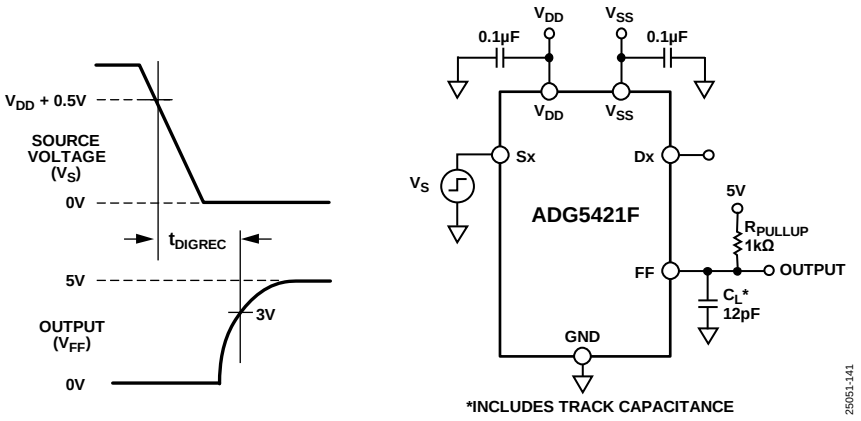

Figure 44. Interrupt Flag Recovery Time, t_{DIGREC}

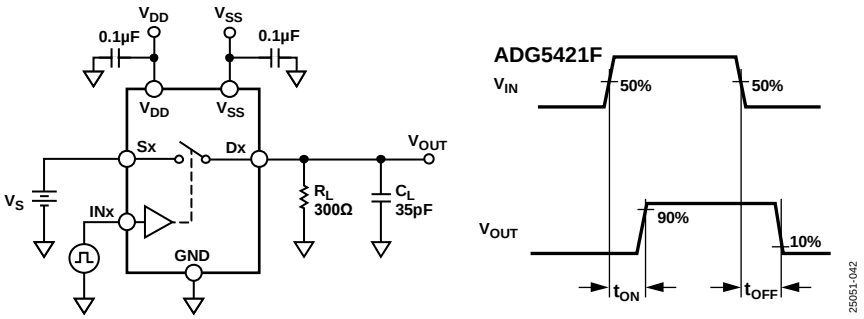

Figure 45. Switching Times, t_{ON} and t_{OFF}

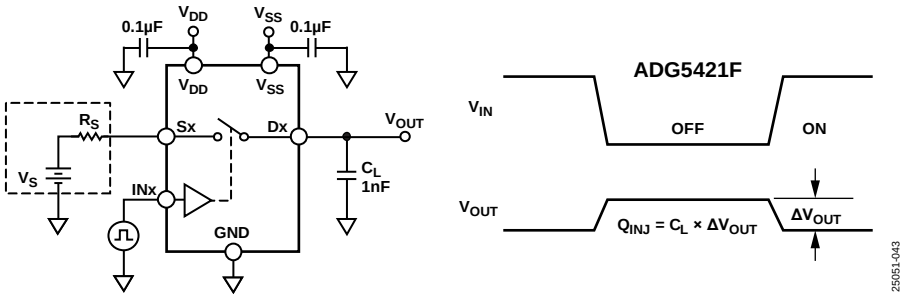

Figure 46. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on the Dx pins and the Sx pins, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between the Dx pins and the Sx pins.

$R_{FLAT (ON)}$
$R_{FLAT (ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch Dx pin capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch Sx pin capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} represents the delay between applying the digital control input and the output switching on.

t_{OFF}
t_{OFF} represents the delay between applying the digital control input and the output switching off.

$t_{DIGRESP}$
$t_{DIGRESP}$ is the time required for the FF pin to go low (0.3 V), measured with respect to voltage on the Sx pin exceeding the source voltage by 0.5 V.

t_{DIGREC}
t_{DIGREC} is the time required for the FF pin to return high, measured with respect to voltage on the Sx pin falling below the source voltage plus 0.5 V.

$t_{RESPONSE}$
$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 90% of the supply voltage.

$t_{RECOVERY}$
$t_{RECOVERY}$ represents the delay between an overvoltage on the Sx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 10% of the supply voltage.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

−3 dB Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

THD + N
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)
AC PSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. AC PSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pins to the output of the switch (see Figure 20). The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

V_T
V_T is the voltage threshold at which the overvoltage protection circuitry engages.

THEORY OF OPERATION

SWITCH ARCHITECTURE

The ADG5421F consists of two switch channels of N channel diffused metal-oxide semiconductor (NDMOS) transistors. This construction provides excellent performance in a small area. The ADG5421F operates as a standard switch when input signals with a voltage between V_{SS} and V_{DD} − 2 V are applied. For example, the on resistance is 11 Ω typically, and the INx pins controls when the switches open or close.

Additional internal circuitry enables the switches to detect overvoltage inputs by comparing the voltage on both the S1 and S2 pins with the V_{DD} and V_{SS} pins. A signal is considered overvoltage when the signal exceeds the supply voltages by V_T. V_T is typically 0.7 V but can range from 0.76 V at −40°C down to 0.5 V at +125°C. See Figure 25 to see the change in V_T with the operating temperature.

When an overvoltage condition is detected on either the S1 or S2 pins, both switches automatically open regardless of the digital logic state (INx). The S1 to D1 and S2 to D2 become high impedance and ensure that no current flows through the switches. In Figure 28, the voltage on the Dx pin follows the voltage on the Sx pins until the main channel switch turns off completely, and the drain voltage discharges through the load. The maximum voltage on the drain is limited by the internal ESD diodes and the rate at which the output voltage discharges is dependent on the load at the Dx pins.

The maximum voltage that can be applied to any source input is +60 V or −60 V. When the ADG5421F is powered using a single supply of 25 V or greater, the maximum negative signal level reduces to remain within the 80 V maximum rating. For example, at V_{DD} = +40 V, the maximum negative signal drops from −60 V to −40 V. Construction of the process allows the channel to withstand 80 V across either switch when the switches are open. Note that these overvoltage limits apply whether the power supplies are present or not.

During overvoltage conditions, the leakage current into and out of the Sx pins is limited to tens of microamperes and nanoamperes only for the Dx pins. This limit protects the switches and connected circuitry from overstresses and restricts the current drawn from the signal source.

ESD Performance

The ADG5421F has an ESD rating of 3.5 kV for the HBM.

The Dx pins have ESD protection diodes to the rails, and the voltage at these pins must not exceed the supply voltage. The Sx pins have specialized ESD protection that allow the signal voltage to reach ±60 V regardless of the supply voltage level. See Figure 47 for the switch channel overview.

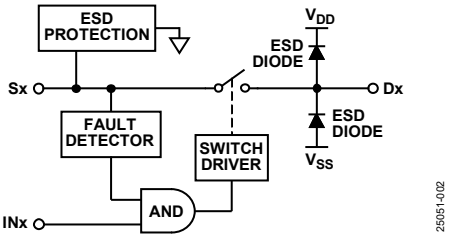

Figure 47. Switch Channel and Control Function

Trench Isolation

In the ADG5421F, an insulating oxide layer (trench) is placed between the NDMOS and the P-channel DMOS (PDMOS) transistors in the circuit. Parasitic junctions that occur between the transistors in the junction isolated switches are eliminated, and the result is a switch that is latch-up immune under all circumstances. These devices pass the JESD78D latch-up test.

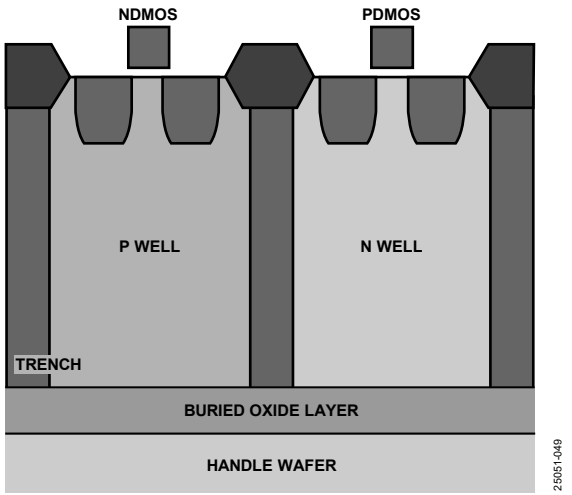

Figure 48. Trench Isolation

OVERVOLTAGE FAULT PROTECTION

When the voltage at the Sx inputs exceed V_{DD} or V_{SS} by V_T, both switches turn off, or, if the device is unpowered, the switches remain off. Both switch inputs remain high impedance regardless of the digital input state or the load resistance, and the output acts as a virtual open circuit. Signal levels up to +60 V and −60 V are blocked in both the powered and unpowered condition as long as the +80 V absolute maximum rating limitation between the Sx pins and V_{DD} or V_{SS} pins is met (see Figure 49). For example with a +40 V single-supply, the overvoltage protection is +60 V and −40 V.

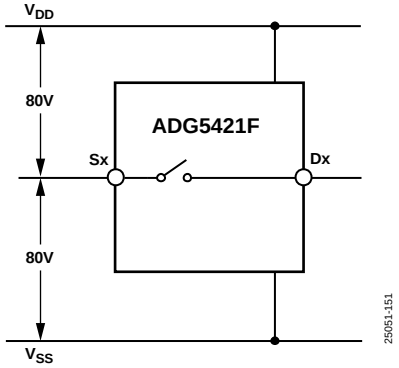

Figure 49. Sx to V_{DD} or V_{SS} Maximum Rating

Power-On Protection

To activate the switches, the three following conditions must be meet:

- The minimum supply operating conditions in Table 1.
- The input signal must be between $V_{SS} - V_T$ and $V_{DD} + V_T$.
- The digital logic control input, INx, is on.

When the switches are on, signal levels from V_{SS} up to $V_{DD} - 2$ V are passed.

The switches respond to a voltage on either of the Sx pins that exceeds V_{DD} or V_{SS} by V_T by turning off. The absolute input voltage limits are −60 V and +60 V, while maintaining an +80 V limit between the Sx pins and the supply rails. The switches remain off until the voltage at the Sx pins return to between V_{DD} and V_{SS}.

When powered by the ±15 V dual supply, the positive $t_{RESPONSE}$ is typically 160 ns, and $t_{RECOVERY}$ is 9.8 µs. These values vary with different supply voltage and output load conditions.

Exceeding ±60 V on either Sx input may damage the ESD protection circuitry on the ADG5421F.

Power-Off Protection

When no power supplies are present, the switches remain in an off state, and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switches or downstream circuitry. The switch outputs are a virtual open circuit.

The switches remain off regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to ±60 V are blocked when powered off.

Overvoltage Interrupt Flag

The voltages on the Sx inputs of the ADG5421F are continuously monitored, and the active low digital output pin, FF, indicates the fault state.

The voltage on the FF pin indicates if either of the Sx pins are experiencing a fault condition. The FF pin is an open-drain output that requires an external pull-up resistor. The output of the FF pin is high when both the Sx pins are within the normal operating range. If either of the Sx pin voltages exceeds the supply voltage (V_{DD} or V_{SS}) by V_T, the FF output provides a low impedance path to GND.

APPLICATIONS INFORMATION

The ADG5421F overvoltage protected switches provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments where overvoltage signals can be present, and the system must remain operational both during and after an overvoltage occurs.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 µF decoupling capacitors are required on both V_{DD} and V_{SS} to GND.

The ADG5421F can operate with bipolar supplies between ±5 V and ±22 V. Note that the V_{DD} and V_{SS} supplies do not have to be symmetrical, but the supply range must not exceed 44 V. The ADG5421F can also operate with single supplies between 8 V and 44 V with V_{SS} connected to GND.

The ADG5421F is fully specified at the ±15 V, ±20 V, +12 V, and +36 V supply ranges.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 50. The ADP5070 (dual switching regulator) generates a positive and negative supply rail for the ADG5421F amplifier and/or a precision converter in a typical signal chain. Also shown in Figure 50 are two optional LDOs, ADP7118 and ADP7182, positive and negative low dropout (LDOs) regulators, respectively, that can be used to reduce the output ripple of the ADP5070 in ultralow noise sensitive applications.

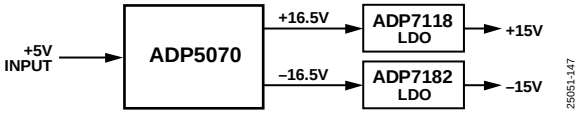

Figure 50. Bipolar Power Solution

Table 11. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, CMOS LDO linear regulator
ADP7182	−28 V, −200 mA, low noise, LDO linear regulator

POWER SUPPLY SEQUENCING PROTECTION

When the ADG5421F is off, the switch channels remain open and signals from −60 V to +60 V can be applied without damaging the device. The switch channels only close when the supplies are connected, a suitable digital control signal is placed on the INx pins, and the signal is within the normal operating range. Note that placing the ADG5421F between external connectors and sensitive components offers protection in systems where a signal is presented to the Sx pins before the supply voltages are available.

SIGNAL RANGE

The ADG5421F switches have overvoltage detection circuitry on the S1 and S2 pins that compares the voltage levels with V_{DD} and V_{SS}. To protect downstream circuitry from overvoltages, supply the ADG5421F with voltages that match the intended signal range. The NDMOS only architecture used in this switch allows signals up to V_{DD} − 2 V to be passed with little distortion. A signal that exceeds the supply rail by V_T is then blocked. This signal block offers protection to both the device and any downstream circuitry.

INTELLIGENT FAULT DETECTION

The ADG5421F digital output pin (FF) can interface with a microprocessor or control system and be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which the device connects.

The control system can use the digital interrupt to start a variety of actions, such as the following:

- Initiating investigation into the source of the overvoltage fault
- Shutting down critical systems in response to the overvoltage
- Data recorders marking data during these events as unreliable or out of specification

For systems that are sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the ADG5421F powers on and that all input voltages are within the normal operating range before initiating operation.

The FF pin is an open drain that requires an external pull-up resistor, which allows signals to be combined into a single interrupt for larger modules that contain multiple devices.

SWITCH IN A KNOWN STATE

If no digital inputs are present on the switch control lines, INx, the switches remain in an off state to prevent any unwanted signals passing through the switch.

HIGH VOLTAGE SURGE SUPPRESSION

To achieve protection from high voltage transients, such as IEC 61000-4-2 ESD, IEC 61000-4-4 electrical fast transient (EFT), and IEC 61000-4-5 surge, implement the circuit shown in Figure 51 by using discrete resistor and a transient voltage suppression (TVS) device.

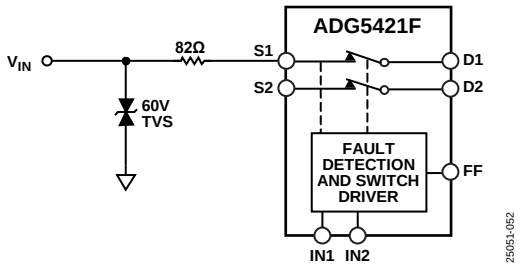

Figure 51. High Voltage Transient Protection

Table 12 details the results achieved by using the discrete protection circuit shown in Figure 51. To replicate the harshest environments, the surge test was performed by striking the Sx pins directly through a 40 Ω resistor and a 0.5 µF capacitor coupling network. The EFT test was performed by striking the Sx pins directly without any capacitive coupling through cables.

Table 12. High Voltage Transient Protection

IEC 61000-4 Transient	Protection Level (kV)
ESD (Contact)	±8
EFT	±4
Surge	±1

RELATED PRODUCTS

Table 13. Related Products to the ADG5421F

Device(s)	Configuration	Fault Limit	Fault Indicator	Package	Function
ADG5401F	SPST	Voltage rails	General flag	LFCSP	±60 V fault protection, 6 Ω R_{ON}, SPST switch with 0.6 kΩ feedback channel
ADG5412F/ADG5413F	Quad SPST	Voltage rails	General flag	TSSOP/LFCSP	±55 V fault protection and detection, 10 Ω R_{ON}, quad SPST switches
ADG5412BF/ADG5413BF	Quad SPST	Voltage rails	General flag	TSSOP/LFCSP	±55 V bidirectional fault protection and detection, 10 Ω R_{ON}, quad SPST switches
ADG5404F	4:1 mux	Voltage rails	General and specific flags	TSSOP/LFCSP	±55 V fault protection and detection, 10 Ω R_{ON}, 4-channel multiplexer
ADG5436F	Dual SPDT	Voltage rails	General and specific flags	TSSOP/LFCSP	±55 V fault protection and detection, 10 Ω R_{ON}, dual SPDT switch
ADG5462F	Quad channel protector	Secondary supplies	General flag	TSSOP/LFCSP	±55 V fault protection and detection, 10 Ω R_{ON}, quad channel protector

OUTLINE DIMENSIONS

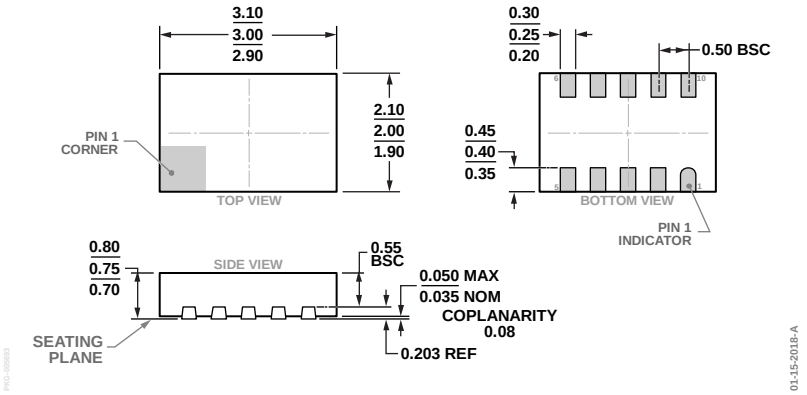

Figure 52. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 2 mm Body and 0.75 mm Package Height
(CP-10-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5421FBCPZ-RL7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP]	CP-10-16
EVAL-ADG5421FEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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