CAB006M12GM3

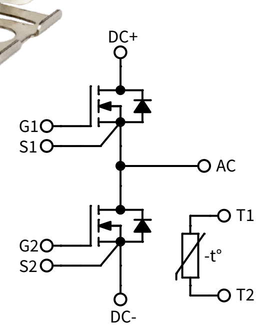
1200 V, 6 mΩ All-Silicon Carbide Half-Bridge Module

V_{DS}	1200 V
$R_{DS(on)}$	6 mΩ

Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation

Package



Applications

- EV Chargers
- Solar
- High-Efficiency Converters / Inverters
- Motor & Traction Drives
- Smart-Grid / Grid-Tied Distributed Generation

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Maximum Parameters (Verified by Design)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{DS\ max}$	Drain-Source Voltage			1200	V		
$V_{GS\ max}$	Gate-Source Voltage, Maximum Value	-8		+19	V	Transient, <100 ns	Fig. 33
$V_{GS\ op}$	Gate-Source Voltage, Recommended	-4		+15	V	Static	Fig. 33
I_D	DC Continuous Drain Current ($T_{VJ} \le 150\ ^\circ C$)			200	A	$V_{GS} = 15\ V$, $T_{HS} = 50\ ^\circ C$, $T_{VJ} \le 150\ ^\circ C$	Note 1
I_D	DC Continuous Drain Current ($T_{VJ} \le 175\ ^\circ C$)			200	A	$V_{GS} = 15\ V$, $T_{HS} = 50\ ^\circ C$, $T_{VJ} \le 175\ ^\circ C$	Note 1
$I_{SD\ BD}$	DC Source-Drain Current (Body Diode)		101		A	$V_{GS} = -4\ V$, $T_{HS} = 50\ ^\circ C$, $T_{VJ} \le 175\ ^\circ C$	
$I_{D\ (pulsed)}$	Maximum Pulsed Drain Current			400	A	t_{Pmax} limited by $T_{VJ\text{-}max}$ $V_{GS} = 15\ V$, $T_{HS} = 50\ ^\circ C$	
$T_{VJ\ op}$	Maximum Virtual Junction Temperature under Switching Conditions	-40		150	°C	Operation	
$T_{VJ\ op}$	Maximum Virtual Junction Temperature under Switching Conditions	-40		175	°C	Intermittent with Reduced Life	

Note 1 DC continuous drain current, I_D, set by press-fit pin limit.

MOSFET Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, T_{VJ} = -40°C	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6	V	$V_{DS} = V_{GS}$, I_D = 69 mA	
			2.1			$V_{DS} = V_{GS}$, I_D = 69 mA, T_{VJ} = 150°C	
I_{DSS}	Zero Gate Voltage Drain Current		6	114	μA	V_{GS} = 0 V, V_{DS} = 1200 V	
I_{GSS}	Gate-Source Leakage Current		0.06	1.5	μA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance (Devices Only)		5.3	6.9	mΩ	V_{GS} = 15 V, I_D = 200 A	Fig. 2 Fig. 3
			8.5			V_{GS} = 15 V, I_D = 200 A, T_{VJ} = 150°C	
			9.6			V_{GS} = 15 V, I_D = 200 A, T_{VJ} = 175°C	
g_{fs}	Transconductance		162		S	V_{DS} = 20 V, I_{DS} = 200 A	Fig. 4
			145			V_{DS} = 20 V, I_{DS} = 200 A, T_{VJ} = 150°C	
E_{On}	Turn-On Switching Energy, T_{VJ} = 25°C T_{VJ} = 125°C T_{VJ} = 150°C		4.76 5.12 5.41		mJ	V_{DD} = 600 V, I_D = 200 A, V_{GS} = -4 V/15 V, $R_{G(OFF)}$ = 0.0 Ω, $R_{G(ON)}$ = 1.5 Ω, L = 40 μH	Fig. 11 Fig. 13
E_{Off}	Turn-Off Switching Energy, T_{VJ} = 25°C T_{VJ} = 125°C T_{VJ} = 150°C		0.44 0.45 0.46		mJ		
$R_{G(int)}$	Internal Gate Resistance		1.12		Ω	f = 100 kHz, V_{AC} = 25 mV	
C_{iss}	Input Capacitance		20.4		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
C_{oss}	Output Capacitance		0.79		nF		
C_{rss}	Reverse Transfer Capacitance		43		pF		
Q_{GS}	Gate to Source Charge		240		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 200 A Per IEC60747-8-4 pg 21	
Q_{GD}	Gate to Drain Charge		204		nC		
Q_G	Total Gate Charge		708		nC		
$R_{th\ JH}$	FET Thermal Resistance, Junction to Heatsink		0.295		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Body Diode Forward Voltage		4.9		V	V_{GS} = -4 V, I_{SD} = 200 A	Fig. 7
			4.4			V_{GS} = -4 V, I_{SD} = 200 A, T_{VJ} = 150°C	
			4.3			V_{GS} = -4 V, I_{SD} = 200 A, T_{VJ} = 175°C	
t_{rr}	Reverse Recovery Time		29		ns	V_{GS} = -4 V, I_{SD} = 200 A, V_R = 600 V di/dt = 20.0 A/ns, T_{VJ} = 150°C	Fig. 32
Q_{RR}	Reverse Recovery Charge		4.8		µC		
I_{RRM}	Peak Reverse Recovery Current		275		A		
E_{RR}	Reverse Recovery Energy, T_{VJ} = 25°C T_{VJ} = 125°C T_{VJ} = 150°C		0.14 0.45 0.63		mJ	V_{DD} = 600 V, I_D = 200 A, V_{GS} = -4 V/15 V, $R_{G(ON)}$ = 1.5 Ω, L= 40 µH	Fig. 14

Module Physical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R_{HS}	Package Resistance, M1 (High-Side)		0.98		mΩ	T_C = 25°C, I_D = 200 A, Note 2
			1.37			T_C = 125°C, I_D = 200 A, Note 2
R_{LS}	Package Resistance, M2 (Low-Side)		0.90			T_C = 25°C, I_D = 200 A, Note 2
			1.25			T_C = 125°C, I_D = 200 A, Note 2
L_{Stray}	Stray Inductance		7.1		nH	Between DC- and DC+, f = 10 MHz
T_C	Case Temperature	-40		125	°C	
W	Weight		39		g	
M_S	Mounting Torque		2.0	2.3	N-m	M4 bolts
V_{isol}	Case Isolation Voltage		3		kV	AC, 50 Hz, 1 min
CTI	Comparative Tracking Index	200				
	Clearance Distance		5.0		mm	Terminal to Terminal
			10.0			Terminal to Heatsink
	Creepage Distance		6.3			Terminal to Terminal
			11.5			Terminal to Heatsink

Note 2 Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance.

NTC Thermistor Characterization

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
R_{NTC}	Rated Resistance		5.0		kΩ	T_{NTC} = 25°C	Fig. 23
ΔR/R	Resistance Tolerance at 25°C	-5		5	%		
$\beta_{25/50}$	Beta Value (T_2 = 50°C)		3380		K		
$\beta_{25/80}$	Beta Value (T_2 = 80°C)		3468		K		
$\beta_{25/100}$	Beta Value (T_2 = 100°C)		3523		K		
P_{Max}	Power Dissipation			10	mW	T_{NTC} = 25°C	

Typical Performance

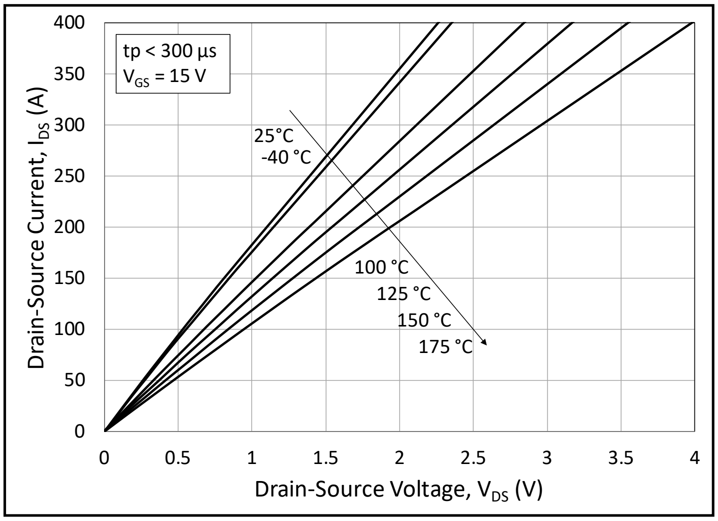


Figure 1. Output Characteristics for Various Junction Temperatures

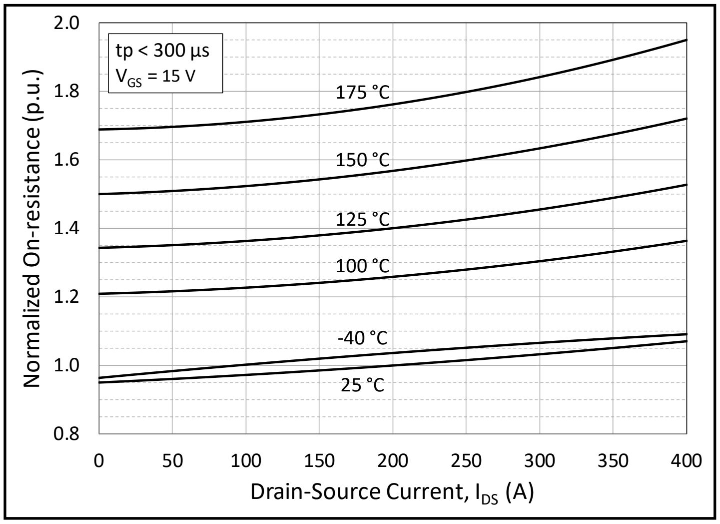


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

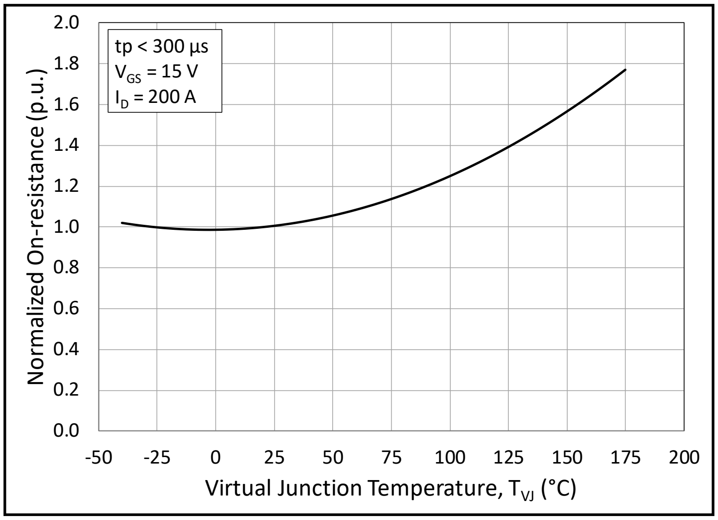


Figure 3. Normalized On-State Resistance vs. Junction Temperature

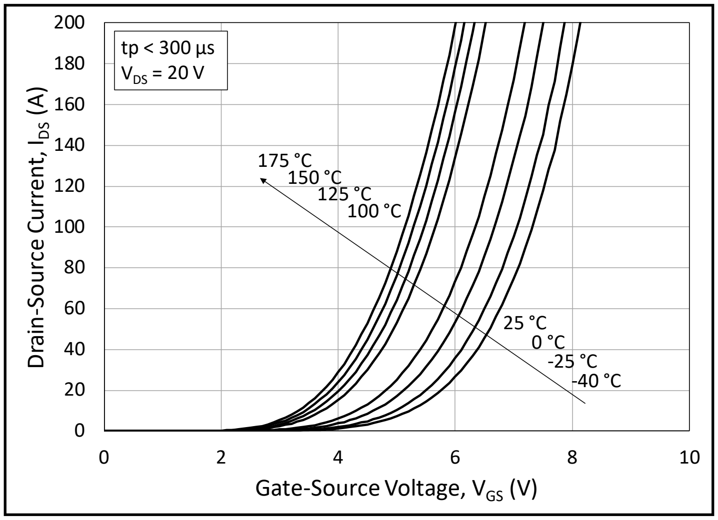


Figure 4. Transfer Characteristic for Various Junction Temperatures

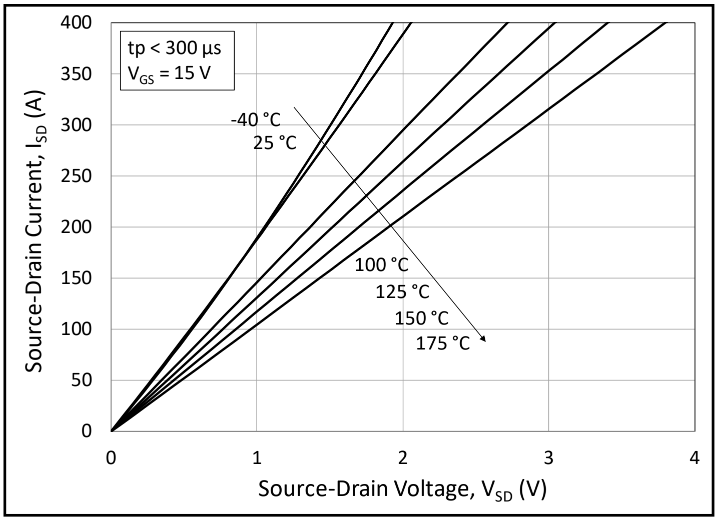


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

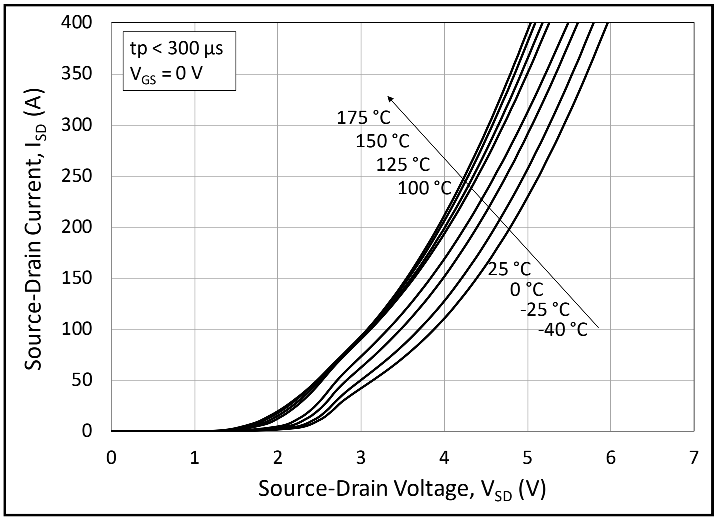


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

Typical Performance

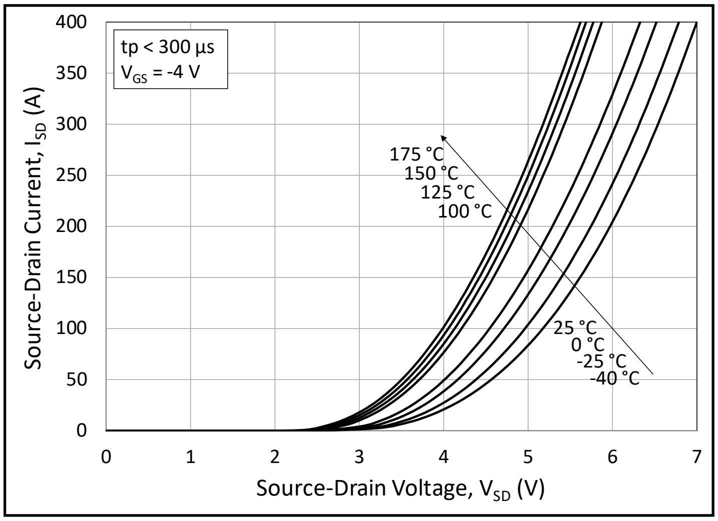


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = -4 V (Body Diode)

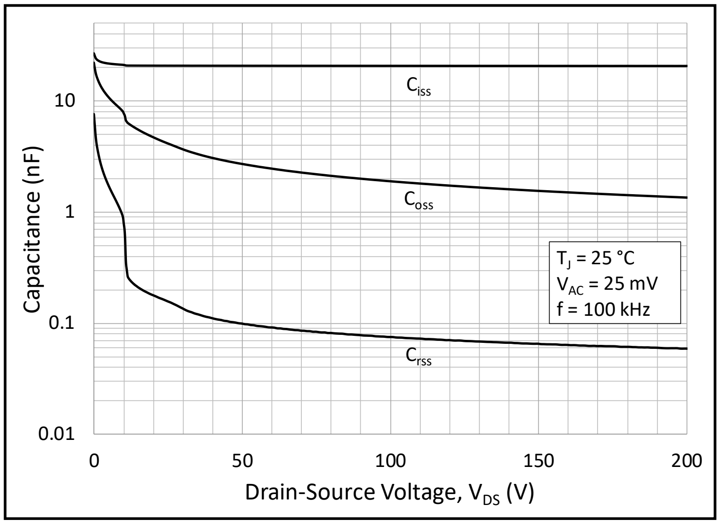


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

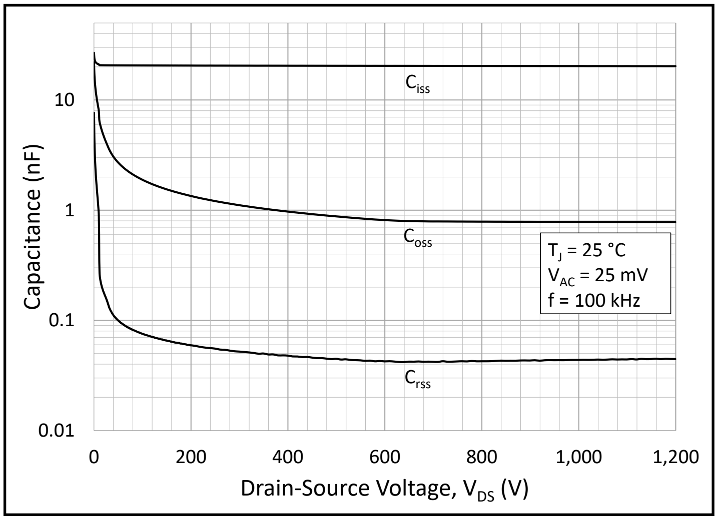


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

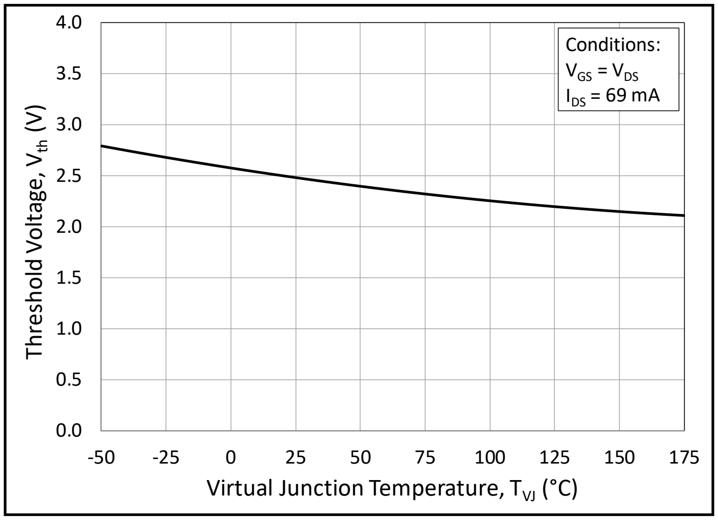


Figure 10. Threshold Voltage vs. Junction Temperature

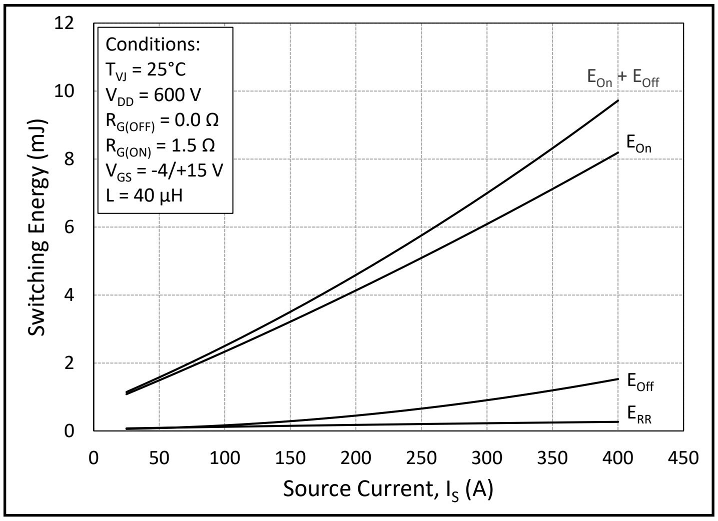


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

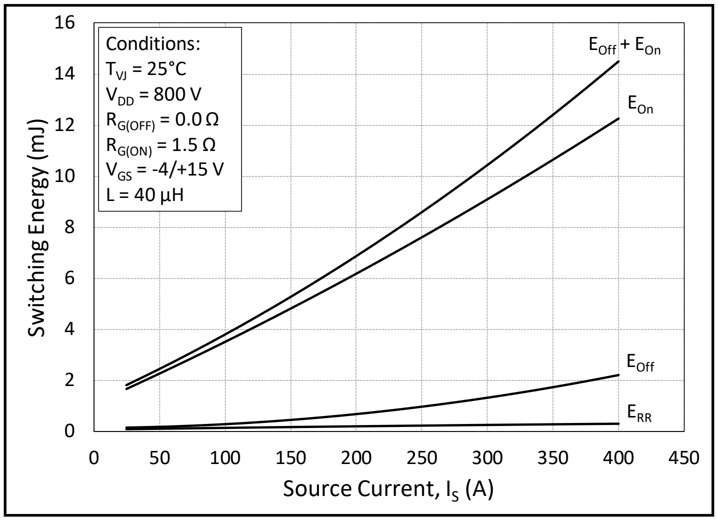


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

Typical Performance

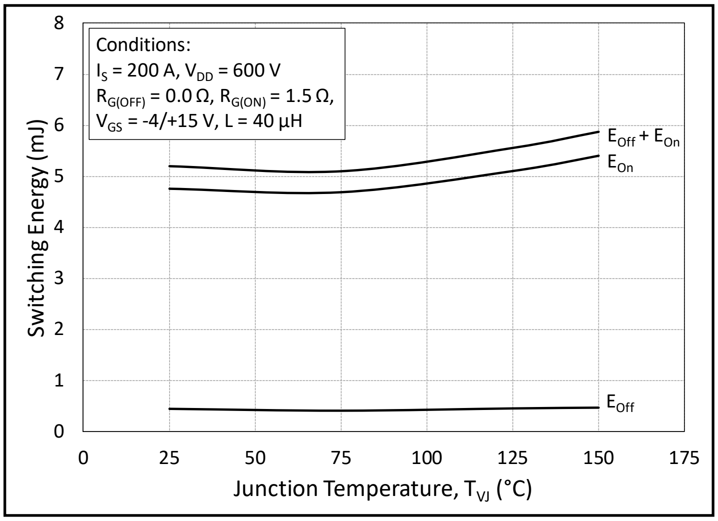


Figure 13. MOSFET Switching Energy vs. Junction Temperature

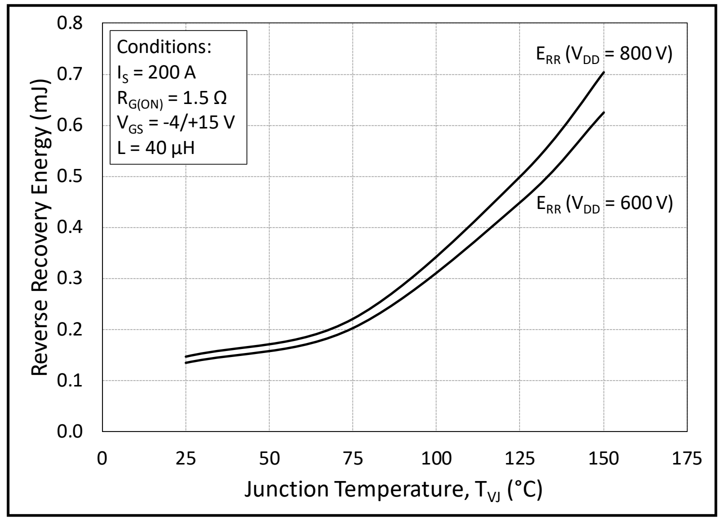


Figure 14. Reverse Recovery Energy vs. Junction Temperature

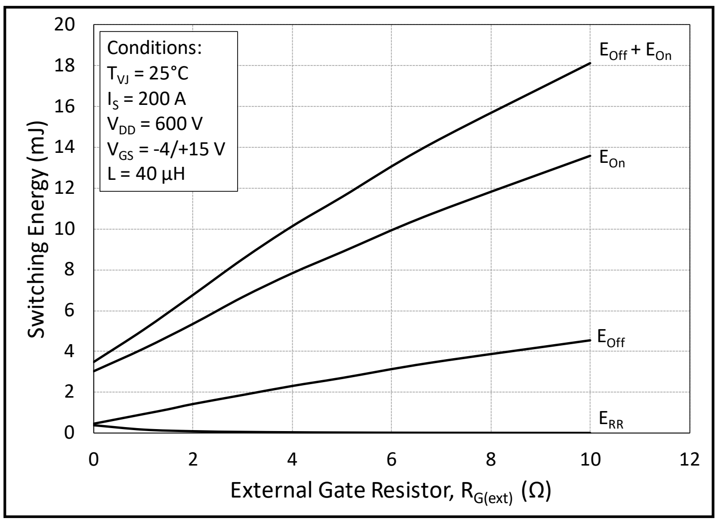


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

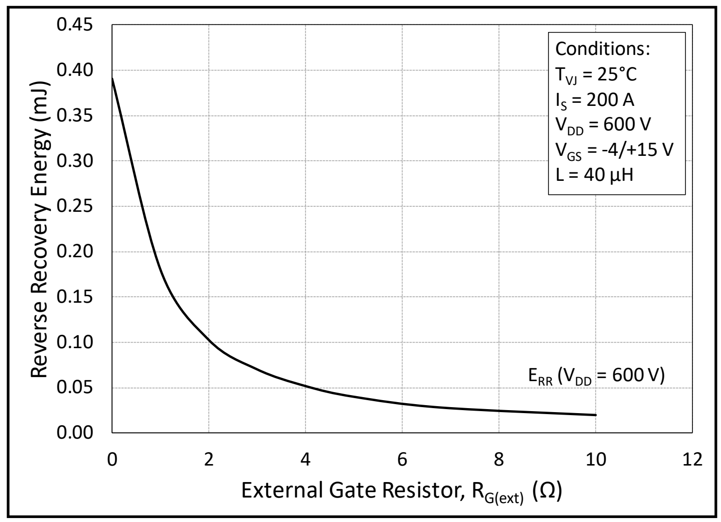


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

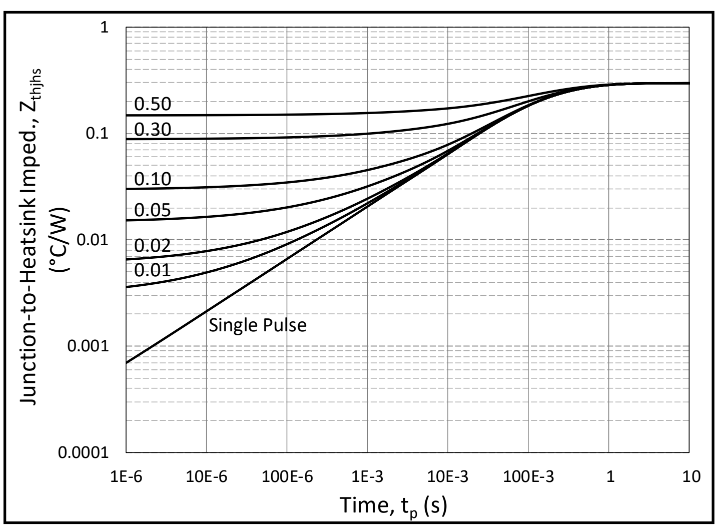


Figure 17. MOSFET Junction to Heatsink Transient Thermal Impedance, $Z_{th\ JHS}$ (°C/W)

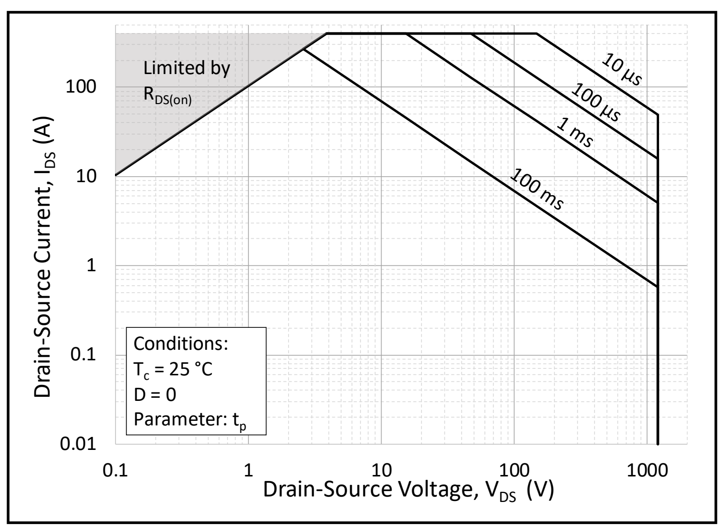


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

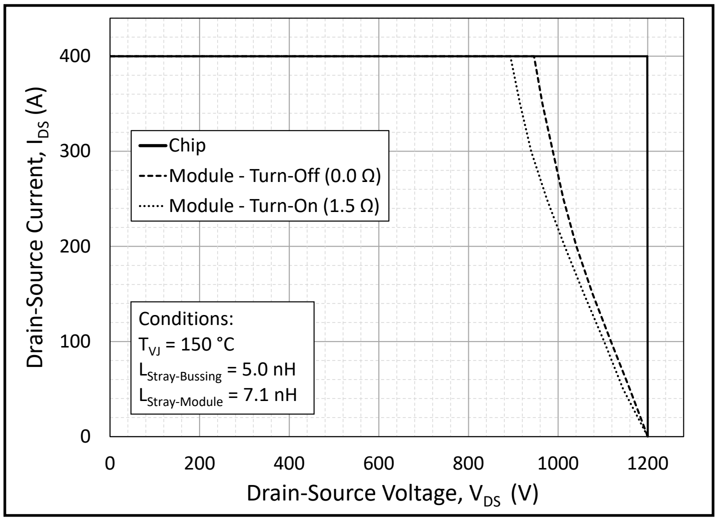


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

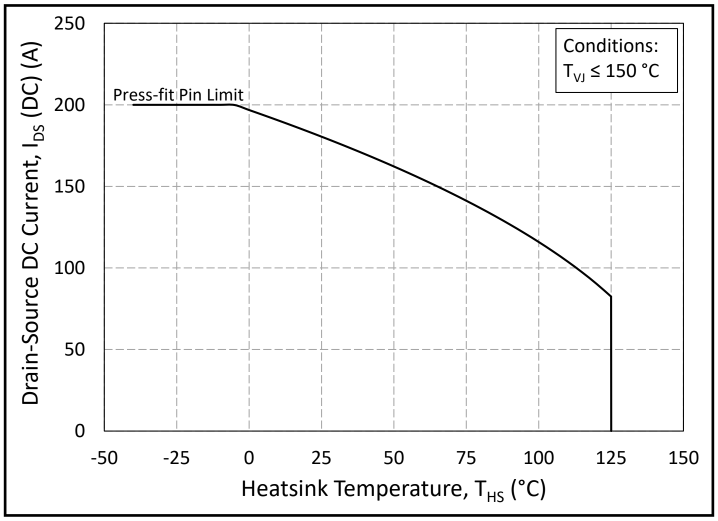


Figure 20. Continuous Drain Current Derating vs. Heatsink Temperature

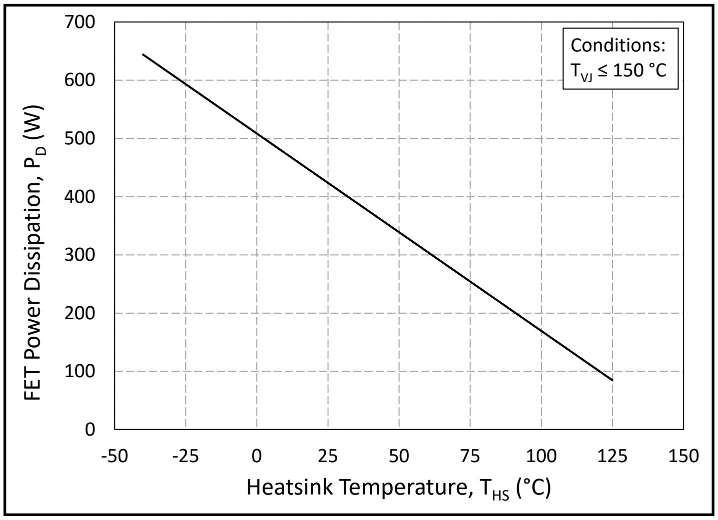


Figure 21. Maximum Power Dissipation Derating vs. Heatsink Temperature

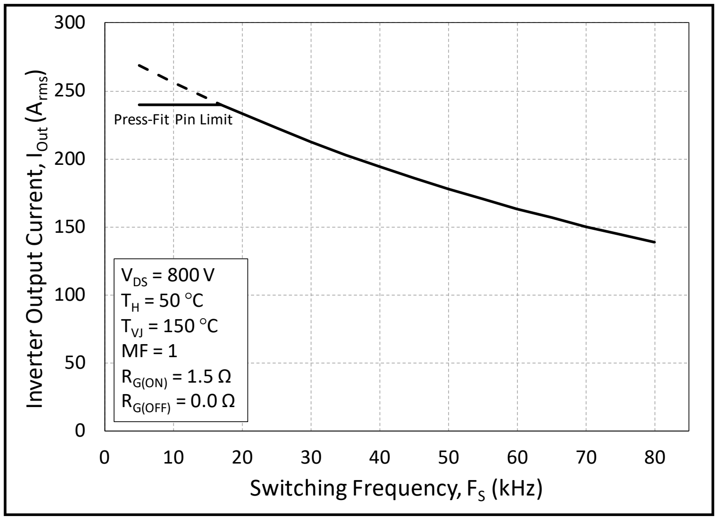


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

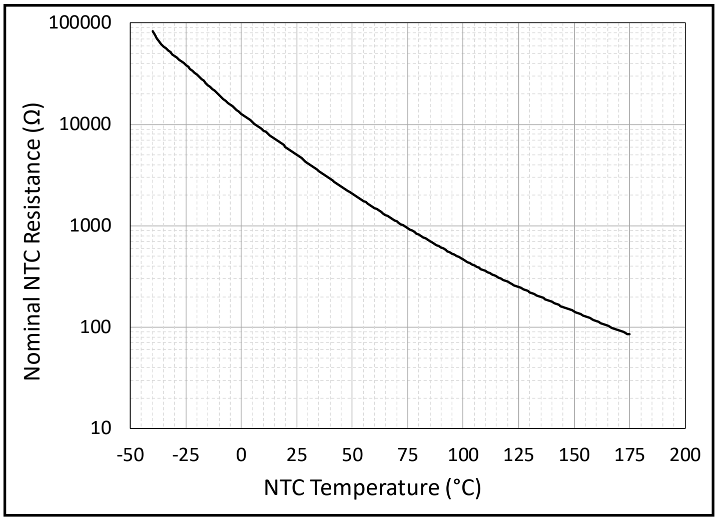


Figure 23. Nominal NTC Resistance vs. NTC Temperature

Timing Characteristics

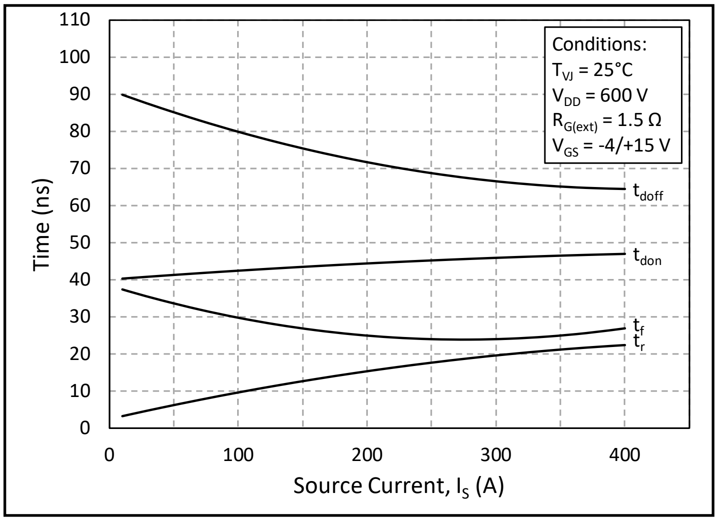


Figure 24. Timing vs. Source Current

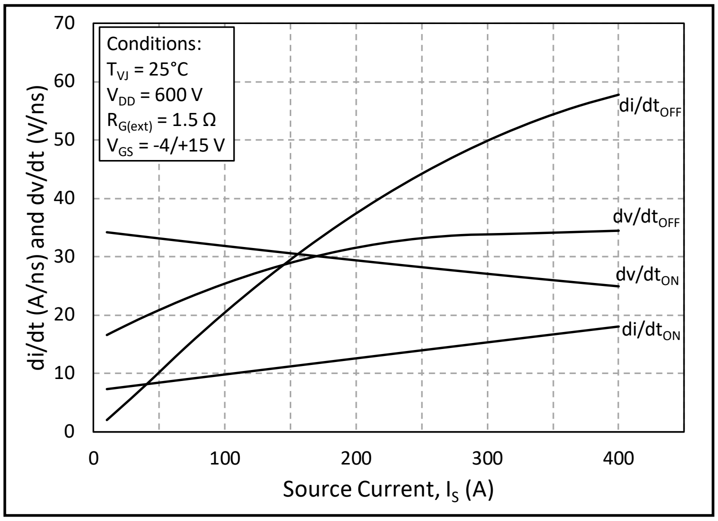


Figure 25. dv/dt and di/dt vs. Source Current

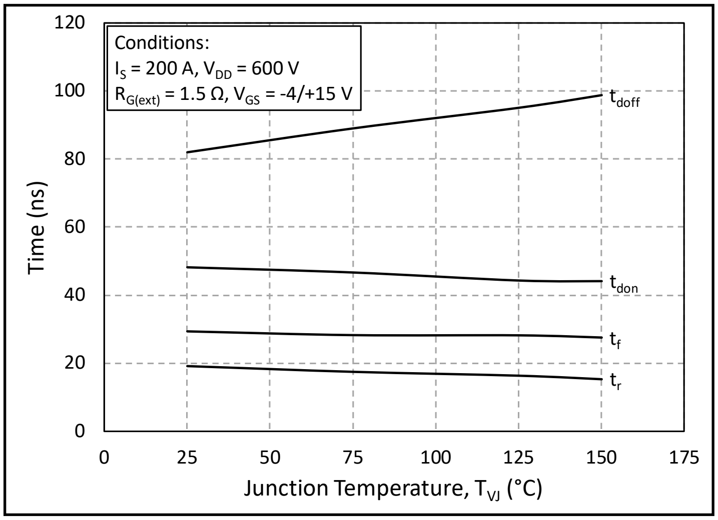


Figure 26. Timing vs. Junction Temperature

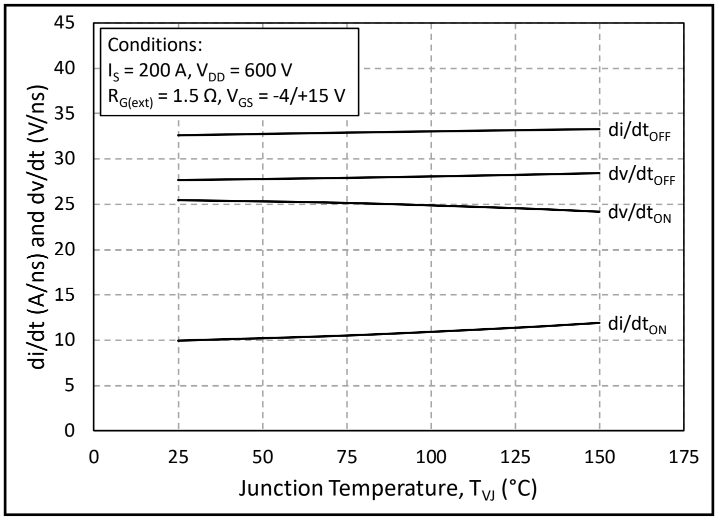


Figure 27. dv/dt and di/dt vs. Junction Temperature

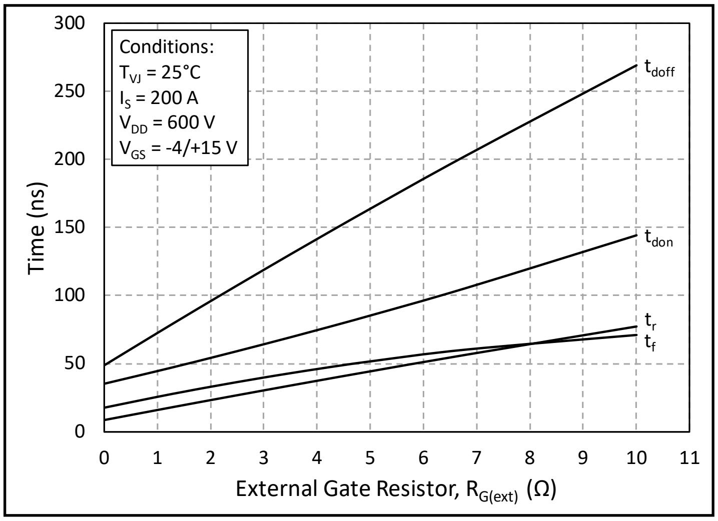


Figure 28. Timing vs. External Gate Resistance

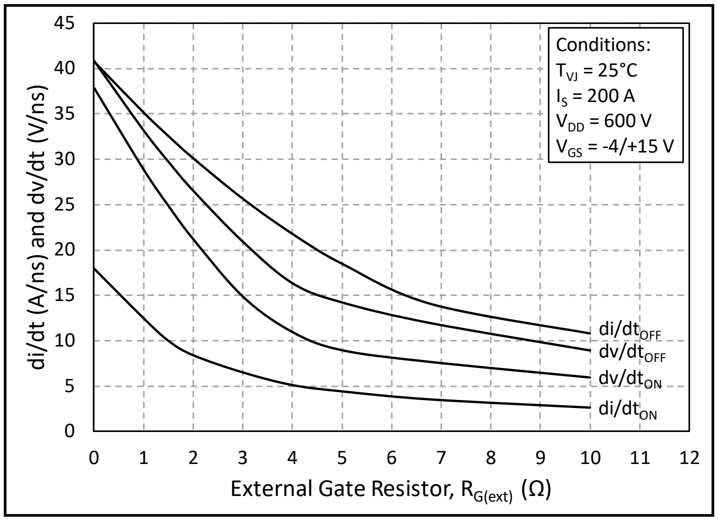


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

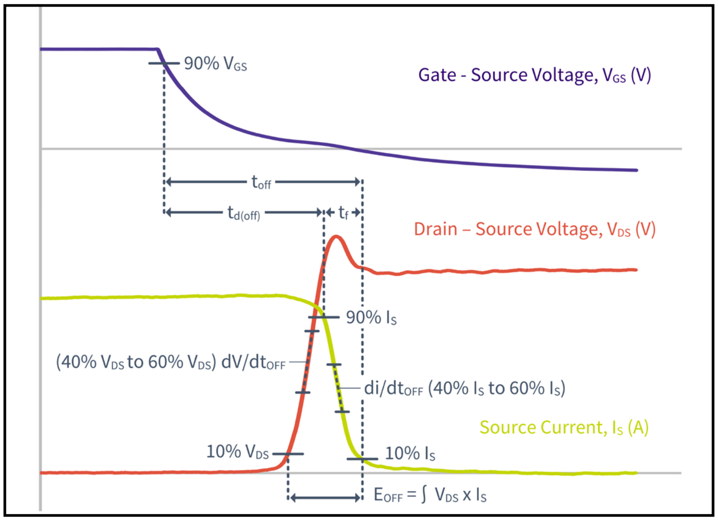


Figure 30. Turn-off Transient Definitions

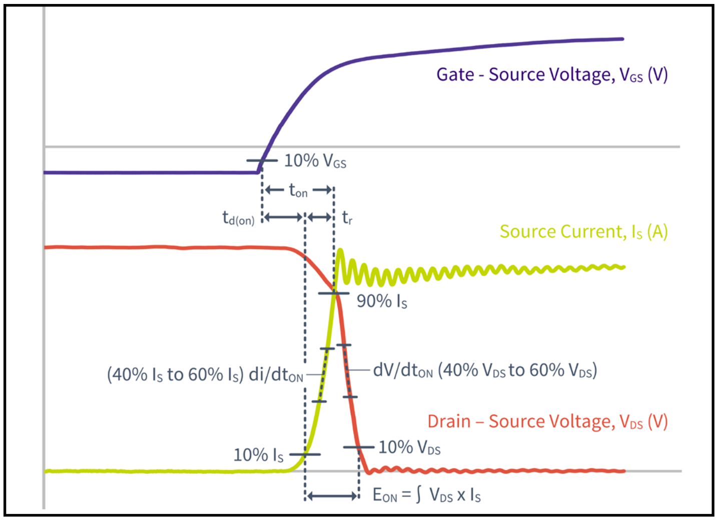


Figure 31. Turn-on Transient Definitions

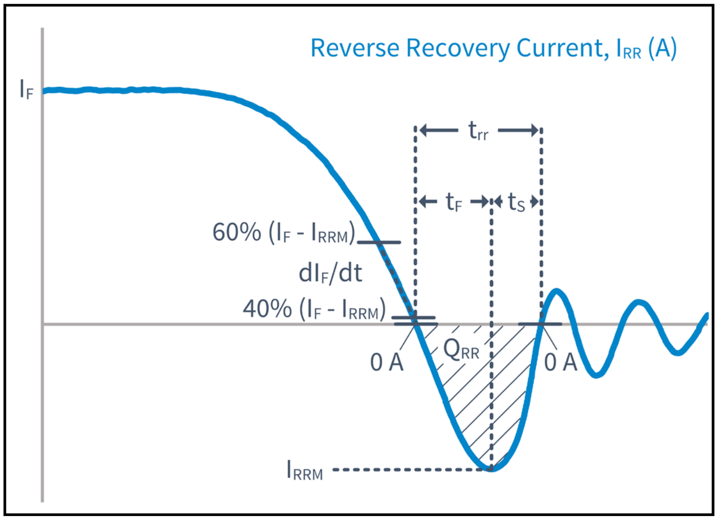


Figure 32. Reverse Recovery Definitions

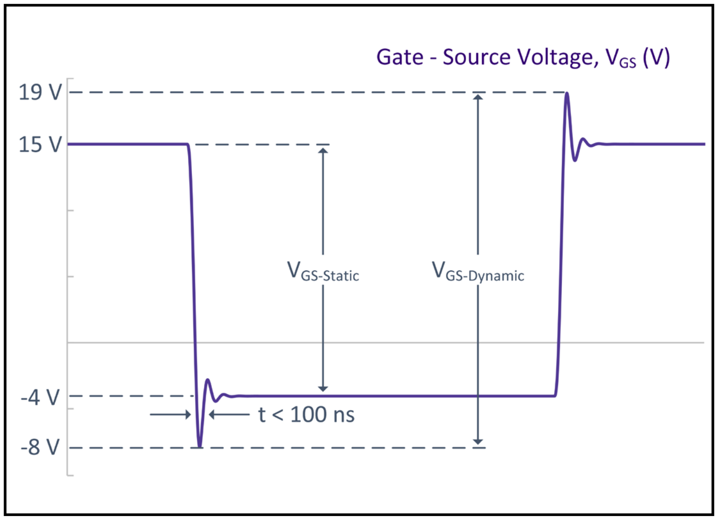
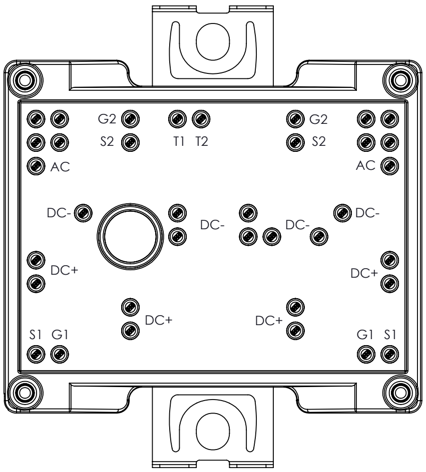
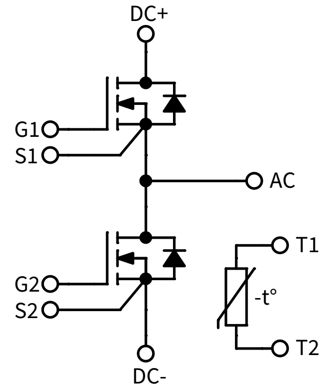


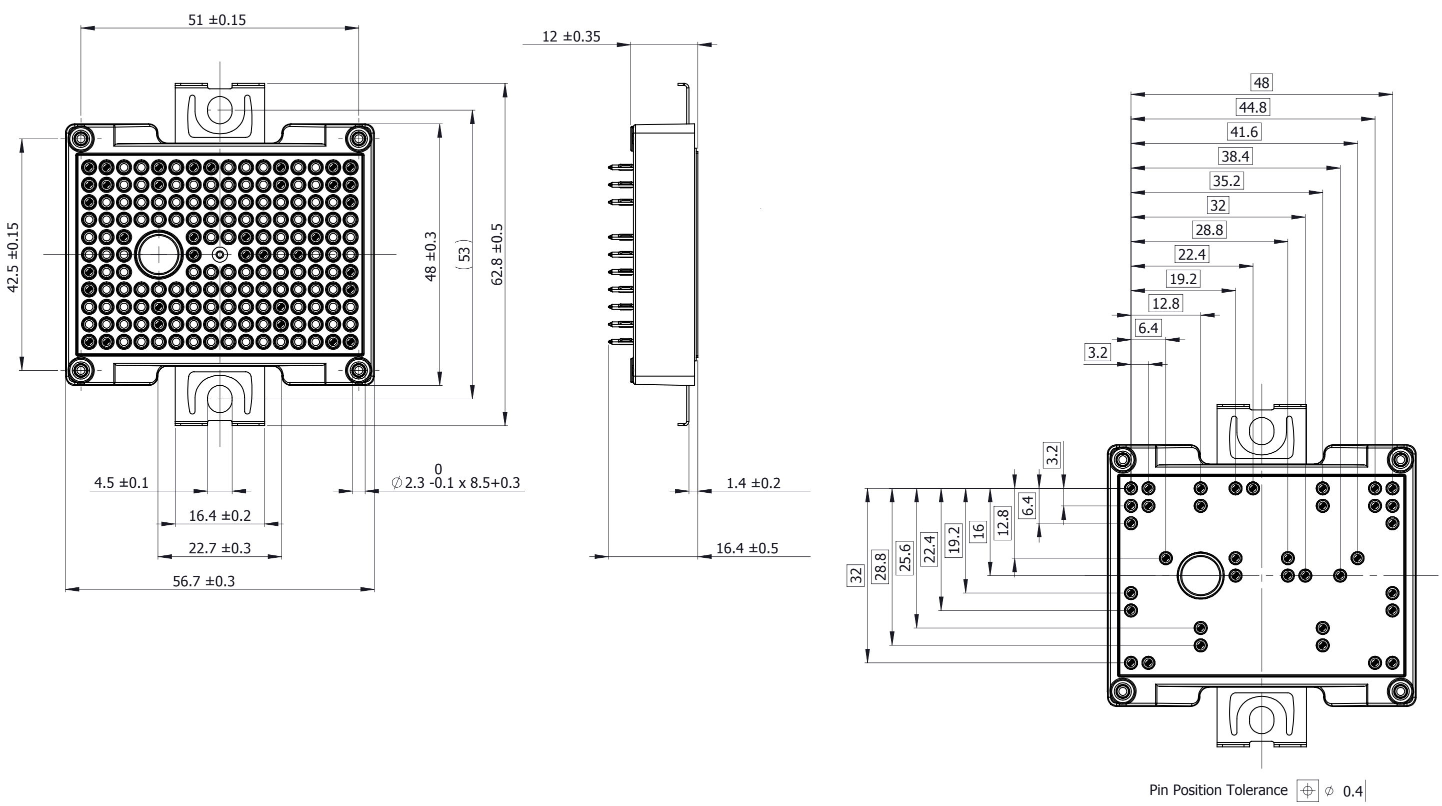
Figure 33. V_{GS} Transient Definitions

Schematic and Pin Out





Package Dimension (mm)



Supporting Links & Tools

Evaluation Tools
- KIT-CRD-CIL12N-GMA: Dynamic Evaluation Board for Half-Bridge GM3 Modules
- CAB006M12GM3 PLECS Model
- SpeedFit 2.0 Design Simulator™

Dual-Channel Companion Gate Driver Boards
- EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board
- Si823H-AxWA-KIT: Skyworks® Gate Driver Board
- CGD1700HB2M-UNA: Wolfspeed Gate Driver Board
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes
- CPWR-AN41: Mounting Instructions and PCB Requirements
- CPWR-AN42: Thermal Interface Material Application Note
- CPWR-AN45: Dynamic Performance Application Note

Notes

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