

4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
 - $t_{AA} = 10 \text{ ns} / 15 \text{ ns}$
- Embedded ECC for single-bit error correction^[1]
- Low active and standby currents
 - □ Active current: I_{CC} = 38-mA typical
 - □ Standby current: I_{SB2} = 6-mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Pb-free 44-pin SOJ, 44-pin TSOP II, and 48-ball VFBGA packages

Functional Description

CY7C1041G and CY7C1041GE are high-performance CMOS fast static RAM devices with embedded ECC. Both devices are offered in single and dual chip-enable options and in multiple pin configurations. The CY7C1041GE device includes an ERR pin that signals an error-detection and correction event during a read cycle.

Data writes are performed by asserting the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW, while providing the data on I/O₀ through I/O₁₅ and address on A₀ through A₁₇ pins. The Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}) inputs control write operations to the upper and lower bytes of the specified memory location. \overline{BHE} controls I/O₈ through I/O₁₅ and \overline{BLE} controls I/O₀ through I/O₇.

Data reads are performed by asserting the Chip Enable (CE) and Output Enable (\overline{OE}) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O₀ through I/O₁₅). Byte accesses <u>can</u> be <u>performed</u> by asserting the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O $_0$ through I/O $_{15}$) are placed in a high-impedance state during the following events:

- The device is deselected (CE HIGH)
- The control signals (OE, BLE, BHE) are de-asserted

On the CY7C1041GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = HIGH)^[1]. See the Truth Table on page 14 for a complete description of read and write modes.

The logic block diagram is on page 2.

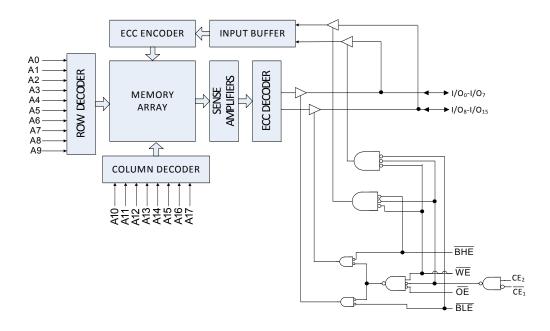
Product Portfolio

	Features and Options (see Pin		V _{CC} Range	Speed	Power Dissipation				
Product [2]		Range		(ns)	Operating I _{CC} , (mA)		- Tannan, 1362		
Floudet	Configurations on page 4)	italige	ge (V) 10/15		f = f _{max}		(mÅ)		
				10/13	Typ ^[3]	Max	Тур ^[3]	Max	
CY7C1041G(E)18	Single or Dual Chip Enables	Industrial	1.65 V-2.2 V	15	_	40	6	8	
CY7C1041G(E)30	Optional ERR pins		2.2 V-3.6 V	10	38	45			
CY7C1041G(E)	Optional ETAT pino		4.5 V–5.5 V	10	38	45			

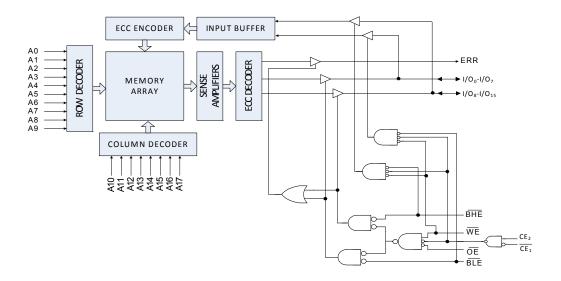
- 1. This device does not support automatic write-back on error detection.
- 2. The ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer Ordering Information on page 15 for details.
- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.



Logic Block Diagram - CY7C1041G



Logic Block Diagram - CY7C1041GE



CY7C1041G CY7C1041GE



Contents

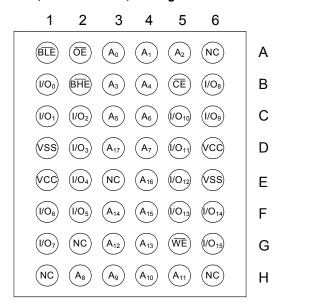
Pin Configurations	4
Maximum Ratings	
Operating Range	6
DC Electrical Characteristics	
Capacitance	7
Thermal Resistance	
AC Test Loads and Waveforms	7
Data Retention Characteristics	
Data Retention Waveform	
AC Switching Characteristics	
Switching Waveforms	
Truth Table	
ERR Output - CY7C1041GE	

Ordering Information	15
Ordering Code Definitions	
Package Diagrams	
Acronyms	
Document Conventions	18
Units of Measure	18
Document History Page	19
Sales, Solutions, and Legal Information	
Worldwide Sales and Design Support	
Products	
PSoC® Solutions	20
Cypress Developer Community	
Technical Support	
and the state of t	



Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, CY7C1041G $^{[4]}$, Package/Grade ID: BVXI $^{[6]}$ with ERR, CY7C1041GE $^{[4,\ 5]}$, Package/Grade ID: BVXI $^{[6]}$



1 2 3 4 5 BLE OE) (NC A₀ A₁ A₂ Α (I/O₀) (BHE) A₃ A_4 (CE) (I/O₈) В C (I/O₁) (I/O₂) (I/O₁₀) (I/O₉) A₅ A_6 (vss) (I/O₃) (I/O₁₁ (vcc) D (A₁₇) A_7 (vcc) (I/O₄) (ERR) $\left(A_{16}\right)$ (I/O₁₂) Ε (I/O₆) (I/O₅) (A₁₄) $\left(A_{15}\right)$ (I/O₁₃) F (NC (WE) (I/O₇) (I/O₁₅ (A₁₂) (A₁₃) G (A₁₁) (NC) (NC A₈ A₉ (A₁₀ Н

Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, CY7C1041G $^{[4]}$, Package/Grade ID: BVJXI $^{[6]}$

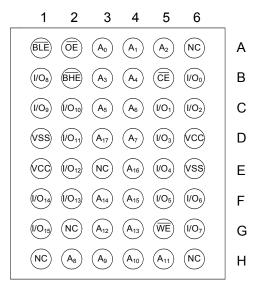


Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable with ERR, CY7C1041GE $^{[4, 5]}$, Package/Grade ID: BVJXI $^{[6]}$

1	2	3	4	5	6	_
BLE	(OE)	\bigcirc A ₀	\bigcirc A ₁	\bigcirc A ₂	NC	Α
(I/O ₈)	BHE	\bigcirc A ₃	$\overbrace{A_4}$	$\overline{\widehat{CE}}$	(I/O ₀)	В
(I/O ₉)	(I/O ₁₀)	\bigcirc A ₅	\bigcirc A ₆	$\overline{\text{I/O}_1}$	(I/O ₂)	С
VSS	(I/O ₁₁)	$\left(A_{17}\right)$	\bigcirc A ₇	(I/O ₃)	vcc	D
VCC	(I/O ₁₂)	ERR	(A ₁₆)	(I/O ₄)	vss	E
(I/O ₁₄)	(I/O ₁₃)	$\left(A_{14} \right)$	$\left(A_{15}\right)$	(I/O ₅)	(I/O ₆)	F
(I/O ₁₅)	NC	$\left(A_{12} \right)$	$\left(A_{13}\right)$	$\overline{\overline{\text{WE}}}$	(I/O ₇)	G
NC	\bigcirc A ₈	\bigcirc A ₉	$\left(A_{10}\right)$	$\left(A_{11}\right)$	NC	Н
						_

- 4. NC pins are not connected internally to the die.
- 5. ERR is an output pin.
- Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O_[7:0] and I/O_[15:8] balls are swapped.

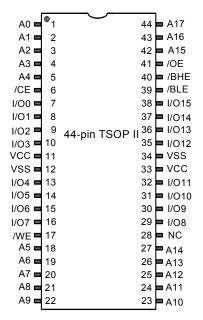


Pin Configurations (continued)

Figure 5. 44-pin TSOP II/44-pin SOJ Single Chip Enable with ERR, CY7C1041GE [7, 8]

A0=	1		44	_	A17
A1=	2		43	-	A16
A2=	3		42	-	A15
A3=	4		41	-	/OE
A4 ■	5		40	-	/BHE
/CE=	6		39	-	/BLE
I/O0 =	7		38	-	I/O15
I/O1 =	8		37	-	I/O14
I/O2=	9	44- pin TSOP	₁ 36	-	I/O13
I/O3=	10	11 piii 1001	35	-	I/O12
VCC=	11		34	-	VSS
VSS=	12		33	-	VCC
I/O4 =	13		32	-	I/O11
I/O5 =	14		31	-	I/O10
I/O6 =	15		30	-	I/O9
I/O7 =	16		29	-	I/O8
/WE=	17		28	-	ERR
A5 =	18		27	-	A14
A6 =	19		26	-	A13
A7 □	20		25	-	A12
A8 ■	21		24	-	A11
A9 ■	22		23	-	A10

Figure 6. 44-pin TSOP II/44-pin SOJ Single Chip Enable without ERR, CY7C1041G $^{[7]}$



- 7. NC pins are not connected internally to the die.
- 8. ERR is an output pin.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C Ambient temperature with power applied -55 °C to +125 °C Supply voltage on V_{CC} relative to GND ^[9] -0.5 V to V_{CC} + 0.5 V DC voltage applied to outputs

DC input voltage [9]	–0.5 V to V_{CC} + 0.5 V
Current into outputs (in LOW state)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	>2001 V
Latch-up current	> 140 mA

Operating Range

Grade	Ambient Temperature	V _{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Davamatav	Description		T4 O 4!4!		10	Unit			
Parameter	Desc	ription	Test Conditions		Min	Typ [10]	Max	Jill	
V _{OH}	Output HIGH	1.65 V to 2.2 V	$V_{\rm CC}$ = Min, $I_{\rm OH}$ = -0.1 m	ıΑ	1.4	_	_	V	
	voltage	2.2 V to 2.7 V	$V_{\rm CC}$ = Min, $I_{\rm OH}$ = -1.0 m	Α	2	-	_		
		2.7 V to 3.6 V	$V_{\rm CC}$ = Min, $I_{\rm OH}$ = -4.0 m	ıΑ	2.2	_	-		
		4.5 V to 5.5 V	$V_{\rm CC}$ = Min, $I_{\rm OH}$ = -4.0 m	ıΑ	2.4	_	-		
		4.5 V to 5.5 V	$V_{\rm CC}$ = Min, $I_{\rm OH}$ = -0.1 m	Α	$V_{CC} - 0.5^{[11]}$	_	_		
V _{OL}	Output LOW	1.65 V to 2.2 V	V _{CC} = Min, I _{OL} = 0.1 mA		_	-	0.2	V	
	voltage	2.2 V to 2.7 V	V _{CC} = Min, I _{OL} = 2 mA		_	-	0.4		
		2.7 V to 3.6 V	V _{CC} = Min, I _{OL} = 8 mA		_	-	0.4		
		4.5 V to 5.5 V	V _{CC} = Min, I _{OL} = 8 mA		_	_	0.4		
V _{IH}	Input HIGH	1.65 V to 2.2 V			1.4	-	V _{CC} + 0.2 ^[9]	V	
	voltage	2.2 V to 2.7 V			2	-	V _{CC} + 0.3 ^[9]		
		2.7 V to 3.6 V			2	-	V _{CC} + 0.3 ^[9]		
		4.5 V to 5.5 V	-		2.2	_	V _{CC} + 0.5 ^[9]		
V _{IL}	Input LOW	1.65 V to 2.2 V	-		-0.2 ^[9]	_	0.4	V	
	voltage	2.2 V to 2.7 V			-0.3 ^[9]	-	0.6		
		2.7 V to 3.6 V	-		-0.3 ^[9]	_	0.8		
		4.5 V to 5.5 V	-		-0.5 ^[9]	_	0.8		
I _{IX}	Input leakage co	urrent	$GND \le V_{IN} \le V_{CC}$		-1	_	+1	μΑ	
I _{OZ}	Output leakage	current	GND \leq V _{OUT} \leq V _{CC} , Out	put disabled	-1	_	+1	μΑ	
I _{CC}	Operating suppl	ly current	Max V _{CC} , I _{QUT} = 0 mA,	f = 100 MHz	_	38	45	mA	
			CMOS levels	f = 66.7 MHz	_	_	40		
I _{SB1}	Automatic CE power-down current – TTL inputs			= f _{MAX}	_	_	15	mA	
I _{SB2}	Automatic CE p current – CMOS	ower-down S inputs	$\begin{array}{c} \text{Max V}_{\text{CC}}, \ \overline{\text{CE}} \geq \text{V}_{\text{CC}} - 0.\\ \text{V}_{\text{IN}} \geq \text{V}_{\text{CC}} - 0.2 \ \text{V or V}_{\text{IN}} \end{array}$		_	6	8	mA	

^{9.} $V_{IL(min)}$ = -2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 2 ns.

^{10.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V – 2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2V – 3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V – 5.5 V), V_{CC} = 3 V (for V_{CC} range of 2.2V – 3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V – 5.5 V), V_{CC} = 25 °C.

^{11.} This parameter is guaranteed by design and not tested.



Capacitance

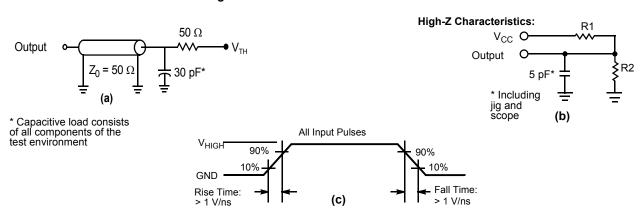
Parameter [12]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz,	10	10	10	pF
C _{OUT}	I/O capacitance	$V_{CC} = V_{CC(typ)}$	10	10	10	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	48-ball VFBGA	44-pin SOJ	44-pin TSOP II	Unit
$\Theta_{\sf JA}$	(junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer	31.35	55.37	68.85	°C/W
00	Thermal resistance (junction to case)	printed circuit board	14.74	30.41	15.97	°C/W

AC Test Loads and Waveforms

Figure 7. AC Test Loads and Waveforms [13]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

^{12.} Tested initially and after any design or process changes that may affect these parameters.

^{13.} Full-device AC operation assumes a 100- μ s ramp time from 0 to $V_{CC(min)}$ and a 100- μ s wait time after V_{CC} stabilization.



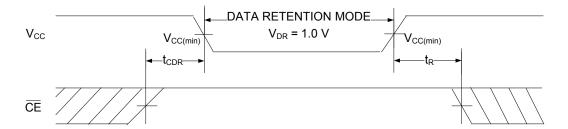
Data Retention Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V _{CC} for data retention		1	-	V
I _{CCDR}	Data retention current	$V_{CC} = 1.2 \text{ V}, \overline{CE} \ge V_{CC} - 0.2 \text{ V}^{[14]},$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}, \text{ or } V_{IN} \le 0.2 \text{ V}$	-	8	mA
t _{CDR} ^[15]	Chip deselect to data retention time		0	_	ns
t _R ^[14, 15]	Operation recovery time	V _{CC} ≥ 2.2 V	10	ı	ns
		V _{CC} < 2.2 V	15	_	ns

Data Retention Waveform

Figure 8. Data Retention Waveform [14]



^{14.} Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \ge 100 \, \mu s$ or stable at $V_{CC \, (min)} \ge 100 \, \mu s$.

 $^{15. \,} These \ parameters \ are \ guaranteed \ by \ design.$



AC Switching Characteristics

Over the operating range of -40 °C to 85 °C

Parameter [16]	Donasis tina	10	ns	15 ns		
Parameter	Description	Min	Max	Min	Max	Unit
Read Cycle		•	•	•	•	
t _{RC}	Read cycle time	10	_	15	_	ns
t _{AA}	Address to data / ERR valid	_	10	_	15	ns
t _{OHA}	Data / ERR hold from address change	3	_	3	_	ns
t _{ACE}	CE LOW to data / ERR valid [17]	_	10	-	15	ns
t _{DOE}	OE LOW to data / ERR valid	_	4.5	-	8	ns
t _{LZOE}	OE LOW to low impedance [18, 19]	0	_	0	_	ns
t _{HZOE}	OE HIGH to HI-Z [18, 19]	_	5	-	8	ns
t _{LZCE}	CE LOW to low impedance [17, 18, 19]	3	_	3	_	ns
t _{HZCE}	CE HIGH to HI-Z [17, 18, 19]	_	5	-	8	ns
t _{PU}	CE LOW to power-up [17, 19, 20]	0	_	0	_	ns
t _{PD}	CE HIGH to power-down [17, 19, 20]	_	10	-	15	ns
t _{DBE}	Byte enable to data valid	_	4.5	-	8	ns
t _{LZBE}	Byte enable to low impedance [19]	0	_	0	_	ns
t _{HZBE}	Byte disable to HI-Z [19]	_	6	-	8	ns
Write Cycle [2	0, 21]					
t _{WC}	Write cycle time	10	_	15	_	ns
t _{SCE}	CE LOW to write end [17]	7	_	12	_	ns
t _{AW}	Address setup to write end	7	_	12	_	ns
t _{HA}	Address hold from write end	0	_	0	_	ns
t _{SA}	Address setup to write start	0	_	0	_	ns
t _{PWE}	WE pulse width	7	_	12	_	ns
t _{SD}	Data setup to write end	5	_	8	_	ns
t _{HD}	Data hold from write end	0	_	0	_	ns
t _{LZWE}	WE HIGH to low impedance [18, 19]	3	_	3	_	ns
t _{HZWE}	WE LOW to HI-Z [18, 19]	_	5	_	8	ns
t _{BW}	Byte Enable to write end	7	_	12	_	ns

^{16.} Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \ge 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \ge 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 7 on page 7, unless specified otherwise.

^{17.} For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$. When $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or $\overline{\text{CE}}_2$ is HIGH.

^{18.} t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZOE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 7 on page 7. Transition is measured ±200 mV from steady state voltage.

^{19.} These parameters are guaranteed by design and are not tested.

^{20.} The internal write time of the memory is defined by the overlap of WE = V_{IL}, \(\overline{CE} = V_{IL} \), and \(\overline{BHE} = V_{IL} \). These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

^{21.} The minimum write cycle pulse width in Write Cycle No 2 (WE Controlled, OE LOW) should be equal to sum of t_{sd} and t_{HZWE}.



Switching Waveforms

Figure 9. Read Cycle No. 1 of CY7C1041G (Address Transition Controlled) $^{[22,\,23]}$

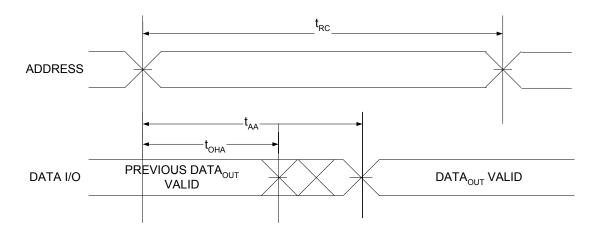
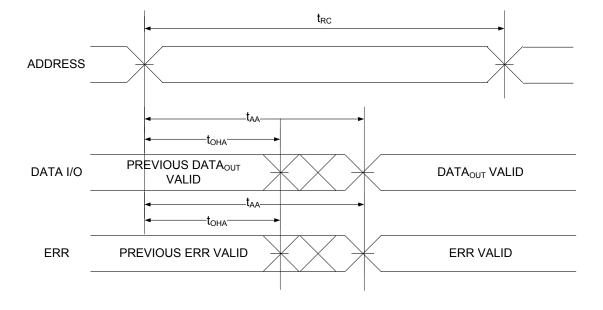


Figure 10. Read Cycle No. 1 of CY7C1041GE (Address Transition Controlled) $^{[22,\ 23]}$

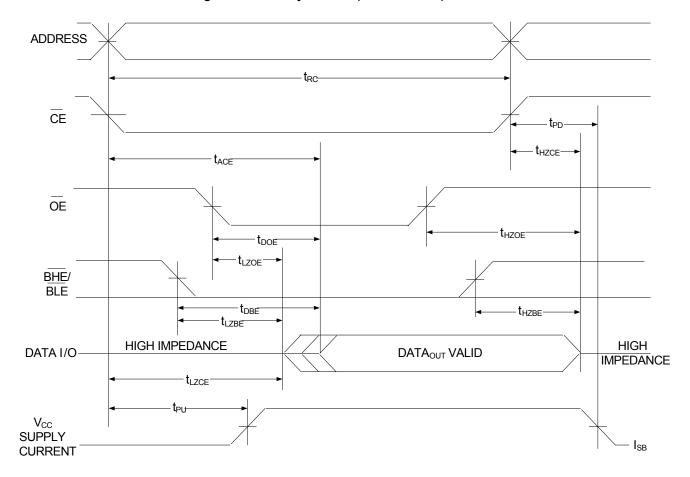


Notes22. The device is continuously selected, $\overline{OE} = V_{|L}$, $\overline{CE} = V_{|L}$, \overline{BHE} or \overline{BLE} or both = $V_{|L}$.
23. \overline{WE} is HIGH for the read cycle.



Switching Waveforms (continued)

Figure 11. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [24, 25, 26]



^{24.} For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.

25. WE is HIGH for the read cycle.

^{26.} Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.



Switching Waveforms (continued)

Figure 12. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) $^{[27, 28, 29]}$

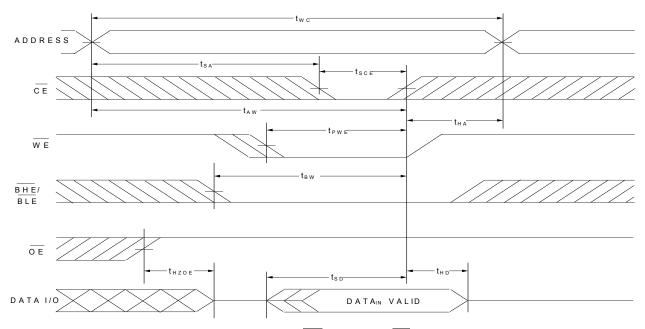
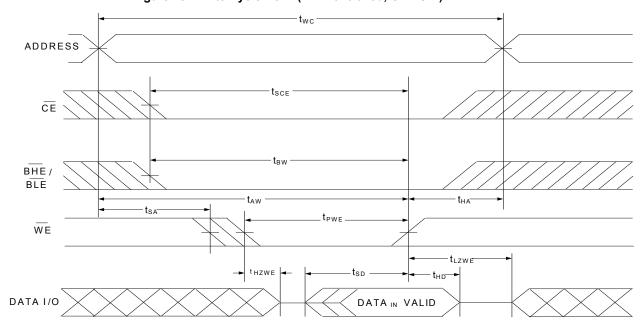


Figure 13. Write Cycle No. 2 (WE Controlled, $\overline{\text{OE}}$ LOW) $^{[27,\ 28,\ 29,\ 30]}$



- 27. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
- 28. The internal write time of the memory is defined by the overlap of WE = V_{IL}, CE = V_{IL}, and BHE or BLE = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 29. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
- 30. The minimum write cycle pulse width should be equal to sum of $t_{\mbox{\footnotesize SD}}$ and $t_{\mbox{\footnotesize HZWE}}$



Switching Waveforms (continued)

Figure 14. Write Cycle No. 3 ($\overline{\rm BLE}$ or $\overline{\rm BHE}$ Controlled) $^{[31,\ 32,\ 33]}$

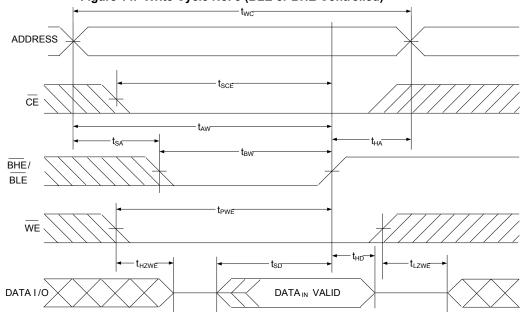
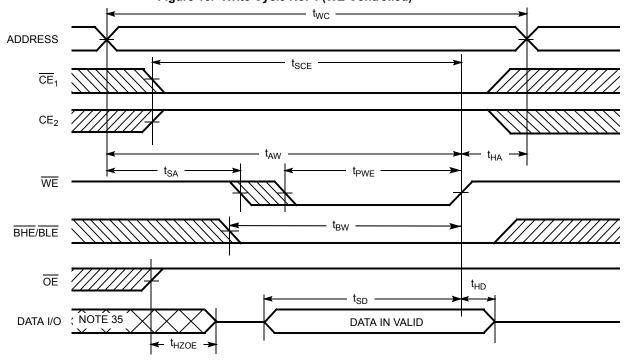


Figure 15. Write Cycle No. 4 ($\overline{\text{WE}}$ Controlled) [31, 32, 33, 34]



- 31. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and \overline{CE}_2 . When \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW,
- 32. The internal write time of the memory is defined by the overlap of WE = V_{IL}, $\overline{CE} = V_{IL}$, and \overline{BHE} or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 33. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$, or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
- 34. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 35. During this period the I/Os are in output state. Do not apply input signals.



Truth Table

CE [36]	OE	WE	BLE	BHE	I/O ₀ –I/O ₇	I/O ₈ -I/O ₁₅	Mode	Power
Н	X ^[37]	X ^[37]	X ^[37]	X ^[37]	HI-Z	HI-Z	Power down	Standby (I _{SB})
L	L	Н	Г	L	Data out	Data out	Read all bits	Active (I _{CC})
L	L	Н	L	Н	Data out	HI-Z	Read lower bits only	Active (I _{CC})
L	L	Н	Н	L	HI-Z	Data out	Read upper bits only	Active (I _{CC})
L	Х	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
L	Х	L	L	Н	Data in	HI-Z	Write lower bits only	Active (I _{CC})
L	Х	L	Н	L	HI-Z	Data in	Write upper bits only	Active (I _{CC})
L	Н	Н	Х	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I _{CC})
L	Х	Х	Ι	Н	HI-Z	HI-Z	Selected, outputs disabled	Active (I _{CC})

ERR Output - CY7C1041GE

Output [38] Mode		
0	Read operation, no single-bit error in the stored data.	
1 Read operation, single-bit error detected and corrected.		
HI-Z Device deselected or outputs disabled or Write operation		

^{36.} For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.

^{37.} The input voltage levels on these pins should be either at V_{IH} or V_{IL} .

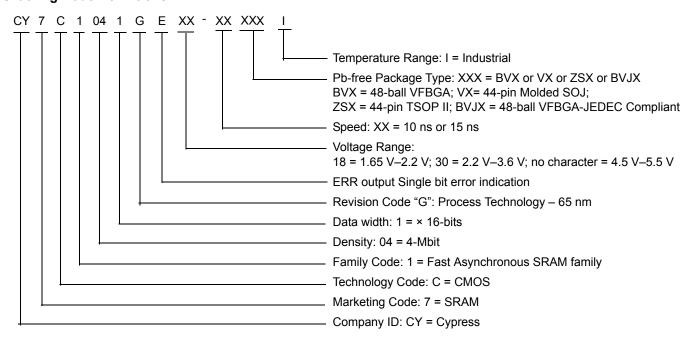
^{38.} ERR is an Output pin.If not used, this pin should be left floating



Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V-3.6 V	CY7C1041GE30-10ZSXI	51-85087	44-pin TSOP II, ERR output	Industrial
		CY7C1041G30-10ZSXI	51-85087	44-pin TSOP II	
		CY7C1041GE30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), ERR output	
		CY7C1041G30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	
		CY7C1041G30-10BVJXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm), JEDEC	
		CY7C1041G30-10VXI	51-85082	44-pin SOJ (400 Mils)	
		CY7C1041GE30-10VXI	51-85082	44-pin SOJ (400 Mils), ERR output	
	4.5 V–5.5 V	CY7C1041G-10ZSXI	51-85087	44-pin TSOP II	
		CY7C1041GE-10ZSXI	51-85087	44-pin TSOP II, ERR output	
		CY7C1041GE-10VXI	51-85082	44-pin SOJ (400 Mils), ERR output	
		CY7C1041G-10VXI	51-85082	44-pin SOJ (400 Mils)	
15	15 1.65 V-2.2 V	CY7C1041G18-15ZSXI	51-85087	44-pin TSOP II	
		CY7C1041G18-15VXI	51-85082	44-pin SOJ (400 Mils)	
		CY7C1041G18-15BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	

Ordering Code Definitions





Package Diagrams

Figure 16. 44-pin TSOP II (Z44) Package Outline, 51-85087

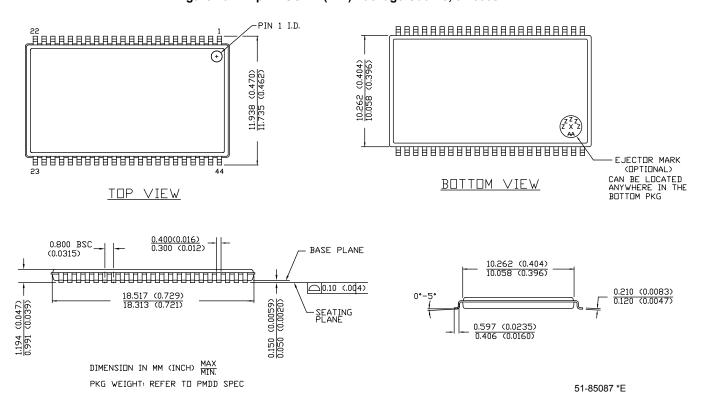
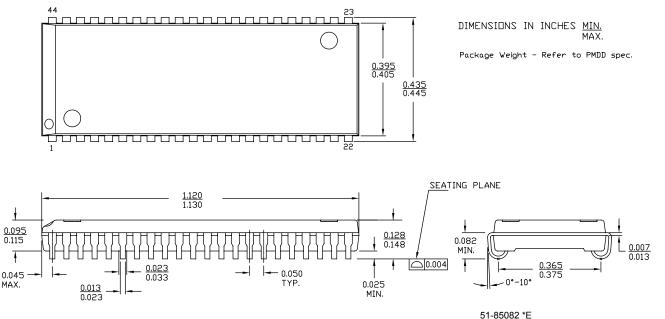


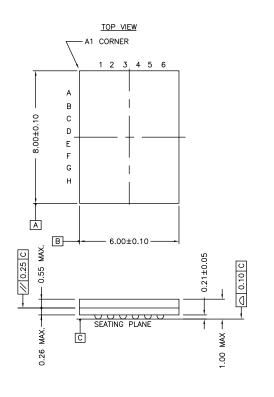
Figure 17. 44-pin SOJ (400 Mils) Package Outline, 51-85082

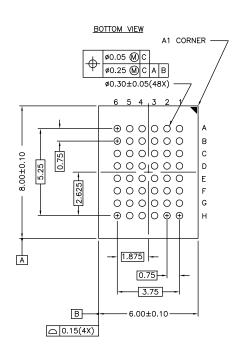




Package Diagrams (continued)

Figure 18. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150





NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
posted on the Cypress web.

51-85150 *H



Acronyms

Acronym	Description
BHE byte high enable	
BLE	byte low enable
CE	chip enable
CMOS complementary metal oxide semiconductor	
I/O input/output	
OE output enable	
SRAM static random access memory	
TSOP	thin small outline package
TTL transistor-transistor logic	
VFBGA very fine-pitch ball grid array	
WE write enable	

Document Conventions

Units of Measure

Symbol	Unit of Measure		
°C	Degrees Celsius		
MHz	megahertz		
μΑ	microamperes		
μS	microseconds		
mA	milliamperes		
mm	millimeters		
ns	nanoseconds		
Ω	ohms		
%	percent		
pF	picofarads		
V	volts		
W	watts		



Document History Page

ocument Title: CY7C1041G/CY7C1041GE, 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC) ocument Number: 001-91368				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*F	4867081	NILE	07/31/2015	Changed status from Preliminary to Final.
*G	4876251	NILE	08/07/2015	Updated Ordering Information: Updated part numbers.
*H	4968879	NILE	10/16/2015	Fixed typo in bookmarks.
*	5019226	VINI	11/18/2015	Updated Ordering Information: Updated part numbers.
*J	5122043	NILE	02/02/2016	Updated Truth Table.



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive
Clocks & Buffers
Interface

Lighting & Power Control

Memory
PSoC
Touch Sensing
USB Controllers

Wireless/RF

cypress.com/go/automotive cypress.com/go/clocks cypress.com/go/interface cypress.com/go/powerpsoc cypress.com/go/memory cypress.com/go/psoc cypress.com/go/touch cypress.com/go/USB cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2014-2016. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.