

# CSD23280F3 –12-V P-Channel FemtoFET™ MOSFET

## 1 Features

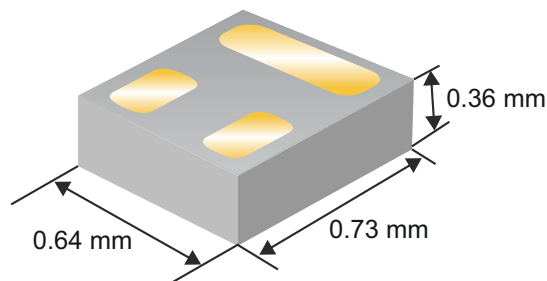
- Low On-Resistance
- Ultra-Low  $Q_g$  and  $Q_{gd}$
- High-operating drain current
- Ultra-small footprint
  - 0.73 mm × 0.64 mm
- Ultra-low profile
  - 0.36-mm max height
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

## 2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

## 3 Description

This –12-V, 97-m $\Omega$ , P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.



Typical Part Dimensions

## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	–12	V
$Q_g$	Gate Charge Total (4.5 V)	0.95	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	0.068	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = -1.5\text{ V}$	230
		$V_{GS} = -1.8\text{ V}$	180
		$V_{GS} = -2.5\text{ V}$	129
		$V_{GS} = -4.5\text{ V}$	97
$V_{GS(th)}$	Threshold Voltage	–0.65	V

## Device Information<sup>(1)</sup>

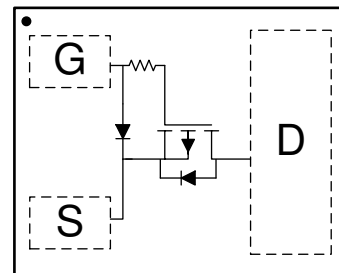
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD23280F3	3000	7-Inch Reel	Femto 0.73-mm × 0.64-mm Land Grid Array (LGA)	Tape and Reel
CSD23280F3T	250			

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	–12	V
$V_{GS}$	Gate-to-Source Voltage	–6	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	2.9	A
	Continuous Drain Current <sup>(2)</sup>	1.8	
$I_{DM}$	Pulsed Drain Current <sup>(1) (3)</sup>	11.4	A
$P_D$	Power Dissipation <sup>(1)</sup>	1.4	W
	Power Dissipation <sup>(2)</sup>	0.5	
$V_{(ESD)}$	Human-Body Model (HBM)	4000	V
	Charged-Device Model (CDM)	2000	
$T_J, T_{stg}$	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$

- (1) Typical  $R_{\theta JA} = 90^\circ\text{C/W}$  on 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB  
 (2) Typical  $R_{\theta JA} = 255^\circ\text{C/W}$  on min Cu board  
 (3) Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .



Top View



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>6 Device and Documentation Support</b> .....	<b>7</b>
<b>2 Applications</b> .....	<b>1</b>	6.1 Receiving Notification of Documentation Updates.....	7
<b>3 Description</b> .....	<b>1</b>	6.2 Trademarks.....	7
<b>4 Revision History</b> .....	<b>2</b>	<b>7 Mechanical, Packaging, and Orderable Information</b> ....	<b>8</b>
<b>5 Specifications</b> .....	<b>3</b>	7.1 Mechanical Dimensions.....	8
5.1 Electrical Characteristics.....	3	7.2 Recommended Minimum PCB Layout.....	9
5.2 Thermal Information.....	3	7.3 Recommended Stencil Pattern.....	9
5.3 Typical MOSFET Characteristics.....	4		

## 4 Revision History

### Changes from Revision A (August 2017) to Revision B (February 2022)

Page

• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....	1
• Added max Cu currents and power dissipation limits .....	1
• Added min Cu footnote .....	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	8
• Added FemtoFET Surface Mount Guide note.....	9

### Changes from Revision \* (April 2016) to Revision A (August 2017)

Page

• Added the <a href="#">Section 6.1</a> section in <a href="#">Section 6</a> .....	7
• Updated the <a href="#">Section 7.3</a> .....	9

## 5 Specifications

### 5.1 Electrical Characteristics

T<sub>A</sub> = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>DS</sub> = -250 μA	-12			V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -9.6 V			-50	nA
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -5 V			-25	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = -250 μA	-0.40	-0.65	-0.95	V
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = -1.5 V, I <sub>DS</sub> = -0.1 A		230	399	mΩ
		V <sub>GS</sub> = -1.8 V, I <sub>DS</sub> = -0.4 A		180	250	
		V <sub>GS</sub> = -2.5 V, I <sub>DS</sub> = -0.4 A		129	165	
		V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -0.4 A		97	116	
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = -1.2 V, I <sub>DS</sub> = -0.4 A		3		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -6 V, f = 1 MHz		180	234	pF
C <sub>oss</sub>	Output capacitance			73	95	pF
C <sub>rss</sub>	Reverse transfer Capacitance			8.5	11.1	pF
R <sub>G</sub>	Series gate resistance			9		Ω
Q <sub>g</sub>	Gate charge total (4.5 V)	V <sub>DS</sub> = -6 V, I <sub>DS</sub> = -0.4 A		0.95	1.23	nC
Q <sub>gd</sub>	Gate charge gate-to-drain			0.068		nC
Q <sub>gs</sub>	Gate charge gate-to-source			0.30		nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			0.15		nC
Q <sub>oss</sub>	Output charge		V <sub>DS</sub> = -6 V, V <sub>GS</sub> = 0 V		1.07	
t <sub>d(on)</sub>	Turnon delay time	V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -0.4 A, R <sub>G</sub> = 0 Ω		8		ns
t <sub>r</sub>	Rise time			4		ns
t <sub>d(off)</sub>	Turnoff delay time			21		ns
t <sub>f</sub>	Fall time			8		ns
<b>DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode forward voltage	I <sub>SD</sub> = -0.4 A, V <sub>GS</sub> = 0 V		-0.73	-1.0	V

### 5.2 Thermal Information

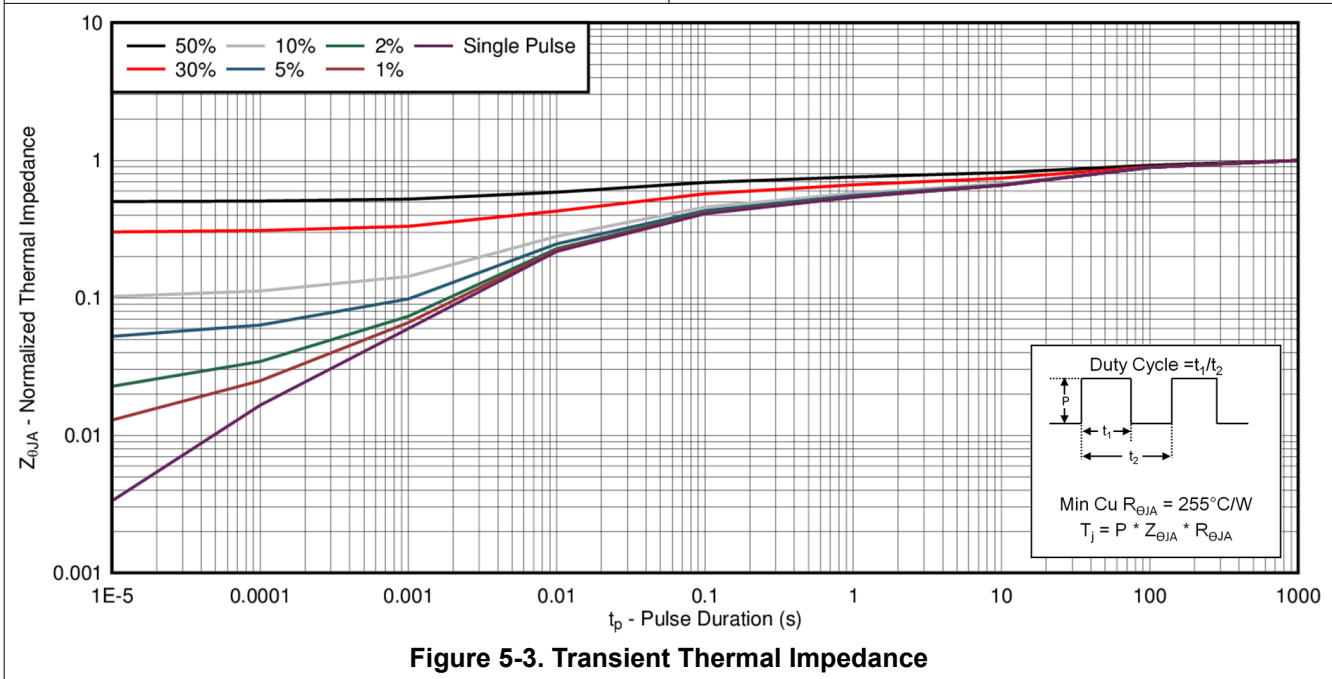
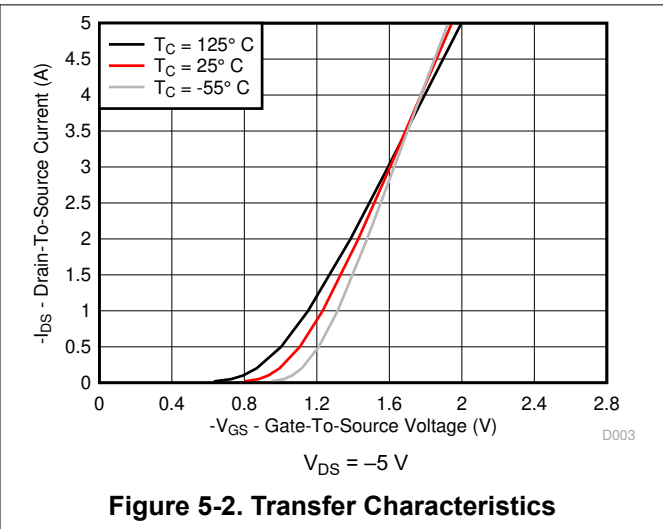
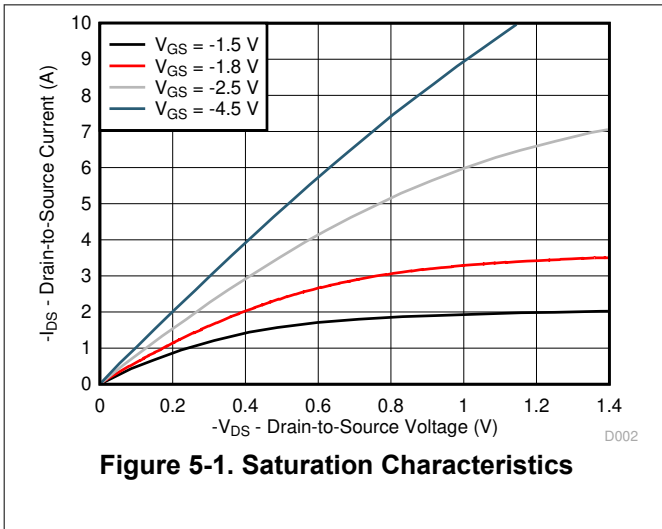
T<sub>A</sub> = 25°C (unless otherwise stated)

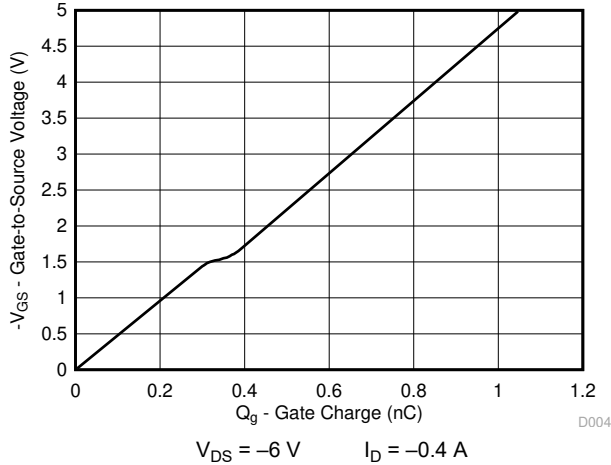
THERMAL METRIC		TYPICAL VALUES	UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	90	°C/W
	Junction-to-ambient thermal resistance <sup>(2)</sup>	255	

- (1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm) thick Cu.  
(2) Device mounted on FR4 material with minimum Cu mounting area.

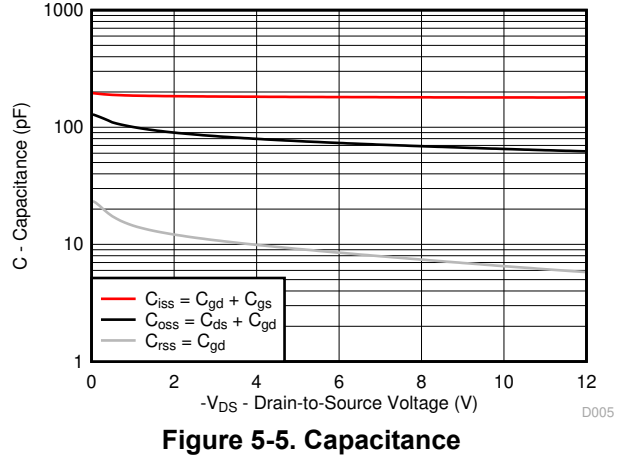
### 5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

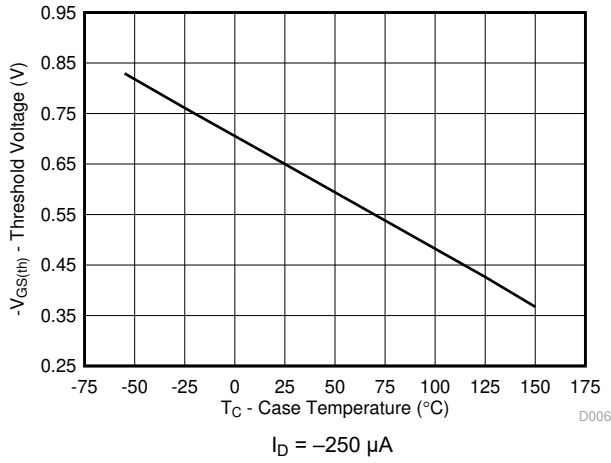




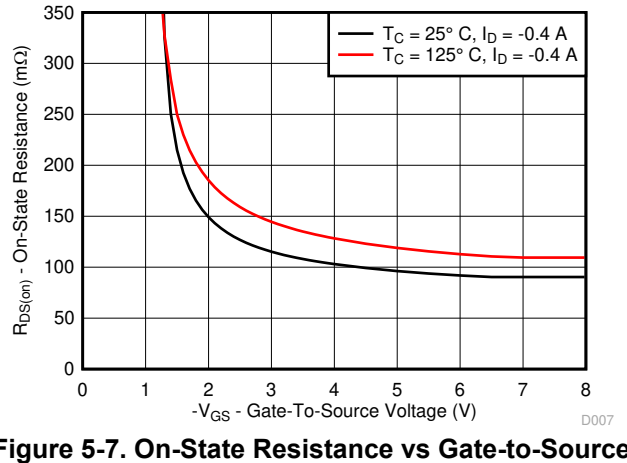
**Figure 5-4. Gate Charge**



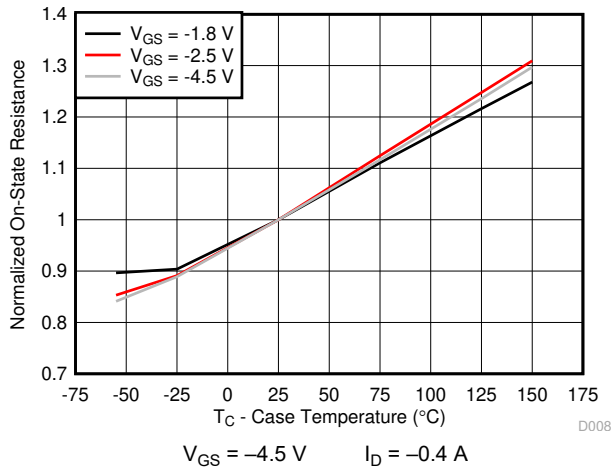
**Figure 5-5. Capacitance**



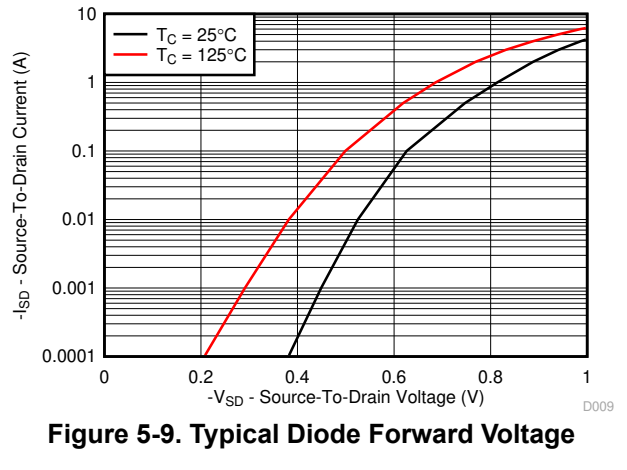
**Figure 5-6. Threshold Voltage vs Temperature**



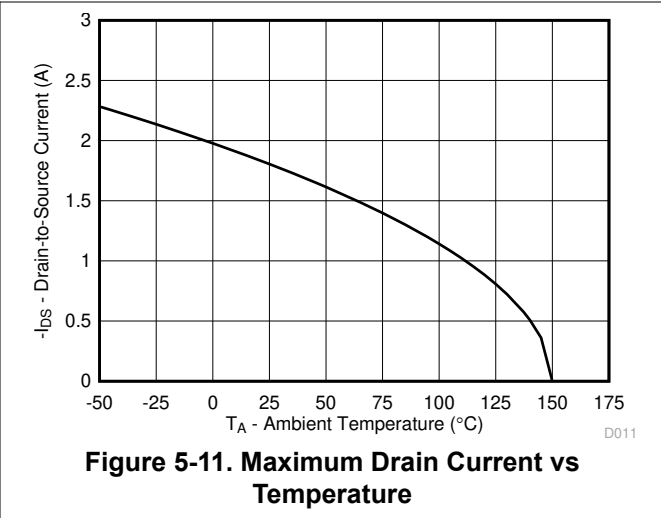
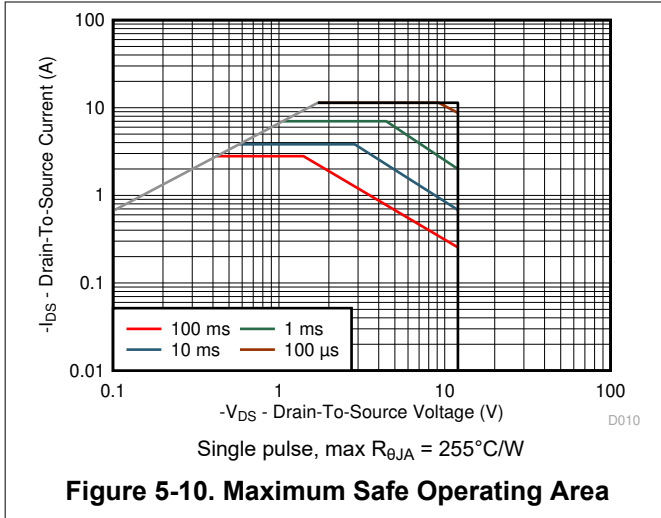
**Figure 5-7. On-State Resistance vs Gate-to-Source Voltage**



**Figure 5-8. Normalized On-State Resistance vs Temperature**



**Figure 5-9. Typical Diode Forward Voltage**



## **6 Device and Documentation Support**

### **6.1 Receiving Notification of Documentation Updates**

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

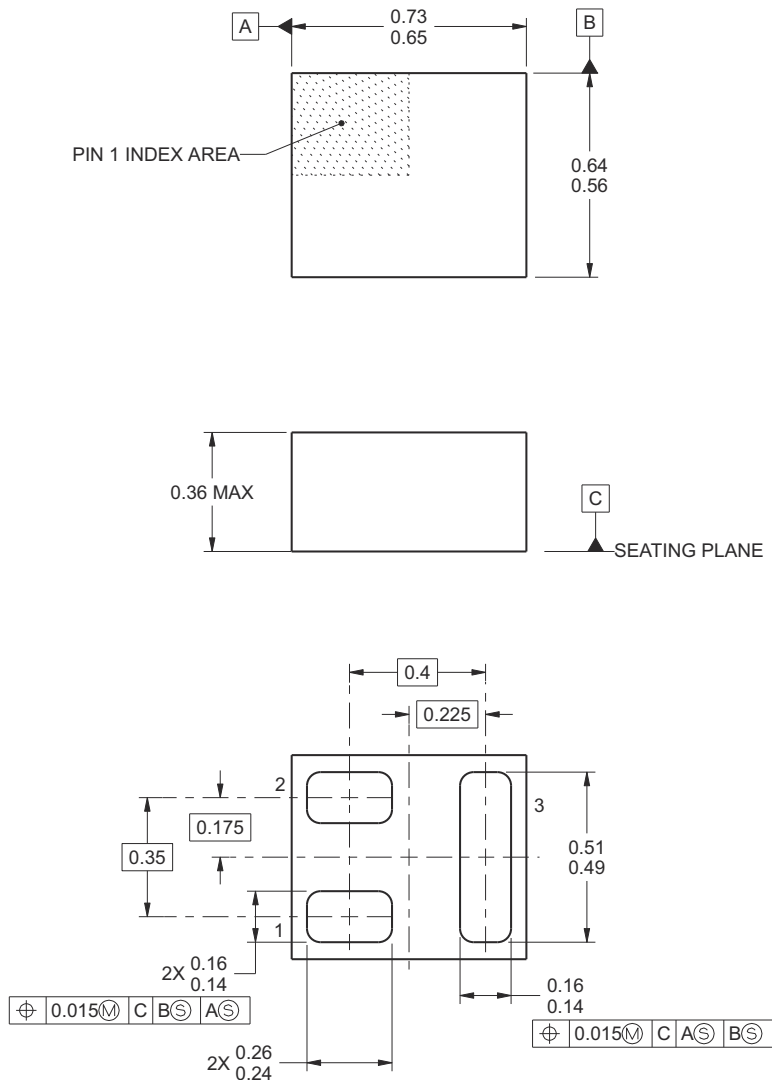
### **6.2 Trademarks**

FemtoFET™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Mechanical Dimensions



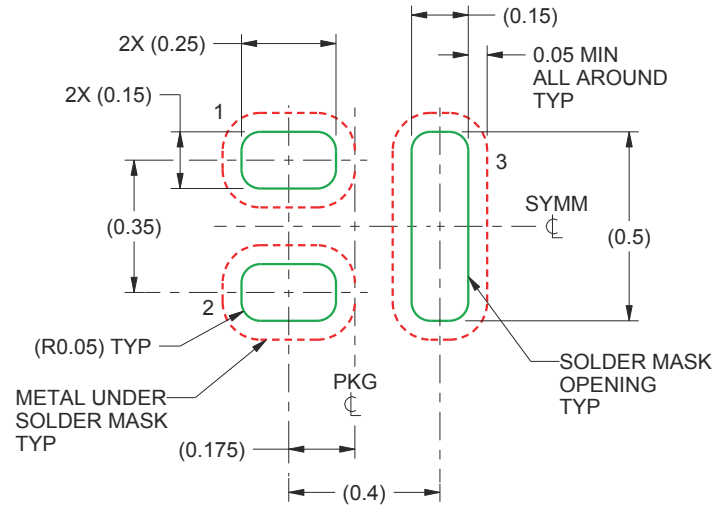
- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a lead-free solder land design.

**Table 7-1. Pin Configuration**

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

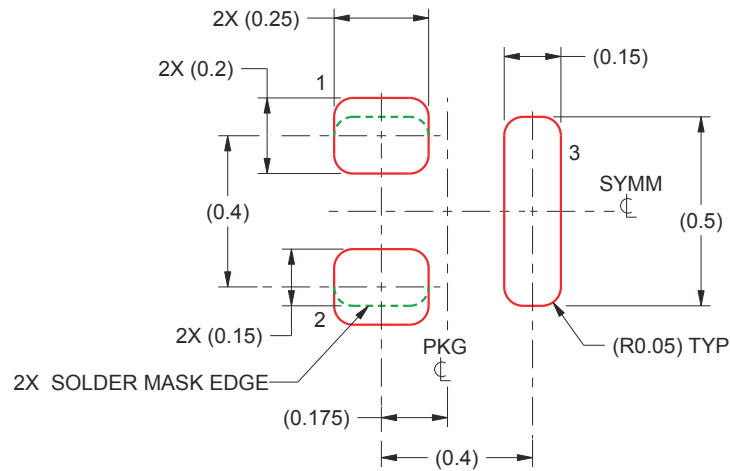


## 7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

## 7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23280F3	ACTIVE	PICOSTAR	YJM	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	5	<a href="#">Samples</a>
CSD23280F3T	ACTIVE	PICOSTAR	YJM	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	5	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD23280F3	PICOST AR	YJM	3	3000	178.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2
CSD23280F3	PICOST AR	YJM	3	3000	180.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2
CSD23280F3T	PICOST AR	YJM	3	250	180.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD23280F3	PICOSTAR	YJM	3	3000	220.0	220.0	35.0
CSD23280F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD23280F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated