

LVDS Single Port High Speed Repeater

FIN1101



SOIC8
CASE 751EB



US8
CASE 846AN

General Description

This single port repeater is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. It accepts and outputs LVDS levels with a typical differential output swing of 330 mV which provides low EMI at ultra low power dissipation even at high frequencies. It can directly accept multiple differential I/O including: LVPECL, HSTL, and SSTL-2 for translating directly to LVDS.

Features

- Up to 1.6 Gb/s Full Differential Path
- 3.5 ps Max Random Jitter and 135 ps Max Deterministic Jitter
- 3.3 V Power Supply Operation
- Wide Rail-To-Rail Common Mode Range
- Ultra Low Power Consumption
- LVDS Receiver Inputs Accept LVPECL, HSTL, and SSTL-2 Directly
- Power Off Protection
- 7 kV HBM ESD Protection (All Pins)
- Meets or Exceed the TA/EIA-644-A LVDS Standard
- Packaged in 8-Pin SOIC and US8
- Open Circuit Fail Safe Protection
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

PIN DESCRIPTIONS

| Pin Name | Description |
|-------------------|------------------------------|
| R _{IN+} | Non-Inverting LVDS Inputs |
| R _{IN-} | Inverting LVDS Inputs |
| D _{OUT+} | Non-Inverting Driver Outputs |
| D _{OUT-} | Inverting Driver Outputs |
| EN | Driver Enable Pin |
| V _{CC} | Power Supply |
| GND | Ground |

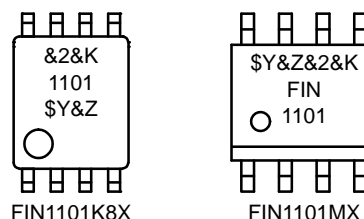
FUNCTION TABLE

| Inputs | | | Outputs | |
|--------|------------------|------------------|-------------------|-------------------|
| EN | R _{IN+} | R _{IN-} | D _{OUT+} | D _{OUT-} |
| H | H | L | H | L |
| H | L | H | L | H |
| H | Fail Safe Case | | H | L |
| L | X | X | Z | Z |

H = HIGH Logic Level
X = Don't Care

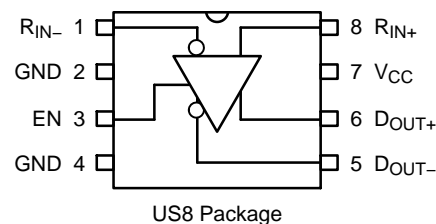
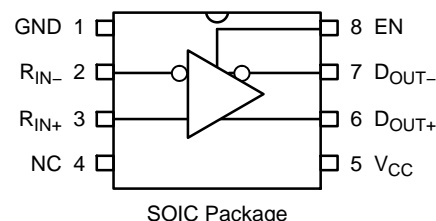
L = LOW Logic Level
Z = High Impedance

MARKING DIAGRAM

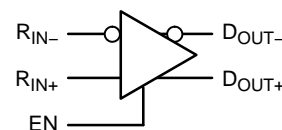


- \$Y = Logo
- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code
- &K = 2-Digits Lot Run Traceability Code
- 1101, FIN1101 = Specific Device Code

CONNECTION DIAGRAMS



FUNCTIONAL DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Rating |
|------------------|--|------------------|
| V _{CC} | Supply Voltage | -0.5 V to +4.6 V |
| V _{IN} | LVDS DC Input Voltage | -0.5 V to +4.6 V |
| V _{OUT} | LVDS DC Output Voltage | -0.5 V to +4.6 V |
| I _{OSD} | Driver Short Circuit Current | Continuous 10 mA |
| T _{STG} | Storage Temperature Range | -65°C to +150°C |
| T _J | Max Junction Temperature | 150°C |
| T _L | Lead Temperature (Soldering, 10 seconds) | 260°C |
| | ESD (Human Body Model) | 7000 V |
| | ESD (Machine Model) | 300 V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value |
|-----------------|---|--|
| V _{CC} | Supply Voltage | 3.0 V to 3.6 V |
| T _A | Operating Temperature | -40°C to +85°C |
| V _{ID} | Magnitude of Input Differential Voltage | 100 mV to V _{CC} |
| V _{IC} | Common Mode Input Voltage | (0 V + V _{ID} / 2) to (V _{CC} - V _{ID} / 2) |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Over supply voltage and operating temperature ranges, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ (Note 1) | Max | Unit |
|------------------|--|---|------------------------------|--------------|--|------|
| V _{TH} | Differential Input Threshold HIGH | See Figure 1; V _{IC} = +0.05 V, +1.2 V, or (V _{CC} - 0.05 V) | - | - | 100 | mV |
| V _{TL} | Differential Input Threshold LOW | See Figure 1; V _{IC} = +0.05 V, +1.2 V, or (V _{CC} - 0.05 V) | -100 | - | - | mV |
| V _{IH} | Input High Voltage (EN) | | 2.0 | - | V _{CC} | V |
| V _{IL} | Input Low Voltage (EN) | | GND | - | 0.8 | V |
| V _{OD} | Output Differential Voltage | R _L = 100 Ω, Driver Enabled, See Figure 2 | 250 | 330 | 450 | mV |
| ΔV _{OD} | V _{OD} Magnitude Change from Differential LOW-to-HIGH | R _L = 100 Ω, Driver Enabled, See Figure 2 | - | - | 25 | mV |
| V _{OS} | Offset Voltage | R _L = 100 Ω, Driver Enabled, See Figure 2 | 1.125 | 1.23 | 1.375 | V |
| ΔV _{OS} | Offset Magnitude Change from Differential LOW-to-HIGH | R _L = 100 Ω, Driver Enabled, See Figure 2 | - | - | 25 | mV |
| I _{OS} | Short Circuit Output Current | D _{OUT+} = 0 V & D _{OUT-} = 0 V, Driver Enabled | - | -3.4 | -6 | mA |
| I _{OS} | Short Circuit Output Current | V _{OD} = 0 V, Driver Enabled | - | ±3.4 | ±6 | mA |
| I _{IN} | Input Current (EN, D _{INX+} , D _{INX-}) | V _{IN} = 0 V to V _{CC} , Other Input = V _{CC} or 0 V (for Differential Inputs) | - | - | ±20 | μA |
| I _{OFF} | Power-Off Input or Output Current | V _{CC} = 0 V, V _{IN} or V _{OUT} = 0 V to 3.6 V | - | - | ±20 | μA |
| I _{CCZ} | Disabled Power Supply Current | Drivers Disabled | - | 3.2 | 5.5 | mA |
| I _{CC} | Power Supply Current | Drivers Enabled, Any Valid Input Condition | - | 9.3 | 13.5 | mA |
| I _{OZ} | Disabled Output Leakage Current | Driver Disabled, D _{OUT+} = 0 V to 3.6 V or D _{OUT-} = 0 V to 3.6 V | - | - | ±20 | μA |
| V _{IC} | Common Mode Voltage Range | V _{ID} = 100 mV to V _{CC} | 0 V + V _{ID} / 2 | - | V _{CC} - (V _{ID} / 2) | V |
| C _{IN} | Input Capacitance | EN Input | - | 2.2 | - | pF |
| | | Data Input | - | 2.0 | - | pF |
| C _{OUT} | Output Capacitance | | - | 2.6 | - | pF |

1. All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

AC ELECTRICAL CHARACTERISTICS (Over supply voltage and operating temperature ranges, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min | Typ (Note 2) | Max | Unit |
|---------------------|---|--|------|--------------|------|------|
| t _{PLHD} | Differential Propagation Delay LOW-to-HIGH | R _L = 100 Ω, C _L = 5 pF, V _{ID} = 200 mV to 450 mV, V _{IC} = V _{ID} / 2 to (V _{CC} - (V _{ID} / 2)), Duty Cycle = 50%, See Figure 3 and Figure 4 | 0.75 | 1.1 | 1.75 | ns |
| t _{PHLD} | Differential Propagation Delay HIGH-to-LOW | | 0.75 | 1.1 | 1.75 | ns |
| t _{TLHD} | Differential Output Rise Time (20% to 80%) | | 0.29 | 0.40 | 0.58 | ns |
| t _{THLD} | Differential Output Fall Time (80% to 20%) | | 0.29 | 0.40 | 0.58 | ns |
| t _{SK(P)} | Pulse Skew t _{PLH} - t _{PHL} | | - | 0.01 | 0.2 | ns |
| t _{SK(PP)} | Part-to-Part Skew (Note 3) | | - | - | 0.5 | ns |
| f _{MAX} | Maximum Frequency (Note 4) (Note 5) | | 400 | 800 | - | MHz |
| t _{pZHD} | Differential Output Enable Time from Z to HIGH | R _L = 100 Ω, C _L = 5 pF, See Figure 2 and Figure 3 | - | 2.1 | 5 | ns |
| t _{pZLD} | Differential Output Enable Time from Z to LOW | | - | 2.3 | 5 | ns |
| t _{pHZD} | Differential Output Disable Time from HIGH to Z | | - | 1.5 | 5 | ns |
| t _{pLZD} | Differential Output Disable Time from LOW to Z | | - | 1.8 | 5 | ns |
| t _{DJ} | LVDS Data Jitter, Deterministic | V _{ID} = 300 mV, PRBS = 2 ²³ - 1, V _{IC} = 1.2 V at 800 Mbps | - | 85 | 135 | ps |
| t _{RJ} | LVDS Clock Jitter, Random (RMS) | V _{ID} = 300 mV V _{IC} = 1.2 V at 400 MHz | - | 2.1 | 3.5 | ps |

2. All typical values are at T_A = 25°C and with V_{CC} = 3.3 V, V_{ID} = 300 mV, V_{IC} = 1.2 V unless otherwise specified.
3. t_{SK(PP)} is the magnitude of the difference in differential propagation delay times between identical channels of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.
4. Passing criteria for maximum frequency is the output V_{OD} > 200 mV and the duty cycle is 45% to 55% with all channels switching.
5. Output loading is transmission line environment only; C_L is < 1 pF of stray test fixture capacitance.

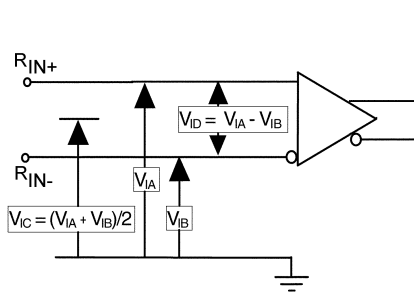


Figure 1. Differential Receiver Voltage Definitions and Propagation I and Transition Time Test Circuit

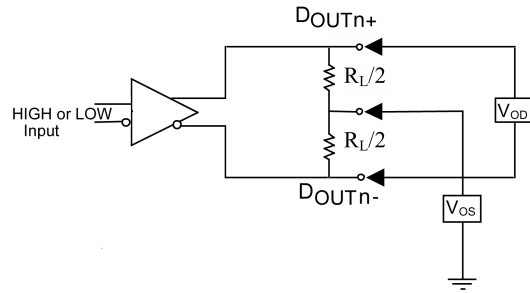
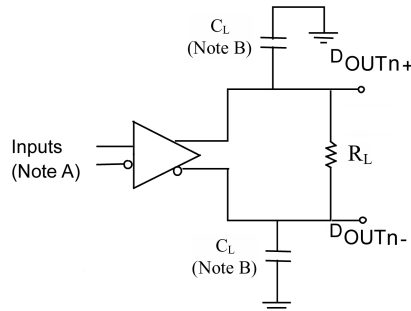


Figure 2. Differential Driver DC Test Circuit



Note A: All LVDS input pulses have frequency = 10 MHz, t_R or t_F ≤ 0.5 ns
 Note B: C_L includes all probe and test fixture capacitances

Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit

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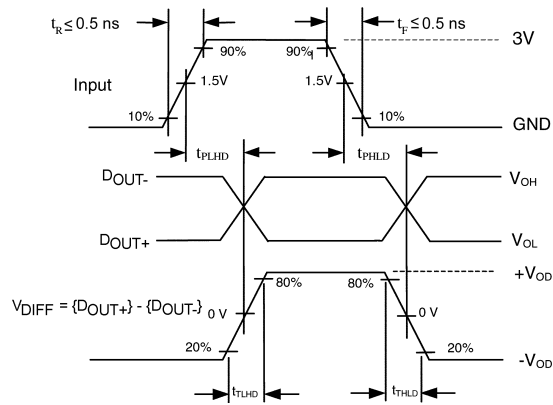
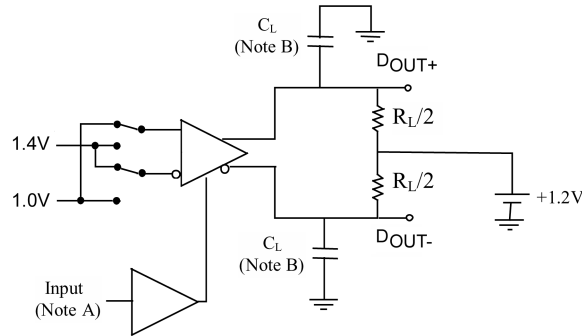


Figure 4. AC Waveforms



Note A: All LVTTTL input pulses have frequency = 10 MHz, t_R or $t_F \leq 2$ ns
 Note B: C_L includes all probe and test fixture capacitances

Figure 5. Differential Driver Enable and Disable Test Circuit

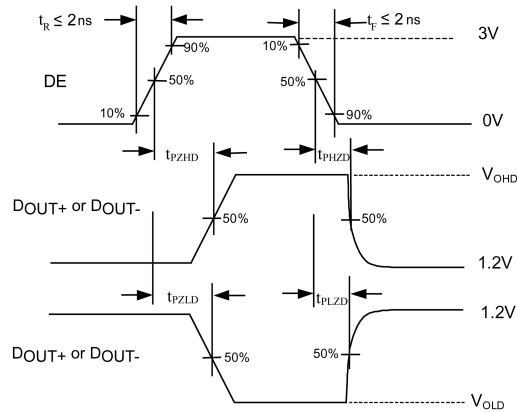


Figure 6. Enable and Disable AC Waveforms

ORDERING INFORMATION

| Order Number | Package Number | Package Description | Shipping† |
|--------------|----------------|---|--------------------|
| FIN1101MX | M08A | 8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow (Pb-Free) | 2500 / Tape & Reel |
| FIN1101K8X | MAB08A | 8-Lead US8, JEDEC MO-187, Variation CA 3.1 mm Wide (Pb-Free) | 3000 / Tape & Reel |

†For Information On Tape And Reel Specifications, Including Part Orientation And Tape Sizes, Please Refer To Our Tape And Reel Packaging Specifications Brochure, Brd8011/D.

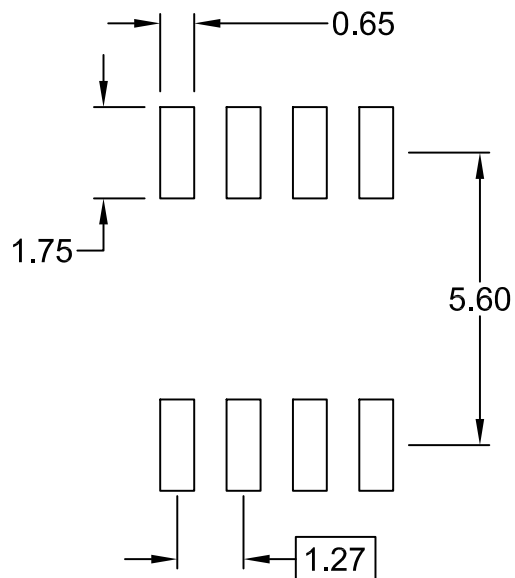
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

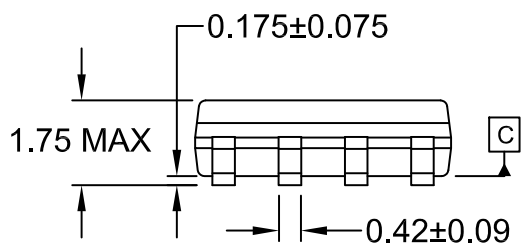


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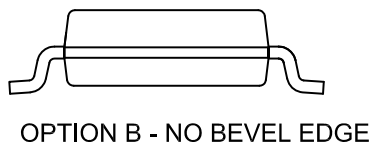
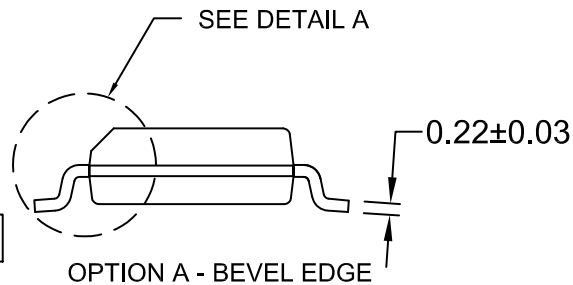
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⊕ 0.25 (M) C B A



⌒ 0.10



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

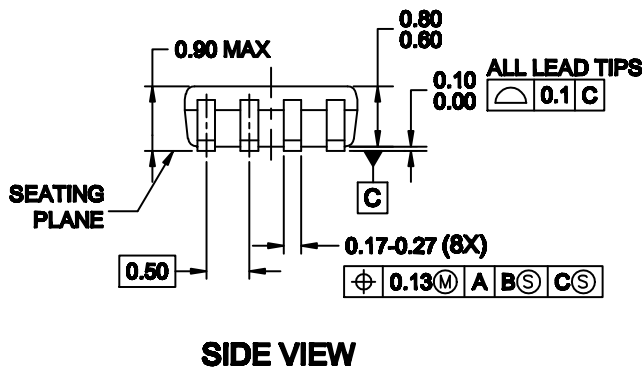
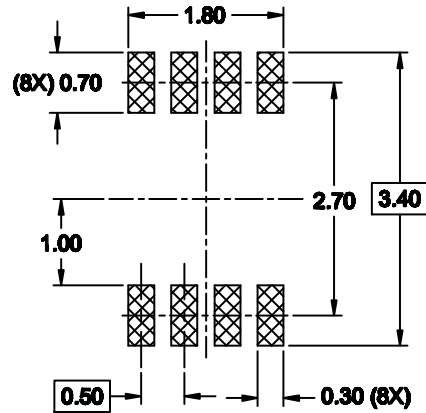
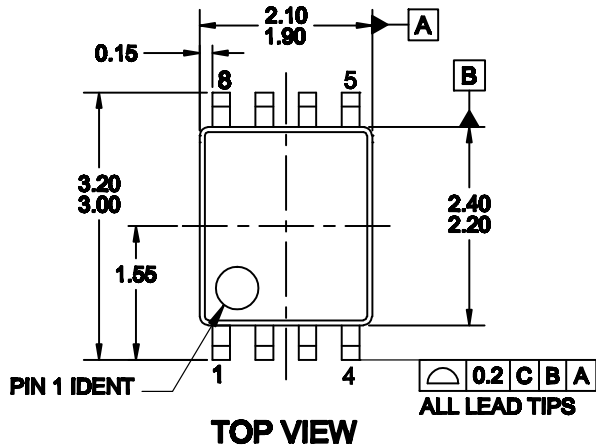
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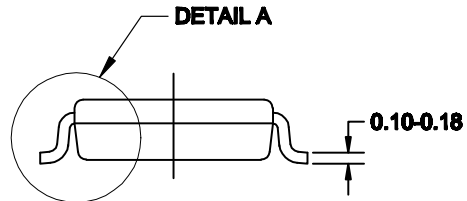
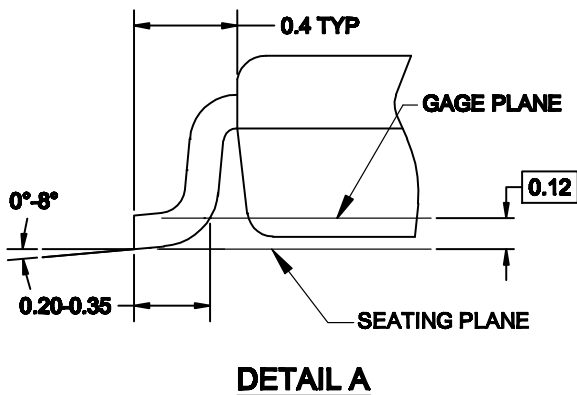
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NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.



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