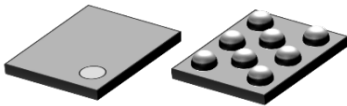


400 mA nano-quiescent synchronous step-down converter with digital voltage selection and Power Good



Flip-Chip8 (1.14x1.44 mm)

Features

- 500 nA input quiescent current at $V_{IN}=3.6$ V (not switching)
- 94% typical efficiency at 1 mA load ($V_{IN}=3.6$ V, $V_{OUT}=3.3$ V)
- 100% duty cycle
- 1.8 V to 5.5 V input operating range
- Undervoltage lockout: 1.57 V (V_{IN} falling, typ.)
- Up to 400 mA output current capability
- Low power control operation for the best efficiency
- Embedded soft-start circuit
- Tiny external components: $L=2.2$ μ H typ.
- Selectable output voltages: 1.8 V to 3.3 V
- Output voltage Power Good
- $\pm 1.5\%$ output voltage accuracy (V_{OUT} , $T_A=25$ °C)
- Dynamic output voltage selection (D0, D1)
- Available in Flip-Chip package

Applications

- Wearable applications
- Personal tracking monitors
- Smart watches, sport bands
- Energy harvesting, wireless sensors
- Wearable and fitness accessories
- Industrial sensors, portable low power devices
- Single cell Li-Ion battery applications
- Bluetooth® low energy
- Zigbee

Description

The **ST1PS01** is a nano-quiescent miniaturized synchronous step-down converter, which is able to provide up to 400 mA output current with an input voltage ranging from 1.8 V to 5.5 V. This converter is specifically designed for applications where high efficiency, PCB size and thickness are the key factors. The output voltage can be set using two digital control inputs, a V_{OUT} from 1.8 V to 3.3 V can be dynamically selected. Thanks to the enhanced PCC (peak current control) the **ST1PS01** reaches very high efficiency conversion using just a 2.2 μ H inductor and two small capacitors. Advanced design circuitry is implemented to minimize the quiescent current. The device is available in Flip-Chip package.

| Product status link | |
|-------------------------|---|
| ST1PS01 | |
| Product summary | |
| Order code | ST1PS01AJR |
| | ST1PS01DJR |
| | ST1PS01EJR |
| Output voltages | 1.9 V, 2.0 V, 2.1 V, 2.8 V (A vers.) |
| | 1.8 V, 2.3 V, 2.5 V, 2.8 V (D vers.) |
| | 1.8 V, 2.7 V, 3.0 V, 3.3 V (E vers.) |
| Package | Flip-Chip (1.11x1.41mm) 400 μ m pitch |

1 Application schematic

Figure 1. ST1PS01 application schematic

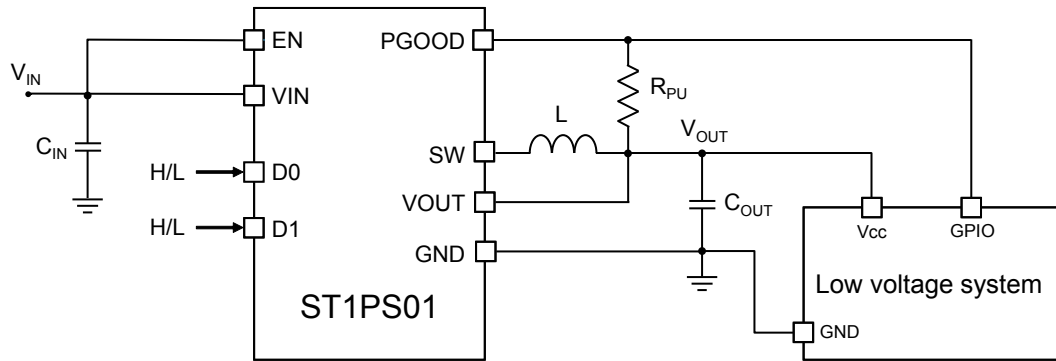


Table 1. Typical external components

| Component | Description | Value | Size - imperial (metric) |
|-----------|---------------------------------------|--------------|--------------------------|
| C_{IN} | Ceramic capacitor with low ESR values | 10 μ F | 0603 (1608) |
| C_{OUT} | Ceramic capacitor with low ESR values | 10 μ F | 0603 (1608) |
| L | Inductor | 2.2 μ H | 0806 (2016) |
| R_{PU} | Pull-up resistor | 1 M Ω | 0402 (1005) |

2 Pin configuration (top through view)

Figure 2. Flip-Chip8 package

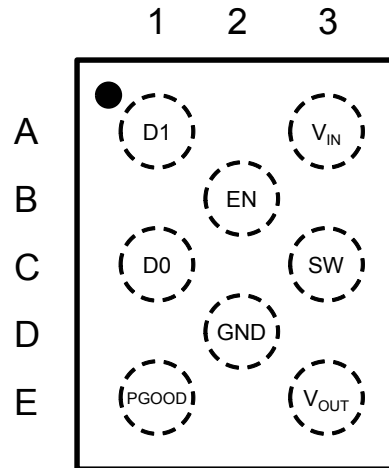


Table 2. Pin description

| Name | Bump name | Description |
|------------------|-----------|--|
| V _{IN} | A3 | Input supply voltage. Bypass this pin to ground with a 10 μF capacitor |
| SW | C3 | Switching node. Inductor connection |
| V _{OUT} | E3 | Sense pin used to monitor output voltage |
| EN | B2 | Enable pin. High logic level turns on the IC. V _{IN} referred |
| GND | D2 | Ground |
| D1 | A1 | Output voltage selection inputs (Refer to the Table 7. Output voltage settings for order codes and configuration matrix) |
| D0 | C1 | |
| PGOOD | E1 | Open drain output. It is in high impedance when the output voltage reaches 97.5% of the target V _{OUT} |

3 Functional pin description

GND

Device ground pin.

VIN

Supply voltage. This pin supplies power to the internal analog and digital circuitries when voltage is higher than V_{UVLO} . Bypass this pin to GND with a 10 μ F ceramic capacitor. Input capacitor C_{IN} must be chosen with low ESR to reduce the input voltage ripple.

SW

Inductor connection to internal PMOS and NMOS switches.

VOUT

Output voltage sense input. It provides the feedback voltage level to the regulation circuitry. 10 μ F output capacitor C_{OUT} must be connected close to the pin or through a short trace and should have low ESR to reduce the output voltage ripple.

EN

Enable pin. A logic low level on this pin disables the device. High level enables the device. Do not leave this pin floating.

D1, D2

Output voltage selection pins. See the [Table 7. Output voltage settings](#) for V_{OUT} selection. Do not leave these pins floating. These pins can be dynamically changed during operation.

PGOOD

Power Good open drain output. If used it requires a pull-up resistor to hold a high level signal. High impedance indicates that V_{OUT} is above proper good threshold.

4 Maximum ratings

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------------------|------|
| V_{IN} | Power and signal supply voltage | - 0.3 to + 6.5 | V |
| EN, D0, D1 | Logic input pins | - 0.3 to + 6.5 | V |
| V_{OUT} , SW | Output signal monitoring and switching pins | -0.3 to $V_{IN} + 0.3$ | V |
| PGOOD | Power Good open drain output pin | - 0.3 to + 6.5 | V |
| T_{AMB} | Operating ambient temperature | -40 to 85 | °C |
| T_J | Junction temperature | -40 to 125 | °C |
| T_{STG} | Storage temperature | -55 to 150 | °C |

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4. Thermal data

| Symbol | Parameter | Flip-Chip8 | Unit |
|------------|-------------------------------------|------------|------|
| R_{thJA} | Thermal resistance junction-ambient | 60 | °C/W |

Table 5. Recommended operating conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------|----------------------|------|------|------|------|
| V_{IN} | Input supply voltage | 1.8 | | 5.5 | V |

5 Electrical characteristics

$C_{IN}= 10 \mu\text{F}$, $C_{OUT}= 10 \mu\text{F}$, $L=2.2 \mu\text{H}$, $V_{IN}=3.6 \text{ V}$, $V_{EN}= V_{IN}$, $V_{OUT}=1.8 \text{ V}$, $T_A=25 \text{ }^\circ\text{C}$ unless otherwise specified.

Table 6. Electrical characteristics

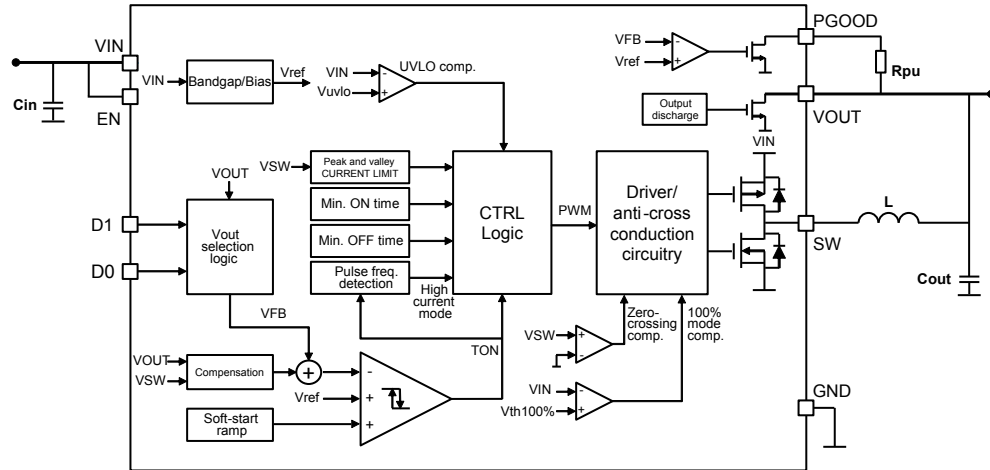
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------------|---|---|------|-------|------|----------|
| General section | | | | | | |
| I_Q | Quiescent current | $V_{IN}=V_{IN}$, $I_{OUT}=0 \mu\text{A}$, $V_{OUT}=1.8 \text{ V}$, device does not switch, $V_{IN}=2.5 \text{ V}$ to 5.5 V | | 500 | 1000 | nA |
| I_{SD} | Shutdown current | $V_{IN}=GND$, shutdown current into V_{IN} | | 10 | 200 | nA |
| V_{UVLO} | Undervoltage lockout threshold | V_{IN} rising | | 1.63 | 1.72 | V |
| | | V_{IN} falling | 1.51 | 1.57 | | V |
| | | Hysteresis | | 65 | | mV |
| $V_{th100\%+}$ | 100% mode leave threshold | V_{IN} rising, 100% mode is disabled with $V_{IN} = V_{OUTnom} + V_{th100\%+}$ | | 300 | | mV |
| $V_{th100\%-}$ | 100% mode enter threshold | V_{IN} falling, 100% mode is entered with $V_{IN} = V_{OUTnom} + V_{th100\%-}$ | | 200 | | |
| Output voltage | | | | | | |
| V_{OUT} | Output voltage range | Output voltages are selected with pins D0, D1 | 1.8 | | 3.3 | V |
| | Output voltage accuracy | $V_{IN} = 3.6 \text{ V}$, whole V_{OUT} range, $I_{OUT}=100 \text{ mA}$ | -1.5 | | 1.5 | % |
| t_{ONmin} | Minimum on-time | $V_{IN} = 3.6 \text{ V}$, $V_{OUT}= 2 \text{ V}$, $I_{OUT}= 0 \text{ mA}$ | | 200 | | ns |
| t_{OFFmin} | Minimum off-time | $V_{IN}=2.3\text{V}$ | | 50 | | ns |
| $t_{startupd}$ | Start-up delay time | V_{EN} from low to high, $V_{IN} = 3.6 \text{ V}$, $V_{OUT} = 1.8 \text{ V}$ | 0.5 | | 4 | ms |
| R_{OUTDIS} | Output discharge MOSFET on-resistance | $V_{EN}= GND$ | | 30 | | Ω |
| Logic inputs (EN, D0, D1) | | | | | | |
| V_{IL} | Low level input voltage threshold | $V_{IN}=1.8 \text{ V}$ to 5.5 V | | | 0.3 | V |
| V_{IH} | High level input voltage threshold | | 1 | | | |
| Power switch | | | | | | |
| $R_{DS(on)}$ | High-side MOSFET on-resistance | $V_{IN} = 3.6 \text{ V}$, $I_{sw} = 400 \text{ mA}$ | | 0.38 | 0.45 | Ω |
| | Low-side MOSFET on-resistance | | | 0.14 | 0.2 | |
| I_{LIM1} | High-side MOSFET switch current limit | $1.8 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$ | 580 | 700 | 820 | mA |
| | Low-side MOSFET switch current limit | | | 500 | | |
| I_{LIMSS} | High-side MOSFET switch current limit during soft-start | Reduced switch current limit during soft-start period (typ. $400 \mu\text{s}$) | 200 | 280 | 360 | |
| Power Good output (PGOOD) | | | | | | |
| V_{thpg-} | Power Good threshold voltage | Rising output voltage on V_{OUT} pin, referred to V_{OUT} selected (D0, D1) | 95 | 97.5 | | % |
| V_{thpgH} | | Hysteresis. To see plot for temperature variation | -6 | -4.25 | -2.5 | |
| V_{OL} | Low level output voltage | $1.8 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$, $V_{EN} = GND$, current into PGOOD pin, $I_{PGOOD} = 4 \text{ mA}$ | | | 0.23 | V |

Table 7. Output voltage settings

| Device | D1 | D0 | V _{OUT} |
|------------|----|----|------------------|
| ST1PS01AJR | 0 | 0 | 1.9 V |
| | 0 | 1 | 2.0 V |
| | 1 | 0 | 2.1 V |
| | 1 | 1 | 2.8 V |
| ST1PS01DJR | 0 | 0 | 1.8 V |
| | 0 | 1 | 2.3 V |
| | 1 | 0 | 2.5 V |
| | 1 | 1 | 2.8 V |
| ST1PS01EJR | 0 | 0 | 1.8 V |
| | 0 | 1 | 2.7 V |
| | 1 | 0 | 3.0 V |
| | 1 | 1 | 3.3 V |

6 ST1PS01 block diagram

Figure 3. Block diagram



7 Operation description

The ST1PS01 is an ultra-low quiescent new generation buck converter. It targets a very small quiescent current consumption (typical 500 nA) and it guarantees high efficiency operation even down to few microampere loads. It is based on a hysteretic comparator that senses the coil ripple current that is always held constant in all operation modes. The device has seamless transition between PFM (pulse frequency modulation) and PWM (pulse width modulation) mode with low ripple and good load transient response. In order to maintain constant ripple current on the selected coil, the device changes switching frequency, which also depends on input supply voltage. During PWM mode (heavy load), the device operates in continuous conduction up to 400 mA and switching frequency can reach 2 MHz maximum.

7.1 Power save mode

At light load the device enters automatically power save mode with total current consumption from the input power supply of 500 nA typical; during this condition most of the internal blocks are turned off in order to reach ultra-low power consumption. During this time, the load current is supported by the output capacitor.

7.2 Output voltage

The device allows output voltage selection without external resistor divider. A couple of standard digital inputs are used to configure the device to supply a fixed output voltage according to [Table 7. Output voltage settings](#). The V_{OUT} pin **must be connected directly and as close as possible to the inductor terminal** to obtain the best performance and get the best output voltage regulation. The output voltage can be dynamically changed to implement voltage scaling.

7.3 Output discharge and UVLO

The device embeds a fast output discharge circuitry active when the enable pin is held to ground (EN=gnd) or when the input supply voltage reaches the minimum voltage level set by the UVLO protection circuit (undervoltage lock-out protection circuit). The UVLO rising threshold at 1.63 V (typ.) guarantees a proper device supply voltage operation.

7.4 Soft-start and current limitation

The device embeds a fixed soft-start circuit active during a limited time period (few ms). This feature allows the inrush current to be minimized from the power supply in case of weak source. During this period internal circuit reduces to 280 mA the typical switch current limit.

7.5 100% duty cycle operation

The device enters 100% duty cycle operation if the input voltage comes close to the selected output voltage. During this mode, the regulator is turned off and output pin is directly connected to the input pin through the high-side MOSFET. The output voltage follows the input level minus the voltage drop across the internal MOSFET and the inductor. Once the input voltage exceeds the 100% duty cycle leave threshold, the device restarts to switch and regulates the selected output voltage again.

7.6 Power Good flag

The Power Good comparator monitors the selected V_{OUT} voltage. The Power Good open drain output is in high impedance when the V_{OUT} reaches the correct voltage level while it switches to low level when V_{OUT} falls below the normal voltage level.

8 Typical performance characteristics

Figure 4. Efficiency vs load, $V_{OUT} = 1.8\text{ V}$

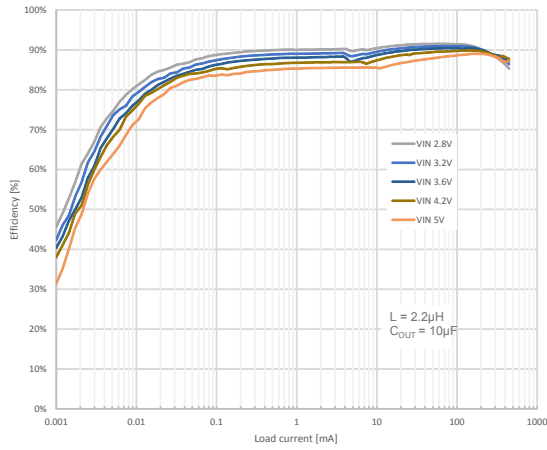


Figure 5. Efficiency vs V_{IN} , $V_{OUT} = 1.8\text{ V}$

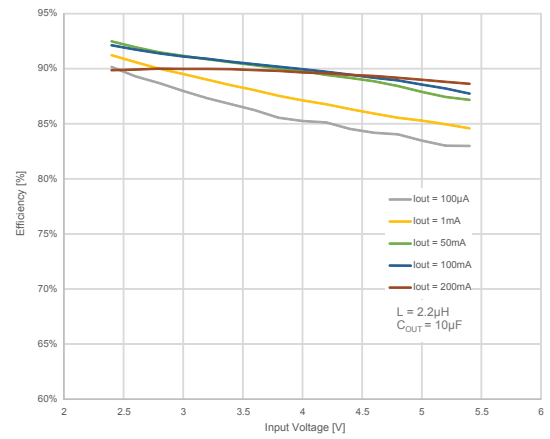


Figure 6. Efficiency vs load, $V_{OUT} = 3.3\text{ V}$

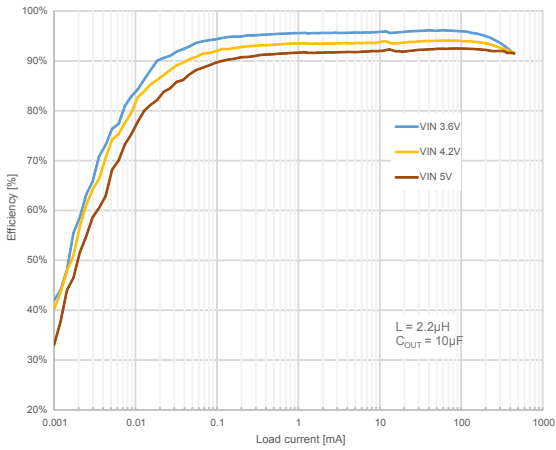


Figure 7. Efficiency vs V_{IN} , $V_{OUT} = 3.3\text{ V}$

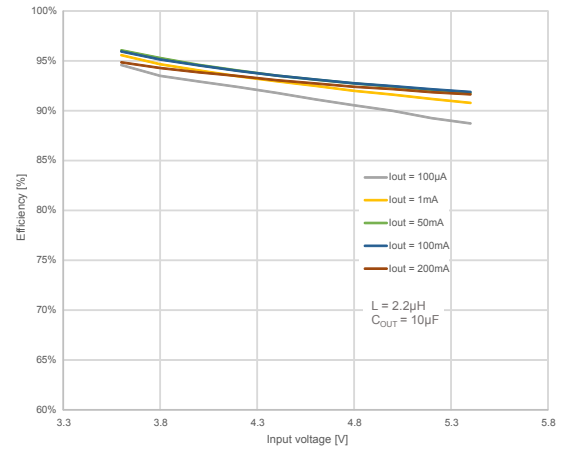


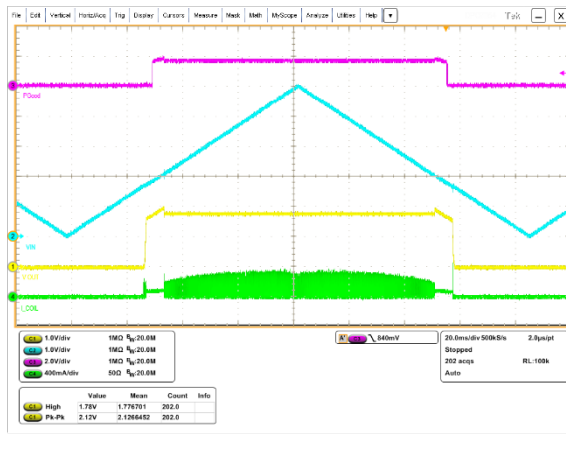
Figure 8. 100% mode, $V_{OUT} = 1.8\text{ V}$

Figure 9. 100% mode, $V_{OUT} = 3.0\text{ V}$

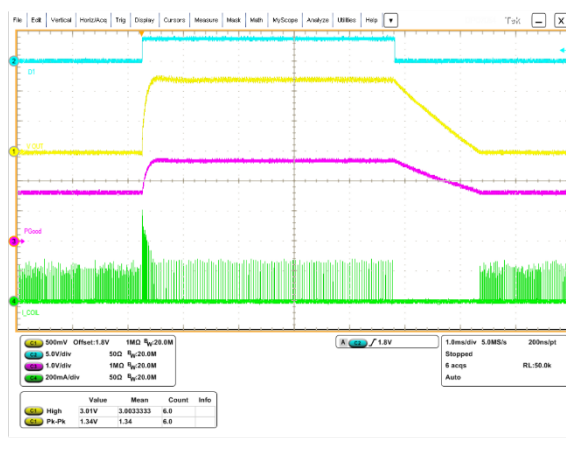
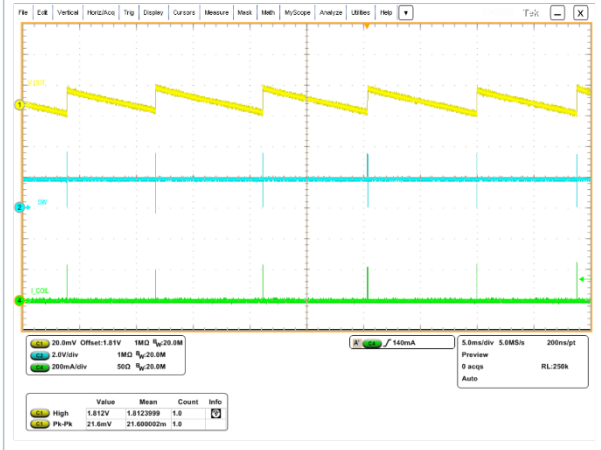
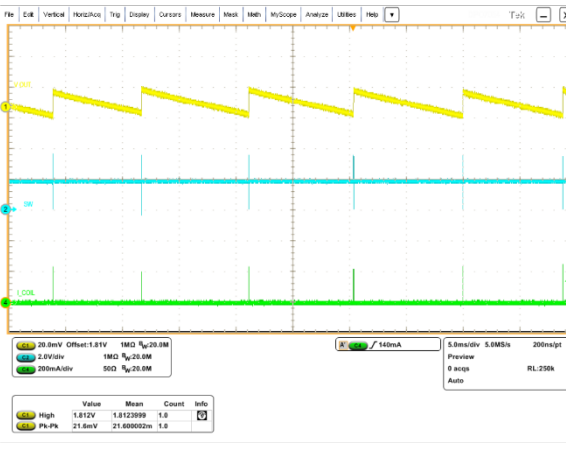
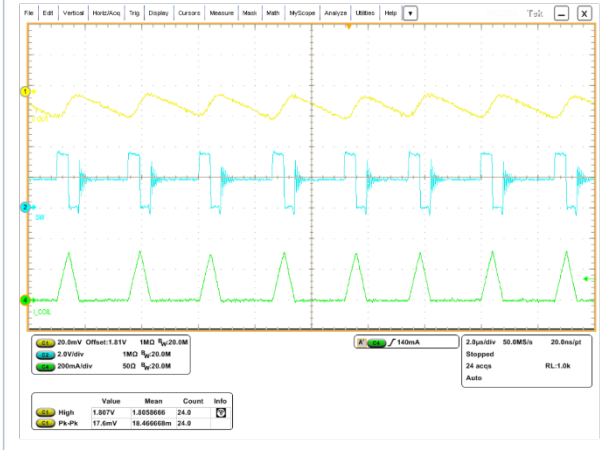
Figure 10. V_{OUT} change, 1.8 V to 3.3 V to 1.8 V, $I_{OUT}=5\text{ mA}$

Figure 11. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=10\text{ }\mu\text{A}$

Figure 12. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=10\text{ mA}$

Figure 13. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=50\text{ mA}$


Figure 14. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=150\text{ mA}$

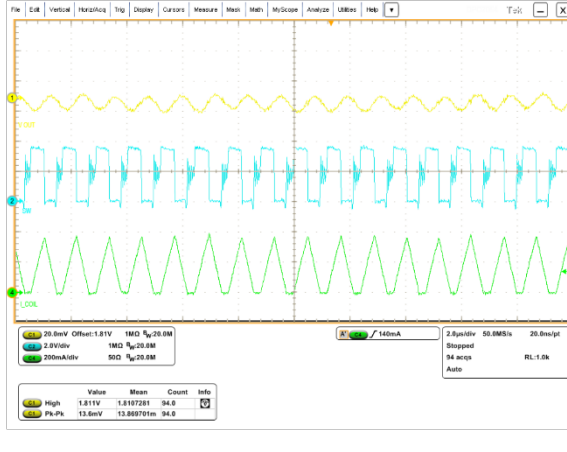


Figure 15. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=250\text{ mA}$

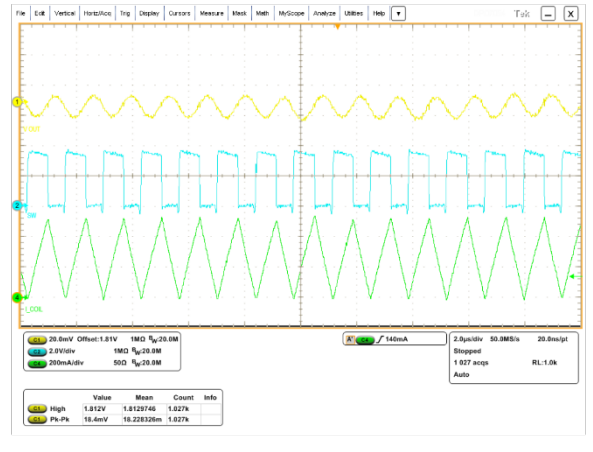


Figure 16. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, no load

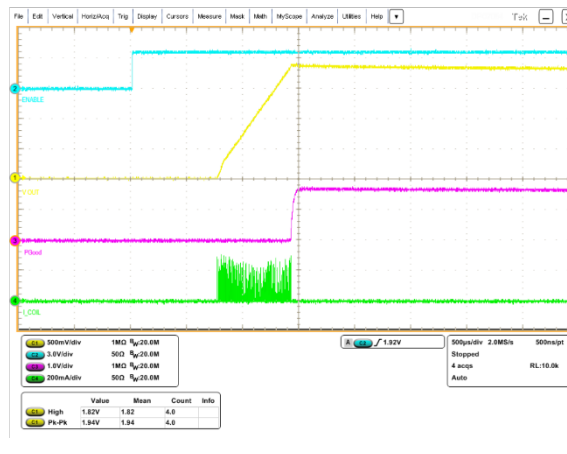


Figure 17. Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, no load

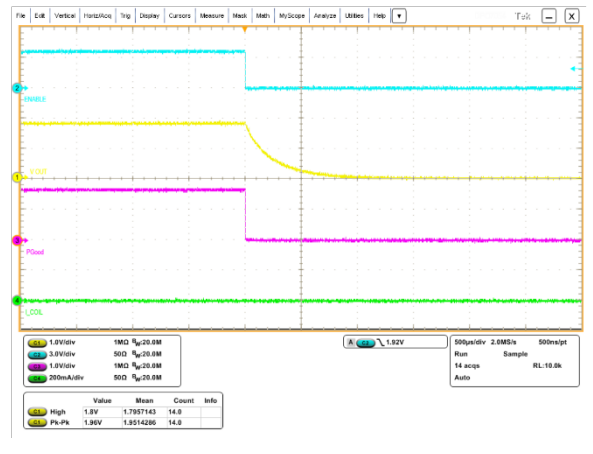


Figure 18. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=100\text{ mA}$

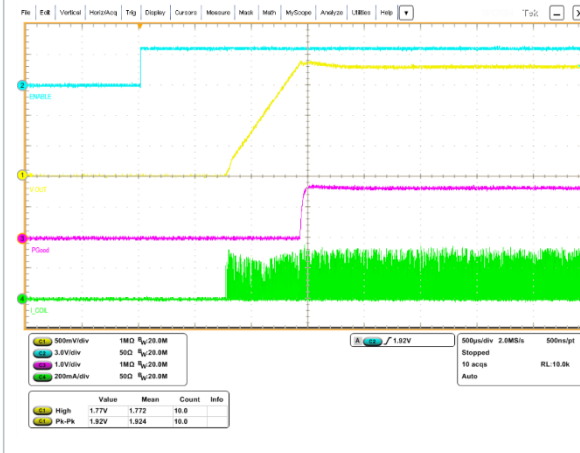
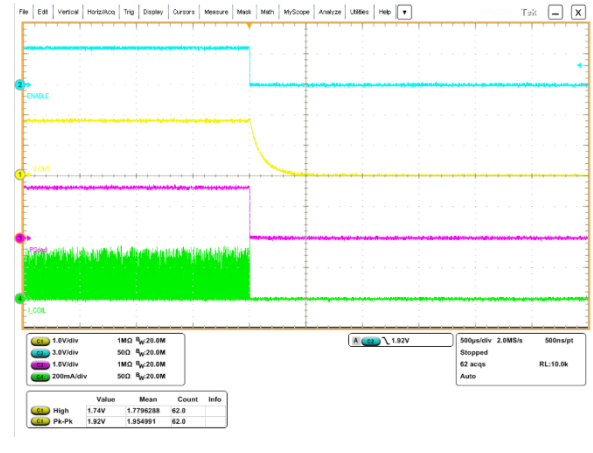


Figure 19. Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=100\text{ mA}$



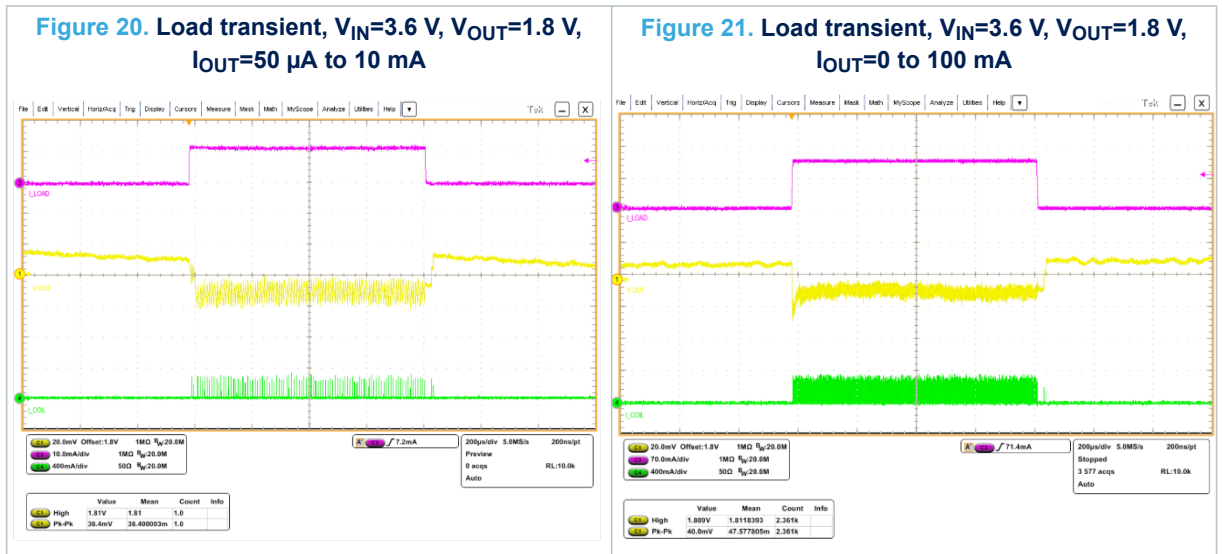
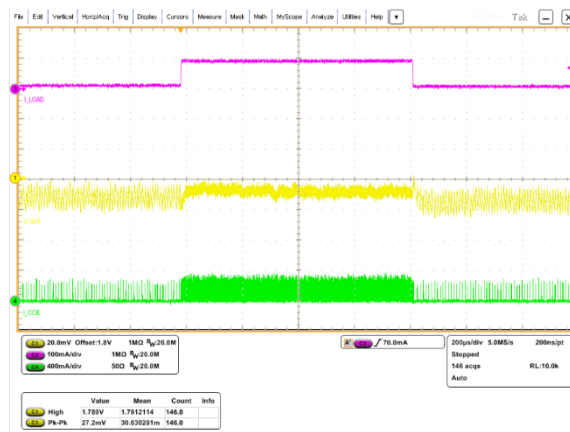


Figure 22. Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=10$ to 100 mA



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Flip-Chip 8 (1.14x1.44 mm) package information

Figure 23. Flip-Chip 8 (1.14x1.44 mm) package outline

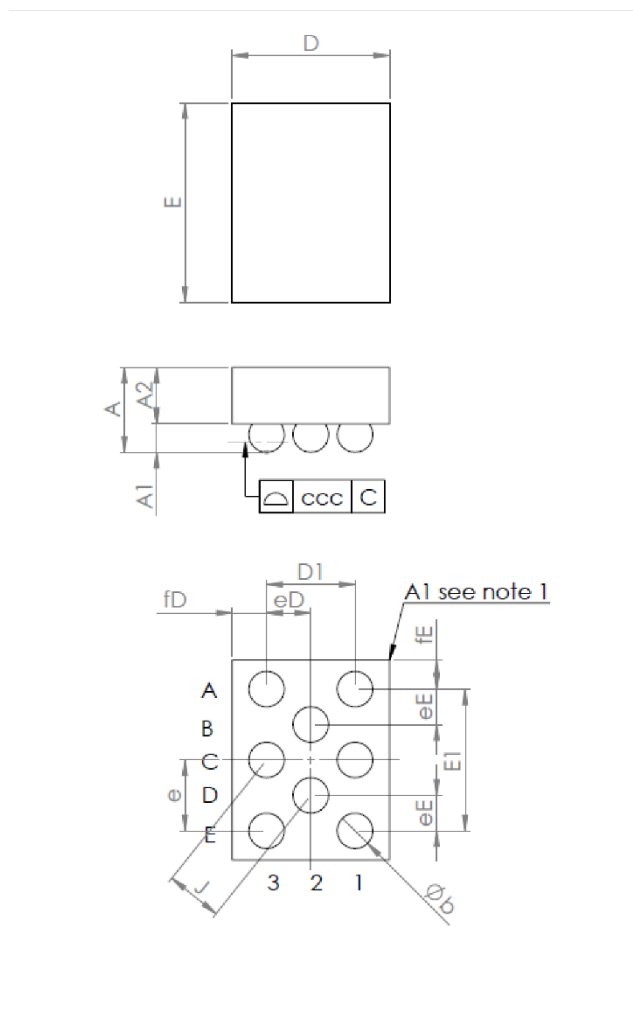
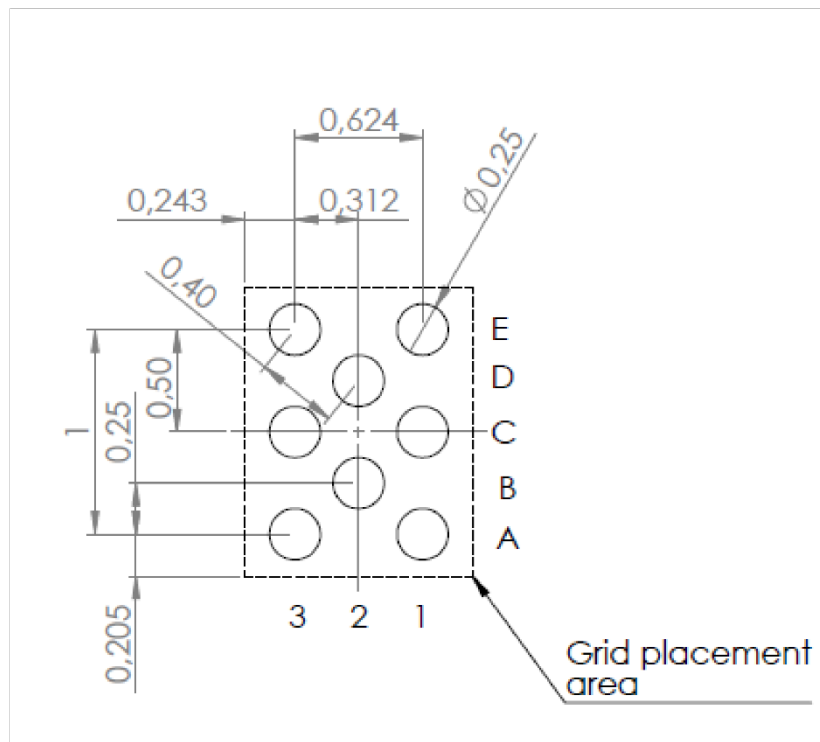


Table 8. Flip-Chip 8 (1.14x1.44 mm) mechanical data

| Symbol | Millimeters | | |
|--------|-------------|-------|-------|
| | Min. | Typ. | Max. |
| A | 0.500 | 0.550 | 0.600 |
| A1 | 0.170 | 0.200 | 0.230 |
| A2 | 0.330 | 0.350 | 0.370 |
| b | 0.230 | 0.250 | 0.270 |
| D | 1.08 | 1.11 | 1.14 |
| D1 | | 0.624 | |
| E | 1.38 | 1.41 | 1.44 |
| E1 | | 1.00 | |
| fE | | 0.205 | |
| fD | | 0.243 | |
| eE | | 0.250 | |
| eD | | 0.312 | |
| e | | 0.50 | |
| J | | 0.40 | |
| ccc | | 0.05 | |

Figure 24. Flip-Chip 8 (1.14x1.44 mm) recommended footprint


9.2 Flip-Chip 8 (1.14x1.44 mm) packing information

Figure 25. Flip-Chip 8 (1.14x1.44 mm) tape outline

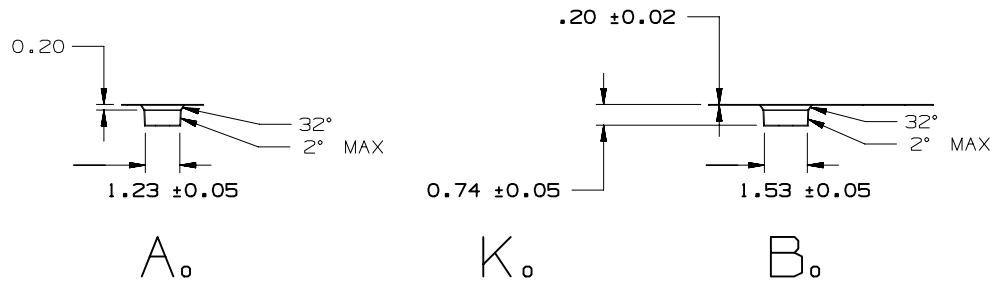
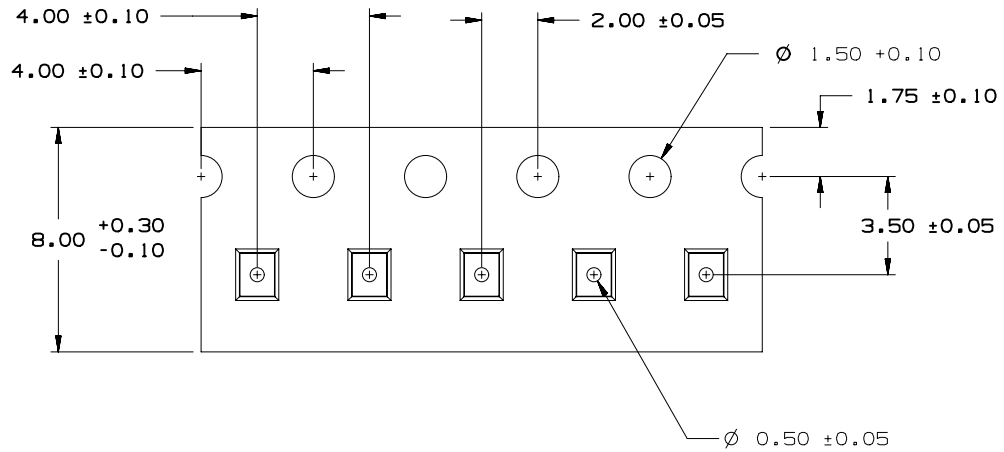


Figure 26. Flip-Chip 8 (1.14x1.44 mm) tape orientation

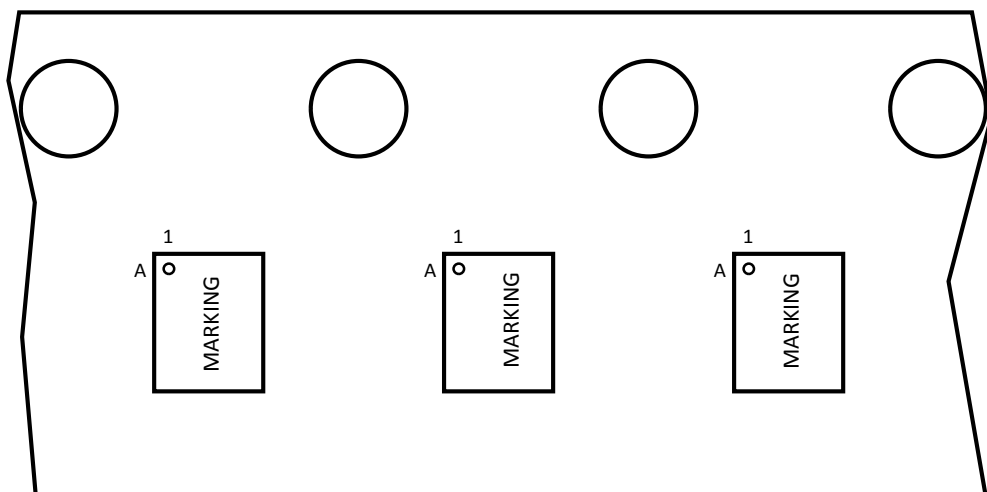


Figure 27. Flip-Chip 8 (1.14x1.44 mm) reel outline

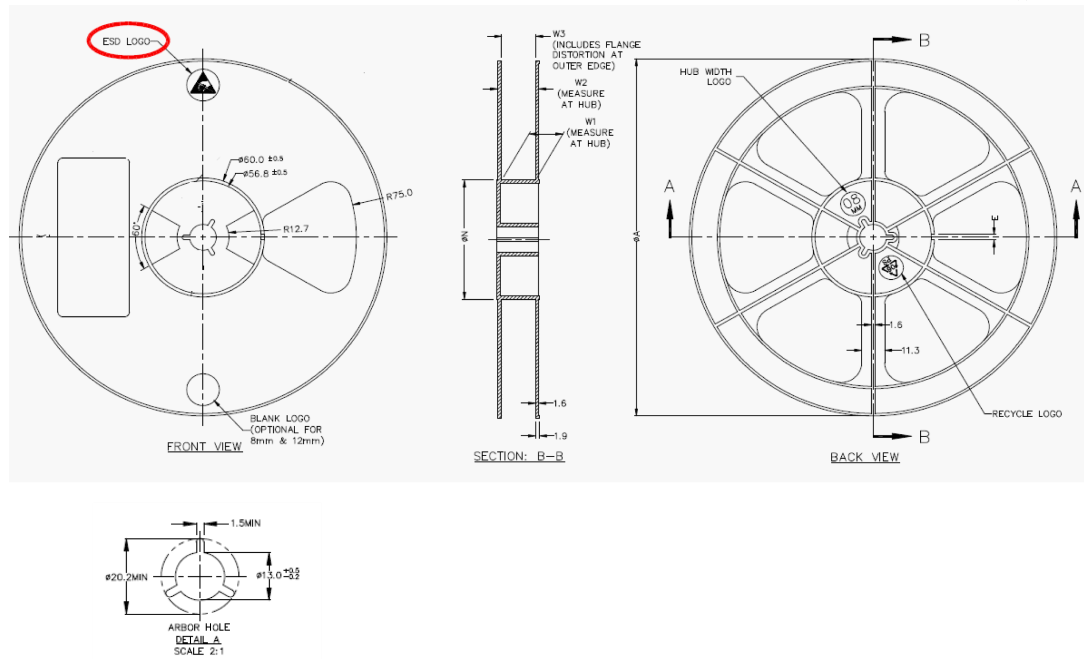


Table 9. Reel mechanical data

| A max. | N min. | W1 max. [mm] | W2 max. [mm] | W3 min./max. [mm] |
|--------|--------|--------------|--------------|-------------------|
| 180 | 60 | 8.4 | 14.4 | 7.9/10.9 |

Revision history

Table 10. Document revision history

| Date | Version | Changes |
|-------------|---------|---|
| 31-Oct-2018 | 1 | Initial release. |
| 13-Dec-2018 | 2 | Updated Section 8 Typical performance characteristics. Added Section 9.2 Flip-Chip 8 (1.14x1.44 mm) packing information. |
| 13-Dec-2019 | 3 | Updated Figure 22. Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}= 10\text{ to }100\text{ mA}$. |

Contents

| | | |
|----------|--|-----------|
| 1 | Application schematic | 2 |
| 2 | Pin configuration (top through view) | 3 |
| 3 | Functional pin description | 4 |
| 4 | Maximum ratings | 5 |
| 5 | Electrical characteristics | 6 |
| 6 | Block diagram | 8 |
| 7 | Operation description | 9 |
| 7.1 | Power save mode | 9 |
| 7.2 | Output voltage | 9 |
| 7.3 | Output discharge and UVLO | 9 |
| 7.4 | Soft-start and current limitation | 9 |
| 7.5 | 100% duty cycle operation | 9 |
| 7.6 | Power Good flag | 9 |
| 8 | Typical performance characteristics | 10 |
| 9 | Package information | 14 |
| 9.1 | Flip-Chip8 (1.14x1.44 mm) package information | 14 |
| 9.2 | Flip-Chip 8 (1.14x1.44 mm) packing information | 15 |
| | Revision history | 18 |

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved