

TVS Diode

Transient Voltage Suppressor Diodes

ESD5V3U2U Series

Uni-directional Ultra Low ESD / Transient Protection Diode

ESD5V3U2U-03F
ESD5V3U2U-03LRH

Data Sheet

Revision 1.3, 2013-08-16
Final

Edition 2013-08-16

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2013 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History: Rev. 1.2, 2013-08-16

Page or Item	Subjects (major changes since previous revision)
Revision 1.3, 2013-08-16	
4 + 16	All marking infos for TSLP-3-7 updated

Trademarks of Infineon Technologies AG

AURIX™, BlueMoon™, C166™, CanPAK™, CIPOS™, CIPURSE™, COMNEON™, EconoPACK™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OptiMOS™, ORIGA™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SMARTi™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™, X-GOLD™, X-PMU™, XMM™, XPOSYS™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, μVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. Mifare™ of NXP. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2010-10-26

1 Uni-directional Ultra Low ESD / Transient Protection Diode

1.1 Features

- ESD / Transient protection of High-Speed data lines exceeding
 - IEC61000-4-2 (ESD): ± 20 kV (air / contact)
 - IEC61000-4-4 (EFT): ± 50 A (5/50 ns)
 - IEC61000-4-5 (surge): ± 3 A (8/20 μ s)
- Maximum working voltage: V_{RWM} 5.3 V
- Extremely low capacitance: down to 0.4 pF
- Very low reverse current: $I_R < 1$ nA typical
- Pb-free package (RoHS compliant) and halogen free package



1.2 Application Examples

- ESD / Transient protection of High Speed Interfaces:
 - HDMI, USB 2.0/USB 3.0, DisplayPort, DVI
 - Mobile HDMI Link, MDDI, MIPI.
 - 10/100/1000 Ethernet, Firewire, S-ATA, etc.

1.3 Product Description

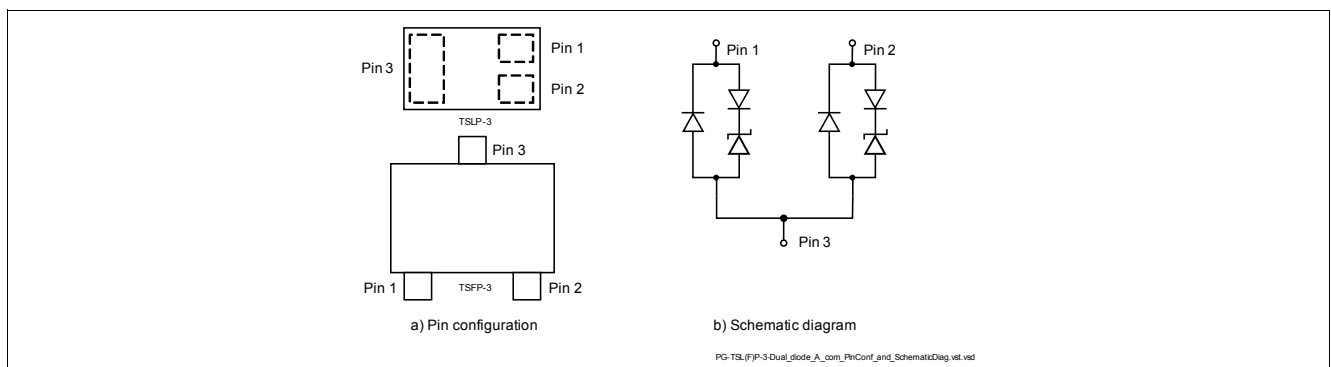


Figure 1-1 Pin Configuration (a) and Schematic Diagram (b)

Table 1-1 Ordering information

Type	Package	Configuration	Marking code
ESD5V3U2U-03F	PG-TSFP-3-1	2 lines, uni-directional ¹⁾	Z1
ESD5V3U2U-03LRH	PG-TSLP-3-7	2 lines, uni-directional ¹⁾	Z1

1) Or 1 line, bi-directional between pins 1 and 2, if pin 3 is not connected

2 Characteristics

Table 2-1 Maximum Rating at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge ¹⁾	V_{ESD}	-20	–	20	kV
Peak pulse current ($t_p = 8/20\text{ }\mu\text{s}$) ²⁾	I_{PP}	-3	–	3	A
Operating temperature range	T_{OP}	-40	–	125	$^\circ\text{C}$
Storage temperature	T_{stg}	-65	–	150	$^\circ\text{C}$

1) V_{ESD} according to IEC61000-4-2

2) I_{PP} according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

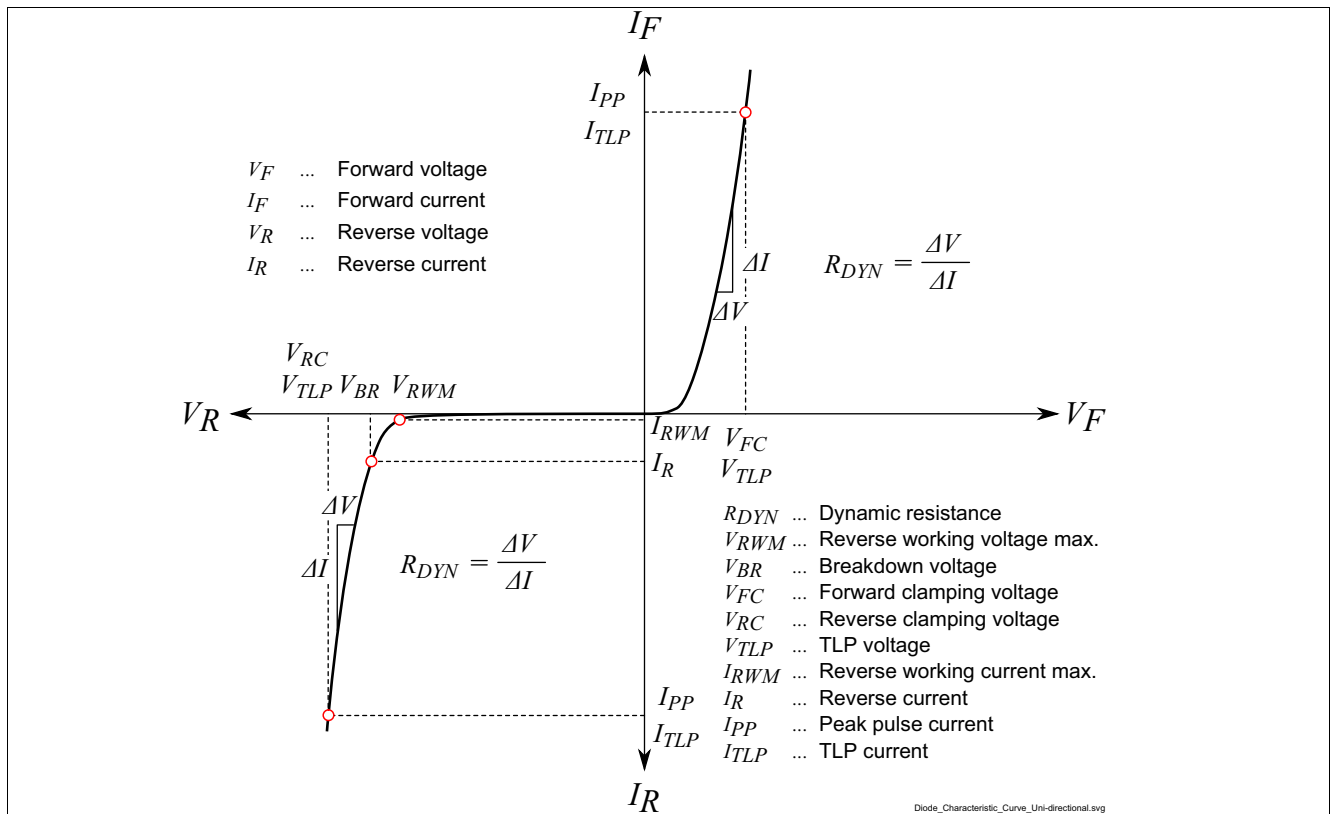


Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	5.3	V	
Breakdown voltage	V_{BR}	6	–	–	V	$I_{BR} = 1\text{ mA}$, from Pin 1/2 to Pin 3
Reverse current	I_R	–	<1	50	nA	$V_R = 5.3\text{ V}$, from Pin 1/2 to Pin 3

Table 2-3 RF characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance ¹⁾	C_L	–	0.4	0.6	pF	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ from pin 1/2 to pin 3
		–	0.2	0.4	pF	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ from pin 1 to 2, pin 3 ¹⁾ not connected

1) Total capacitance line to ground

Table 2-4 ESD Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ¹⁾	V_{CL}	–	19	–	V	$I_{TLP} = 16\text{ A}$, from Pin 1/2 to Pin 3
		–	28	–	V	$I_{TLP} = 30\text{ A}$, from Pin 1/2 to Pin 3
Forward clamping voltage ¹⁾	V_{FC}	–	10	–	V	$I_{TLP} = 16\text{ A}$, from Pin 3 to Pin 1/2
		–	17	–	V	$I_{TLP} = 30\text{ A}$, from Pin 3 to Pin 1/2
Dynamic resistance ¹⁾	R_{DYN}	–	0.6	–	V	Pin 1/2 to Pin 3
		–	0.4	–	V	Pin 3 to Pin 1/2

1) Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$, averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 10\text{ A}$ and $I_{PP2} = 40\text{ A}$.

Table 2-5 Surge characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage	V_{CL}	–	10	13	V	$I_{PP} = 1\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}^{1)}$ from Pin 1/2 to Pin 3
		–	12	15	V	$I_{PP} = 3\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}^{1)}$ from Pin 1/2 to Pin 3
Forward clamping voltage	V_{FC}	–	2	4	V	$I_{PP} = 1\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}^{1)}$ from Pin 3 to Pin 1/2
		–	4	6	V	$I_{PP} = 3\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}^{1)}$ from Pin 3 to Pin 1/2

1) I_{PP} according to IEC61000-4-5

3 Typical characteristics

Typical characteristics at = 25 °C, unless otherwise specified

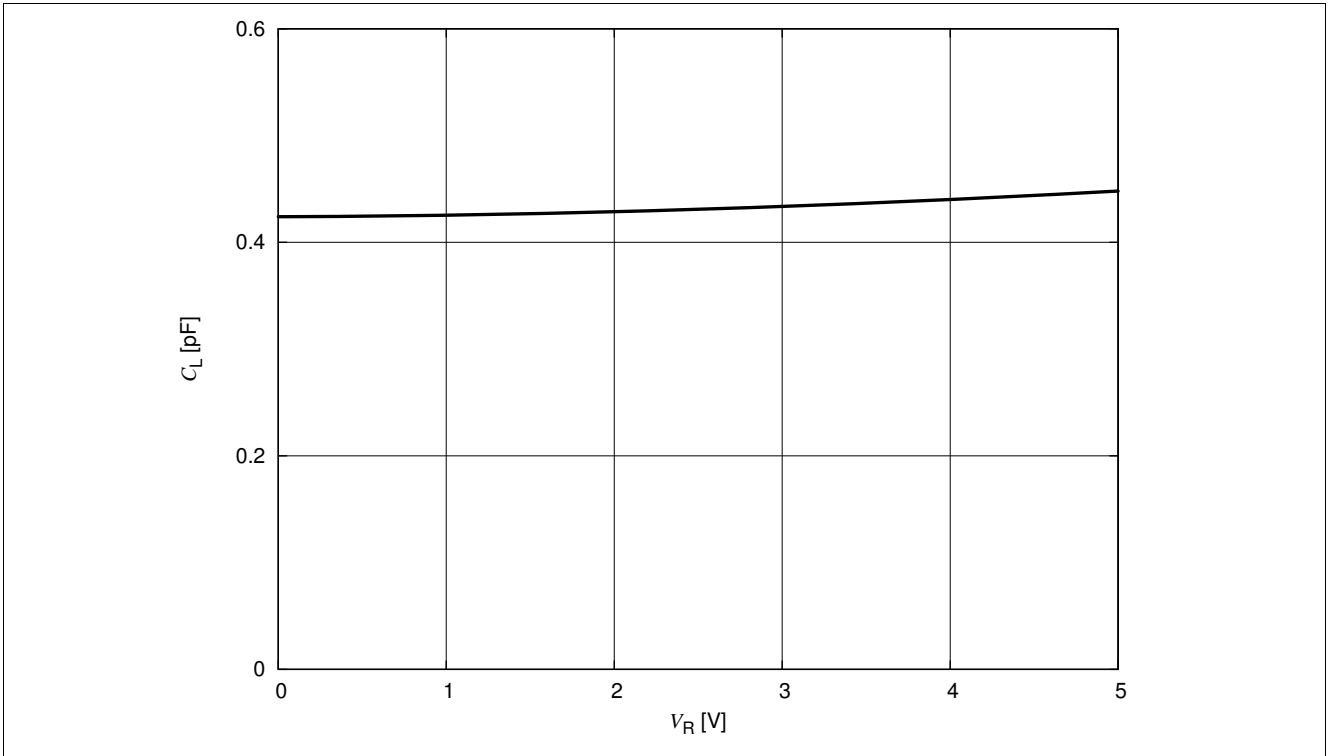


Figure 3-1 Line capacitance $C_L=f(V_R)$, from pin 1/2 to 3, $f = 1$ MHz

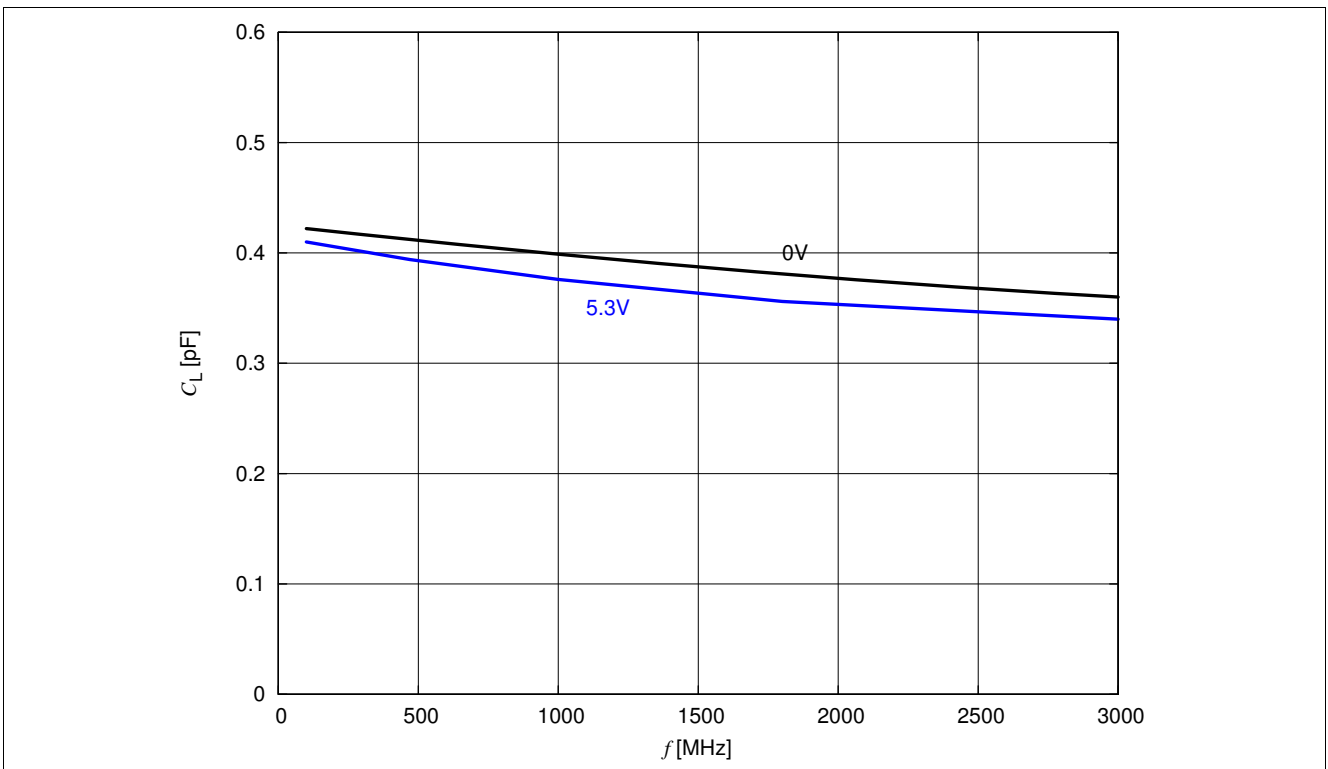


Figure 3-2 Line capacitance $C_L=f(f)$, from pin 1/2 to 3

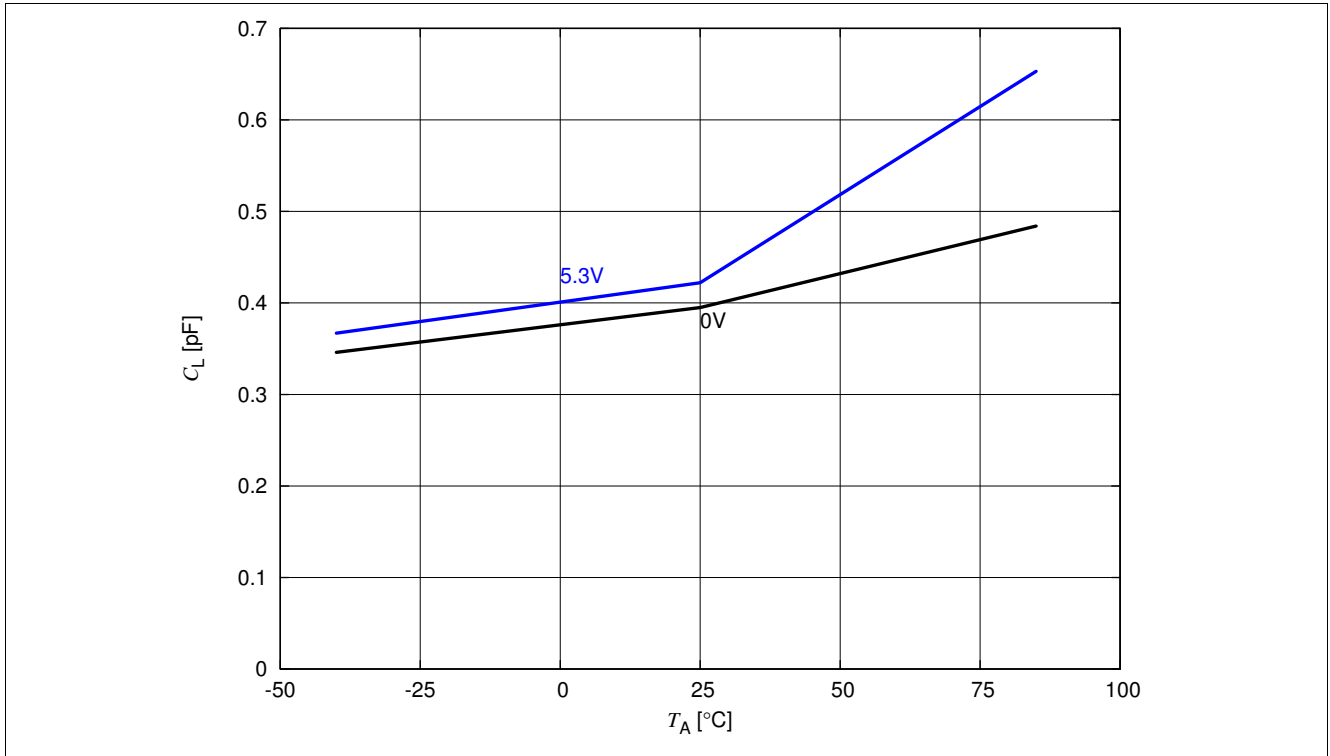


Figure 3-3 Line capacitance $C_L=f(T_A)$

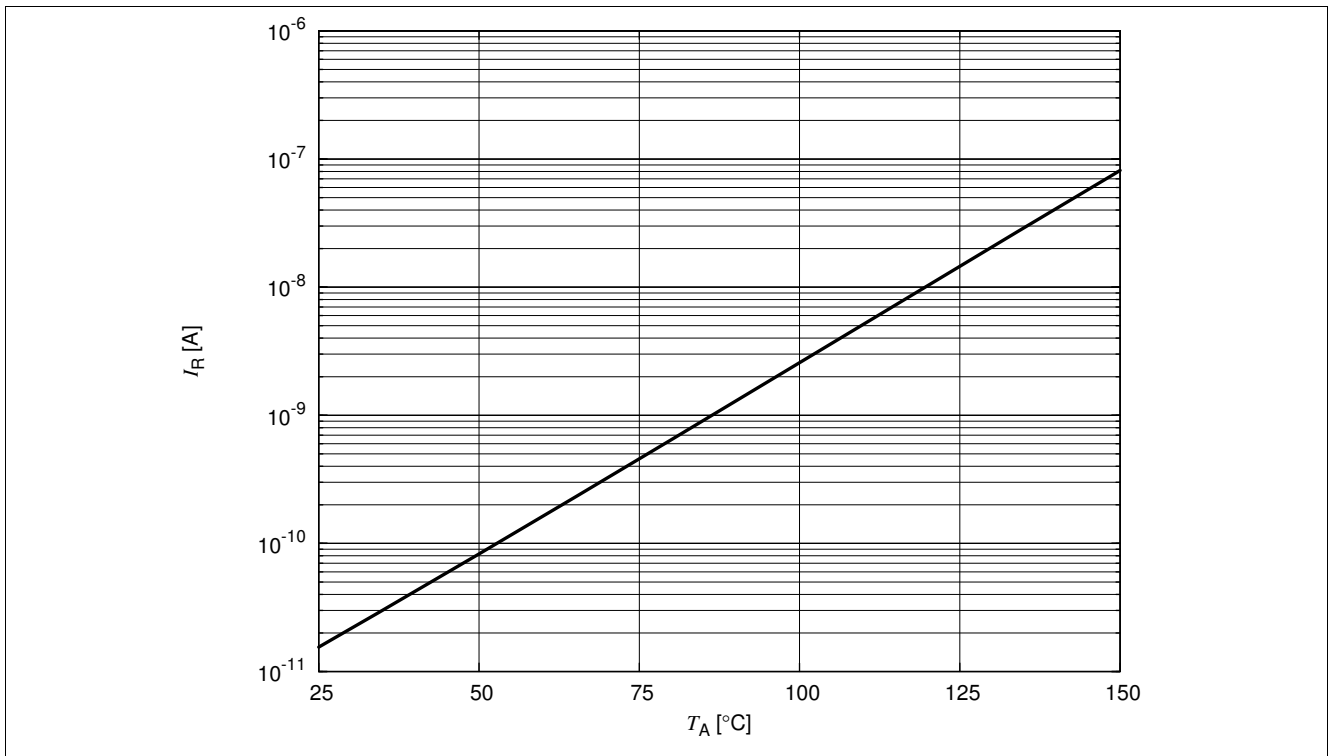


Figure 3-4 Reverse current $I_R=f(T_A)$, $V_R=5.3$ V, from pin 1/2 to pin 3

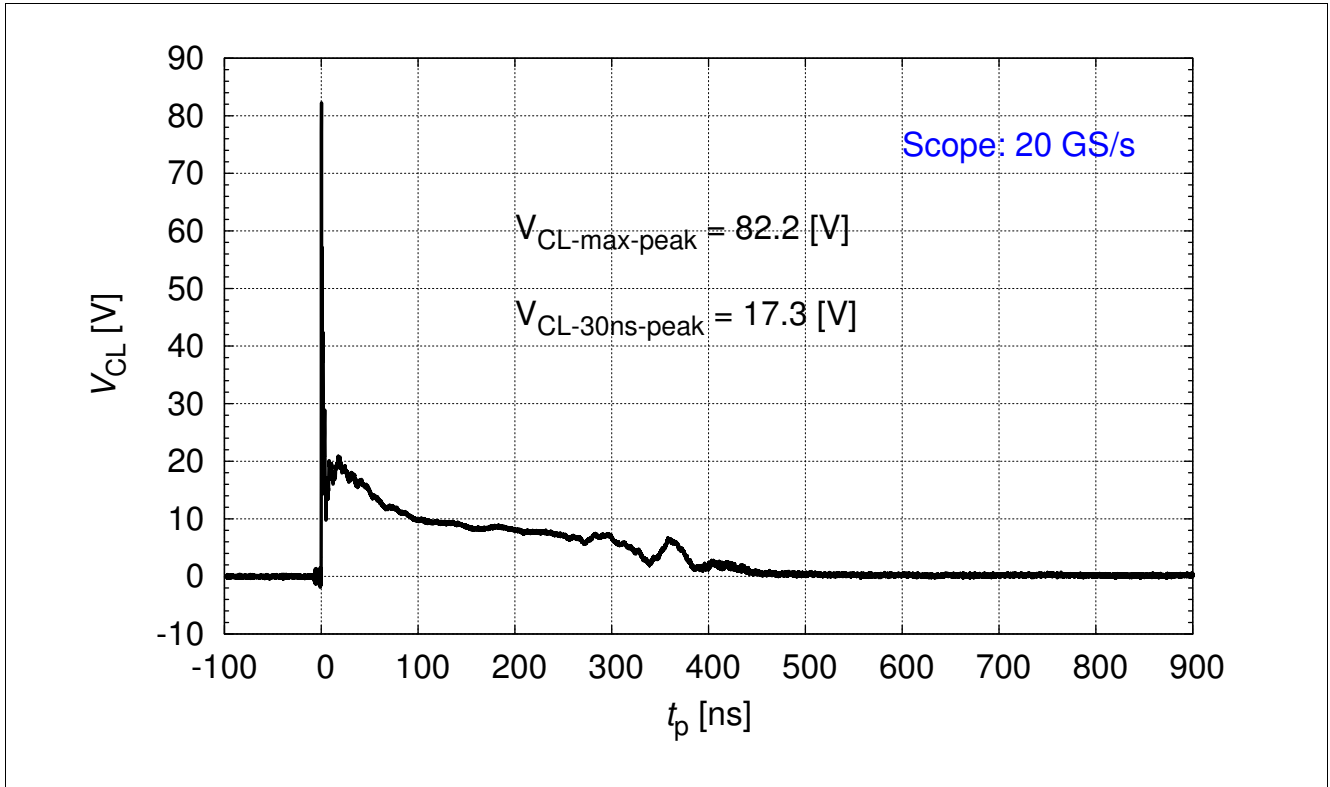


Figure 3-5 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2 ($R = 330 \Omega$, $C = 150$ pF)

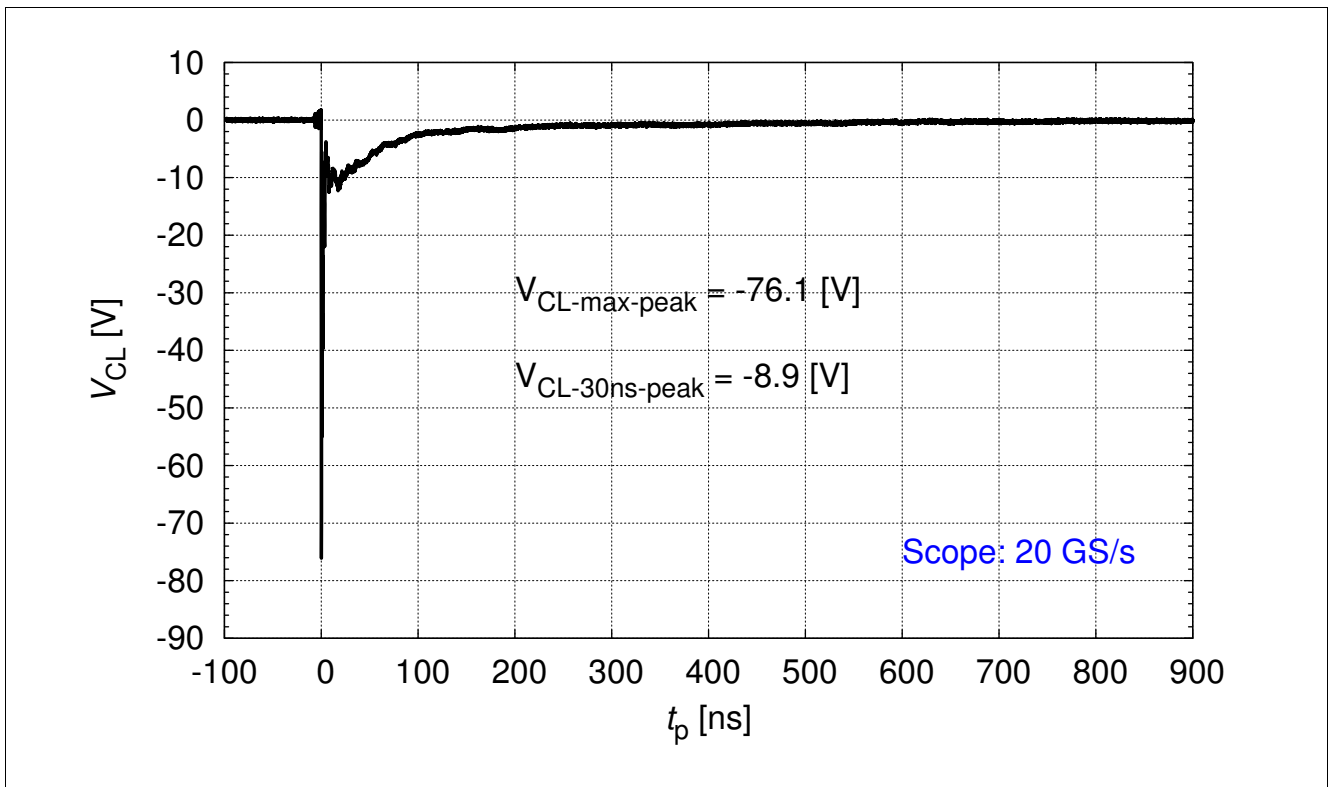


Figure 3-6 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2 ($R = 330 \Omega$, $C = 150$ pF)

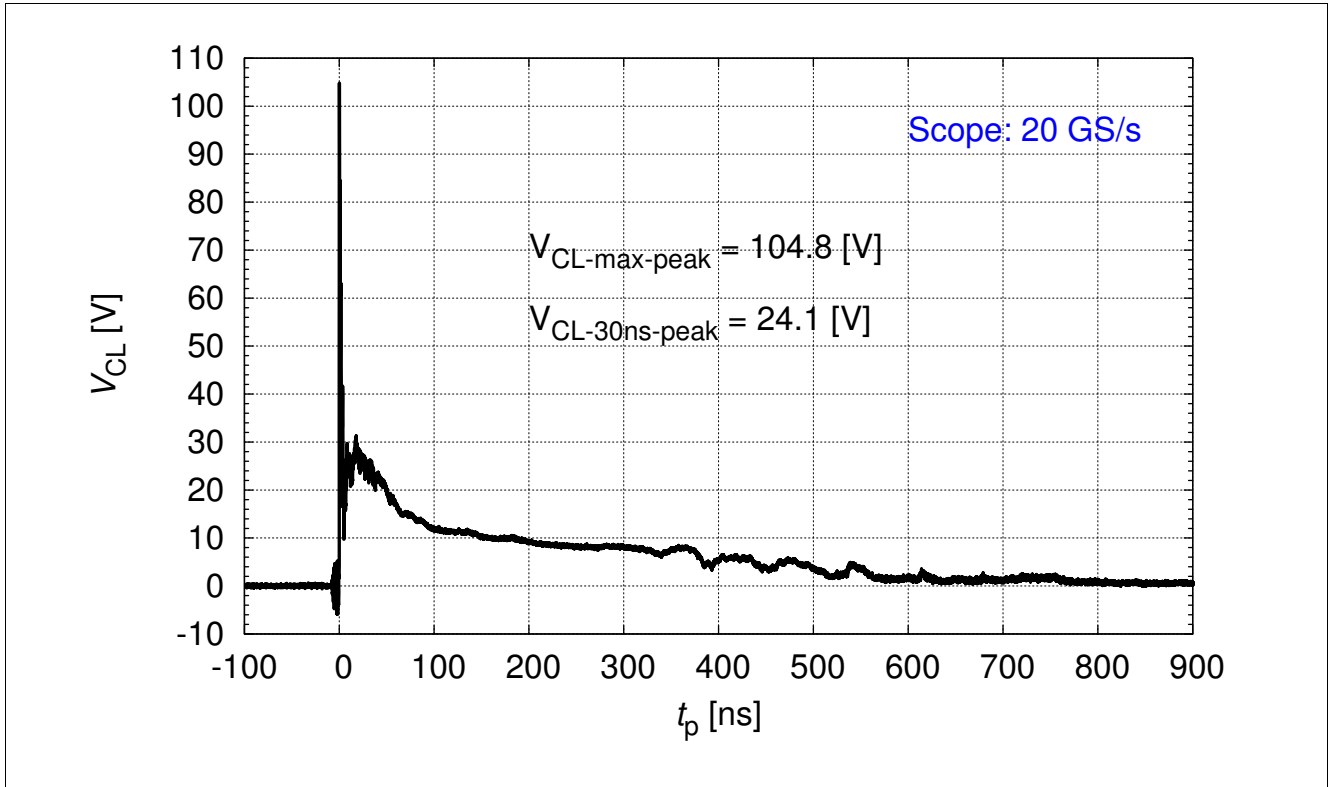


Figure 3-7 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2 ($R = 330 \Omega$, $C = 150 \text{ pF}$)

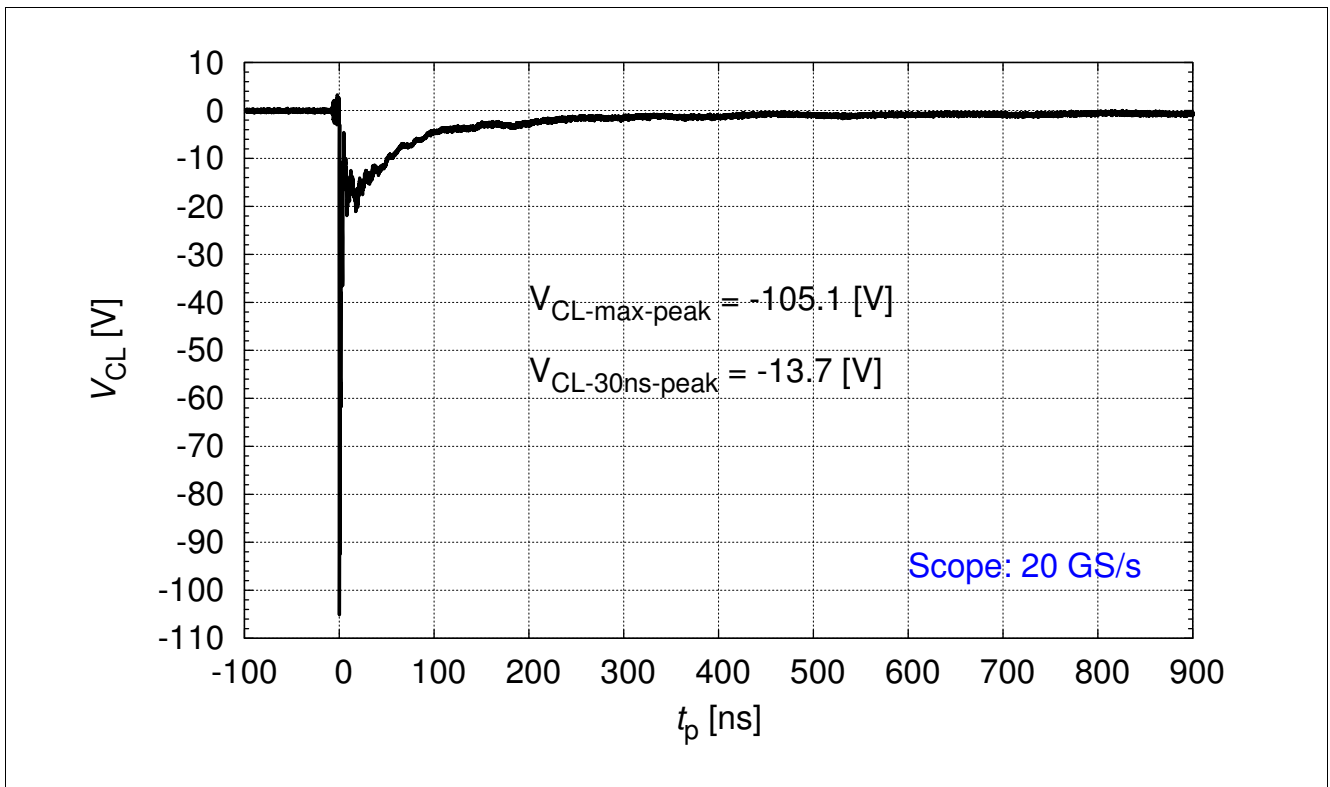


Figure 3-8 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2 ($R = 330 \Omega$, $C = 150 \text{ pF}$)

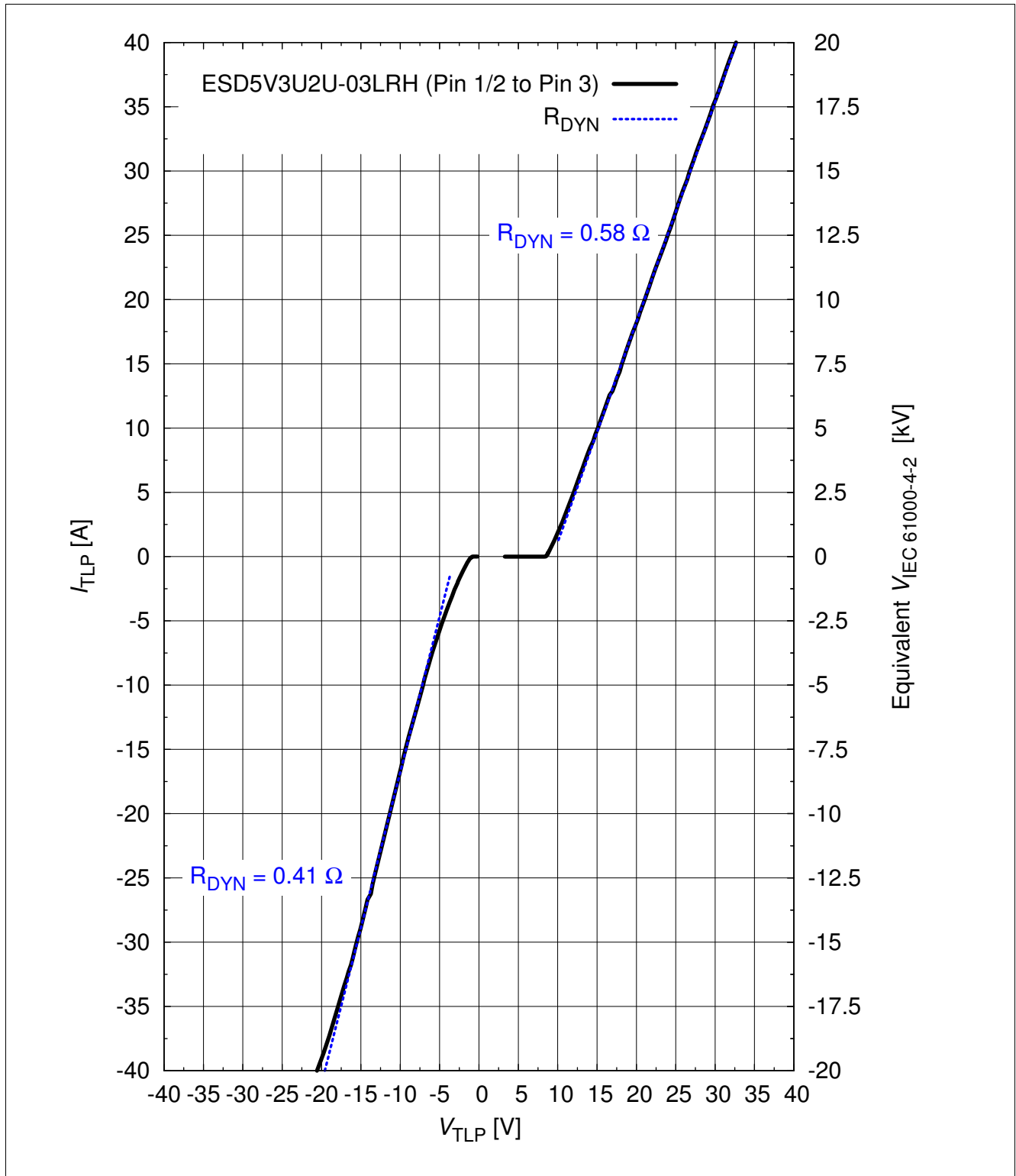


Figure 3-9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1- Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 0.6 \text{ ns}$, I_{TLP} and V_{TLP} averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$, extraction of dynamic resistance using squares fit to ELP characteristic between $I_{TLP1} = 10 \text{ A}$ and $I_{TLP2} = 30 \text{ A}$. Please refer to Application Note AN210 [1]

4 Application Information

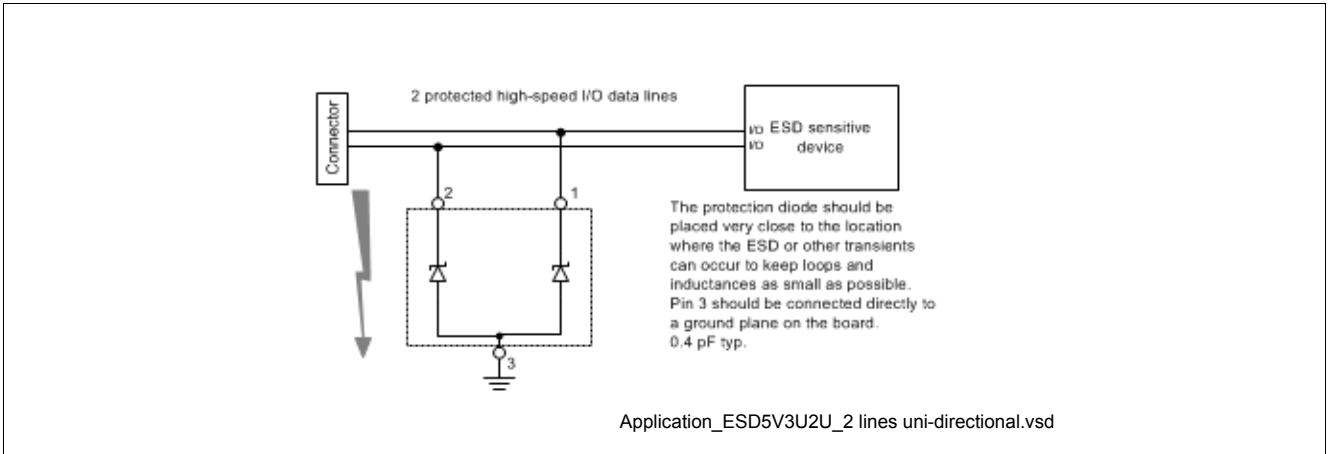


Figure 4-1 2 lines, uni-directional TVS protection

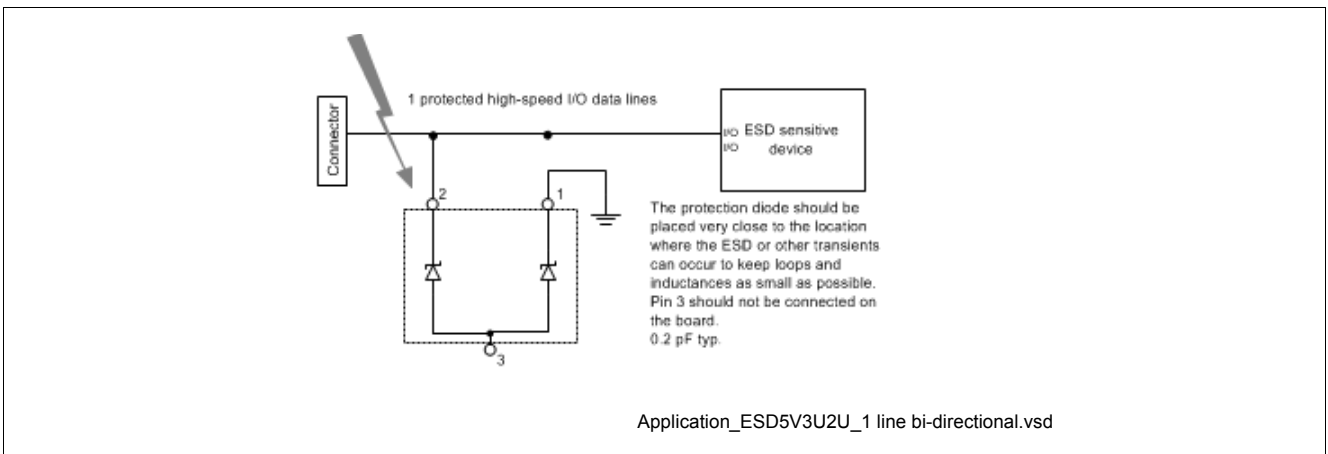


Figure 4-2 1 line, bi-directional TVS protection

5 Ordering information scheme (examples)

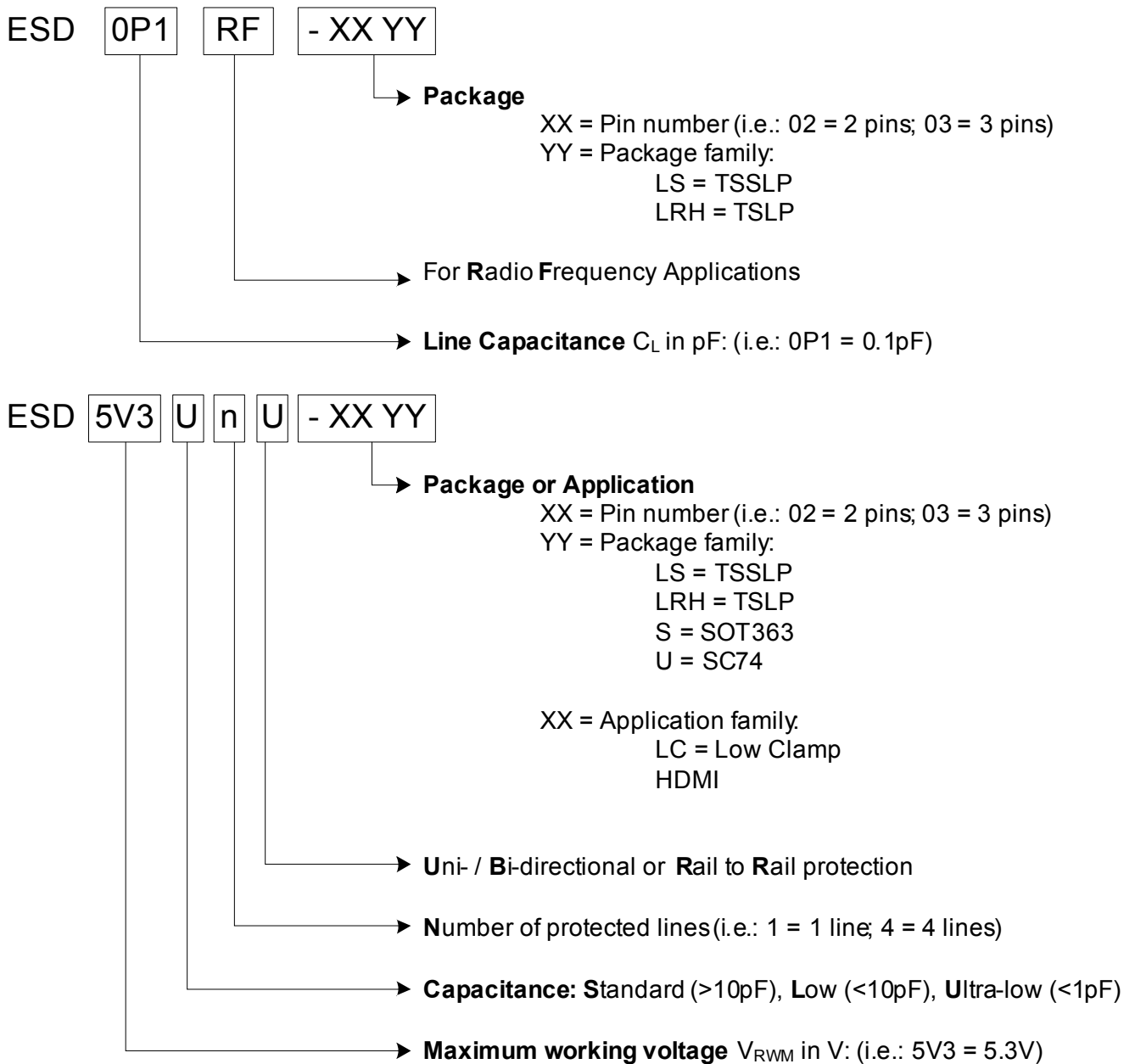


Figure 5-1 Ordering Information Scheme

6 Package Information

6.1 PG-TSFP-3-1

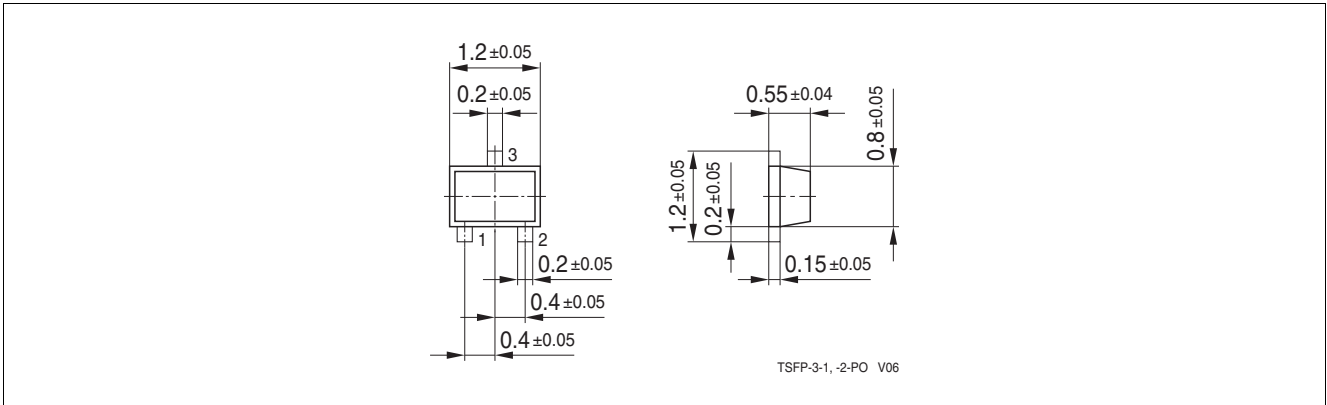


Figure 6-1 PG-TSFP-3-1: Package Overview

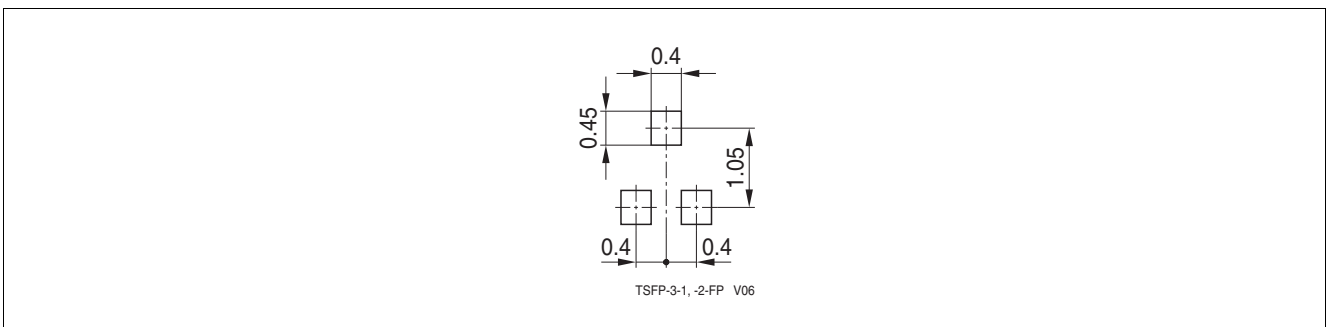


Figure 6-2 PG-TSFP-3-1: Footprint

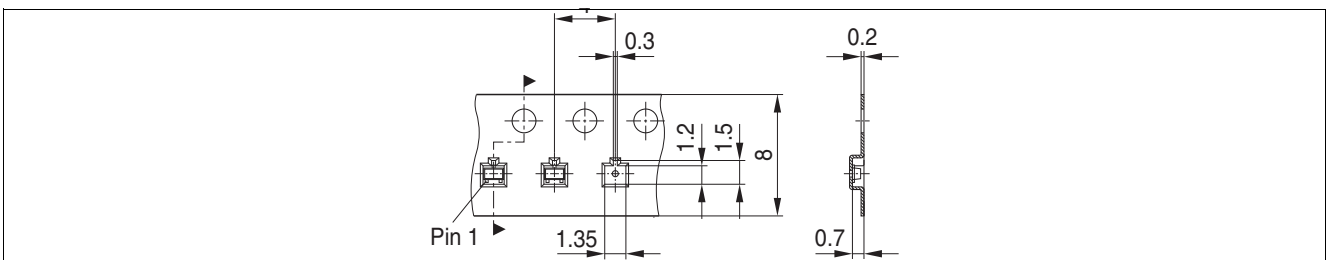


Figure 6-3 PG-TSFP-3-1: Packing

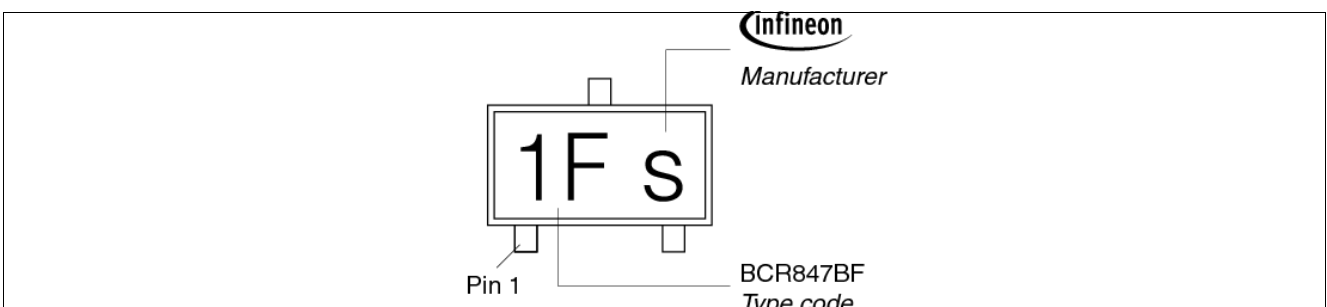


Figure 6-4 PG-TSFP-3-1: Marking (example)

6.2 PG-TSLP-3-7

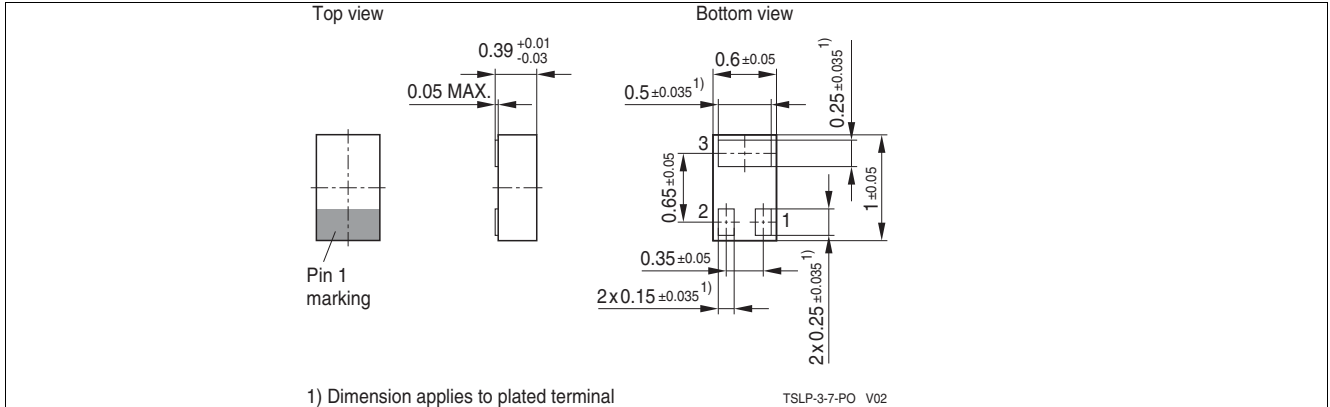


Figure 6-5 PG-TSLP-3-7: Package Overview

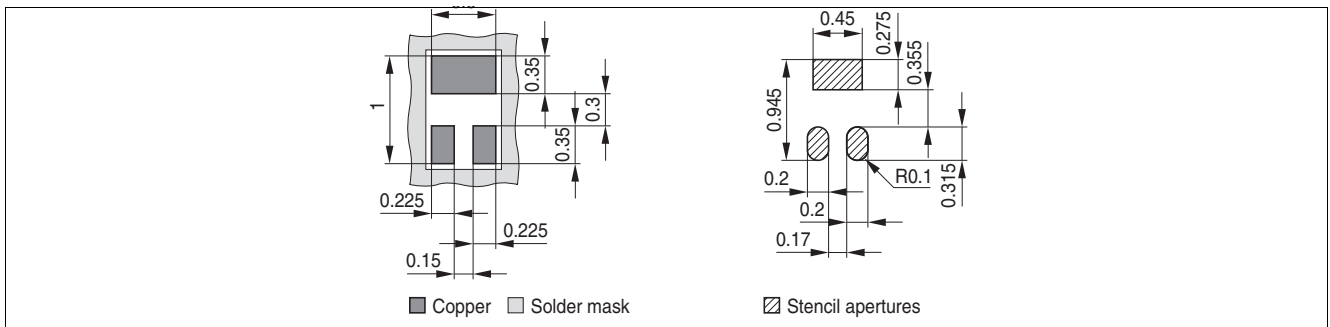


Figure 6-6 PG-TSLP-3-7: Footprint

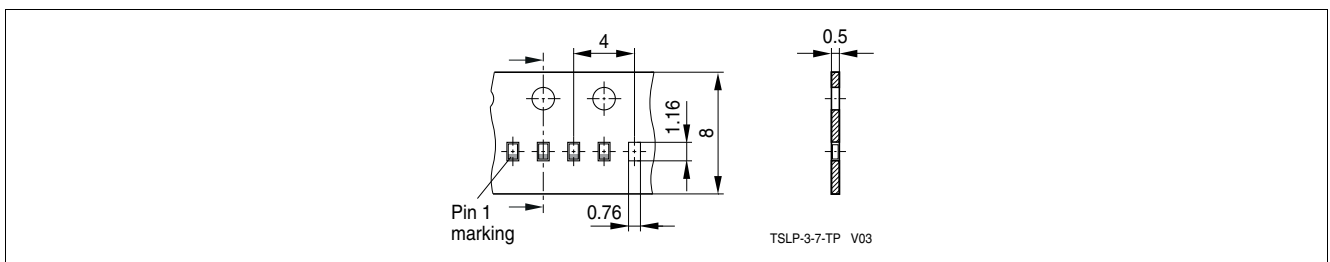


Figure 6-7 PG-TSLP-3-7: Packing

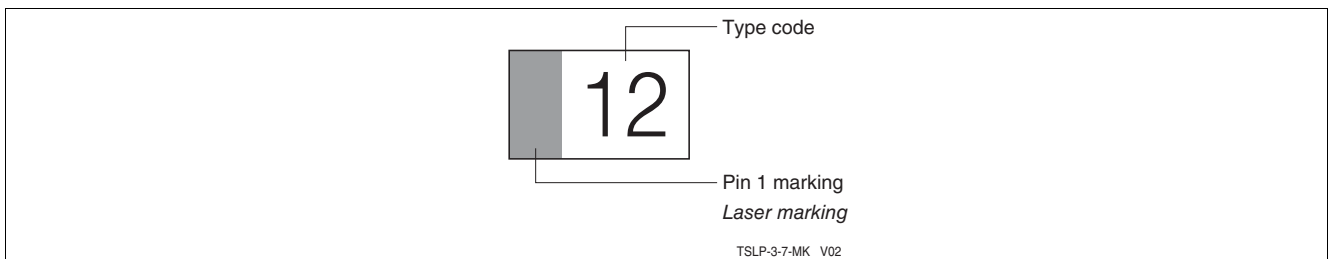


Figure 6-8 PG-TSLP-3-7: Marking (example)

References

- [1] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

www.infineon.com

Published by Infineon Technologies AG