# Quad Channel Active EMI & ESD Suppressor for Ethernet Applications

## Features

- Enables system designers to comply with:
  - CISPR22 and FCC Part 15, Class B requirements for Radiated and Conducted Emissions
  - IEC 61000-4-3 requirements for Radiated and Conducted Immunity, Level 3 or higher
  - IEC 61000-4-2 ESD (Air Discharge) of ±25kV
  - IEC 61000-4-2 ESD (Contact Discharge) of ±12kV
  - Cable Discharge Event (CDE) of ±12kV
- Provides up to 10dB of additional common mode noise suppression over the frequency of 1MHz to 125MHz when used with Ethernet magnetics
- Robust built-in ESD suppressors protect the Ethernet PHY and improve system ESD performance
- JESD22-A114, ESD, HBM of ±8kV
- Interfaces to standard Ethernet transformers and 1000 Ethernet PHYs
- Uses a single standard power rail (3.3V or 2.5V)
- Open drain output stage that can be biased from 1.8V to 3.3V using transformer center-tap supply as needed based on choice of Ethernet PHY.
- Flow-through routing for ease of board layout
- Typical power consumption of 90mW.
- Low power mode available
- Industrial temperature range (-40°C to +85°C)

## Applications

- Ethernet systems requiring additional CM suppression to meet EMC Class B emissions or higher EMI immunity requirements and ESD protection
- POE and Non-PoE Ethernet systems
- VoIP Phones, IP Cameras, WAPs, Routers, Switches
- Set Top Boxes, Networked Printers and Appliances, Desktop and Laptop Computers

## Brief Description

The KTA1552 is a four channel, highly integrated CMOS solution for Common Mode (CM) noise suppression & transient voltage protection in Ethernet applications.

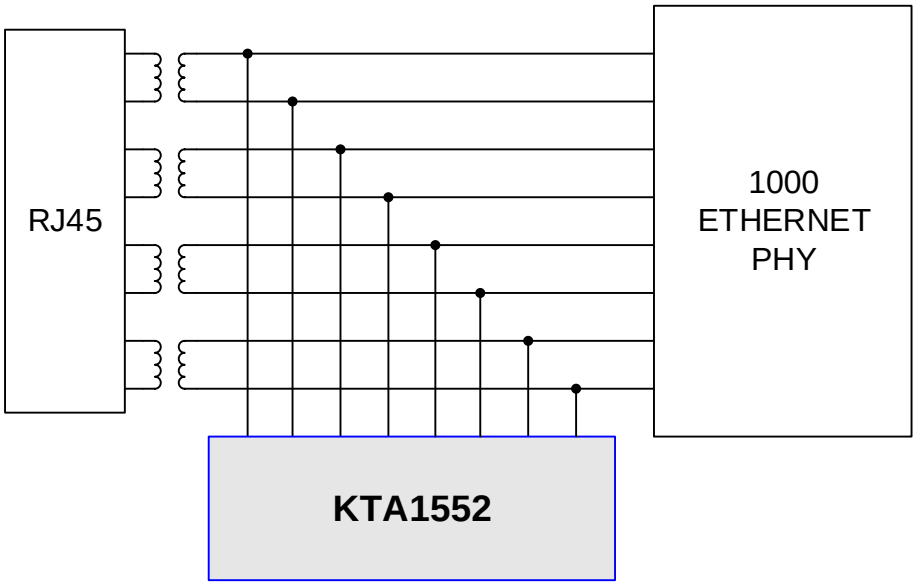
The KTA1552 EMI/ESD Suppressor has been architected and designed to provide system level ESD protection and EMI suppression in Ethernet products, enabling an easier path to system EMC compliance.

The KTA1552 utilizes Kinetic Technologies' patented Active Choke technology which offers superior Common Mode reduction and immunity compared to passive filtering techniques in Ethernet applications. The adaptive and continuous suppression operates over the entire Ethernet signal bandwidth, and it compensates for many variables that are the source of common mode noise in Ethernet systems. It also improves the differential-to-common mode balance of the system. This enables system designers to meet EMI emissions and EMI immunity requirements from the start of the design.

In addition, the KTA1552 includes highly robust ESD/Surge protection diodes to protect the Ethernet PHY from various transient overvoltage events. These are built using Kinetics' proprietary design and layout techniques to safely deal with very high current densities in a CMOS process without creating voltage and/or thermal overstress that causes damage to the device.

The KTA1552 supports four twisted pair interfaces for 1000 applications. The KTA1552 is available in a small footprint 36-pin DFN 9mm x 4mm Reduction of Hazardous Substance (RoHS) compliant package.

## Typical Applications

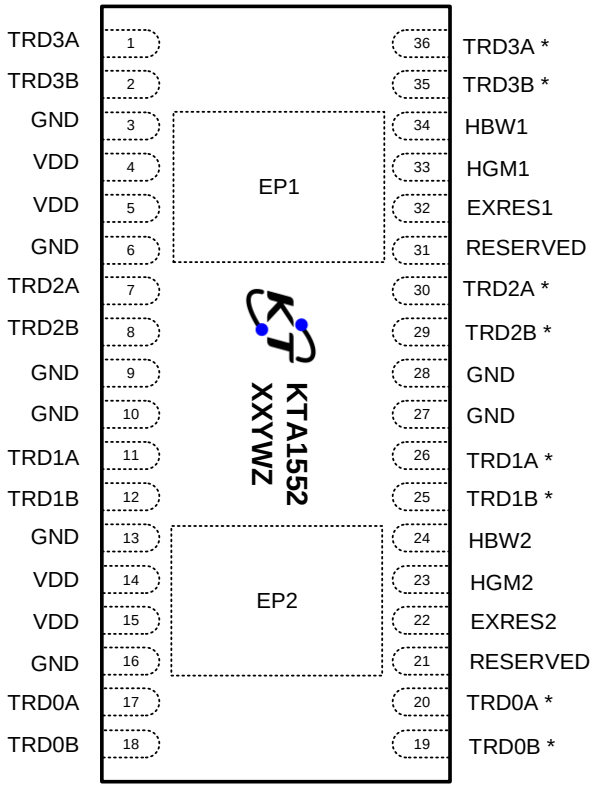


## Pin Descriptions

| Pin # | I/O | Name | Function |
|---|---|---|---|
| 1, 36 | A, OD | TRD3A | PHY media differential pair 3 positive or negative signal. Note that circuit electrical connection is to pin 1 only. Pin 36 is named the same to enable through-routing on the PCB, however it is not connected internally. |
| 2, 35 | A, OD | TRD3B | PHY media differential pair 3 positive or negative signal. Note that circuit electrical connection is to pin 2 only. Pin 35 is named the same to enable through-routing on the PCB, however it is *not* connected internally. |
| 3, 6, 9, 10, 13, 16, 27, 28 | P | GND | Board ground - same as Ethernet PHY ground |
| 4, 5, 14, 15 | P | VDD | Analog VDD. 3.3V ± 5% or 2.5V ± 5% supply can be used. VDD can be shared with transformer center-tap supply, but is not required. Note that the transformer center-tap supply voltage (VCT) must always be *equal* to or less than VDD. |
| 7, 30 | A, OD | TRD2A | PHY media differential pair 2 positive or negative signal. Note that circuit electrical connection is to pin 7 only. Pin 30 is named the same to enable through-routing on the PCB, however it is *not* connected internally. |
| 8, 29 | A, OD | TRD2B | PHY media differential pair 2 positive or negative signal. Note that circuit electrical connection is to pin 8 only. Pin 29 is named the same to enable through-routing on the PCB, however it is *not* connected internally. |
| 11, 26 | A, OD | TRD1A | PHY media differential pair 1 positive or negative signal. Note that circuit electrical connection is to pin 11 only. Pin 26 is named the same to enable through-routing on the PCB, however it is *not* connected internally. |
| 12, 25 | A, OD | TRD1B | PHY media differential pair 1 positive or negative signal. Note that circuit electrical connection is to pin 12 only. Pin 25 is named the same to enable through-routing on the PCB, however it is *not* connected internally. |
| 17, 20 | A, OD | TRD0A | PHY media differential pair 0 positive or negative signal. Note that circuit electrical connection is to pin 17 only. Pin 20 is named the same to enable through-routing on the PCB, however it is *not* connected internally. |
| 18, 19 | A, OD | TRD0B | PHY media differential pair 0 positive or negative signal. Note that circuit electrical connection is to pin 18 only. Pin 19 is named the same to enable through-routing on the PCB, however it is *not* connected internally. |
| 21, 31 | - | RESERVED | Reserved - leave open |
| 22, 32 | A | EXRES1, EXRES2 | External bias resistor. For VDD = 2.5V use 8.06kΩ ±1%. For VDD = 3.3V use 10.7kΩ ±1%. Connect resistor between each EXRES pin and GND |
| 23, 33 | DI | HGM1, HGM2 | Allows trade-off between desired CM rejection performance and device power consumption (Both pins should be set to the same mode):<br>FLOATING: Default setting - recommended normal operating condition<br>LOW: Lower power mode setting - reduces CM rejection performance to reduce power consumption. See "*Performance/Power Control Pins*" for additional details.<br>HIGH: Reserved - should not be used |
| 24, 34 | DI | HBW1, HGM2 | Allows control of CM rejection performance by changing internal loop bandwidth. May be used in some systems to optimize EMI performance. (Both pins should be set to the same mode)<br>FLOATING: Default setting - recommended normal operating condition<br>LOW: Reserved - should not be used<br>HIGH: Increases loop bandwidth to increase CM rejection performance. May be used in some systems to optimize EMI performance. See "*Performance/Power Control Pins*" for additional details |
| EP1, EP2 | Exposed Pad | GND | Connected to GND and can be used to improve thermal performance. Pad can be left floating for normal operation. |

Key: OD = Open Drain, A = Analog Signal, DI = Tri-State Digital Input Signal, P = Power

**36-Pin DFN**
Top View




** Not connected internally – pin named to enable PCB through routing.*

**Top Mark**
XX = Device Code
YWZ = Date Code and Assembly Code

## Absolute Maximum Ratings[1]

($T_A$ = 25°C unless otherwise noted)

| Symbol | Description | Value | Units |
|---|---|---|---|
| TRDn | PHY media TRDn pins | -0.3 to 5 | V |
| EXRES, HGM, HBK, | All other pins | -0.3 to 3.6 | V |
| VDD | Supply voltage | -0.3 to 3.6 | V |
| $T_S$ | Storage Temperature | 165 | °C |
| $T_J$ | Junction Operating Temperature | -40 to 125 | °C |

## ESD Ratings

| Symbol | Description | Conditions | Value | Units |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model (HBM)[2] | JESD22-A114 | 8 | kV |
| | Charged Device Model (CDM)[2] | JESD22-C101 | 500 | V |
| | IEC 61000-4-2 Contact Discharge[3] | TRDn Pins Only | 12 | kV |
| | IEC 61000-4-2 Air-Gap Discharge[3] | | 25 | kV |
| | Cable Discharge Event (CDE)[3] | | 12 | kV |

## Ordering Information

| Part Number | Marking[4] | Operating Temperature | Package |
|---|---|---|---|
| KTA1552EDT-TR | LNYWZ | -40°C to +85°C | 36-Pin DFN 0.5mm pitch |

## Recommended Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | 3.3 V Power supply (VDD) | 3.13 | 3.3 | 3.47 | V |
| | 2.5V Power Supply (VDD) | 2.37 | 2.5 | 2.63 | V |
| $V_{CT}$ | DC common mode of Ethernet signals (transformer center-tap supply[5] | 1.8 -5% | | 3.3 +5% | V |
| $T_A$ | Ambient Operating Temperature Range | -40 | - | +85 | °C |

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Human Body Model and Charged Device Model ESD limits are specified at the chip level.
3. Air Discharge, Contact Discharge, and Cable Discharge Event maximum limits are specified at the system level.
4. “YWZ” is the date code and assembly code.
5. The transformer center-tap supply voltage (VCT) must always be equal to or less than VDD.

## Electrical Characteristics[6]

Unless otherwise noted, specifications are for $T_A$ = -40°C to +85°C. Typical specifications are for $T_A$ = +25ºC and $V_{DD}$ = 2.5V. Typical specifications not 100% tested.

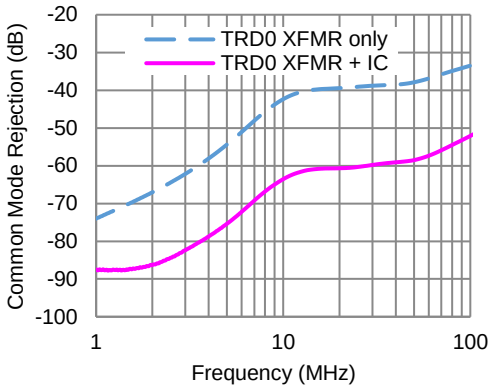
| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Electrical Characteristics[7]** | | | | | | |
| – | Differential signal insertion loss | 0.1MHz - 100MHz | – | 0 | 0.2 | dB |
| – | Differential output capacitance (between TRDnA and TRDnB pins) | | – | 4.5 | – | pF |
| – | Common mode PHY noise rejection (25Ω CM impedance) | at 1MHz | 30 | – | – | dB |
| | | at 100MHz | 10 | – | – | dB |
| – | Common mode PHY noise rejection additive to transformer[8] | at 100MHz | 10 | – | – | dB |
| – | Power Dissipation[9] | Default mode:<br>HGM1, HGM2 = floating<br>$V_{DD}$ = 2.5V, $V_{CT}$ = 1.8V | – | 180 | 260 | mW |
| | | Low Power mode:<br>HGM1, HGM2 = Low<br>$V_{DD}$ = 2.5V, $V_{CT}$ = 1.8V | – | 110 | 160 | mW |
| **Digital Input Characteristics** | | | | | | |
| $V_{IH}$ | Input HIGH level | $V_{CC}$ = 2.5V | 1.78 | | 3.47<br>(3.3V + 5%) | V |
| | | $V_{CC}$ = 3.3V | 2.0 | | 3.47<br>(3.3V + 5%) | V |
| $V_{IL}$ | Input LOW level | $V_{CC}$ = 2.5V | -0.30 | | 0.5 | V |
| | | $V_{CC}$ = 3.3V | -0.30 | | 0.5 | V |
| $I_{IL}$, $I_{IH}$ | Input leakage, LOW and HIGH levels | $V_{CC}$ = 2.5V | ±25 | | ±40 | µA |
| | | $V_{CC}$ = 3.3V | ±33 | | ±53 | µA |

6. KTA1552 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
7. All AC measurements guaranteed by design and not 100% tested
8. This measurement is done with typical Ethernet transformer. Unless otherwise specified, all other performance measurements are for standalone KTA1552 without Ethernet transformer.
9. Maximum power consumption is with +5% supplies and over all process/temperature range.

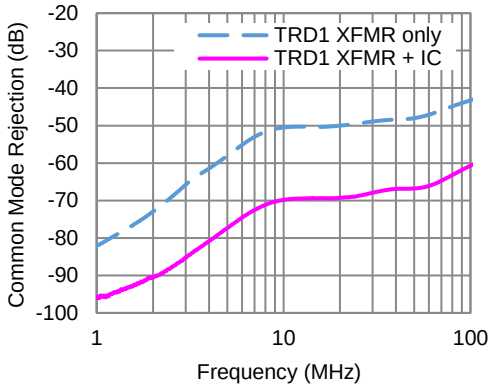
## Typical Characteristics

$V_{IN}$ = 2.5V, Operating Mode = Mode 1 (default mode), $C_{IN}$ = 10µF, Temp = 25°C unless otherwise specified.

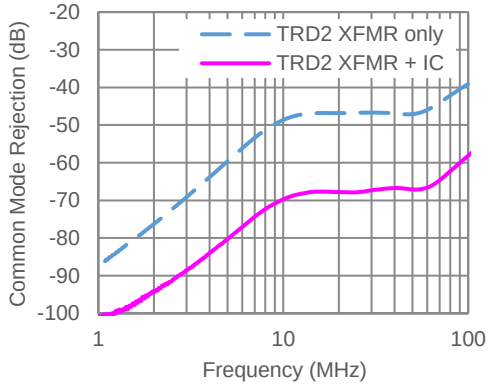
**TRD0 Common Mode Rejection with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**



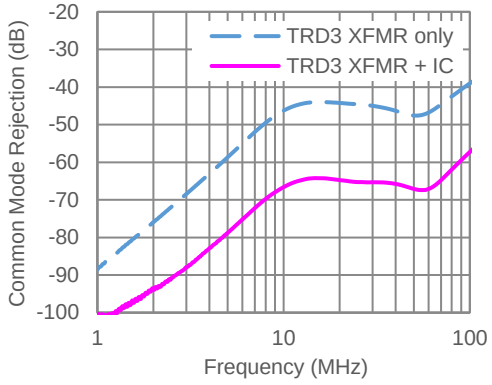

**TRD1 Common Mode Rejection with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**



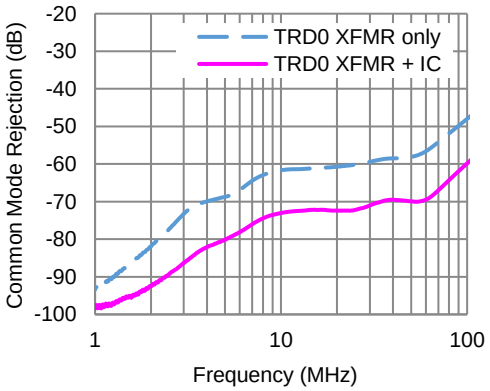

**TRD2 Common Mode Rejection with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**



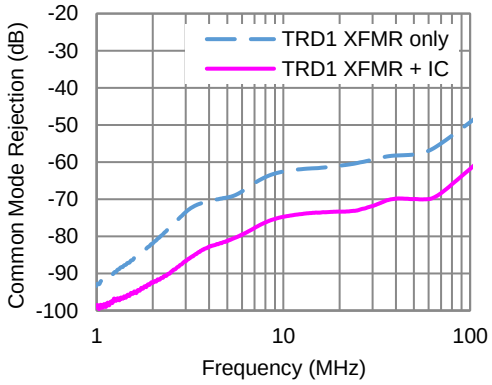

**TRD3 Common Mode Rejection with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**




**TRD0 Common Mode Rejection with Typical 3-Core PoE Compatible Transformer with Media Side Chokes**



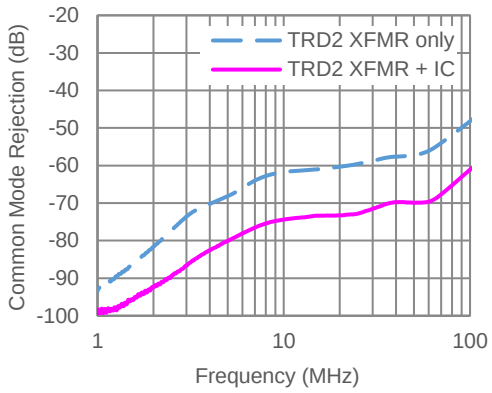

**TRD1 Common Mode Rejection with Typical 3-Core PoE Compatible Transformer with Media Side Chokes**



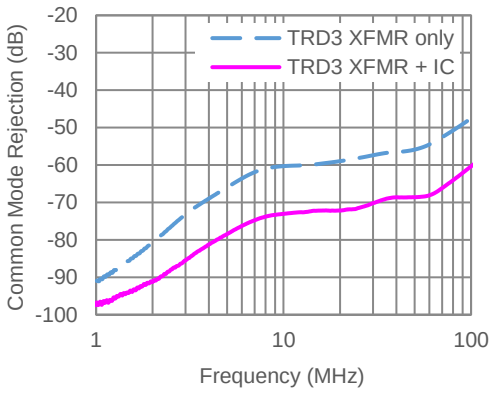
## Typical Characteristics (continued)

$V_{IN}$ = 2.5V, Operating Mode = Mode 1 (default mode), $C_{IN}$ = 10µF, Temp = 25°C unless otherwise specified.

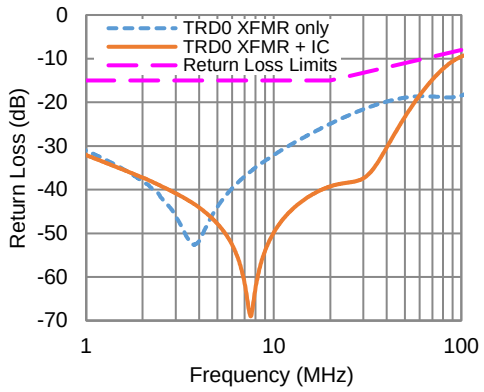
**TRD0 Common Mode Rejection with Typical 3-Core PoE Compatible Transformer using Media Side Choke**



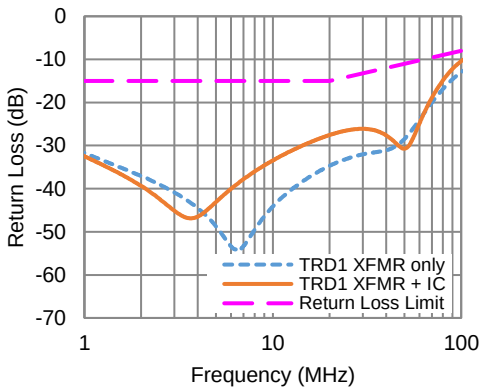

**TRD3 Common Mode Rejection with Typical 3-Core PoE Compatible Transformer using Media Side Choke**



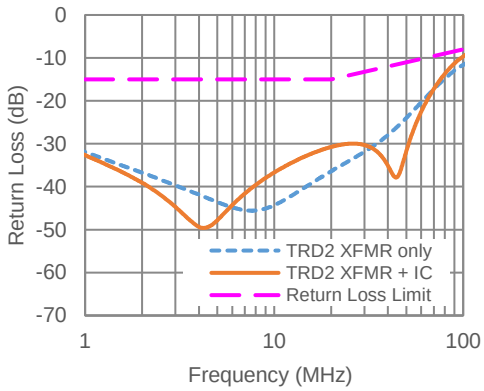

**TRD0 Return Loss with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**



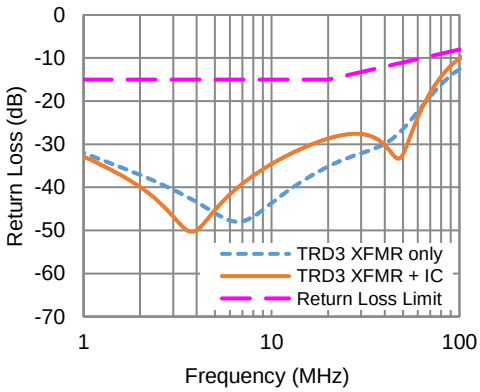

**TRD1 Return Loss with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**




**TRD2 Return Loss with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**



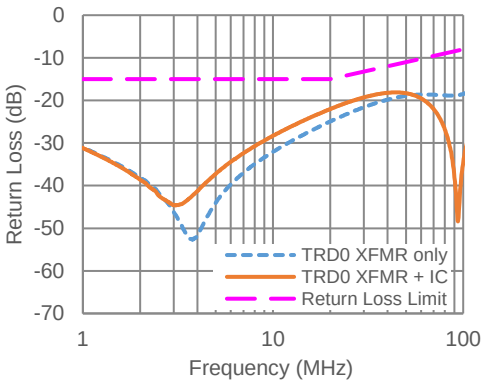

**TRD3 Return Loss with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**



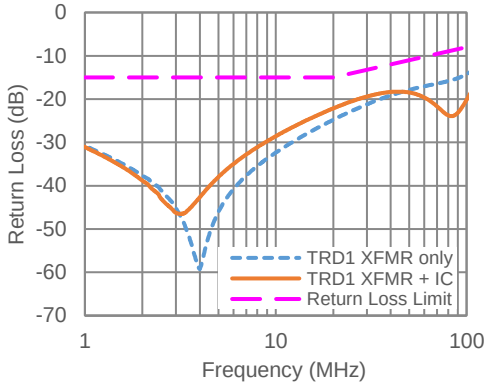
## Typical Characteristics (continued)

$V_{IN}$ = 2.5V, Operating Mode = Mode 1 (default mode), $C_{IN}$ = 10µF, Temp = 25°C unless otherwise specified.

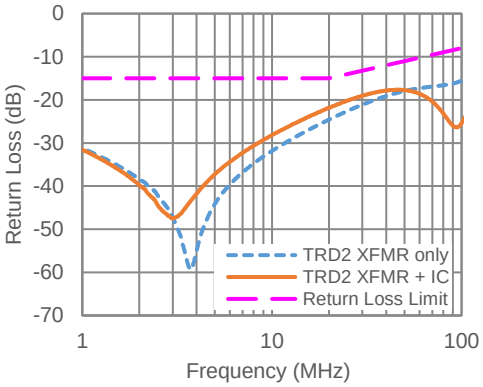
**TRD0 Return Loss with Typical 3-Core PoE Compatible Transformer using Media Side Chokes**



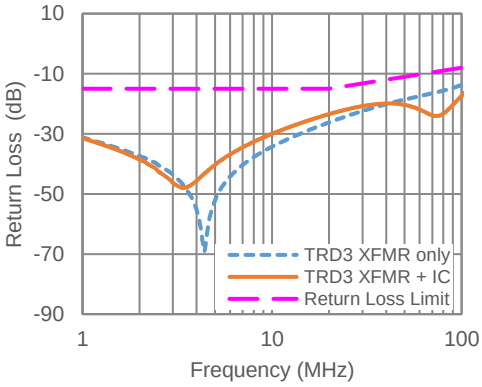

**TRD1 Return Loss with Typical 3-Core PoE Compatible Transformer using Media Side Chokes**



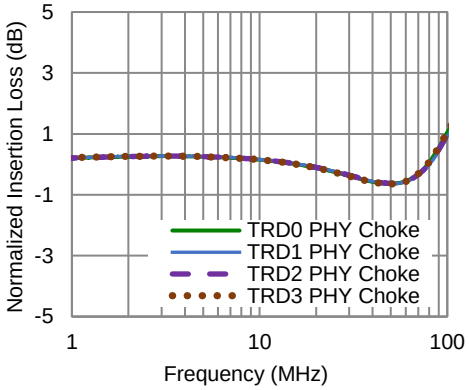

**TRD2 Return Loss with Typical 3-Core PoE Compatible Transformer using Media Side Chokes**



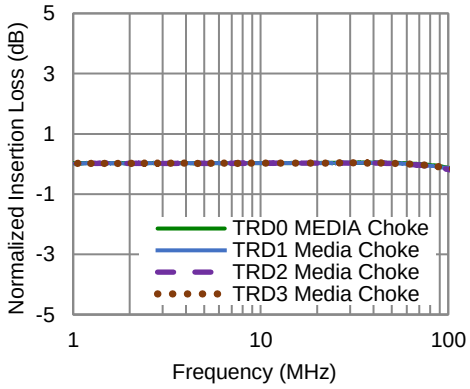

**TRD3 Return Loss with Typical 3-Core PoE Compatible Transformer using Media Side Chokes**




**Insertion Loss with Typical 2-Core PoE Compatible Transformer using 3-Wire PHY-Side Choke**



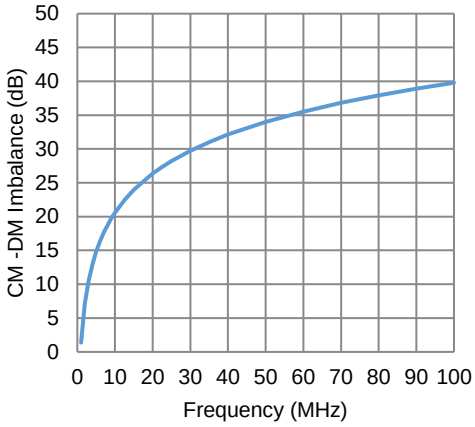

**Insertion Loss with Typical 3-Core PoE Compatible Transformer using Media Side Chokes**



## Typical Characteristics (continued)

$V_{IN}$ = 2.5V, Operating Mode = Mode 1 (default mode), $C_{IN}$ = 10µF, Temp = 25°C unless otherwise specified.

**Common Mode to Differential Mode Imbalance vs Frequency**



## Functional Block Diagram

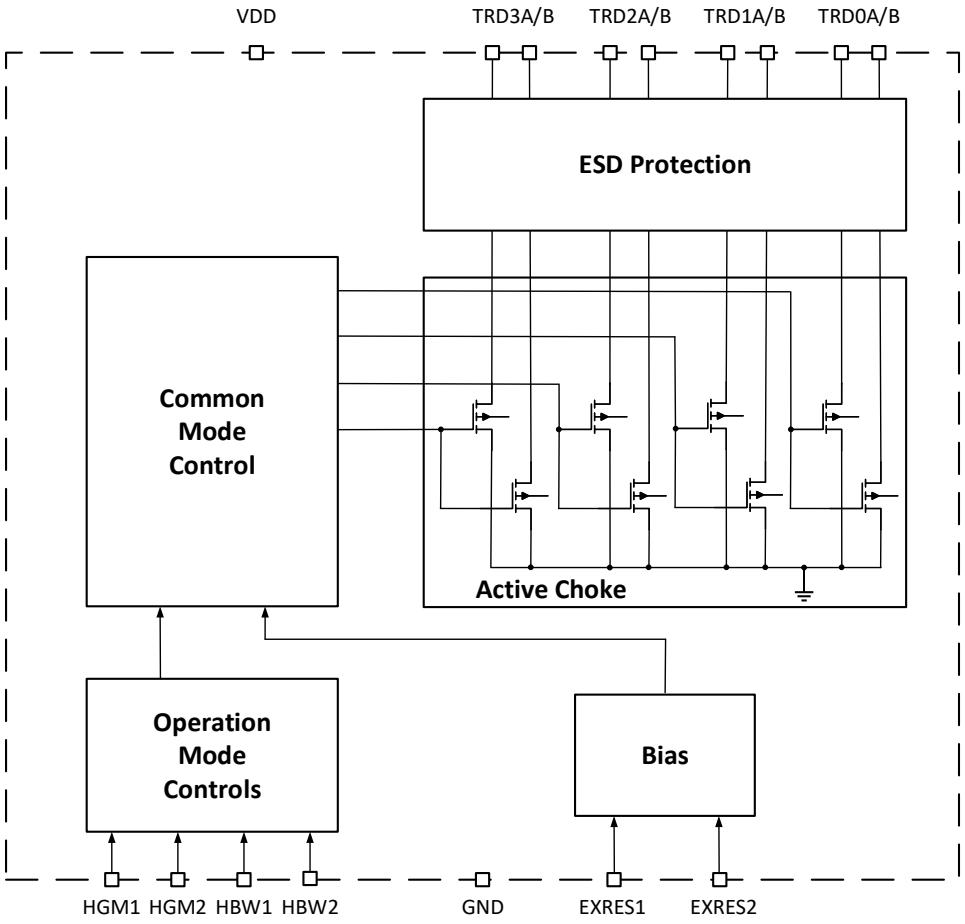



**Figure 1. Block Diagram**

## Functional Description

**Common Mode Noise**

The KTA1552 compensates for many variables that are the source of common mode noise in Ethernet systems. These include: common mode noise from Ethernet PHY DACs and drivers, variations in Ethernet line signals caused by transformer and passive component mismatches, variations in PC board designs, and different vendor PHY designs.

Most Ethernet PHYs use switched mode D/A converters and drivers to transmit complex modulated signals on the twisted pair. There are inherent common mode switching transients that occur in output driver designs. Switched mode drivers coupled with leakage inductance of the line transformer creates a common mode kick. This common mode noise is coupled through to the twisted pair line via transformer interwinding capacitance. This can result in a significant EMI emissions issue for Ethernet systems that desire good margin from CISPR22 and FCC part 15 Class B specifications.

Ethernet transformers provide common mode rejection through PHY-side autoformer and in-line chokes. Mismatches in the autoformer inductance can lead to differential-to-common mode conversion. Parasitic of the autoformer also limit common mode rejection capability. This residual common mode noise is coupled to the line side through interwinding capacitance.

Additional differential to common mode conversion issues come from board layout mismatches and other passive component mismatches on the PCB. Common mode imbalance at the input of the system can create common mode to differential conversion and significantly impact EMI immunity performance.

As a result, meeting system level EMI requirements is very challenging.

**Active Choke Technology**

The KTA1552 incorporates Kinetic Technologies' patented Active Choke technology. The KTA1552 is placed between the Ethernet PHY and the line transformer. Its adaptive circuitry monitors both the positive and negative signals of each differential pair and shunts any common mode noise to ground. As a result, noise is prevented from getting through the transformer to the unshielded twisted-pair (UTP).

The KTA1552 preserves the integrity of the Ethernet signal by providing very low common mode impedance while maintaining high differential impedance and low differential capacitive loading.

The KTA1552 is designed to suppress any common mode noise present in the Ethernet signal pair, irrespective of whether it originates from the PHY side or the UTP side. It provides immunity against large signal common mode events by shunting the common mode signal currents back to ground. Therefore, the Ethernet PHY receiver does not see any common mode movement, enabling it to maintain good link performance.

As shown in Figure 1, the output stage of the KTA1552 uses open-drain drivers similar to the most common Ethernet PHYs. The KTA1552 can tolerate output DC common mode on its TRD pins within a range of 1.8V to 3.3V. This allows the KTA1552 to work seamlessly with any Ethernet PHY and transformer that uses the center-tap to DC-bias the PHY.

The KTA1552 architecture uses high precision active analog circuitry which suppresses only the common mode components of the disturbances without impacting the differential signal. This technology provides superior differential-to-common mode impedance balance over traditional transformer solutions.

The KTA1552 provides low differential capacitive loading to the Ethernet signals and meets all the common mode-to-differential balance and distortion requirements per the 1000 Base-T section of the IEEE® 802.3 Ethernet specification.

**Transient Threats**

Silicon-based electronic devices need protection from spurious events that exert voltage/current stresses exceeding the normal operating limits of the devices. Such events are generally classified as ESD (Electro-Static Discharge) events.

ESD strikes have two modes: differential mode strikes and common mode strikes. Differential mode strikes are strikes which are applied to one pin at a time. These strikes go through the transformer and are the hardest to protect against. Contact/Air Discharge and Cable Discharge event (CDE) can be differential strikes. CDE has become more important in recent years due to advent of cat-5 and better cables. Ethernet cables are frequently dragged across plastic/carpet flooring or through ducts. Charge can accumulate on the cable through triboelectric effect or induction. The newer cat-5 (or better) cables can hold the charge for a longer period of time relative to older cat1-4 cables. As PHY transceivers have been scaling to finer geometry with lower breakdown voltages, their ability to tolerate large cable discharge events is also limited. Plugging a charged cable into RJ45 jack can lead to an over-voltage stress that can damage sensitive PHY devices.

Common mode strikes normally include EFTB (Electrical Fast Transient/Burst) and surge. The first level of protection of common mode strikes is provided by the isolation of the Ethernet transformer.

Both differential mode and common mode strikes have been the major issues for Ethernet equipment. These transient threats can very easily damage the Ethernet PHYs and can also damage the Ethernet transformer if appropriate design precautions are not taken.

**Kinetic ESD Protection Design**

The KTA1552 provides transient protection for both differential mode and common mode ESD events through proprietary CMOS design and layout techniques for low capacitive loading and low inductive effects in protection diodes.

Positive ESD strikes are handled through a stack of diodes that are biased to ensure operation with wide range of VDD and VCT supply voltages and prevent clipping/degradation of Ethernet signals.

Negative ESD strikes are handled through output NMOS bulk diodes, which are also hardened to handle large surge energy. Design prevents snapback of the PHY output NMOS devices by fast turn-on and efficient energy dissipation through ESD structures.

Proprietary design techniques allow the design to handle both moderate energy/fast transients that create high thermal stress as well as high energy/slow transient events that create tremendous voltage overstress.

At the system level, the KTA1552 can tolerate over ±25kV of IEC61000-4-2 air discharge strikes and ±12kV of Cable Discharge Events, and provides protection for Ethernet PHY

**Performance/Power Control Pins**

EMI performance varies significantly from system to system. The KTA1552 provides digital pins (HGM1, HGM2, HBW1 and HBW2) that allow various levels of hardware control and performance optimization of the device. The HGM(1/2) and HBW(1/2) are 3-input state pins (Low, High and Floating). The Floating state is detected internally by the device as a valid state. For default operation, both pins should be left floating. These pins can be driven by another digital IC with tri-state able outputs or tied in hardware to configure the desired operating mode. In all cases, both HGW pins and HBW pins must be programmed to the same state.

**HGM1/HGM2 Pins**

The default configuration is to leave the HGM pins floating which provides a trade-off between CM rejection performance and device power consumption.

If less rejection is needed in the Ethernet path, the HGM pins should be pulled LOW to select the Low Power Mode. In Low Power Mode, device power consumption is reduced by about 40% and CMRR performance is reduced by approximately 1dB at 100MHz.

**HBW1/HBW2 Pins**

Setting the HBW pins HIGH selects HBW mode which allows system designers another dimension to improve performance by increasing the bandwidth of the internal active circuits. In some systems, this can provide additional performance benefits.

There is a broad range of line transformers that can be used in Ethernet applications. Setting HBW mode may cause oscillations in some systems depending on transformer parasitic. Therefore, HBW mode should only be used if the performance improvement of the default setting (HBW(1/2) pins = Floating) is not adequate. Ethernet electrical performance should be tested sufficiently to ensure that no oscillatory behavior is seen when using the HBW mode setting.

HBW mode will typically improve the CMRR performance by approximately 1dB at 100MHz.

Note that the HBW mode can be used in conjunction with the HGM pin’s Low Power mode.

Additional performance/power modulation can be achieved by changing the external bias resistors value (EXRES1/EXRES2). For detailed characterization across operating modes, please refer to the relevant application note document.

## SYSTEM DESIGN & LAYOUT CONSIDERATIONS

### KTA1552 Placement

The KTA1552 is designed to mate closely with Ethernet magnetics for ease of board design. The KTA1552 should be placed physically near the Ethernet transformer or integrated magnetics jack. Placement on same side of the PC-board as the transformer and the PHY is recommended to avoid vias on the Ethernet traces. The KTA1552 should be placed such that pin 1 is facing the transformer or integrated magnetics jack.

### Ethernet Signal Polarity Interchangeability

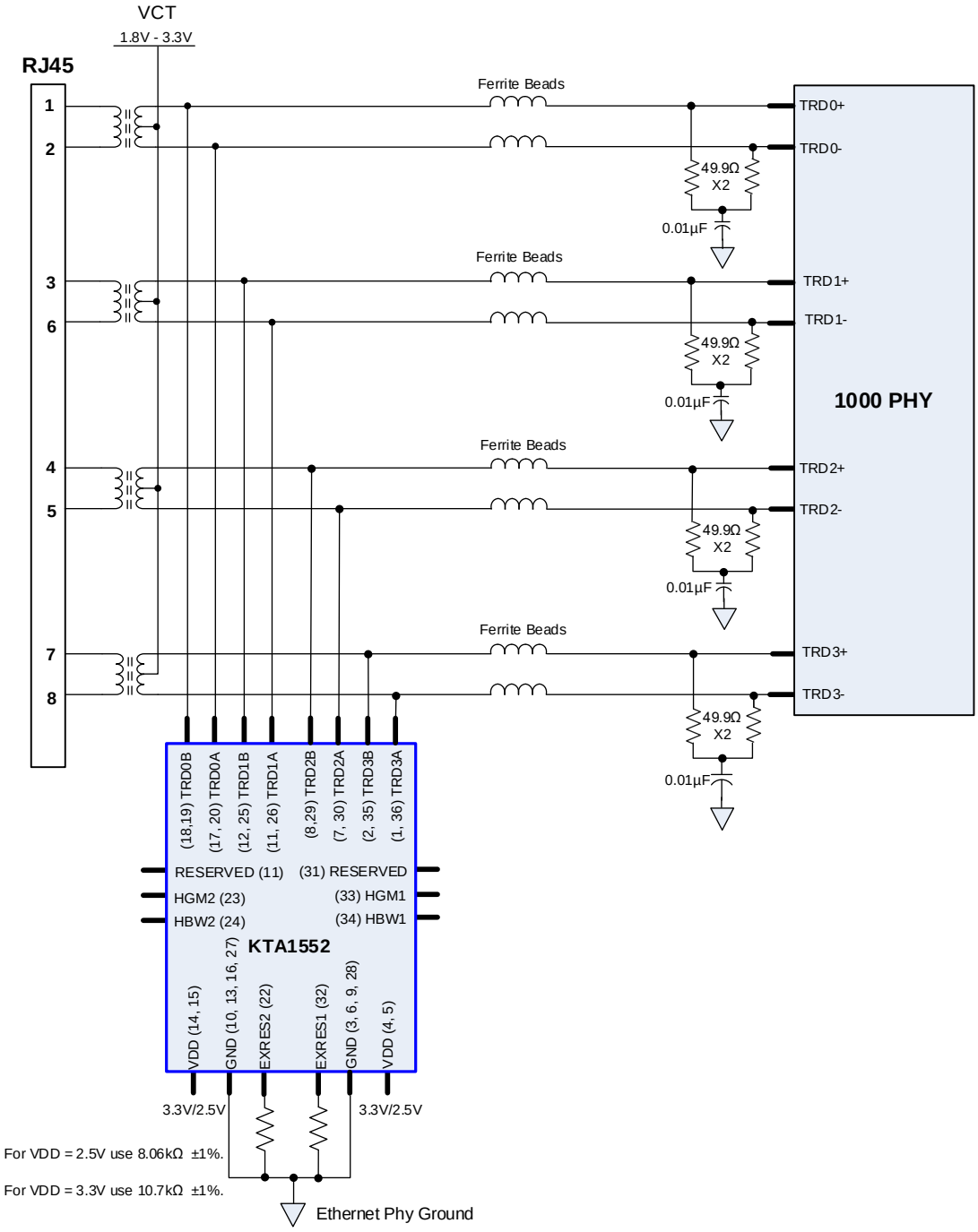
The KTA1552 extracts only the common mode component of the Ethernet signals for processing. As a result, the polarity of the Ethernet signals to the KTA1552 does not matter. This allows system designers to connect either the positive or negative polarity Ethernet signals to either the TRDnA or TRDnB pins - whichever is convenient for board routing and avoids the necessity of swapping the signals and the use of via insertions.

## ETHERNET SIGNAL FLOW-THROUGH ROUTING

KTA1552 is packaged to allow flow-through routing of the Ethernet differential pairs. Only one side of the package's Ethernet pins (1, 2, 7, 8, 11, 12, 17 & 18) are internally electrically connected to the CM rejection circuitry. Mirrored pins (36, 35, 30, 29, 26, 25, 20 & 19 respectively) are given the same name to enable easy flow-through routing with PC-board design tools.

For a more detailed discussion on designing with the KTA1552 and layout considerations, please reference available design guide and application note

## Application Information

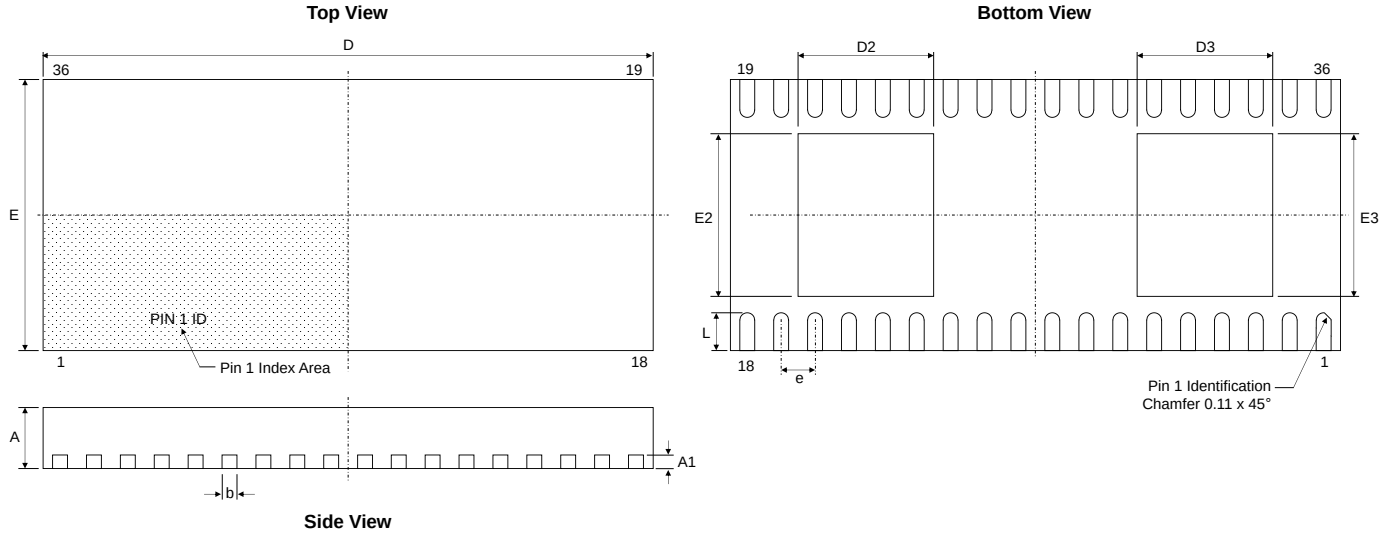



NOTE: *This diagram is preliminary and subject to change at any time. It may not contain all information necessary to implement the application it represents. Please refer to application notes for details.*

**Figure 2. Typical GE Application Circuit**

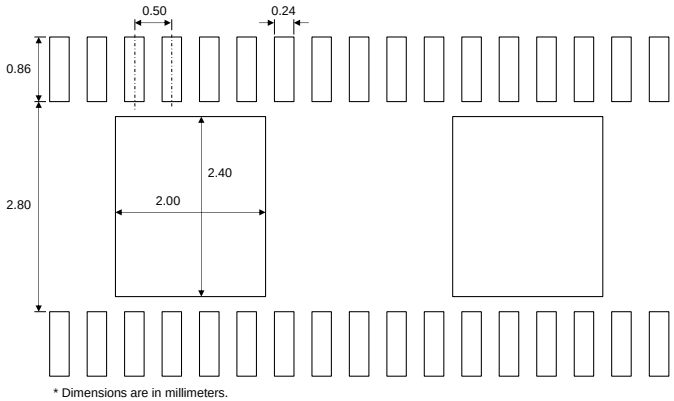
# Packaging Information

## DFN94-36 (9.00mm x 4.00mm x 0.90mm)




| Dimension | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.85 | 0.90 | 0.95 |
| A1 | 0.203 REF | | |
| b | 0.17 | 0.22 | 0.27 |
| D | 8.90 | 9.00 | 9.10 |
| D2 | 1.95 | 2.00 | 2.05 |
| D3 | 1.95 | 2.00 | 2.05 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.35 | 2.40 | 2.45 |
| E3 | 2.35 | 2.40 | 2.45 |
| e | 0.50 BSC | | |
| L | 0.50 | 0.55 | 0.60 |

## Recommended Footprint



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