MXD8668C

SP6T Switch with MIPI for LTE Diversity

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General Description

The MXD8668C is a low loss, high isolation SP6T switch for antenna diversity receiving.

The MXD8668C is compatible with MIPI control, which is a key requirement for many cellular transceivers. This part is packaged in a compact 2mm x 2mm, 14-pin, QFN package which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Features

- Excellent insertion loss
  - 0.50 dB Insertion Loss at 2.7GHz
- P0.1dB @ 27dBm
- Multi-Band operation 700MHz to 3000MHz
- RFFE serial control interface
- Compact 2mm x 2mm in QFN-14 package
- No DC blocking capacitors required (unless external DC is applied to the RF ports)

Applications

- 2G/3G/4G antenna diversity
- Cellular modems and USB Devices

Functional Block Diagram and Pin Function

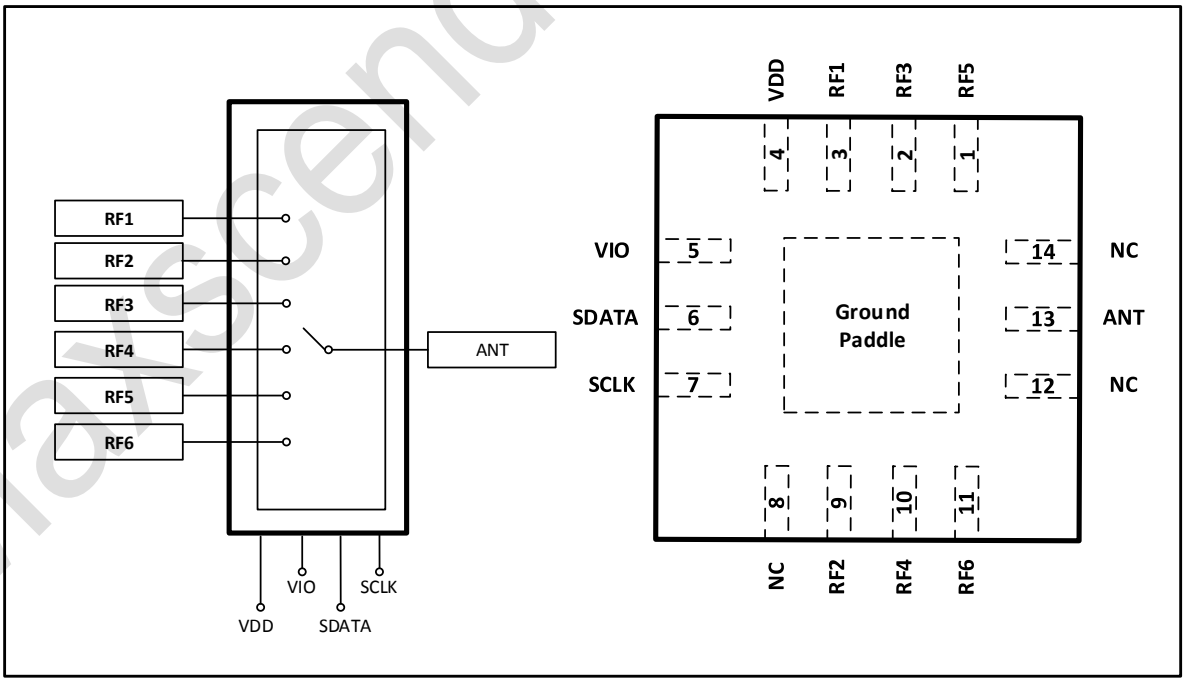

Figure 1. Functional Block Diagram and Pinout (Top View)

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Application Circuit

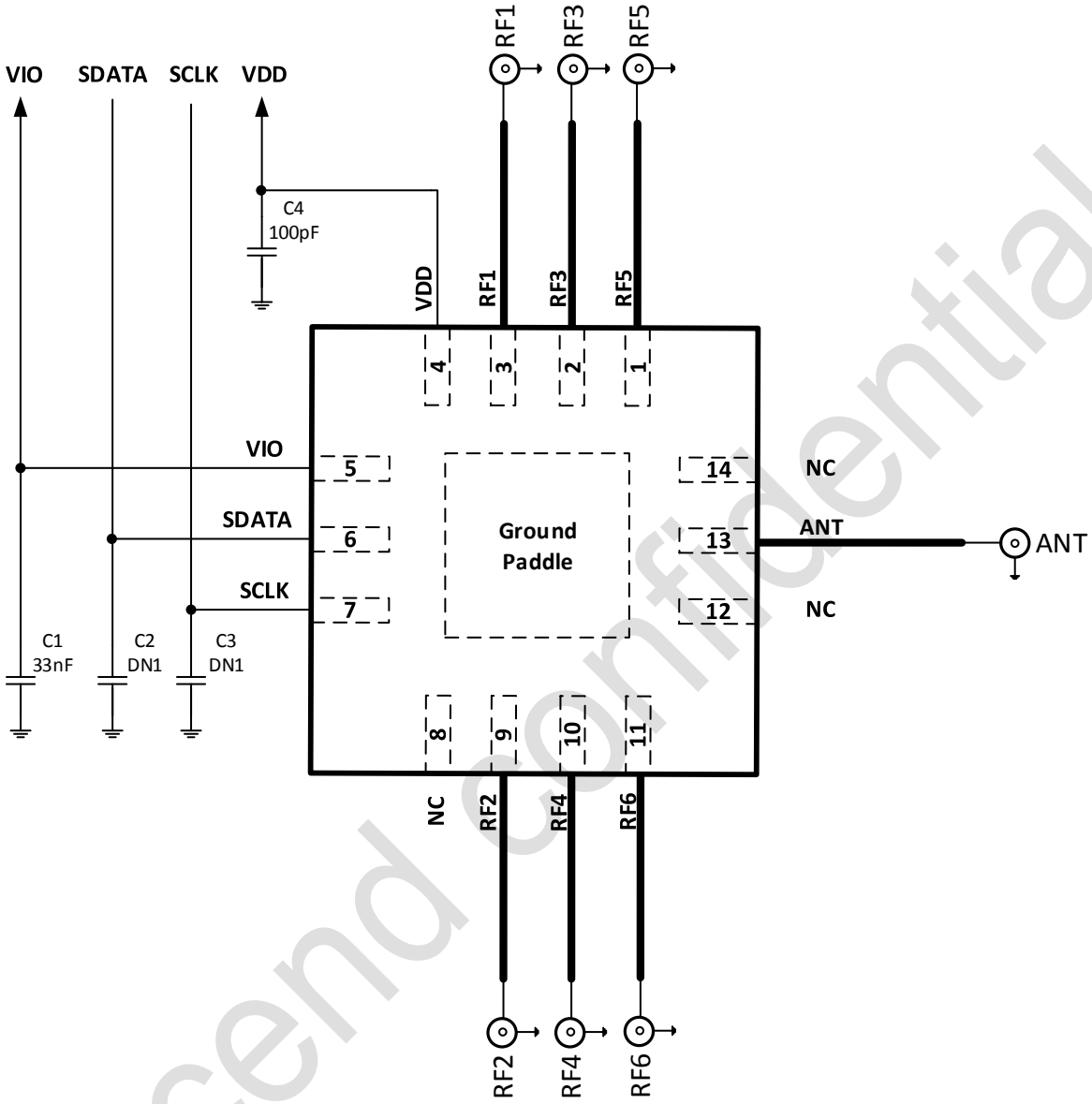

Figure 2. Evaluation Board Schematic

Table 1. Pin Description

Pin No.	Name	Description	Pin No.	Name	Description
1	RF5	RF port5	8	NC	-
2	RF3	RF port3	9	RF2	RF port2
3	RF1	RF port1	10	RF4	RF port4
4	VDD	Power supply	11	RF6	RF port6
5	VIO	Supply voltage for MIPI	12	NC	-
6	SDATA	MIPI data input/output	13	ANT	Antenna port
7	SCLK	MIPI clock	14	NC	-
Ground Paddle	GND	Ground			

Note: Bottom ground paddles must be connected to ground.

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Truth Table

Table 2.

Control	Switched RF Outputs					
Register_0	**RF1**	**RF2**	**RF3**	**RF4**	**RF5**	**RF6**
0x00	**Insertion Loss**	Isolation	Isolation	Isolation	Isolation	Isolation
0x01	Isolation	**Insertion Loss**	Isolation	Isolation	Isolation	Isolation
0x02	Isolation	Isolation	**Insertion Loss**	Isolation	Isolation	Isolation
0x03	Isolation	Isolation	Isolation	**Insertion Loss**	Isolation	Isolation
0x04	Isolation	Isolation	Isolation	Isolation	**Insertion Loss**	Isolation
0x05	Isolation	Isolation	Isolation	Isolation	Isolation	**Insertion Loss**
0x06	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation
0x07	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation

Recommended Operation Range

Table 3. Recommended Operation Condition

Parameters	Symbol	Min	Typ	Max	Units
Operation Frequency	f1	0.7	-	3.0	GHz
Power supply	V_{DD}	2.5	2.8	3.0	V
Power supply for MIPI	V_{IO}	1.65	1.8	1.95	V
MIPI Control Voltage High	V_H	0.8*VIO	1.8	1.95	V
MIPI Control Voltage Low	V_L	0	0	0.3	V

Specifications

Table 4. Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
DC Specifications						
Supply voltage	V_{DD}		2.5	2.8	3.0	V
Supply current	I_{DD}			30	50	uA
V_{IO} supply voltage	V_{IO}		1.65	1.8	1.95	V
V_{IO} Supply current	I_{IO}			4	10	uA
SDATA, SCLK control voltage: High Low	V_{CTL_H} V_{CTL_L}		0.8* V_{IO} 0	V_{IO} 0	1.95 0.3	V V
Switching Speed, one RF to another		10% to 90% RF		1	2	uS
RF Specifications						
Insertion loss (ANT pin to RF1/2/3/4/5/6 pins)	IL	0.1 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 2.7 GHz		0.30 0.40 0.50		dB dB dB
Isolation (ANT pin to RF1/2/3/4/5/6 pins)	Iso	0.1 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 2.7 GHz	35 25 20	40 30 24		dB dB dB
Input return loss (ANT pin to RF1/2/3/4/5/6 pins)	RL	0.1 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 2.7 GHz	20 15 12	25 20 15		dB dB dB
0.1 dB Compression Point (ANT pin to RF1/2/3/4/5/6 pins)	P0.1dB	0.7 GHz to 3.0 GHz		+27		dBm
2nd Harmonic	2f0	900MHz, 1800MHz, +10dBm	-73	-78		dBc
3rd Harmonic	3f0	900MHz, 1800MHz, +10dBm	-93	-95		dBc

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MIPI Read and Write Timing

MIPI supports the following Command Sequences:

• Register Write

• Register_0 Write

• Register Read

Figures 3 and 4 provide the timing diagrams for register write commands and read commands, respectively. Figure 5 shows the Register 0 Write Command Sequence. Refer to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), v1.10 (26 July 2011) for additional information on MIPI USID programming sequences and MIPI bus specifications.

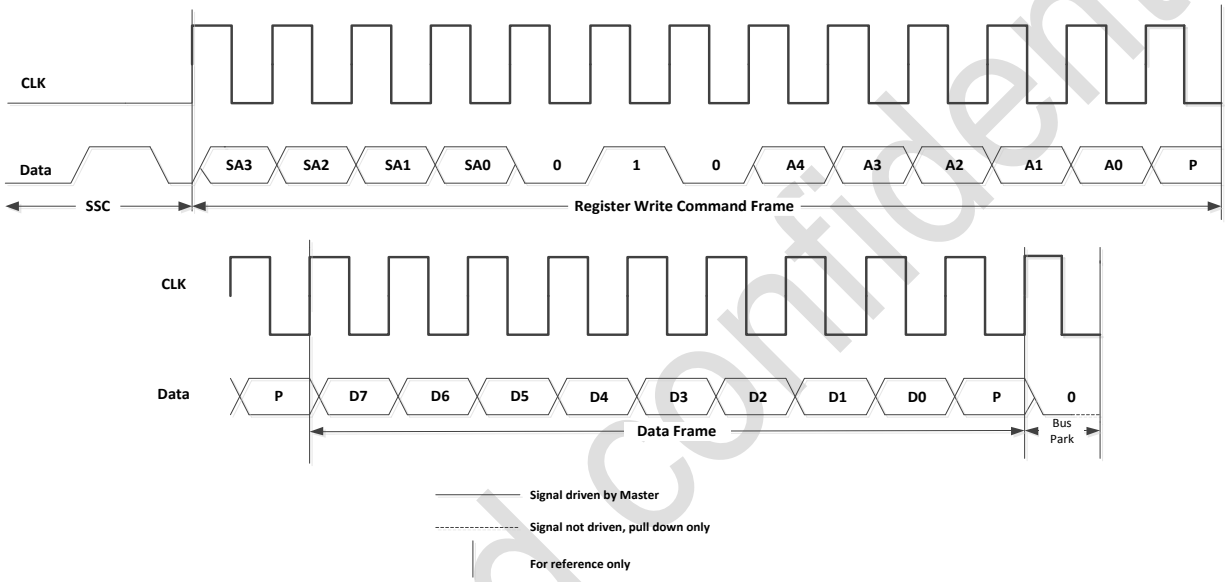

Figure 3. Register Write Command Sequence

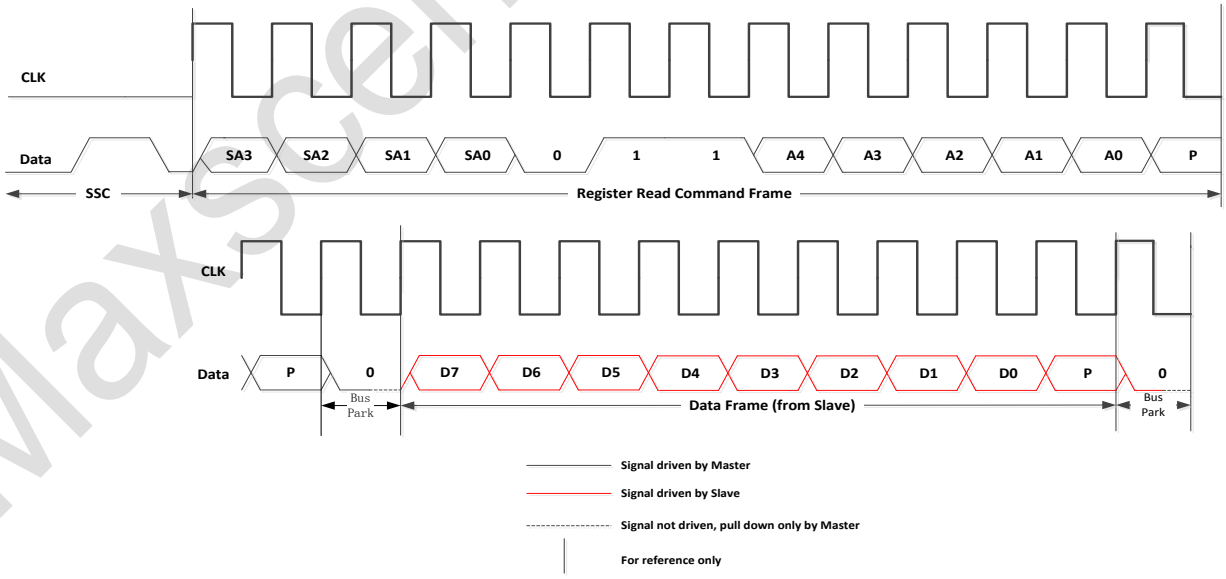

Figure 4. Register Read Command Sequence

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In the timing figures, SA[3:0] is slave address. A[4:0] is register address. D[7:0] is data. “P” is odd parity bit.

Register 0 Write Command Sequence

Figure shows the Register 0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic one, and a seven bit word to be written to Register 0. The Command Sequence ends with a Bus Park Cycle.

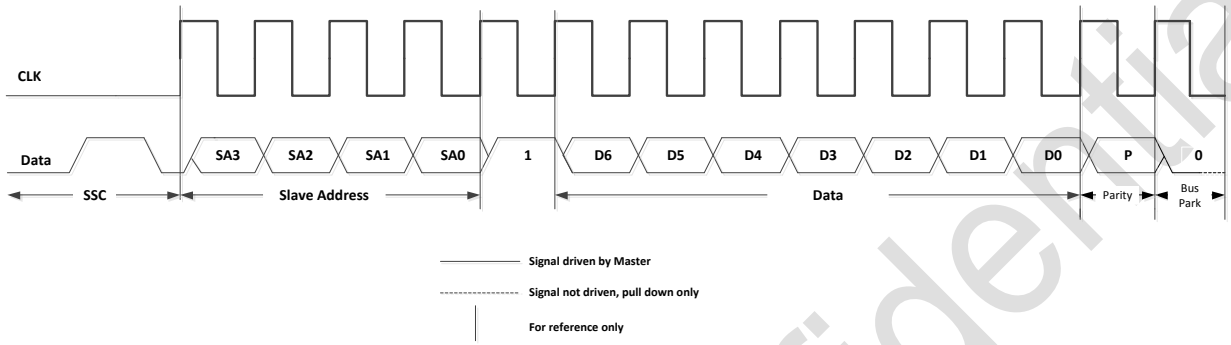

Figure 5. Register 0 Write Command Sequence

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Register definition

Table 5. Register definition table

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x00	REGISTER_0	7:0	R/W	RF Control	Register_0 truth Table: Table 2	0x00	No	Yes
0x001A	RFFE_STATUS	7	R/W	SOFTWARE RESET	0: Normal operation 1: Software reset Note: On software reset, this register and all configurable registers are reset except for USID, GSID, and PM_TRIG.	0	No	No
		6	R/W	COMMAND_FRAME_PARITY_ERR	Command Frame with parity error	0	No	No
		5	R/W	COMMAND_LENGTH_ERR	Command Sequence with incorrect length	0	No	No
		4	R/W	ADDRESS_FRAME_PARITY_ERR	Address Frame with parity error	0	No	No
		3	R/W	DATA_FRAME_PARITY_ERR	Data Frame with parity error	0	No	No
		2	R/W	READ_UNUSED_REG	Read Command Sequence to an invalid address	0	No	No
		1	R/W	WRITE_UNUSED_REG	Write Command Sequence to an invalid address	0	No	No
		0	R/W	BID_GID_ERR	Read Command Sequence with a BSID or GSID Note: Reading this register resets this register.	0	No	No
0x001B	GROUP_SID	7:4	R	RESERVED		0x0	No	No
		3:0	R/W	GSID	Group Slave ID	0x0	No	No
0x001C	PM_TRIG	7:6	R/W	PWR_MODE	00: Normal Operation (ACTIVE) 01: Reset all registers to default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved Note: Write PWR_MODE=2'h1 will reset all register, and puts the device into STARTUP state.	0b10	Yes	No
		5	R/W	Trigger_Mask_2	If this bit is set, trigger 2 is disabled	0	No	No
		4	R/W	Trigger_Mask_1	If this bit is set, trigger 1 is disabled	0	No	No
		3	R/W	Trigger_Mask_0	If this bit is set, trigger 0 is disabled Note: When all triggers are disabled, writing to a register that is associated with trigger 0, 1, or 2, causes the data to go directly to the destination register.	0	No	No
		2	W	Trigger_2	A write of a one to this bit loads trigger 2's registers	0	Yes	No
		1	W	Trigger_1	A write of a one to this bit loads trigger 1's registers	0	Yes	No
		0	W	Trigger_0	A write of a one to this bit loads trigger 0's registers Note: Trigger processed immediately then cleared. Trigger 0, 1, and 2 will always read as 0.	0	Yes	No
0x001D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x5c	No	No
0x001E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x81	No	No
0x001F	MAN_USID	7:6	R	RESERVED		0b00	No	No
		5:4	R	MANUFACTURER_ID[9:8]	Upper two bits of MIPI registered Manufacturer ID	0b11	No	No
		3:0	R/W	USID	USID of the device.	0xb	No	No

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Absolute Maximum Ratings

Table 6. Maximum ratings

Parameters	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}	+2.0	+3.3	V
Supply voltage for MIPI	V_{IO}	+1.0	+2.0	V
MIPI Control voltage (SDATA, SCLK)	V_{CTL}	0	+2.0	V
RF input power (RF1 to RF6)	P_{IN}		+28	dBm
Operating temperature	T_{OP}	–20	+85	℃
Storage temperature	T_{STG}	–40	+125	℃
Electrostatic Discharge Human body model (HBM), Class 1C Machine Model (MM), Class A Charged device model (CDM), Class III	 ESD_HBM ESD_MM ESD_CDM		 1000 100 500	 V

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device

Power ON and OFF sequence

Here is the recommendation about power-on/off sequence in order to avoid damaging the device.

Power ON

1) Apply voltage supply - V_{DD}

2) Apply logic supply - V_{IO}

3) Wait 10μs or greater and then apply MIPI bus signals – SCLK and SDATA

4) Wait 5μs or greater after MIPI bus goes idle and then apply the RF Signal

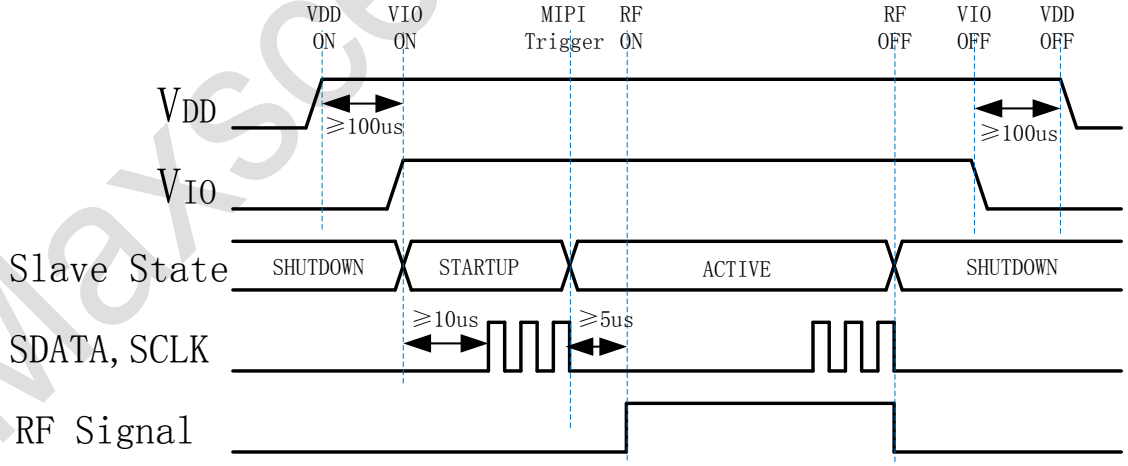
Power OFF

1) Remove the RF Signal

2) Remove MIPI bus – SCLK and SDATA

3) Remove logic supply - V_{IO}

4) Remove voltage supply - V_{DD}



Note: VIO can be applied to the device before VDD or removed after VDD.

It is important to wait 10μs after VIO & VDD are applied before sending SDATA to ensure correction data transmission.

The minimum time between a power up and power down sequence (and vice versa) is ≥ 100us.

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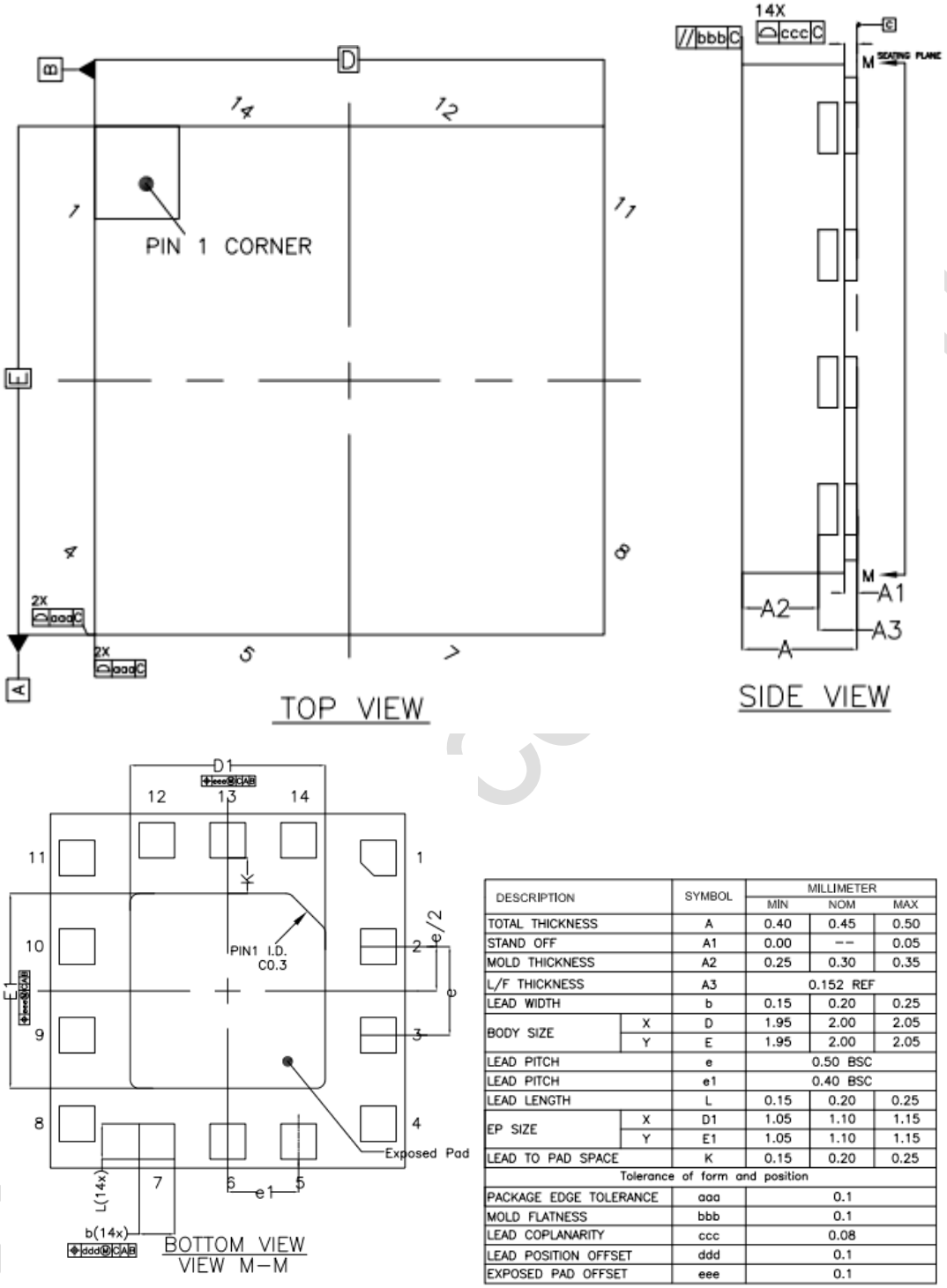
Package Outline Dimension



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.40	0.45	0.50
STAND OFF		A1	0.00	--	0.05
MOLD THICKNESS		A2	0.25	0.30	0.35
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D	1.95	2.00	2.05
	Y	E	1.95	2.00	2.05
LEAD PITCH		e		0.50 BSC	
LEAD PITCH		e1		0.40 BSC	
LEAD LENGTH		L	0.15	0.20	0.25
EP SIZE	X	D1	1.05	1.10	1.15
	Y	E1	1.05	1.10	1.15
LEAD TO PAD SPACE		K	0.15	0.20	0.25
Tolerance of form and position					
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
LEAD COPLANARITY		ccc		0.08	
LEAD POSITION OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 6. package outline dimension

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Reflow Chart

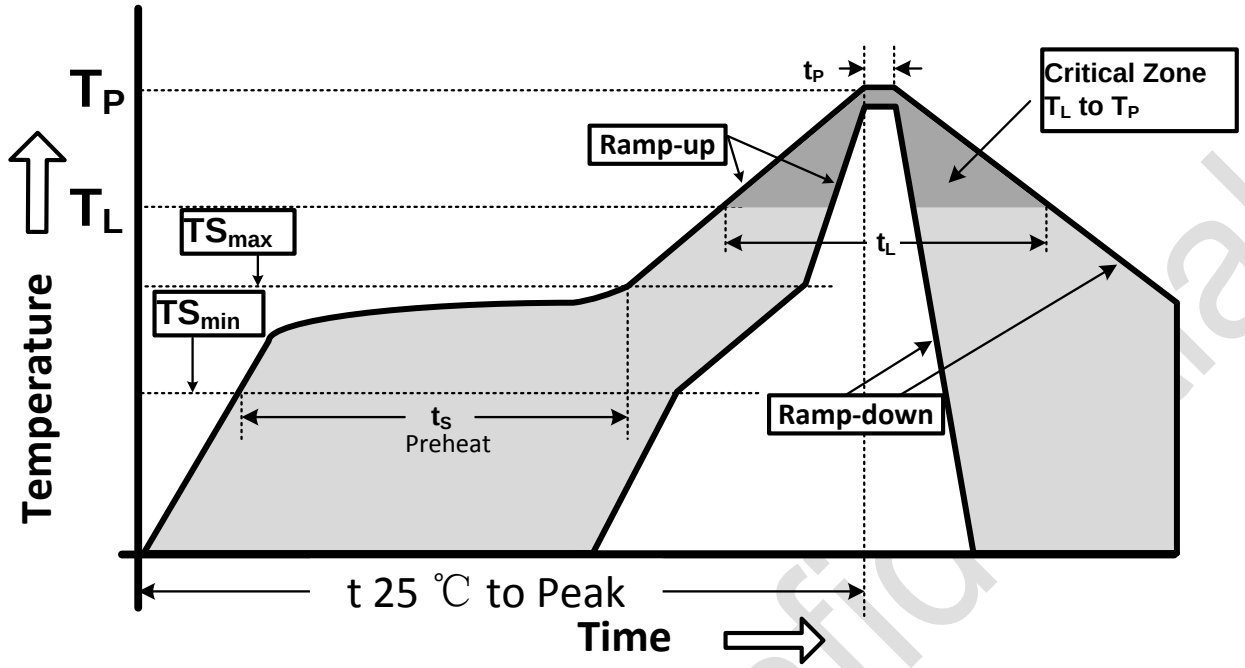

Figure 7. Recommended Lead-Free Reflow Profile

Table 7. Reflow condition

Profile Parameter	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate（TS_{max} to T_p）	3℃/second max.
Preheat temperature（TS_{min} to TS_{max}）	150℃ to 200℃
Preheat time（t_s）	60 - 180 seconds
Time above TL , 217℃（t_L）	60 - 150 seconds
Peak temperature（T_p）	260℃
Time within 5℃ of peak temperature(t_p)	20 - 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be used when handling these devices.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.

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