Low Skew, Low Additive Jitter, 4 Output LVPECL/LVDS/HCSL Fanout Buffer with one LVCMOS output

Features

- 3 to 1 input Multiplexer: Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a single ended signal and the third input accepts a crystal or a single ended signal
- Four differential LVPECL/LVDS/HCSL outputs
- One LVCMOS output
- Ultra-low additive jitter: 24fs (in 12kHz to 20MHz integration band at 625MHz clock frequency)
- Supports clock frequencies from 0 to 1.6GHz
- Supports 2.5V or 3.3V power supplies for LVPECL, LVDS or HCSL outputs
- Supports 1.5V, 1.8V, 2.5V or 3.3V for LVCMOS output
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 40ps
- Device controlled via control pins

Ordering Information

ZL40234LDG1	32 pin QFN	Trays
ZL40234LDF1	32 pin QFN	Tape and Reel

Package size: 5 x 5 mm

-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3/4 clock distribution
- Wireless communications
- High performance microprocessor clock distribution
- Test Equipment

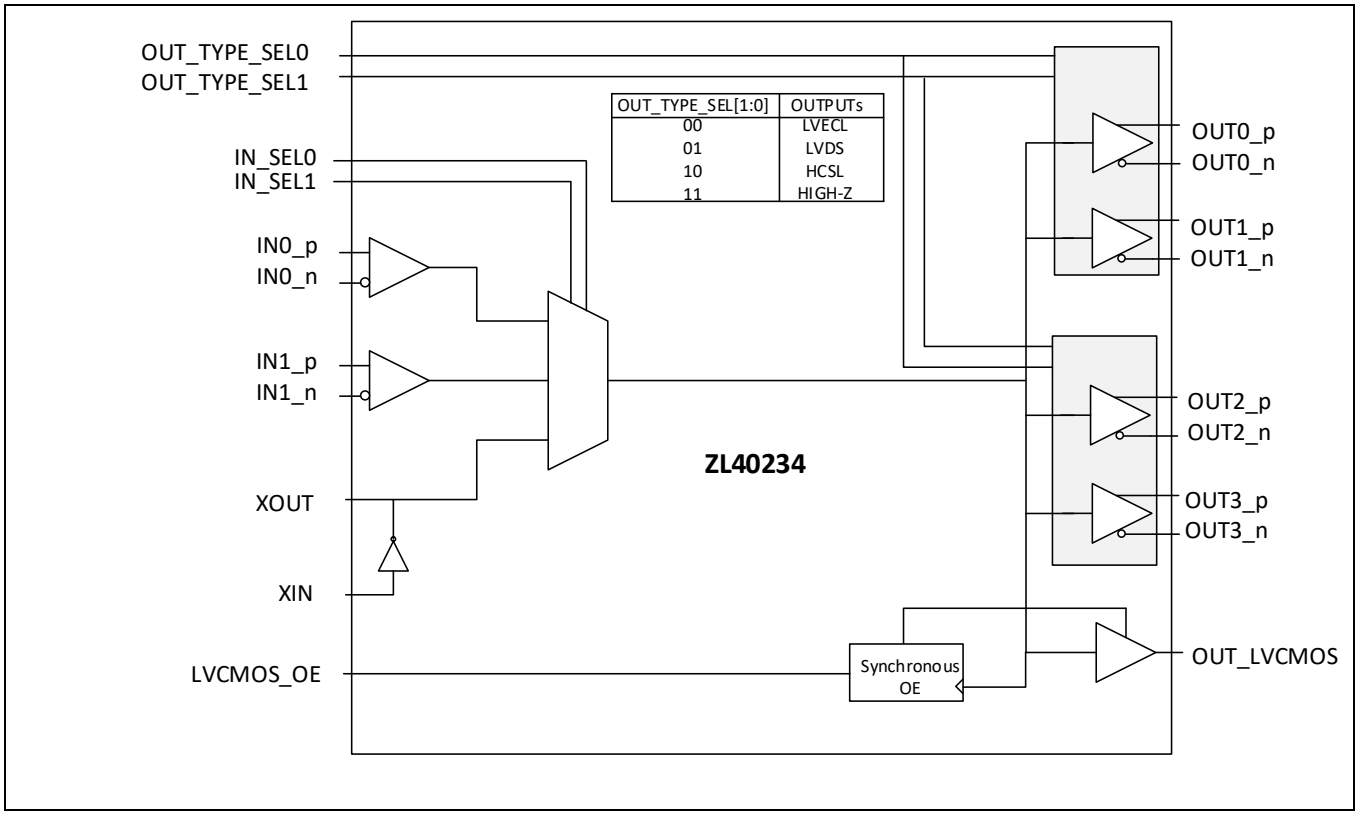

Figure 1. Functional Block Diagram

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Pin Diagram

The device is packaged in a 5x5mm 32-pin QFN.

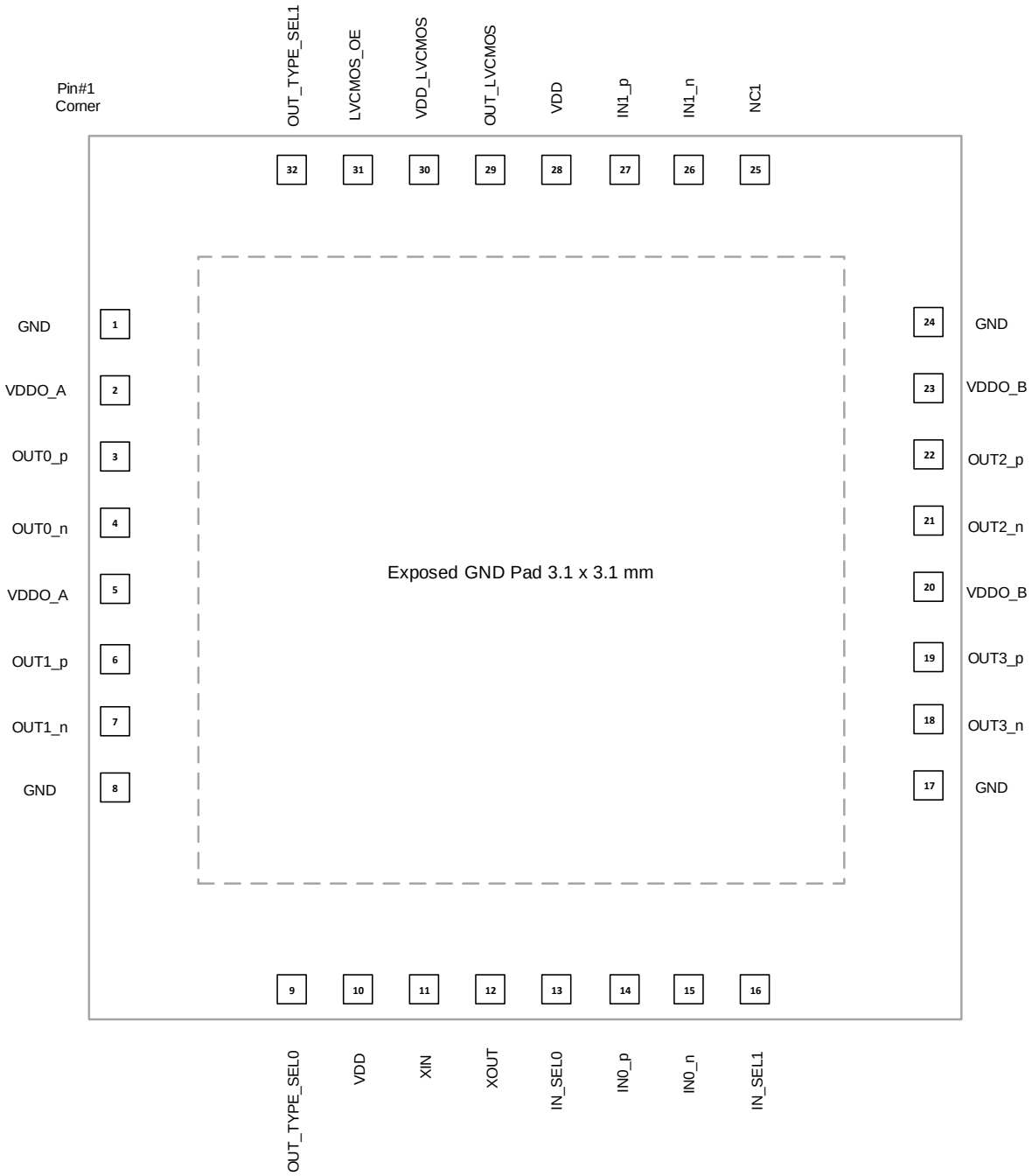


Figure 2. Pin Diagram

Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300kΩ internal pull-up resistor, I_{PD} – input with 300kΩ internal pull-down resistor, I_{APU} – input with 31kΩ internal pull-up resistor, I_{APD} – input with 30kΩ internal pull-down resistor, $I_{APU/APD}$ – input biased to VDD/2 with 60kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC-No connect pin, P – power supply pin.

Table 1Pin Descriptions

#	Name	I/O	Description
Input Reference			
14 15 27 26	IN0_p IN0_n IN1_p IN1_n	I_{APD} $I_{APU/APD}$ I_{APD} $I_{APU/APD}$	**Input Differential or Single Ended References 0 and 1** Input frequency range 0Hz to 1.6GHz. Non- inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60kΩ internal resistors (30kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).
Output Clocks			
3 4 6 7 22 21 19 18	OUT0_p OUT0_n OUT1_p OUT1_n OUT2_p OUT2_n OUT3_p OUT3_n	O	**Ultra-Low Additive Jitter Differential LVPECL/HCSL/LVDS Outputs 0 to 3** Output frequency range 0 to 1.6GHz Type (LVPECL/HCSL/LVDS/High-Z) of the outputs is controlled by OUT_TYPE_SEL0/1 pins.
29	OUT_LVCMOS	O	**Ultra-Low Additive Jitter LVCMOS Output** Output frequency range 0 to 250 MHz
Control			
13 16	IN_SEL0 IN_SEL1	I_{PD}	**Input select pins.** Logic level on these pins selects which input will be passed to the output.

IN_SEL1	IN_SEL0	OUTN
0	0	Input 0 (IN0)
0	1	Input 1 (IN1)
1	X	Crystal Oscillator

<table>
<tr><td>9
32</td><td>OUT_TYPE_SEL0
OUT_TYPE_SEL1</td><td>I</td><td>Output Signal Level: Selects Type of the outputs (Outputs 0 to 4)
<table><tr><th>OUT_TYPE_SEL1</th><th>OUT_TYPE_SEL0</th><th>Output 0 to 4</th></tr><tr><td>0</td><td>0</td><td>LVPECL</td></tr><tr><td>0</td><td>1</td><td>LVDS</td></tr><tr><td>1</td><td>0</td><td>HCSL</td></tr><tr><td>1</td><td>1</td><td>High-Z (Disabled)</td></tr></table></td></tr>
<tr><td>31</td><td>LVCMOS_OE</td><td>I</td><td>LVCMOS Output Enable: When high LVCMOS output is enabled,. When low the output is High-Z.</td></tr>
<tr><td colspan="4">Crystal Oscillator</td></tr>
<tr><td>11</td><td>XIN</td><td>I</td><td>Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode
If crystal oscillator is not used pull down this pin or connect it to the ground.</td></tr>
<tr><td>12</td><td>XOUT</td><td>O</td><td>Crystal Oscillator Output</td></tr>
<tr><td colspan="4">No Connect</td></tr>
<tr><td>25</td><td>NC1</td><td>NC</td><td>No Connects (not connected to the die) Leave unconnected or connect to GND for mechanical support</td></tr>
<tr><td colspan="4">Power and Ground</td></tr>
<tr><td>10
28</td><td>VDD</td><td>P</td><td>Positive Supply Voltage. Connect to 3.3V or 2.5V supply.</td></tr>
<tr><td>30</td><td>VDD_LVCMOS</td><td>P</td><td>Positive Supply Voltage for LVCMOS Output Connect to 3.3V, 2.5V, 1.8V or 1.5V supply</td></tr>
<tr><td>2
5</td><td>VDDO_A</td><td>P</td><td>Positive Supply Voltage for Differential Outputs Bank A Connect 3.3V or 2.5V power supply. VDDO_A does not have to be connected to the same voltage level as VDD or VDDO_B.
These pins power up differential outputs OUT0_p/n and OUT1_p/n.</td></tr>
<tr><td>20
23</td><td>VDDO_B</td><td></td><td>Positive Supply Voltage for Differential Outputs Bank B Connect 3.3V or 2.5V power supply. VDDO_B does not have to be connected to the same voltage level as VDD or VDDO_A.
These pins power up differential outputs OUT2_p/n and OUT3_p/n.</td></tr>
<tr><td>1
8
17
24</td><td>GND</td><td>P</td><td>Ground Connect to the ground</td></tr>
<tr><td>E-Pad</td><td>GND</td><td>P</td><td>Ground. Connect to the ground</td></tr>
</table>

Functional Description

The ZL40234 is a pin configurable low additive jitter, low power 3 x 4 LVPECL/HCSL/LVDS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins.

The ZL40234 has four LVPECL/HCSL/LVDS outputs in two banks and each bank can independently be powered from 3.3V or 2.5V supply. Differential outputs can be set to be LVPECL, LVDS, HCSL or Hi-Z via control OUT_TYPE_SEL0/1 pins.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40234 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and Ro + Rs should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 7). The source resistors of Rs = 270Ω could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16mA.
For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

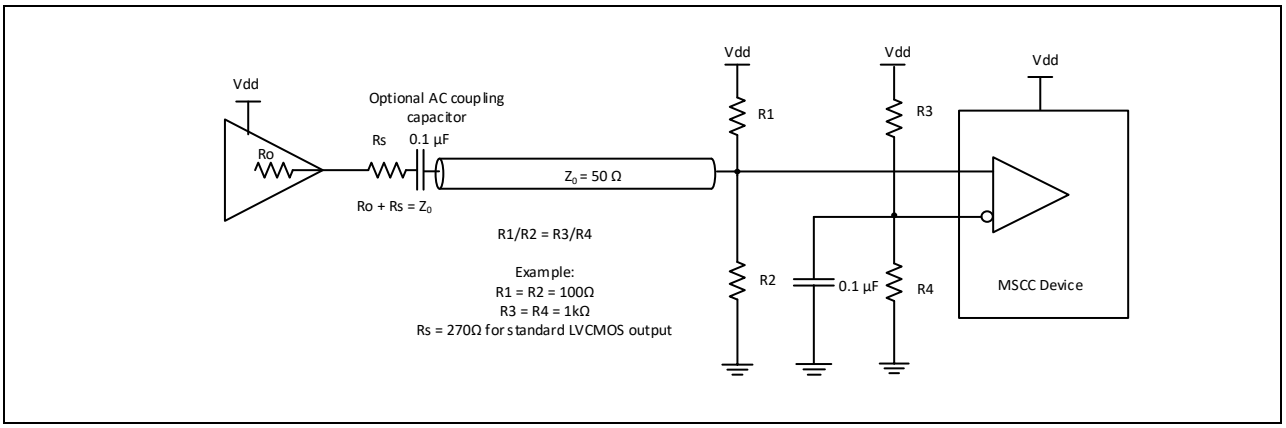


Figure 3. Input driven by a single ended output

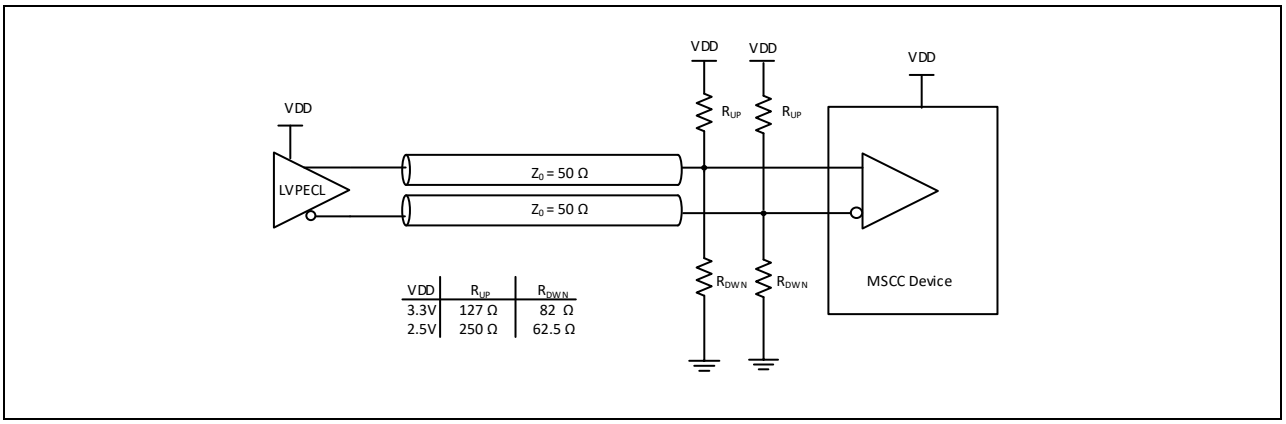


Figure 4. Input driven by DC coupled LVPECL output

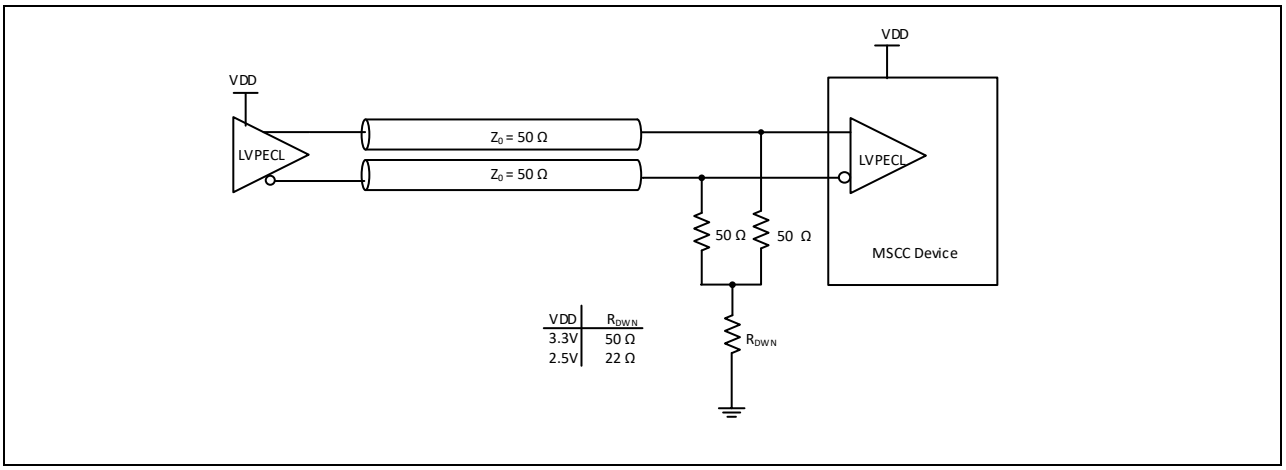


Figure 5. Input driven by DC coupled LVPECL output (alternative termination)

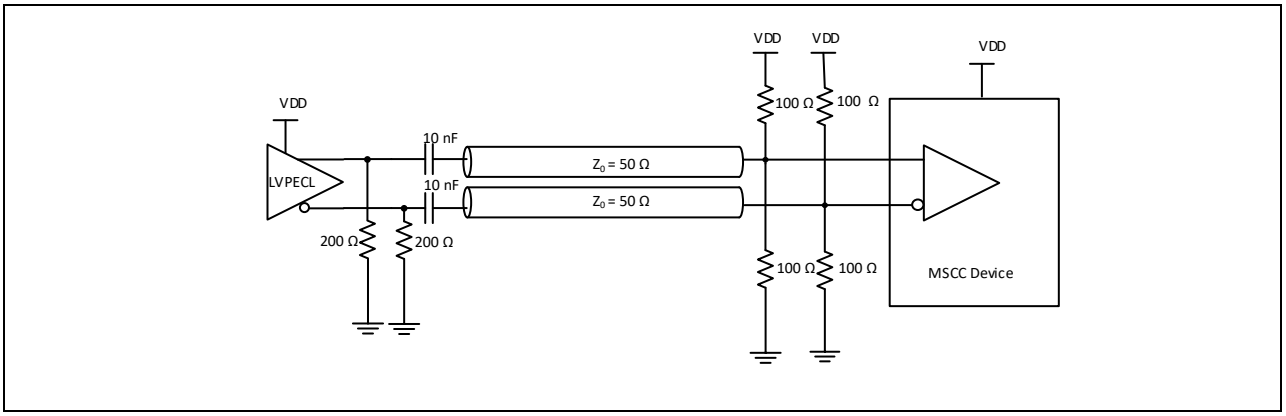


Figure 6. Input driven by AC coupled LVPECL output

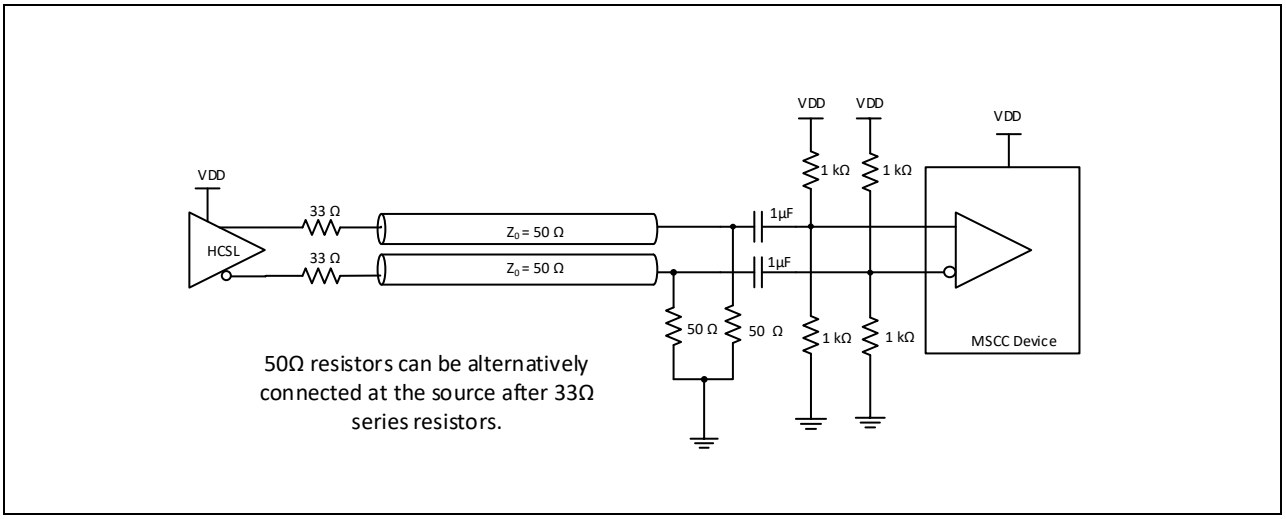


Figure 7. Input driven by HCSL output

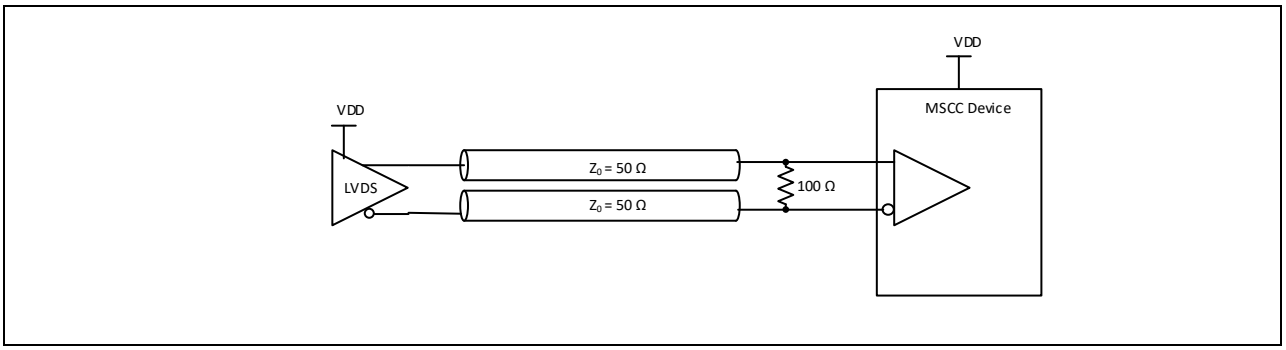


Figure 8. Input driven by LVDS output

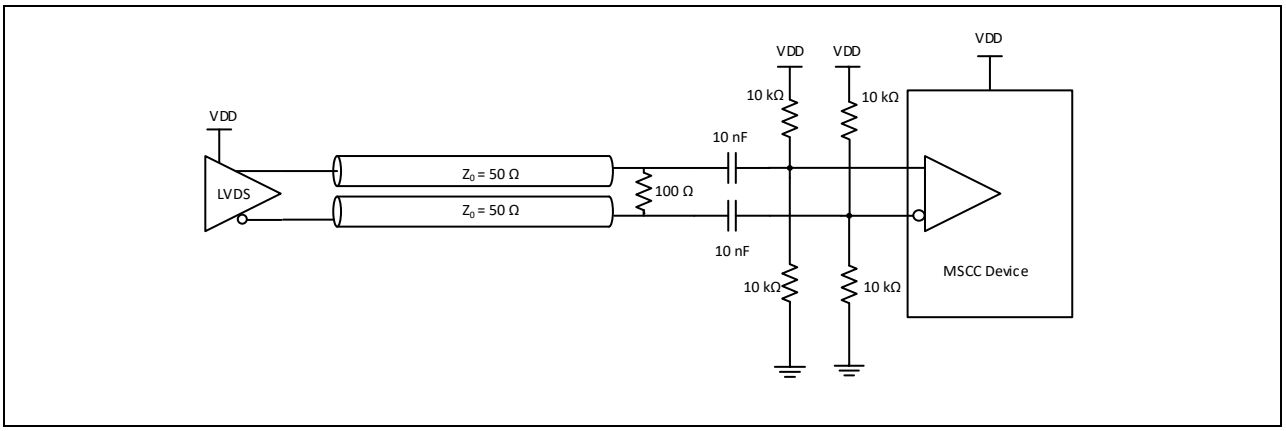


Figure 9. Input driven by AC coupled LVDS

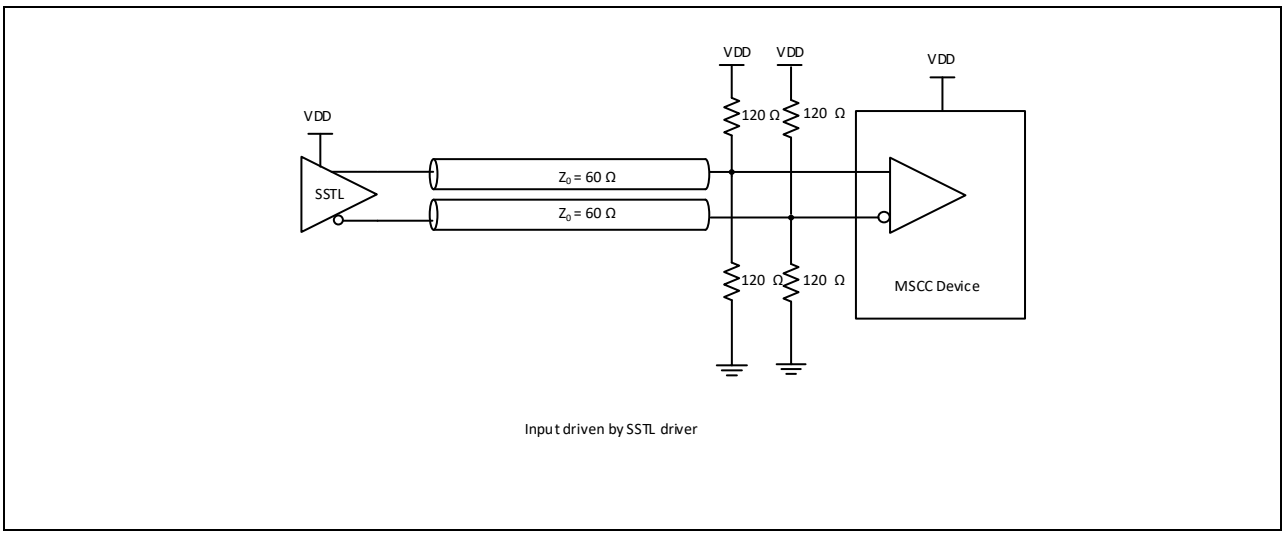


Figure 10. Input driven by an SSTL output

Clock Outputs

LVCMOS output OUT_LVCMOS require only series termination resistor whose value is depending on LVCMOS output voltage as shown in Figure 11.

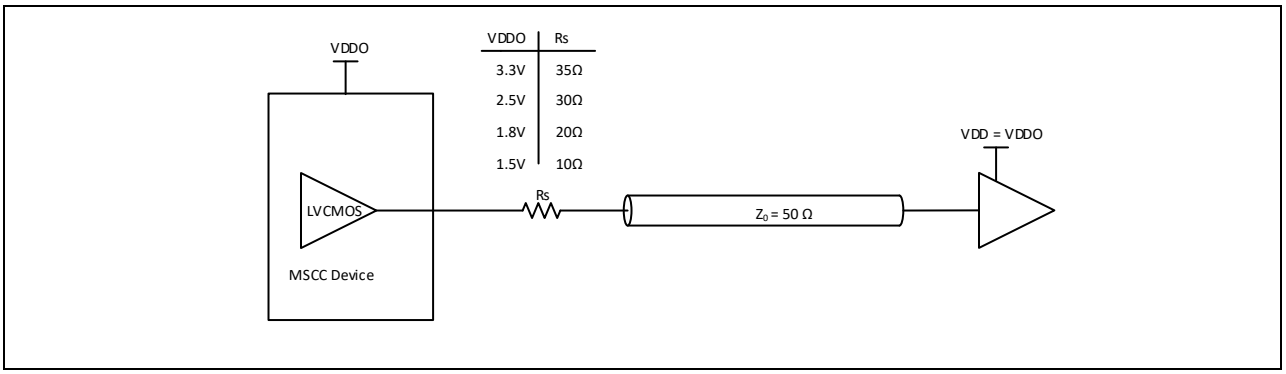


Figure 11. Termination for LVCMOS outputs

Differential outputs LVPECL and LVDS should have same termination as corresponding outputs described in previous section. HCSL outputs should be terminated with 33Ω series resistors at the source and 50Ω shunt resistors at the source or at the end on the transmission line. AC coupling and re-biasing is not required at the outputs when driving native HCSL receivers.

The device is designed to drive differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single ended output (for example driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 12 This is to provide a nominal common mode impedance of 10Ω or higher which is typical for differential terminations.

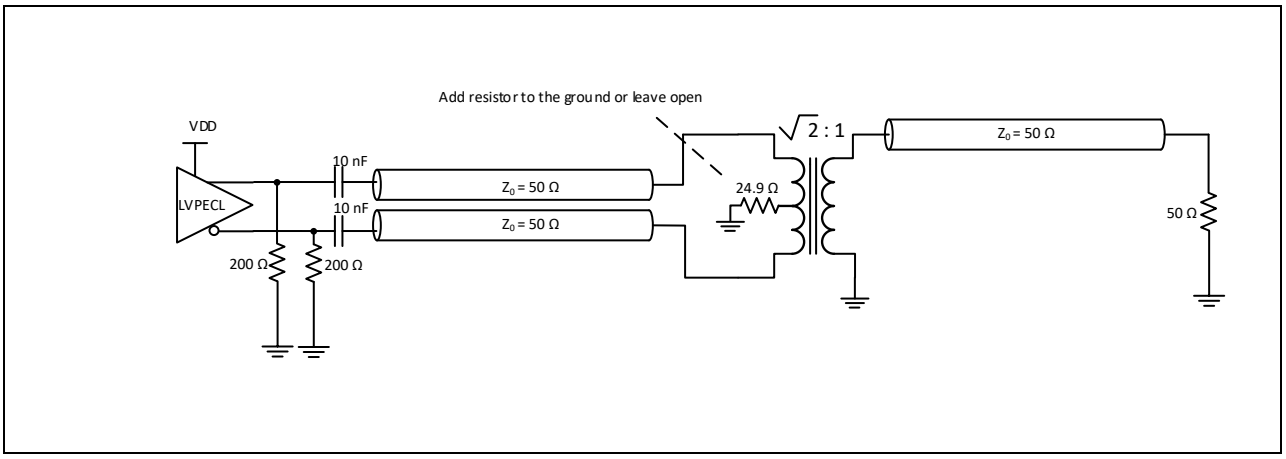


Figure 12. Driving a load via transformer

Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8MHz to 60MHz. Load capacitors C1, C2 and series resistors Rs shall be selected as per crystal vendor recommendation. Shunt resistor is implemented inside the device.

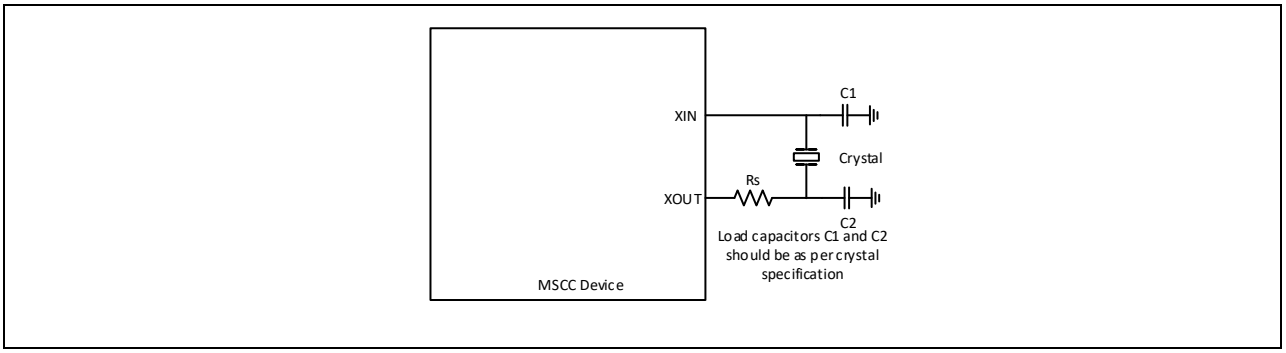


Figure 13. Crystal Oscillator Circuit

Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1kΩ resistor. Unused outputs should be left unconnected.

Power Consumption

The device total power consumption can be calculated as:

$$P_T = P_S + P_{XTAL} + P_C + P_{O\_DIF} + P_{O\_LVCMOS}$$

Where:

$P_S = V_{DD} \times I_S$ — The core power when XTAL is not used. The current is specified in Table 6. .If XTAL is running this power should be set to zero.

$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$ — The core power when XTAL is used. The current is provided in Table 6. If XTAL is not used this power should be set to zero.

$P_C = V_{DDO} \times I_{DD\_CM}$ — Common output power shared among all ten outputs. The current I_{DD_CM} is specified in Table 6.

$P_{O\_DIF} = V_{DDO} \times I_{DD\_LVDS} \times N$ — Output power where output current (I_{DD_LVDS}) is specified in Table 6. For LVPECL or HCSL just replace I_{DD_LVDS} with I_{DD_LVPECL} or I_{DD_HCSL}.
N is either 0 (outputs disabled) or 4 (four differential outputs enabled)

$P_{O\_LVCMOS} = V_{DD\_LVCMOS} \times (I_{DD} \times f / 100MHz + V_{DD\_LVCMOS} \times C_{LOAD} \times f)$ — Dynamic LVCMOS output power. I_{DD} is specified in Table 6. If LVCMOS output is disabled this term is equal to zero.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption. For LVDS outputs it is:

$$P_D = P_T - 4 \times P_{LVDS}$$

For LVPECL or HCSL just replace P_{LVDS} with corresponding P_{LVPECL} or P_{HCSL} below.

$$P_{LVPECL} = (V_{OH} - V_B)^2 / 50\Omega + (V_{OL} - V_B)^2 / 50\Omega + (V_{OH} - V_B) \times V_B / 50\Omega + (V_{OL} - V_B) \times V_B / 50\Omega$$

V_{OH} and V_{OL} are the output high and low voltages respectively for LVPECL output

V_B is LVPECL bias voltage equal to V_{DD} – 2V

$$P_{LVDS} = V_{SW}{}^2 / 100\Omega$$

V_{SW} is voltage swing of LVDS output.

$$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (33\Omega + 50\Omega)$$

V_{SW} is voltage swing of HCSL output. 50Ω is termination resistance and 33Ω is series resistance of the HCSL output.

Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.

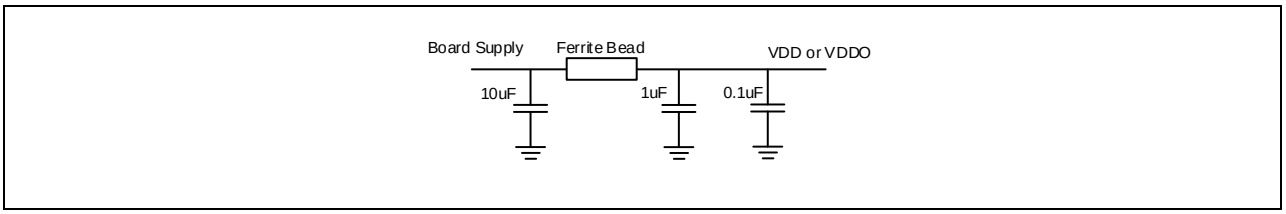


Figure 14. Power Supply Filtering

Power Supplies and Power-up Sequence

The device has four different power supplies: VDD, VDDO_A, VDDO_B and VDD_LVCMOS which are mutually independent. Voltages supported by each of these power supplies are specified in Table 1.

The device is not sensitive to the power-up sequence. For example commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence)

Device Control

ZL40234 is controlled via Input Select (IN_SEL0/1) pins which select which one of three inputs is fed to the output and show in Table 2 and OUT_TYPE_SEL0/1 pins which select signal level (LVPECL, LVDS, HCSL or Hi-Z) as shown in Table 3.
All input control pins have low input threshold voltage so they can be driven from the device with low output voltage (FPGA/CPLD). Supported voltages are between 1.2V and VDD (2.5V or 3.3V).

Table 2 Input clock selection

IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN

Table 3 Output Type Selection

OUT_TYPE_SEL1	OUT_TYPE_SEL0	Output
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	High-Z (Output Disabled)

Typical device performance

The following plots show typical device performances

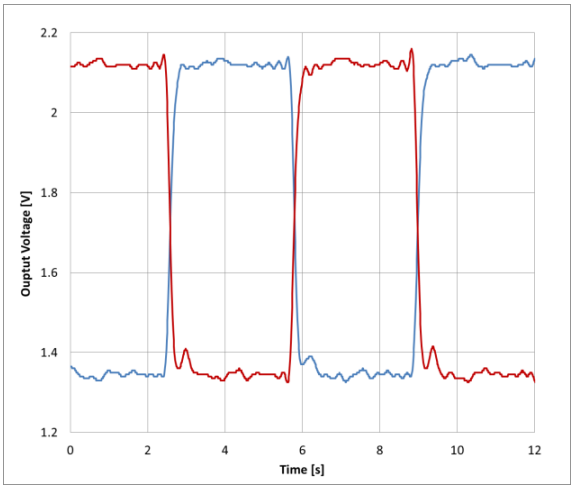


Figure 15. 156.25MHz LVPECL

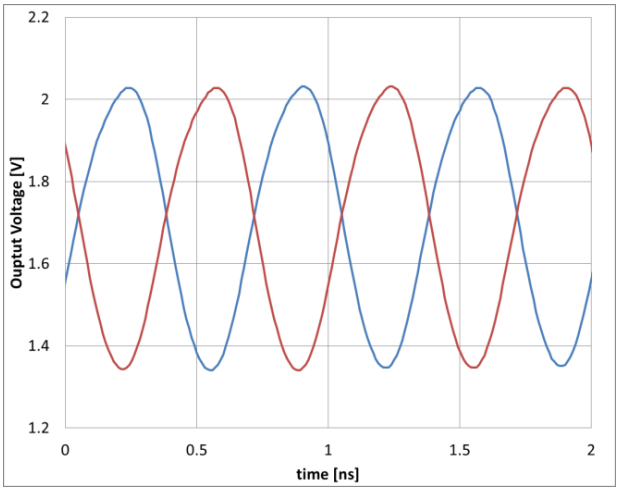


Figure 16. 1.5GHz LVPECL

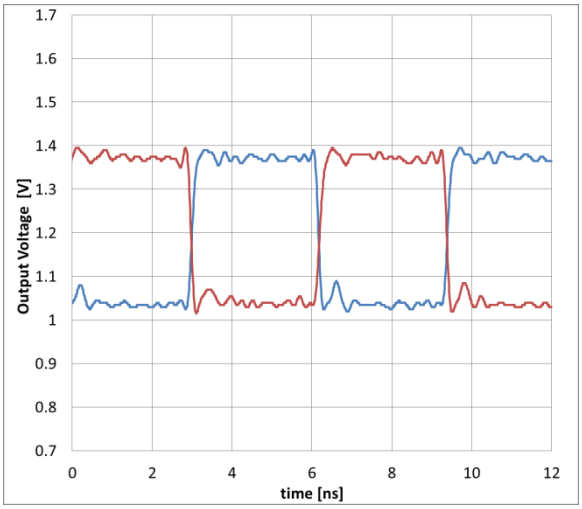


Figure 17. 156.25MHz LVDS

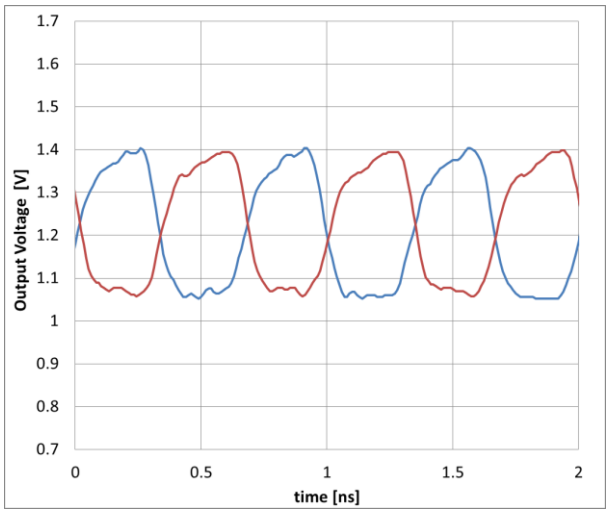


Figure 18. 1.5GHz LVDS

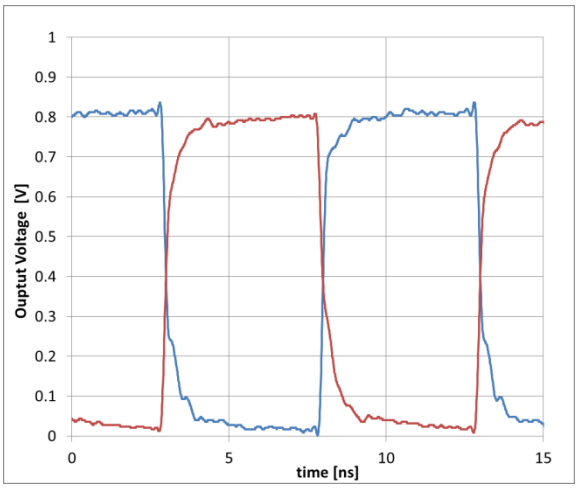


Figure 19. 100MHz HCSL

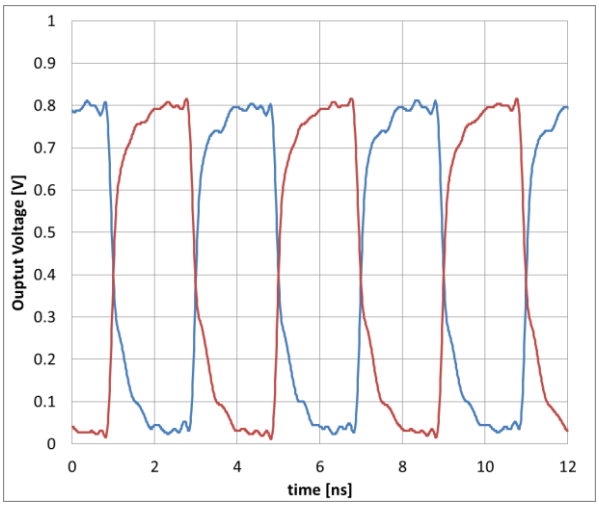


Figure 20. 250MHz HCSL

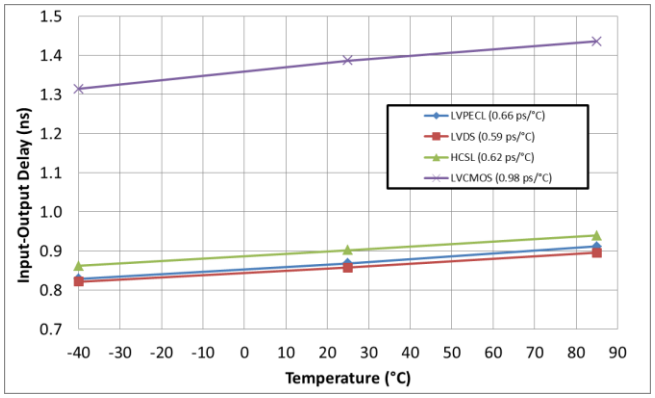


Figure 21. I/O delay vs temperature

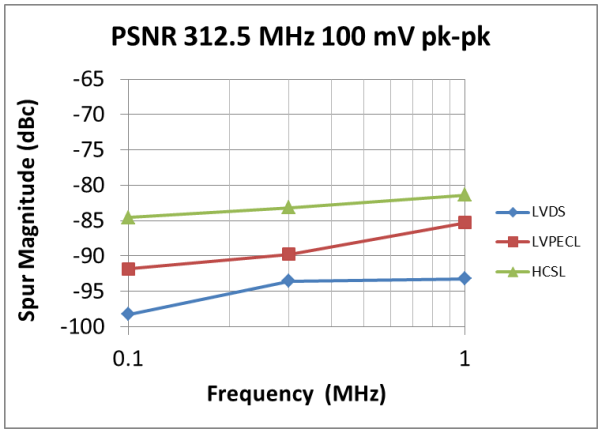


Figure 22. PSNR vs noise frequency

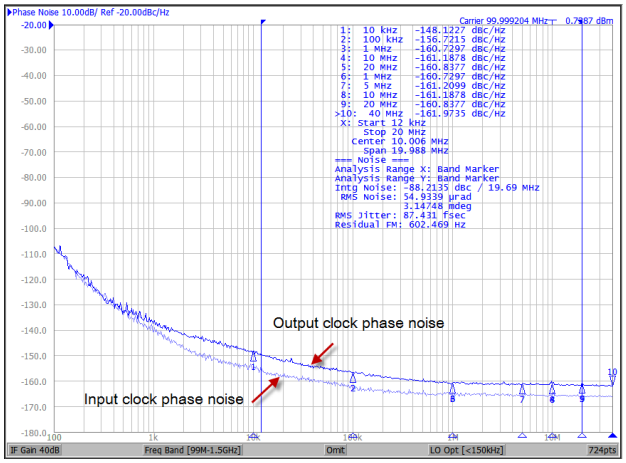


Figure 23. 100MHz LVPECL Phase Noise

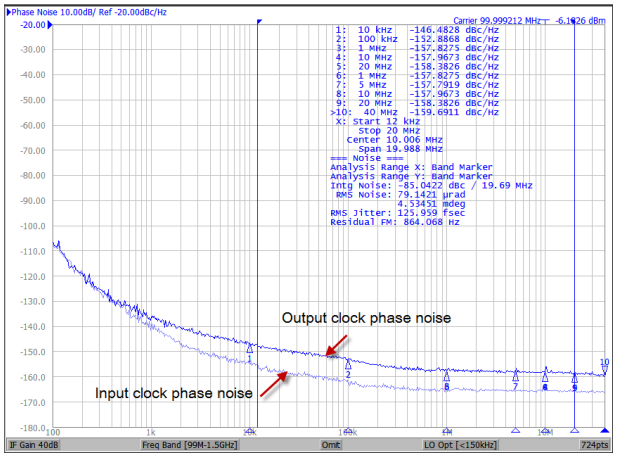


Figure 24. 100MHz LVDS Phase Noise

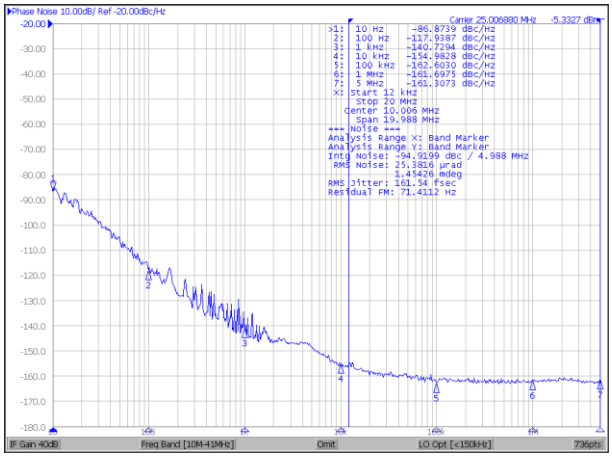


Figure 25. 25MHz LVDS Phase Noise in Xtal mode

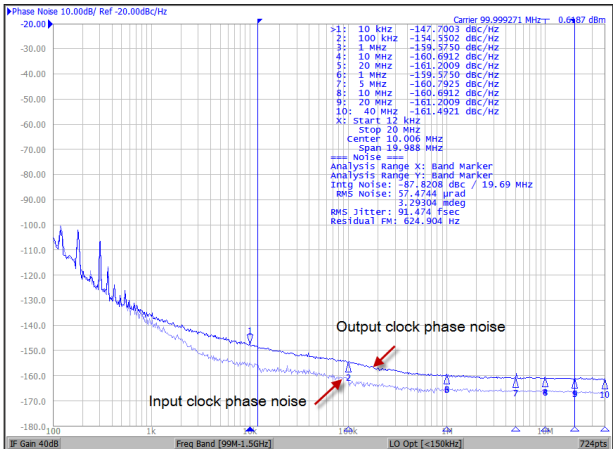


Figure 26. 100MHz HCSL Phase Noise

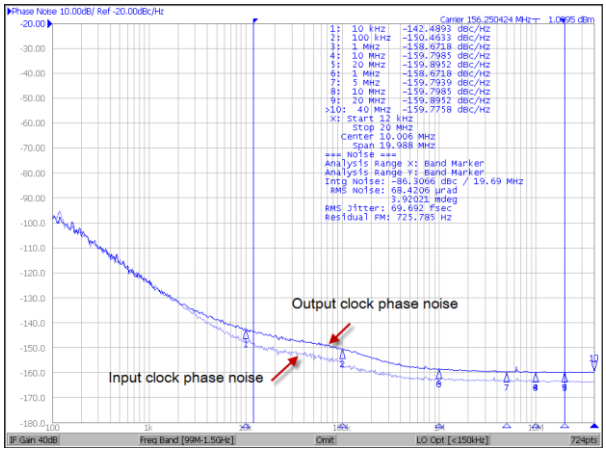


Figure 27. 156.25MHz LVPECL Phase Noise

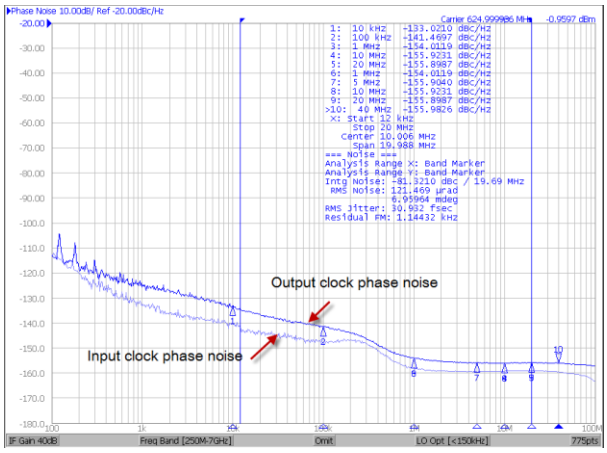


Figure 28. 625MHz LVPECL Phase Noise

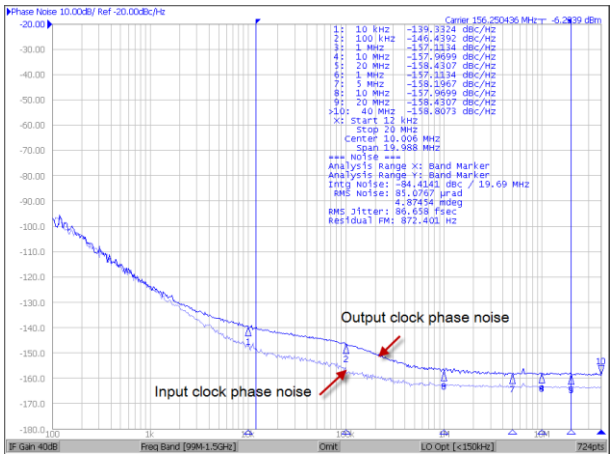


Figure 29. 156.25MHz LVDS Phase Noise

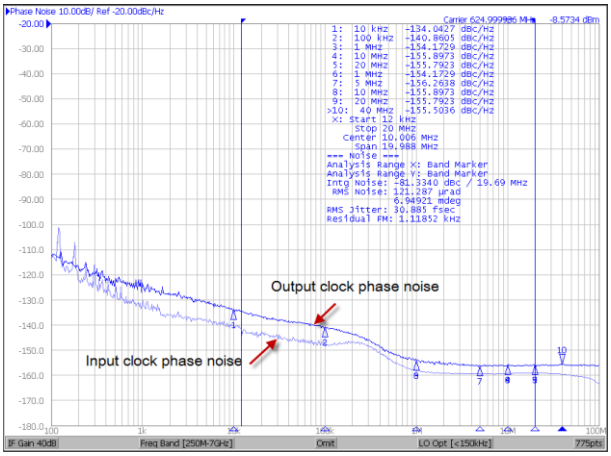


Figure 30. 625MHz LVDS Phase Noise

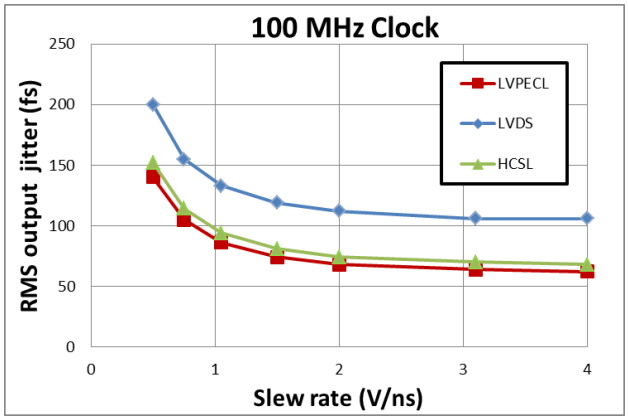


Figure 31. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

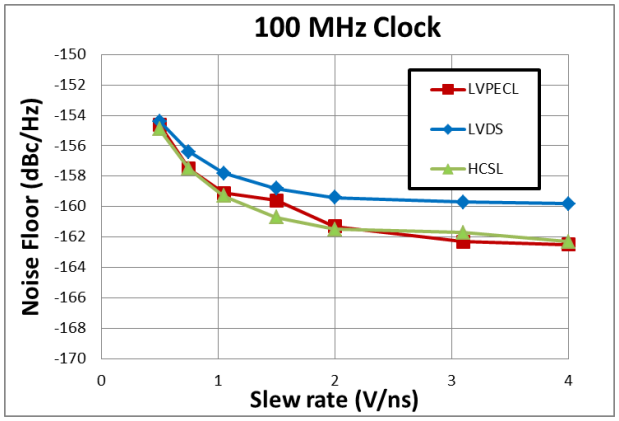


Figure 32. Output clock noise floor vs input clock slew-rate

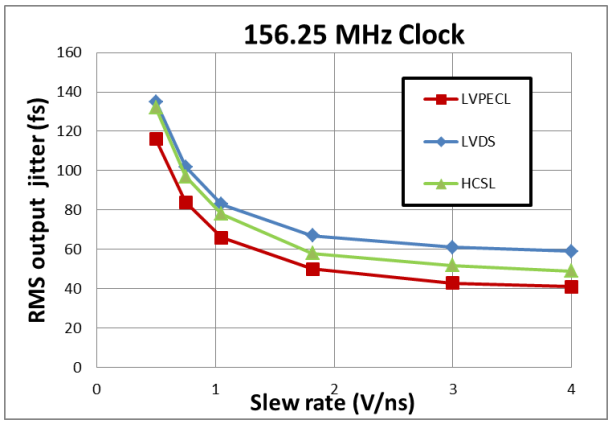


Figure 33. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

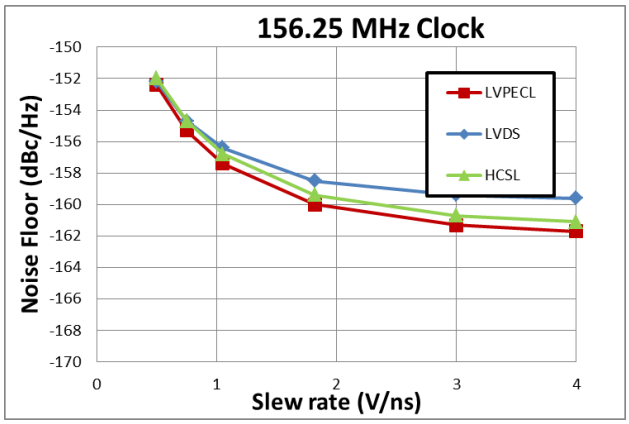


Figure 34. Output clock noise floor vs input clock slew-rate

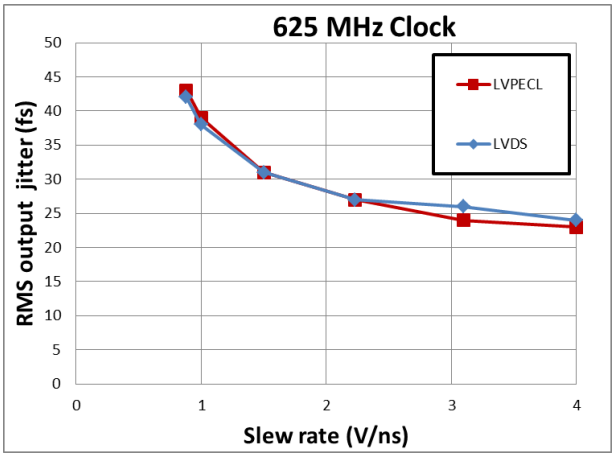


Figure 35. Output RMS jitter (12kHz to 20MHz) vs input clock slew-rate

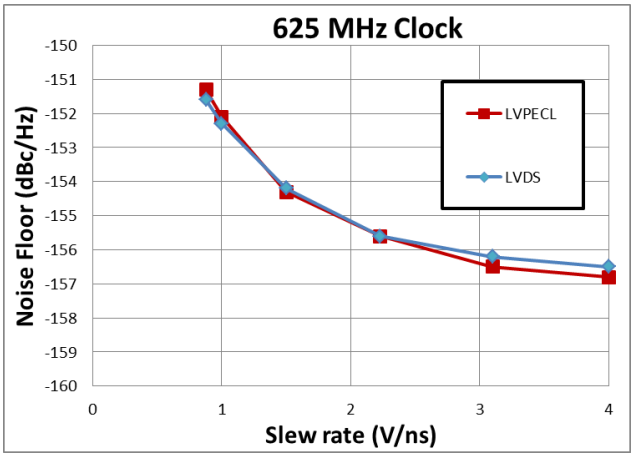


Figure 36. Output clock noise floor vs input clock slew-rate

AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	V_{DD} /V_{DDO}	-0.5		4.6	V	
2	Supply voltage (2.5V)	V_{DD} /V_{DDO}	-0.5		3.5	V	
3	Storage temperature	T_{ST}	-55		125	°C	

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions

Table 5 Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD} /V_{DDO}/V_{DD_LVCMOS}	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V_{DD} /V_{DDO}/V_{DD_LVCMOS}	2.375	2.50	2.625	V	
3	Supply voltage 1.8V	V_{DD_LVCMOS}	1.6	1.8V	2	V	
4	Supply voltage 1.5V	V_{DD_LVCMOS}	1.35	1.5	1.65	V	
5	Operating temperature	T_A	-40	25	85	°C	
6	Input voltage	V_{DD-IN}	- 0.3		V_{DD} + 0.3	V	

* Voltages are with respect to ground (GND) unless otherwise stated
* The device core supports two power supply modes (3.3V and 2.5V)

Table 6 Current consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Core device current (all outputs and XTAL disabled)	$I_{s\_3.3V}$		163	197	mA	VDD= 3.3V+5%
		$I_{s\_2.5V}$		153	187	mA	VDD = 2.5V+5%
2	Core device current (all outputs disabled) XTAL circuit enabled with 25MHz Crystal connected between XIN and XOUT	$I_{DD\_XTAL\_3.3V}$		128	154	mA	VDD= 3.3V+5%
		$I_{DD\_XTAL\_2.5V}$		124	150	mA	VDD= 2.5V+5%
3	Common output current	$I_{DD\_CM\_3.3V}$		13.44	15.05	mA	VDDO= 3.3V+5%
		$I_{DD\_CM\_2.5V}$		12.18	13.65	mA	VDDO= 2.5V+5%
4	Dynamic LVCMOS output current (f = 100MHz) Needs to be scaled for different frequencies by f/100MHz	$I_{DD\_3.3V}$		2.38	2.68	mA	VDDO= 3.3V+5%
		$I_{DD\_2.5V}$		1.74	1.96	mA	VDDO= 2.5V+5%
5	Current dissipation per LVPECL output	$I_{DD\_LVPECL\_3.3V}$		19.36	23.26	mA	VDDO= 3.3V+5%
		$I_{DD\_LVPECL\_2.5V}$		19.38	22.17	mA	VDDO= 2.5V+5%
6	Current dissipation per LVDS output	$I_{DD\_LVDSL\_3.3V}$		6.73	8.00	mA	VDDO= 3.3V+5%
		$I_{DD\_LVDS\_2.5V}$		6.87	7.83	mA	VDDO= 2.5V+5%
7	Current dissipation per HCSL output	$I_{DD\_HCSL\_3.3V}$		16.43	19.87	mA	VDDO= 3.3V+5%
		$I_{DD\_HCSL\_2.5V}$		17.14	19.18	mA	VDDO= 2.5V+5%

Table 7 Input Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage for control inputs	V_{CIH}	1.05			V	
2	CMOS low-level input voltage for control inputs	V_{CIL}			0.45	V	
3	CMOS input leakage current for control inputs (includes current due to pull down resistors)	I_{IL}	-25		50	µA	$V_I = V_{DD}$ or 0 V
4	Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	1		2	V	
5	Differential input voltage difference for IN0_p/n and IN1_p/n f ≤ 1GHz **	V_{ID}	0.15		1.3	V	
6	Differential input voltage difference for IN0_p/n and IN1_p/n for 1GHz < f ≤ 1.6GHz **	V_{ID}	0.35		1.3	V	
7	Differential input leakage current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	-150		150	µA	V_I = 2V or 0V
8	Single ended input voltage for IN0_p and IN1_p	V_{SI}	-0.3		2.7	V	VDD = 3.3V or 2.5V
9	Single ended input common mode voltage (IN0_p/n and IN1_p/n)	V_{SIC}	1		2	V	VDD = 3.3V or 2.5V
10	Single ended input voltage swing for IN0_p and IN1_p	V_{SID}	0.3		1.3	V	VDD = 3.3V or 2.5V
11	Input frequency (differential)	f_{IN}	0		1600	MHz	
12	Input frequency (LVCMOS)	f_{IN_CMOS}	0		250	MHz	
13	Input duty cycle	dc	35%		65%		
14	Input slew rate	slew		2		V/ns	
15	Input pull-up/ pull-down resistance	R_{PU}/R_{PD}		60kΩ			
16	Input pull-down resistance for INx_p	R_{PD}		30kΩ			
17	Input multiplexer isolation IN0_p/n to IN1_p/n and vice versa Power on both inputs 0dBm, f_{OFFSET} > 50kHz	Iso		-84		dBc	f_{IN} = 100 MHz
				-82			f_{IN} = 200 MHz
				-71			f_{IN} = 400 MHz
				-67			f_{IN} = 800 MHz

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
* Input mux isolation is measured as amplitude of f_{OFFSET} spur in dBc on the output clock phase noise plot
**Input differential voltage is calculated as $V_{ID} = V_{IH}-V_{IL}$ where V_{IH} and V_{IL} are input voltage high and low respectively. It should not be confused with $V_{ID} = 2 * (V_{IH}-V_{IL})$ used in some datasheets. Please refer to Figure 37.

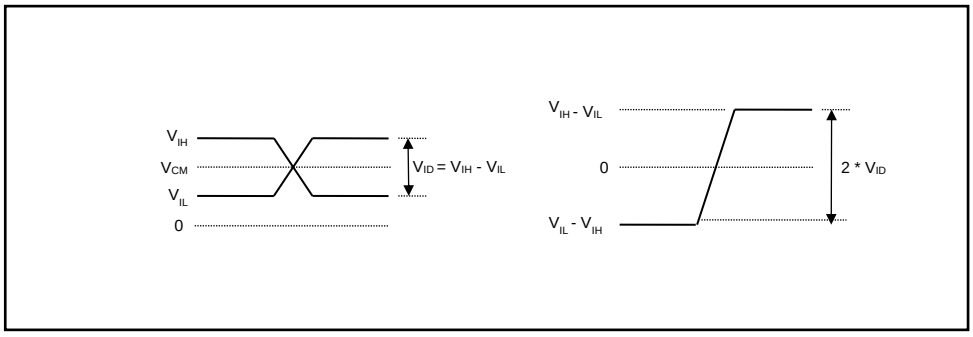


Figure 37. Differential Input Voltage Levels

Table 8 Crystal Oscillator Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Mode of oscillation	mode		Fundamental			
2	Frequency	f	8		60	MHz	
3	On chip load capacitance			1		pF	
4	On chip series resistor			0		Ω	
5	On chip shunt resistor	R		500		kΩ	
6	Frequency in overdrive mode(1)	f_{OV}	0.1		250	MHz	Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1uF assumed)
7	Frequency in bypass mode(2)	f_{BP}	0		250	MHz	Functional but may not meet AC parameters

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
(1) Maximum input level is 2V
(2) Maximum output level is VDD

Table 9 Power Supply Rejection Ratio for VDD = VDDO = 3.3V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	PSRR for LVPECL output	$PSRR_{LVPECL}$		-71.75		dBc	f_{IN} = 156.25 MHz
				-84.45			f_{IN} = 312.5 MHz
				-82.11			f_{IN} = 625 MHz
2	PSRR for LVDS output	$PSRR_{LVDS}$		-95.16		dBc	f_{IN} = 156.25 MHz
				-97.77			f_{IN} = 312.5 MHz
				-79.23			f_{IN} = 625 MHz
3	PSRR for HCSL output	$PSRR_{HCSL}$		-77.15		dBc	f_{IN} = 100 MHz
				-76.75			f_{IN} = 156.25 MHz
				-80.44			f_{IN} = 312.5 MHz

* Values are over Recommended Operating Conditions
* Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp
* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

Table 10 Power Supply Rejection Ratio for VDD = VDDO = 2.5V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	PSRR for LVPECL output	$PSRR_{LVPECL}$		-73.68		dBc	f_{IN} = 156.25 MHz
				-78.88			f_{IN} = 312.5 MHz
				-71.82			f_{IN} = 625 MHz
2	PSRR for LVDS output	$PSRR_{LVDS}$		-90.04		dBc	f_{IN} = 156.25 MHz
				-79.99			f_{IN} = 312.5 MHz
				-73.45			f_{IN} = 625 MHz
3	PSRR for HCSL output	$PSRR_{HCSL}$		-92.16		dBc	f_{IN} = 100 MHz
				-74.08			f_{IN} = 156.25 MHz
				-91.88			f_{IN} = 312.5 MHz

* Values are over Recommended Operating Conditions
* Noise injected to VDDO power supply with frequency 100 kHz and amplitude 100 mVpp
* PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot

Table 11 LVCMOS Output Characteristics for VDDO = 3.3V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage (1mA load)	V_{OH}	VDDO-0.1			V	DC Measurement
2	Output low voltage (1mA load)	V_{OL}			0.1	V	DC Measurement
3	Output High Current (Load adjusted to Vout = VDDO/2)	I_{OH}		30		mA	DC Measurement
4	Output Low Current (Load adjusted to Vout = VDDO/2)	I_{OL}		34		mA	DC Measurement
5	Output impedance	R_O		15		Ω	DC Measurement
6	Rise time (20% to 80%)	t_r		220	310	ps	
7	Fall time (20% to 80%)	t_f		320	365	ps	
8	Output frequency	F_O	0		250	MHz	
9	Input to output delay	t_{IOD}	1.07	1.28	2.07	ns	
10	Output enable time	t_{EN}			3	cycles	
11	Output disable time	T_{DIS}			3	cycles	
12	Additive RMS jitter in 1MHz to 5MHz band	$T_{j\_1M\_5M}$		46	80	fs	Input Clock 25MHz
13	Additive RMS jitter in 12kHz to 5MHz band	$T_{j\_12K\_5M}$		56	90	fs	Input Clock 25MHz
14	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		60	79	fs	Input Clock 125MHz
15	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		65	86	fs	Input Clock 125MHz
16	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		61	94	fs	Input Clock 156.25MHz
17	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		66	100	fs	Input Clock 156.25MHz
18	Noise floor	N_F		-165	-162	dBc/Hz	Input clock: 25 MHz
19				-160	-156	dBc/Hz	Input clock: 125 MHz
20				-158	-153	dBc/Hz	Input clock: 156.25 MHz

* Values are over Recommended Operating Conditions

Table 12 LVCMOS Output Characteristics for VDDO = 2.5V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage (1mA load)	V_{OH}	VDDO-0.1			V	DC Measurement
2	Output low voltage (1mA load)	V_{OL}			0.1	V	DC Measurement
3	Output High Current (Load adjusted to Vout = VDDO/2)	I_{OH}		21		mA	DC Measurement
4	Output Low Current (Load adjusted to Vout = VDDO/2)	I_{OL}		25		mA	DC Measurement
5	Output impedance	R_O		15		Ω	DC Measurement
6	Rise time (20% to 80%)	t_r		225	310	ps	
7	Fall time (20% to 80%)	t_f		320	365	ps	
8	Output frequency	F_O	0		250	MHz	
9	Input to output delay	t_{IOD}	1.10	1.41	2.30	ns	
10	Output enable time	t_{EN}			3	cycles	
11	Output disable time	T_{DIS}			3	cycles	
12	Additive RMS jitter in 1MHz to 5MHz band	$T_{j\_1M\_5M}$		51	104	fs	Input Clock 25MHz
13	Additive RMS jitter in 12kHz to 5MHz band	$T_{j\_12k\_5M}$		62	111	fs	Input Clock 25MHz
14	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		64	81	fs	Input Clock 125MHz
15	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		70	88	fs	Input Clock 125MHz
16	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		62	94	fs	Input Clock 156.25MHz
17	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		68	100	fs	Input Clock 156.25MHz
18	Noise floor	N_F		-164	-161	dBc/Hz	Input clock: 25 MHz
19				-159	-155	dBc/Hz	Input clock: 125 MHz
20				-158	-153	dBc/Hz	Input clock: 156.25 MHz

* Values are over Recommended Operating Conditions

Table 13 LVPECL Output Characteristics for VDDO = 3.3V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{LVPECL_OH}	1.9	2.08	2.4	V	DC Measurement
2	Output low voltage	V_{LVPECL_OL}	1.2	1.36	1.7	V	DC Measurement
3	Output differential swing**	V_{LVPECL_SW}	0.6	0.72	0.9	V	DC Measurement
4	Variation of V_{LVPECL_SW} for complementary output states	ΔV_{LVPECL_SW}	0	0.02	0.07	V	
5	Common mode output	V_{CM}	1.6	1.72	2.1	V	
7	Output frequency when $V_{LVPECL\_SW} \geq 0.6V$	$F_{MAX\_0.6VSW}$			800	MHz	
8	Output frequency when $V_{LVPECL\_SW} \geq 0.4V$	$F_{MAX\_0.4VSW}$			1600	MHz	
9	Rise or fall time (20% to 80%)	t_r, t_f		110	170	ps	
10	Output frequency	F_O	0		1600	MHz	
11	Output to output skew	t_{OOSK}			40	ps	
12	Device to device output skew	t_{DOOSK}			120	ps	
13	Input to output delay	t_{IOD}	0.73	0.87	1.1	ns	
14	Output enable time	t_{EN}			3	cycles	
15	Output disable time	t_{DIS}			3	cycles	
16	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		68	96	fs	Input clock: 100 MHz
				50	64	fs	Input clock: 156.25MHz
				20	32	fs	Input clock: 625 MHz
17	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		71	101	fs	Input clock: 100 MHz
				55	70	fs	Input clock: 156.25MHz
				25	39	fs	Input clock: 625 MHz
18	Noise floor	N_F		-161	-159	dBc/Hz	Input clock: 100 MHz
				-160	-155	dBc/Hz	Input clock: 156.25 MHz
				-155	-151	dBc/Hz	Input clock: 625 MHz

* Values are over Recommended Operating Conditions

**Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets. Please refer to Figure 38.

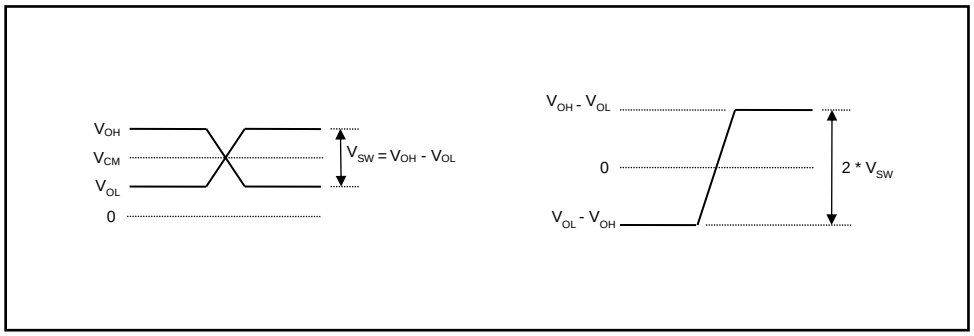


Figure 38. Differential Output Voltage Levels

Table 14 LVPECL Output Characteristics for VDDO = 2.5V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{LVPECL_OH}	1.1	1.28	1.7	V	DC Measurement
2	Output low voltage	V_{LVPECL_OL}	0.4	0.57	0.9	V	DC Measurement
3	Output differential swing**	V_{LVPECL_SW}	0.6	0.71	0.9	V	DC Measurement
4	Variation of V_{LVPECL_SW} for complementary output states	ΔV_{LVPECL_SW}	0	0.02	0.05	V	
5	Common mode output	V_{CM}	0.8	0.92	1.2	V	
7	Output frequency when $V_{LVPECL\_SW} \geq 0.6V$	$F_{MAX\_0.6VSW}$			800	MHz	
8	Output frequency when $V_{LVPECL\_SW} \geq 0.4V$	$F_{MAX\_0.4VSW}$			1600	MHz	
9	Rise or fall time (20% to 80%)	t_r, t_f		120	170	ps	
10	Output frequency	F_O	0		1600	MHz	
11	Output to output skew	t_{OOSK}			40	ps	
12	Device to device output skew	t_{DOOSK}			120	ps	
13	Input to output delay	t_{IOD}	0.75	0.87	1.1	ns	
14	Output enable time	t_{EN}			3	cycles	
15	Output disable time	t_{DIS}			3	cycles	
16	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		65	91	fs	Input clock: 100 MHz
				50	64	fs	Input clock: 156.25MHz
				20	30	fs	Input clock: 625 MHz
17	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		69	99	fs	Input clock: 100 MHz
				54	75	fs	Input clock: 156.25MHz
				26	41	fs	Input clock: 625 MHz
18	Noise floor	N_F		-161	-159	dBc/Hz	Input clock: 100 MHz
				-160	-156	dBc/Hz	Input clock: 156.25 MHz
				-155	-151	dBc/Hz	Input clock: 625 MHz

* Values are over Recommended Operating Conditions
**Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$ It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets. Please refer to Figure 38.

Table 15 LVDS Outputs for VDDO = 3.3V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{LVDS_OH}	1.3	1.39	1.47	V	DC Measurement
2	Output low voltage	V_{LVDS_OL}	1.0	1.07	1.15	V	DC Measurement
3	Output differential swing**	V_{LVDS_SW}	0.25	0.32	0.39	V	DC Measurement
4	Variation of V_{LVDS_SW} for complementary output states	ΔV_{LVDS_SW}	0	0.002	0.01	V	
5	Common mode output	V_{CM}	1.15	1.23	1.3	V	
6	Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.001	0.01	V	
7	Output frequency when $V_{LVDS\_SW} \geq 250mV$	$F_{MAX\_0.25VSW}$			800	MHz	
8	Output frequency when $V_{LVDS\_SW} \geq 200mV$	$F_{MAX\_0.2VSW}$			1600	MHz	
9	Rise or fall time (20% to 80%)	t_r, t_f		110	170	ps	
10	Output frequency	F_O	0		1600	MHz	
11	Output to output skew	t_{OOSK}			20	ps	
12	Device to device output skew	t_{DOOSK}			130	ps	
13	Input to output delay	t_{IOD}	0.76	0.86	1.1	ns	
14	Output Short Circuit Current Single Ended	I_S	-24		24	mA	Single ended outputs shorted to GND
15	Output Short Circuit Current Differential	I_{SD}	-24		24	mA	Complementary outputs shorted
16	Output enable time	t_{EN}			3	cycles	
17	Output disable time	t_{DIS}			3	cycles	
18	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		110	144	fs	Input clock: 100 MHz
				63	81	fs	Input clock: 156.25MHz
				21	33	fs	Input clock: 625 MHz
19	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		115	150	fs	Input clock: 100 MHz
				73	102	fs	Input clock: 156.25MHz
				26	40	fs	Input clock: 625 MHz
20	Noise floor	N_F		-158	-156	dBc/Hz	Input clock: 100 MHz
				-158	-155	dBc/Hz	Input clock: 156.25 MHz
				-154	-151	dBc/Hz	Input clock: 625 MHz

* Values are over Recommended Operating Conditions

**Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets. Please refer to Figure 38.

Table 16 LVDS Outputs for VDDO = 2.5V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{LVDS_OH}	1.3	1.4	1.5	V	DC Measurement
2	Output low voltage	V_{LVDS_OL}	0.97	1.05	1.13	V	DC Measurement
3	Output differential swing**	V_{LVDS_SW}	0.25	0.35	0.44	V	DC Measurement
4	Variation of V_{LVDS_SW} for complementary output states	ΔV_{LVDS_SW}	0	0.001	0.01	V	
5	Common mode output	V_{CM}	1.15	1.23	1.3	V	
6	Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.001	0.01	V	
7	Output frequency when $V_{LVDS\_SW} \geq 250mV$	$F_{MAX\_0.25VSW}$			800	MHz	
8	Output frequency when $V_{LVDS\_SW} \geq 200mV$	$F_{MAX\_0.2VSW}$			1600	MHz	
9	Rise or fall time (20% to 80%)	t_r, t_f		110	170	ps	
10	Output frequency	F_O	0		1600	MHz	
11	Output to output skew	t_{OOSK}			20	ps	
12	Device to device output skew	t_{DOOSK}			130	ps	
13	Input to output delay	t_{IOD}	0.78	0.86	1.12	ns	
14	Output Short Circuit Current Single Ended	I_S	-24		24	mA	Single ended outputs shorted to GND
15	Output Short Circuit Current Differential	I_{SD}	-24		24	mA	Complementary outputs shorted
16	Output enable time	t_{EN}			3	cycles	
17	Output disable time	t_{DIS}			3	cycles	
18	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		107	140	fs	Input clock: 100 MHz
				62	77	fs	Input clock: 156.25MHz
				20	31	fs	Input clock: 625 MHz
19	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		111	146	fs	Input clock: 100 MHz
				66	83	fs	Input clock: 156.25MHz
				24	36	fs	Input clock: 625 MHz
20	Noise floor	N_F		-158	-156	dBc/Hz	Input clock: 100 MHz
				-159	-155	dBc/Hz	Input clock: 156.25 MHz
				-155	-151	dBc/Hz	Input clock: 625 MHz

* Values are over Recommended Operating Conditions

**Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets. Please refer to Figure 38.

Table 17 HCSL Outputs for VDDO = 3.3V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{HCSL_OH}	0.6	0.85	1.1	V	DC Measurement
2	Output low voltage	V_{HCSL_OL}	-0.05	0	0.05	V	DC Measurement
3	Output differential swing**	V_{HCSL_SW}	0.6	0.85	1.1	V	DC Measurement
4	Variation of V_{HCSL_SW} for complementary output states	ΔV_{HCSL_SW}	0	0.003	0.05	V	
5	Common mode output	V_{CM}	0.28	0.43	0.55	V	
6	Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.002	0.05	V	
7	Absolute Crossing Voltage	V_{CROSS}	0.320	0.384	0.447	V	
8	Total Variation of V_{CROSS}	ΔV_{CROSS}			0.127	V	
9	Output frequency	F_{MAX}	0		400	MHz	
10	Rise or fall time (20% to 80%)	t_r, t_f		143	309	ps	
11	Output to output skew	t_{OOSK}			21	ps	
12	Device to device output skew	t_{DOOSK}			129	ps	
13	Input to output delay	t_{IOD}	0.73	0.90	1.08	ns	
14	Output enable time	t_{EN}			3	cycles	
15	Output disable time	t_{DIS}			3	cycles	
16	Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe\_3.0}$		20	40	fs	Input clock: 100MHz
17	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		73	104	fs	Input clock: 100 MHz
				53	69	fs	Input clock: 156.25MHz
18	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		77	112	fs	Input clock: 100 MHz
				64	100	fs	Input clock: 156.25MHz
19	Noise floor	N_F		-161	-159	dBc/Hz	Input clock: 100 MHz
				-159	-155	dBc/Hz	Input clock: 156.25 MHz

* Values are over Recommended Operating Conditions

**Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets. Please refer to Figure 38.

Table 18 HCSL Outputs for VDDO = 2.5V*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{HCSL_OH}	0.6	0.83	1.1	V	DC Measurement
2	Output low voltage	V_{HCSL_OL}	-0.05	0	0.05	V	DC Measurement
3	Output differential swing**	V_{HCSL_SW}	0.5	0.83	1.1	V	DC Measurement
4	Variation of V_{HCSL_SW} for complementary output states	ΔV_{HCSL_SW}	0	0.003	0.05	V	
5	Common mode output	V_{CM}	0.28	0.42	0.55	V	
6	Variation of V_{CM} for complementary output states	ΔV_{CM}	0	0.002	0.05	V	
7	Absolute Crossing Voltage	V_{CROSS}	0.260	0.316	0.372	V	
8	Total Variation of V_{CROSS}	ΔV_{CROSS}			0.108	V	
9	Output frequency	F_{MAX}	0		400	MHz	
10	Rise or fall time (20% to 80%)	t_r, t_f		125	162	ps	
11	Output to output skew	t_{OOSK}			21	ps	
12	Device to device output skew	t_{DOOSK}			129	ps	
13	Input to output delay	t_{IOD}	0.76	0.92	1.10	ns	
14	Output enable time	t_{EN}			3	cycles	
15	Output disable time	t_{DIS}			3	cycles	
16	Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe\_3.0}$		20	40	fs	Input clock: 100MHz
17	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		68	95	fs	Input clock: 100 MHz
				52	66	fs	Input clock: 156.25MHz
18	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		72	102	fs	Input clock: 100 MHz
				56	71	fs	Input clock: 156.25MHz
19	Noise floor	N_F		-161	-158	dBc/Hz	Input clock: 100 MHz
				-160	-153	dBc/Hz	Input clock: 156.25 MHz

* Values are over Recommended Operating Conditions

**Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets. Please refer to Figure 38.

Table 19 LVCMOS Output Phase Noise with 25 MHz XTAL*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 5MHz band		103		fs	VDD = 3.3V, VDDO = 3.3V
			117		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-75		dBc/Hz	@10Hz , VDD = 3.3V, VDDO = 3.3V
			-107		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-132		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-150		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-162		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-166		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-166		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-70		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-102		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-130		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-149		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-161		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-165		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-165		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V

* Values are over Recommended Operating Conditions

Table 20 LVPECL Output Phase Noise with 25 MHz XTAL*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 5MHz band		265		fs	VDD = 3.3V, VDDO = 3.3V
			213		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-75		dBc/Hz	@10Hz , VDD = 3.3V, VDDO = 3.3V
			-107		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-133		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-152		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-158		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-71		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-103		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-130		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-151		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-160		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-159		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V

* Values are over Recommended Operating Conditions

Table 21 LVDS Output Phase Noise with 25 MHz XTAL

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 5MHza band		178		fs	VDD = 3.3V, VDDO = 3.3V
			190		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-75		dBc/Hz	@10Hz , VDD = 3.3V, VDDO = 3.3V
			-107		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-133		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-154		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-161		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-161		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-160		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-68		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-103		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-130		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-152		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-161		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-160		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-159		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V

* Values are over Recommended Operating Conditions

Table 22 HCSL Output Phase Noise with 25 MHz XTAL

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		269		fs	VDD = 3.3V, VDDO = 3.3V
			228		fs	VDD = 2.5V; VDDO = 2.5V
2	Noise floor		-76		dBc/Hz	@10Hz , VDD = 3.3V, VDDO = 3.3V
			-107		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-133		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-152		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-157		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-73		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-105		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-131		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-151		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-158		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-159		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-159		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V

* Values are over Recommended Operating Conditions

Table 23 5x5mm QFN Package Thermal Properties

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance[1] (Note 1)	θ_{JA}	still air	23.5	°C/W
		1m/s airflow	18.9	
		2.5m/s airflow	17.1	
Junction to Board Thermal Resistance	θ_{JB}		7.9	°C/W
Junction to Case Thermal Resistance	θ_{JC}		16.5	°C/W
Junction to Pad Thermal Resistance[2]	θ_{JP}	Still air	3.9	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.2	°C/W

(1) Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power

(2) Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

Change History

June 2017 was the first release of the document.

July 2017 release changes:

- Modified power calculation in the Power Consumption section.

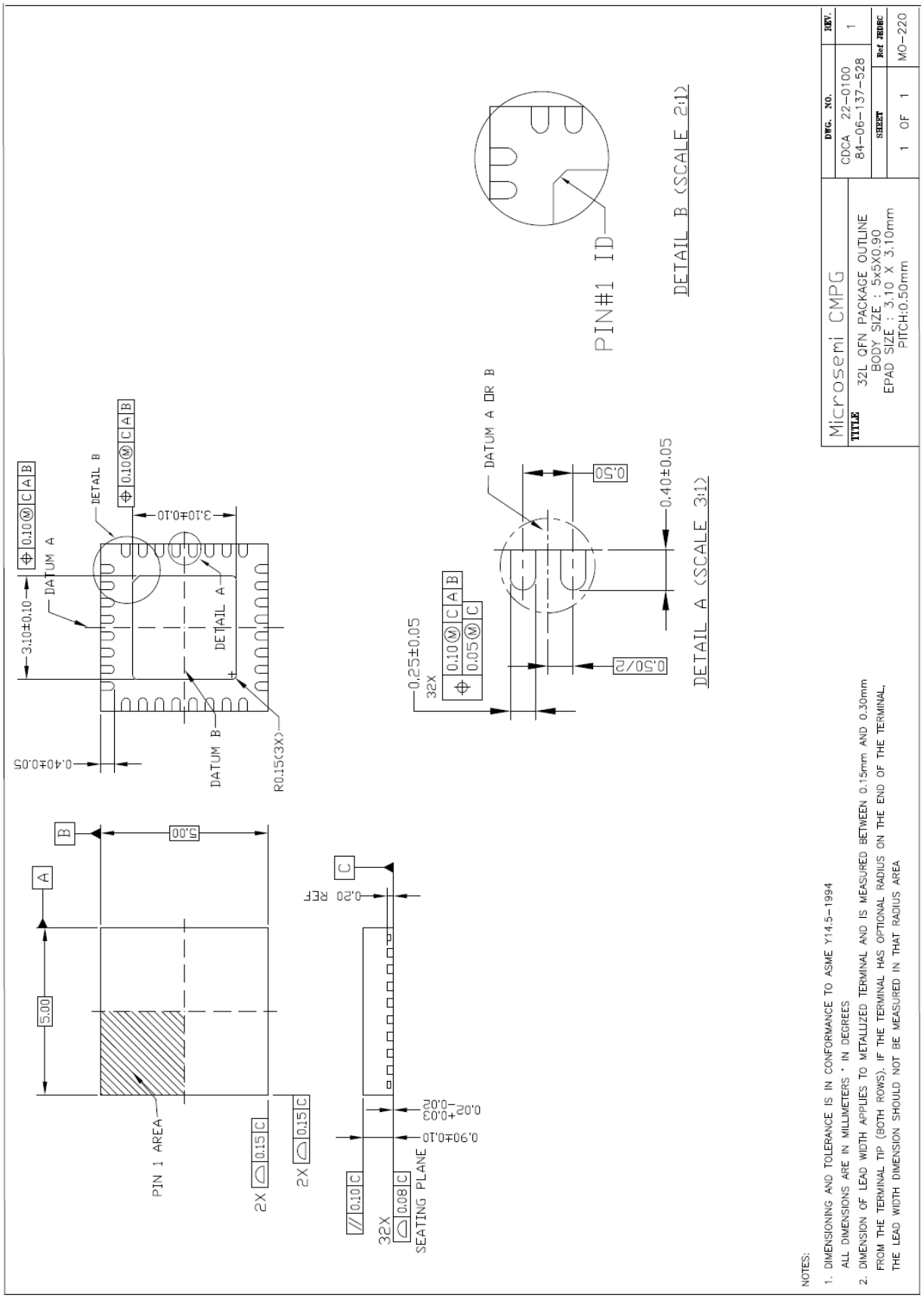
August 2017 release changes:

- Modified “Input driven by HCSL output” figure.
- Modified additive jitter for 156.25MHz input clock.
- Added Figure 37 and Figure 38.

September 2018 release changes:

- Added note in pinout to tie XIN in crystal circuit is not used
- Removed Figures 15 and 16 due to inaccuracy
- Fixed typo in Table 3

Package Outline



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