SLM2104S

600V Half-Bridge Driver

PRODUCT SUMMARY

- **V_{OFFSET}** 600 V max.
- **I_O+/-** 130 mA/270 mA
- **V_{OUT}** 10 V - 20 V
- **$t_{on/off}$ (typ.)** 680 ns/150 ns
- **Deadtime (typ.)** 520 ns

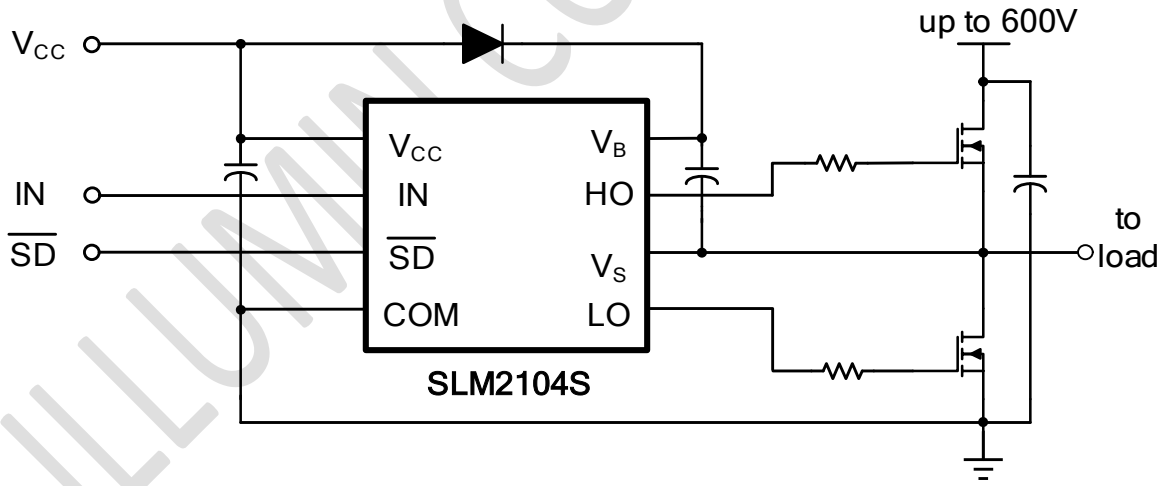
FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- Shutdown input turns off both channels
- RoHS compliant
- SOIC-8 and PDIP-8 package

GENERAL DESCRIPTION

The SLM2104S is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

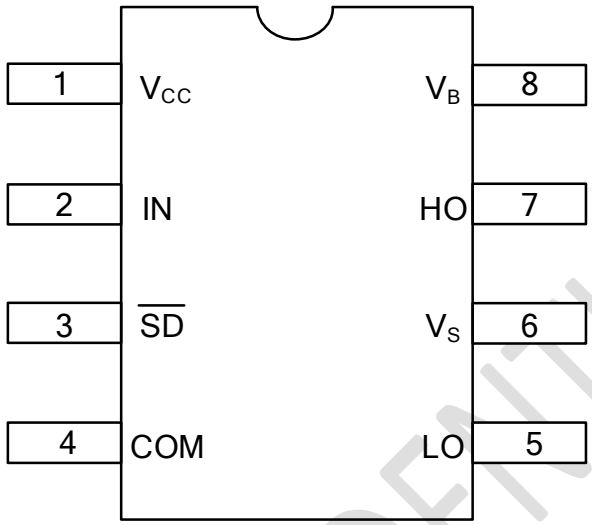
TYPICAL APPLICATION CIRCUIT



(Refer to Lead Assignments for correct configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOIC-8 and PDIP-8	

PIN DESCRIPTION

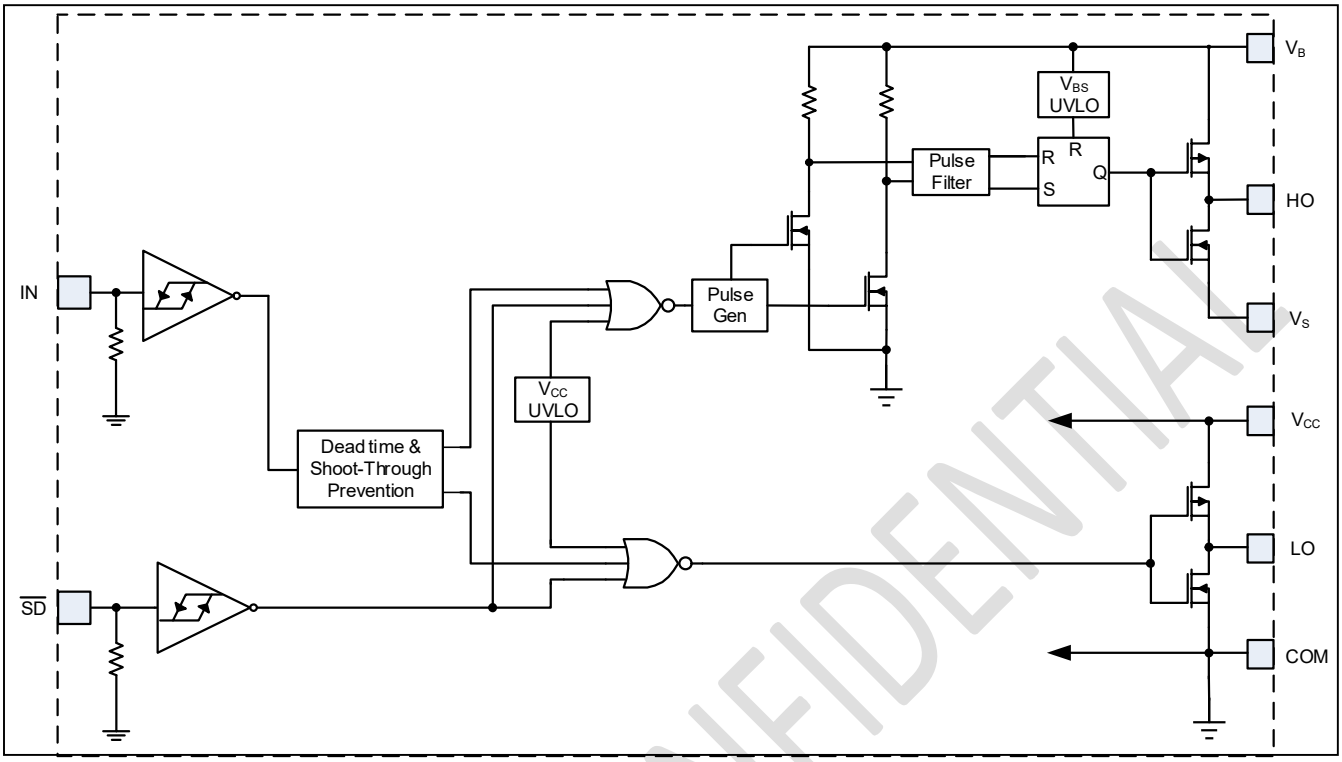
No.	Pin	Description
1	V_{CC}	Low-side and logic fixed supply
2	IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
3	$\overline{SD}$	Logic input for shutdown
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2104SCA-13GTR	SOIC8, Pb-Free	2500/Reel
SLM2104SCA-GT	SOIC8, Pb-Free	100/Tube
SLM2104SDA-GT	PDIP8, Pb-Free	100/Tube

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	625	V
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		---	50	V/ns
P_D	Package power dissipation @ $T_A \leqslant +25°C$	PDIP-8	---	1.0	W
		SOIC-8	---	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	PDIP-8	---	125	°C/W
		SOIC-8	---	200	
T_J	Junction temperature		---	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	

Note:
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATIONG CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage	Note 1	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	0	V_{CC}	
T_A	Ambient temperature	- 40	125	°C

Note:
The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	680	820	ns
t_{off}	Turn-off propagation delay	V_S = 600 V	---	150	220	
t_{sd}	Shutdown propagation delay		---	160	220	
t_r	Turn-on rise time		---	70	170	
t_f	Turn-off fall time		---	35	90	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off		400	520	650	
MT	Delay matching, HS & LS turn-on/off		---	---	60	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “1” input voltage	V_{CC} = 10 V to 20V	2.5	---	---	V
V_{IL}	Logic “0” input voltage		---	---	0.8	
VSD, TH+	SD input positive going threshold		2.5	---	---	
VSD, TH-	SD input negative going threshold		---	---	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2 mA	---	0.05	0.2	
V_{OL}	Low level output voltage, V_O		---	0.02	0.1	
I_{LK}	Offset supply leakage current	V_B = V_S = 600 V	---	---	50	µA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V or 5 V	---	60	75	
I_{QCC}	Quiescent V_{CC} supply current		---	170	270	
I_{IN+}	Logic “1” input bias current	V_{IN} = 5 V	---	3	10	
I_{IN-}	Logic “0” input bias current	V_{IN} = 0 V	---	---	5	
V_{CCUV+} V_{BSUV+}	V_{CC} & V_{BS} supply undervoltage positive going threshold		8	8.9	9.8	V
V_{CCUV-} V_{BSUV-}	V_{CC} & V_{BS} supply undervoltage negative going threshold		7.4	8.2	9	
I_{O+}	Output high short circuit pulsed current	V_O = 0 V, V_{IN} = V_{IH} PW ≤ 10 µs	130	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15 V, V_{IN} = V_{IL} PW ≤ 10 µs	270	600		

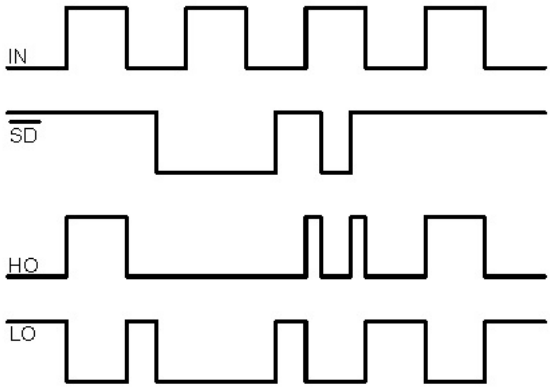


Figure 1. Input/Output Timing Diagram

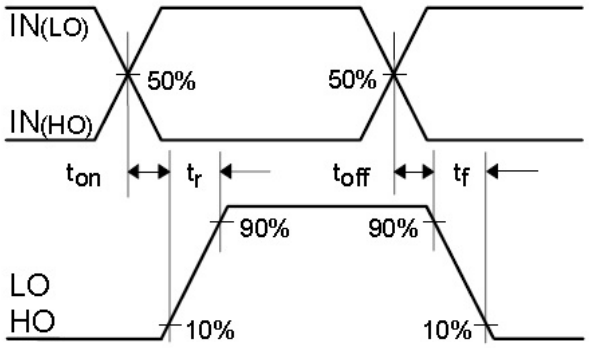


Figure 2. Switching Time Waveform Definitions

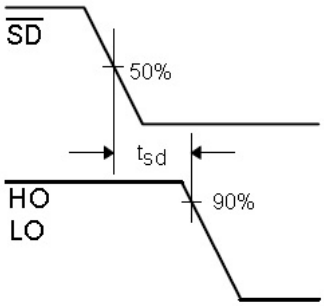


Figure 3. Shutdown Waveform Definitions

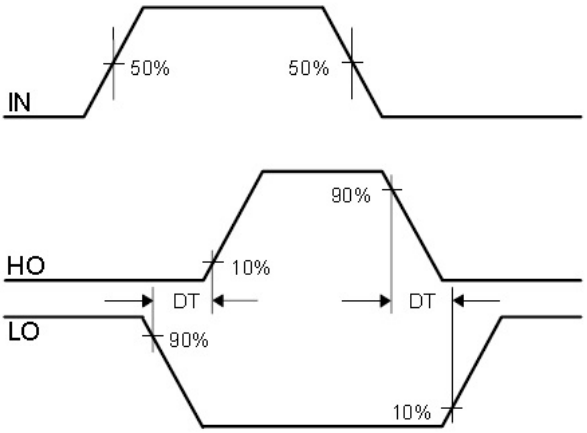


Figure 4. Deadtime Waveform Definitions

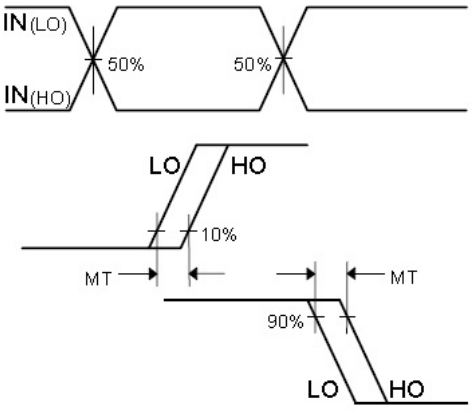


Figure 5. Delay Matching Waveform Definitions

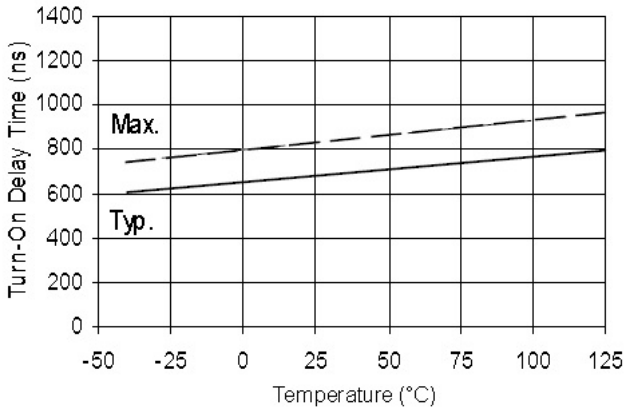


Figure 6A. Turn-On Time vs. Temperature

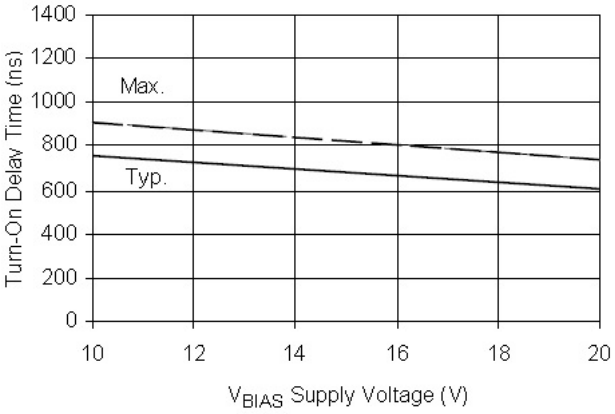


Figure 6B. Turn-On Time vs. Supply Voltage

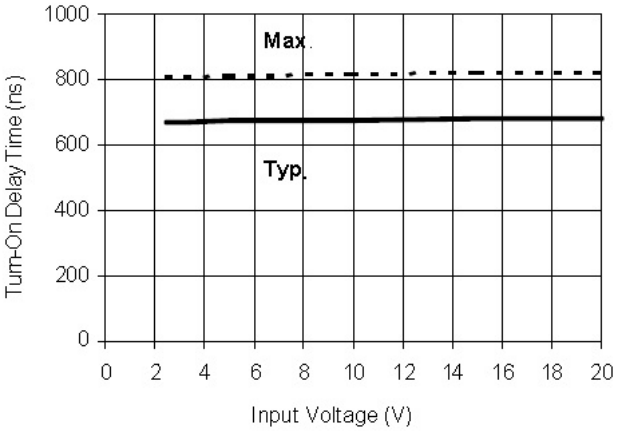


Figure 6C. Turn-On Time vs. Input Voltage

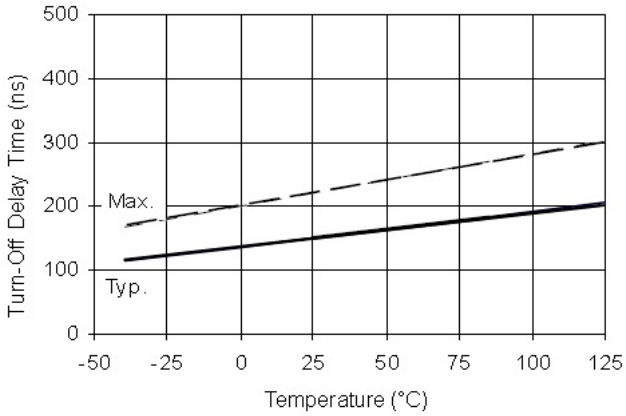


Figure 7A. Turn-Off Time vs. Temperature

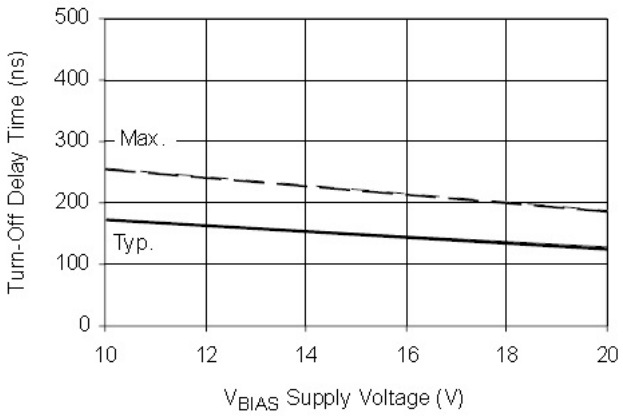


Figure 7B. Turn-Off Time vs. Supply Voltage

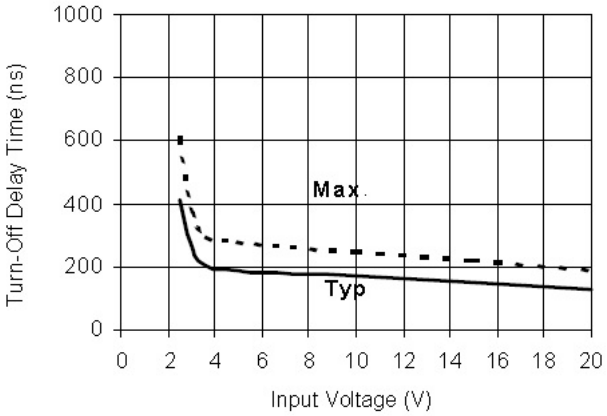


Figure 7C. Turn-Off Time vs. Input Voltage

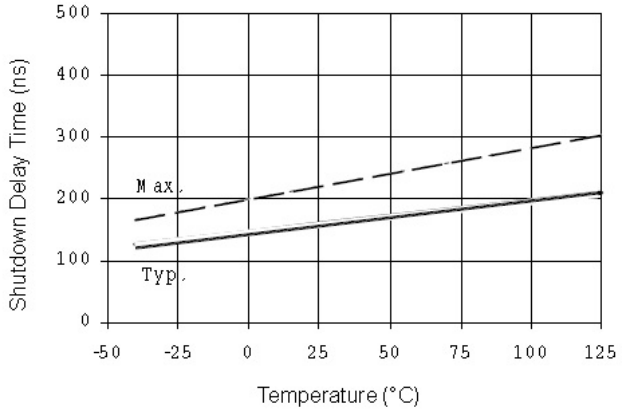


Figure 8A. Shutdown Time vs. Temperature

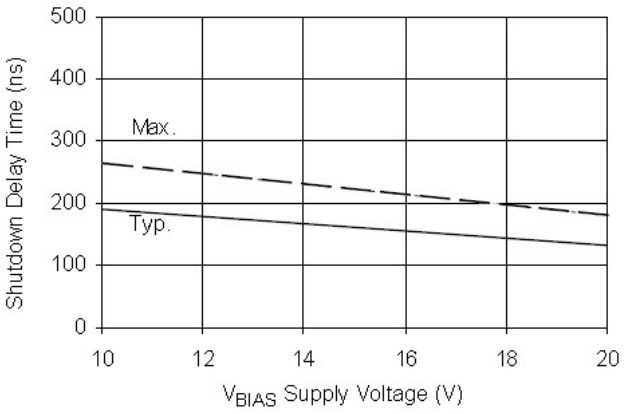


Figure 8B. Shutdown Time vs. Voltage

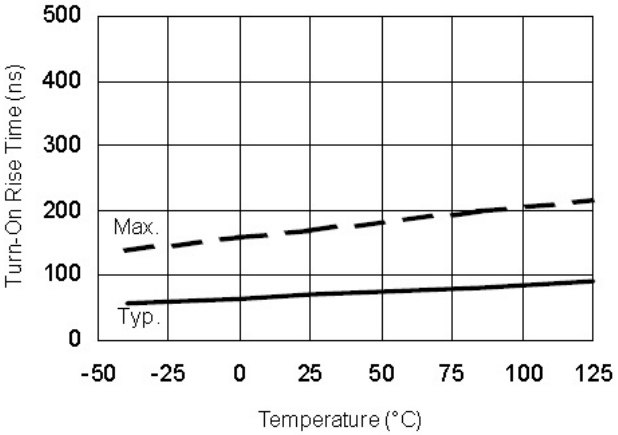


Figure 9A. Turn-On Rise Time vs. Temperature

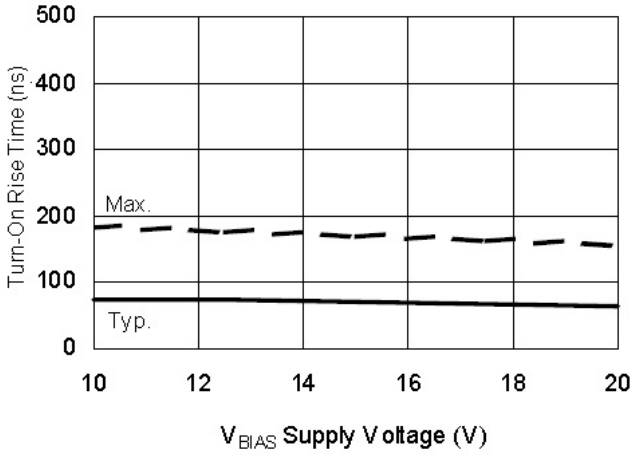


Figure 9B. Turn-On Rise Time vs. Voltage

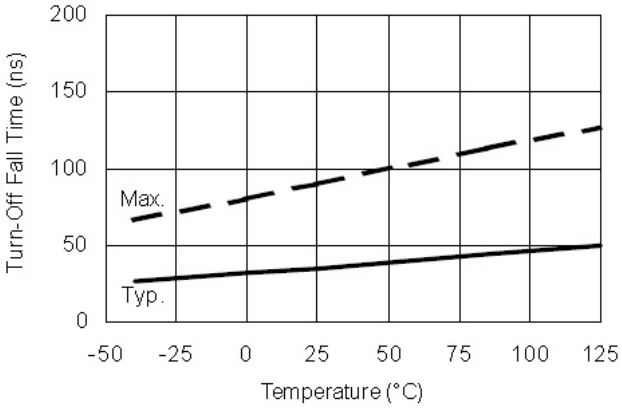


Figure 10A. Turn-Off Fall Time vs. Temperature

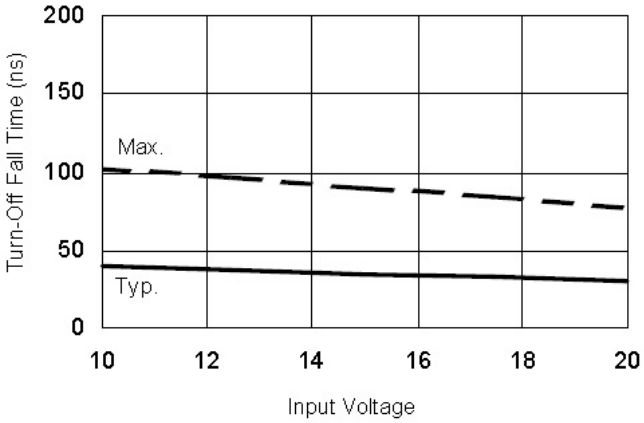


Figure 10B. Turn-Off Fall Time vs. Input Voltage

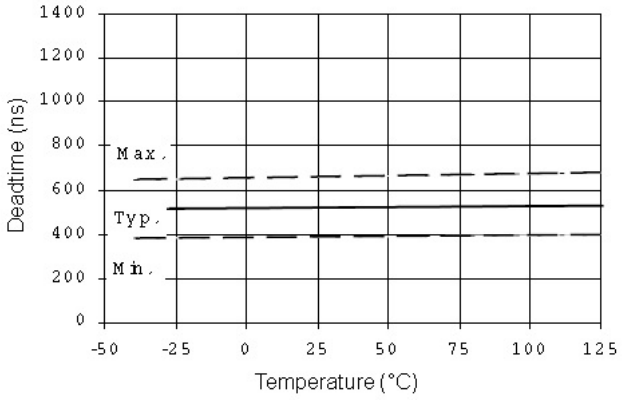


Figure 11A. Deadtime vs. Temperature

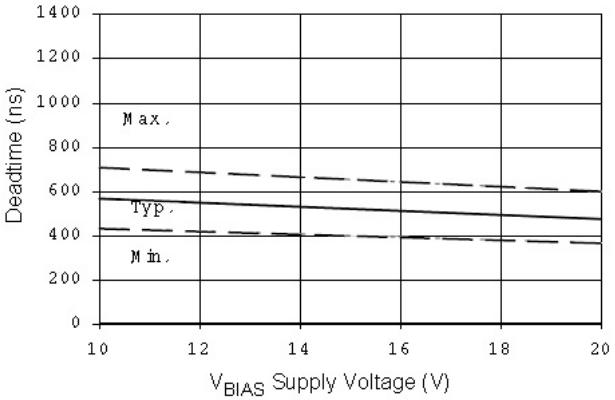


Figure 11B. Deadtime vs. Voltage

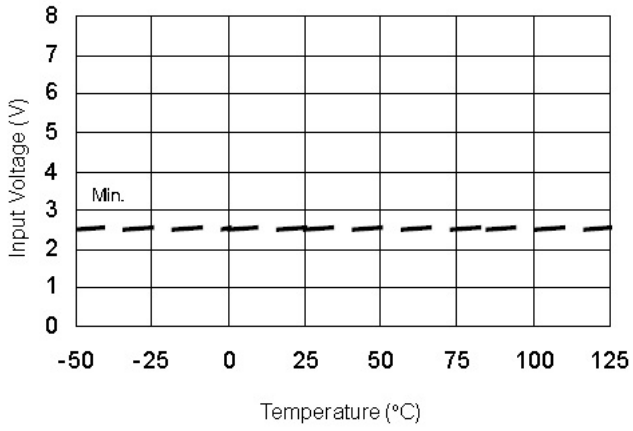


Figure12A. Logic "1" Input Voltage vs. Temperature

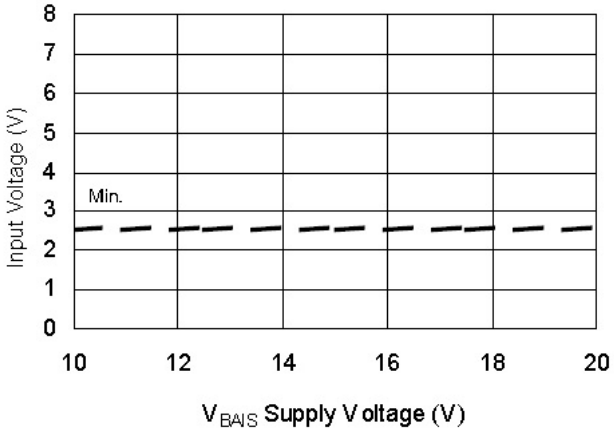


Figure 12B. Logic "1" Input Voltage vs. Supply Voltage

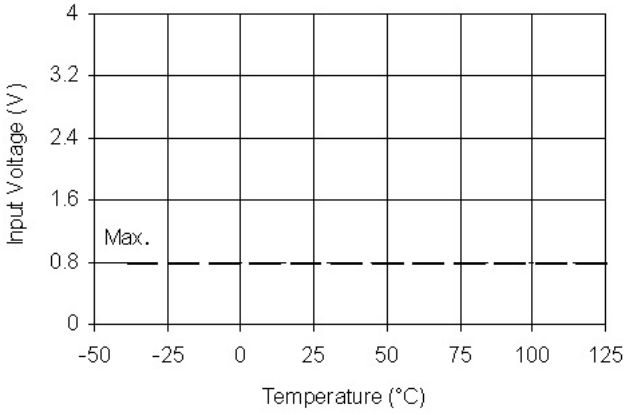


Figure 13A. Logic "0" (HO) & Logic "1" (LO) & Active SD Input Voltage vs. Temperature

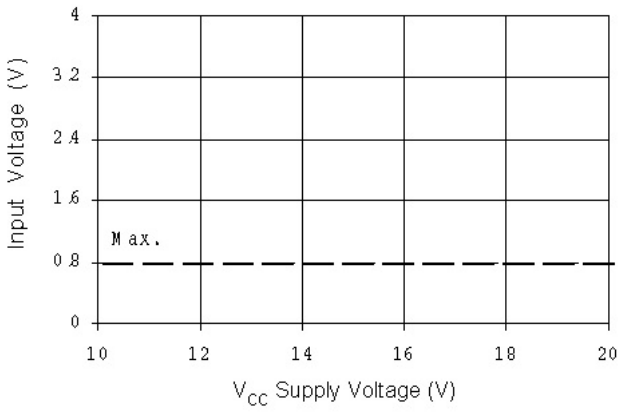


Figure 13B. Logic "0" (HO) & Logic "1" (LO) & Active SD Input Voltage vs. Voltage

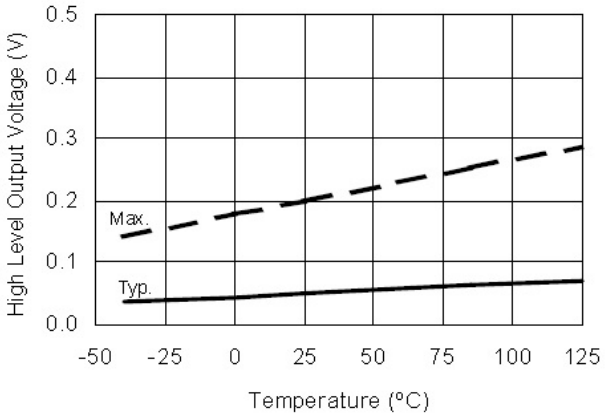


Figure 14A. High Level Output Voltage vs. Temperature

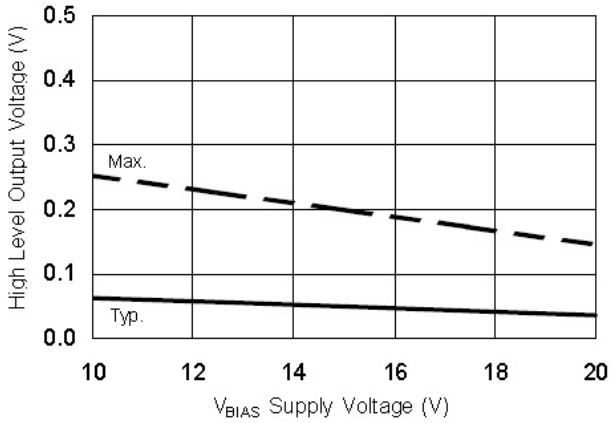


Figure 14B. High Level Output Voltage vs. Supply Voltage

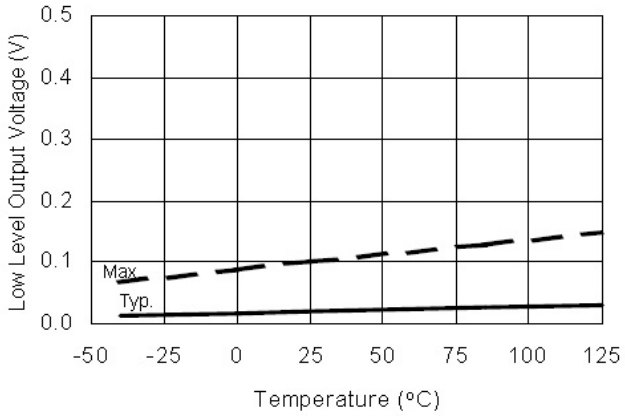


Figure 15A. Low Level Output Voltage vs. Temperature

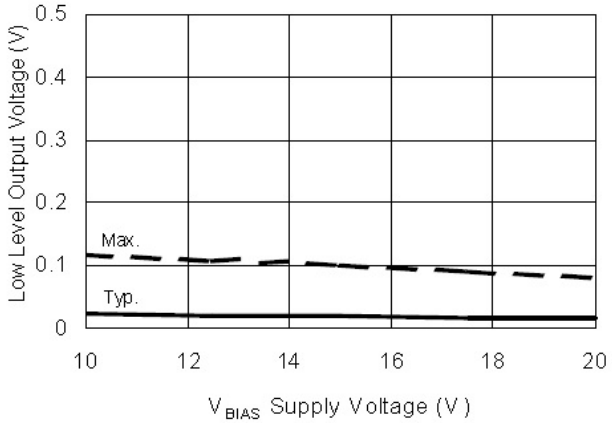


Figure 15B. Low Level Output Voltage vs. Supply Voltage

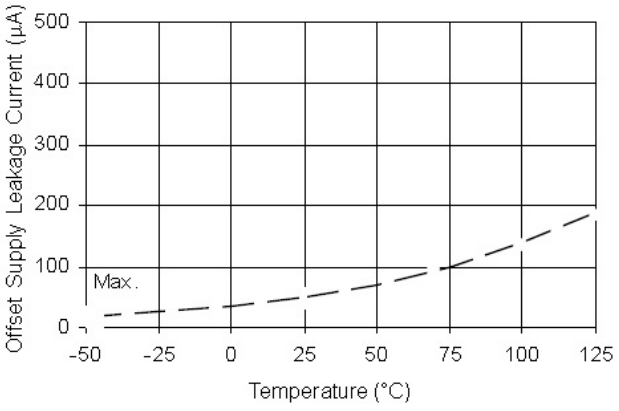


Figure 16A. Offset Supply Current vs. Temperature

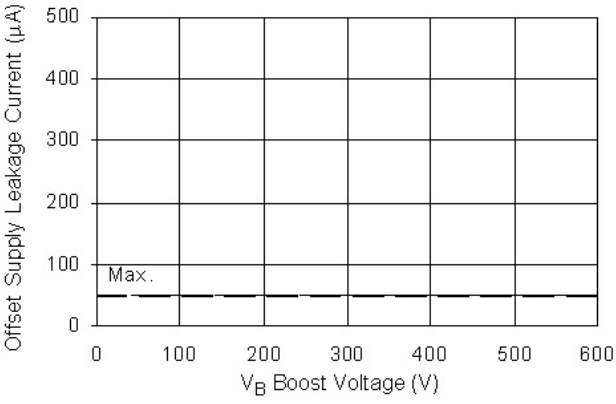


Figure 16B. Offset Supply Current vs. Voltage

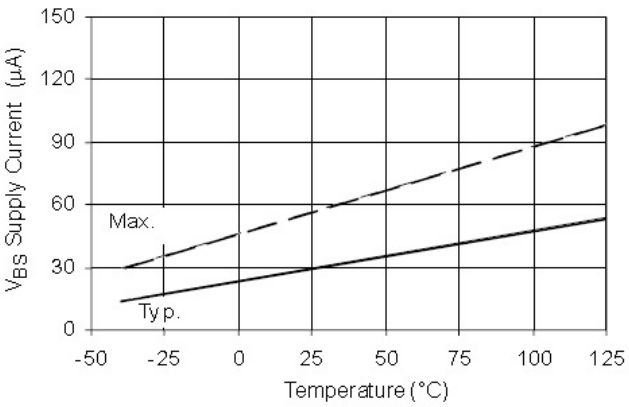


Figure 17A. V_{BS} Supply Current vs. Temperature

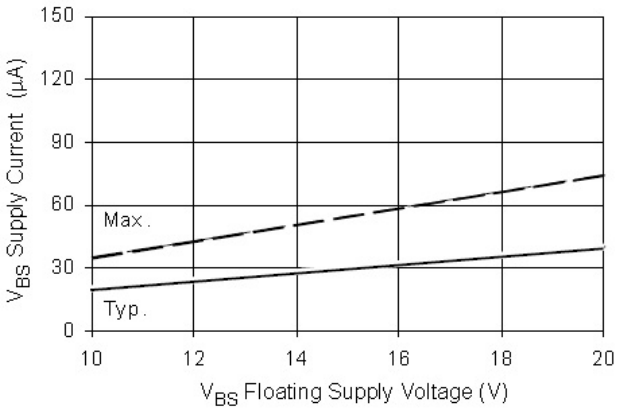


Figure 17B. V_{BS} Supply Current vs. Voltage

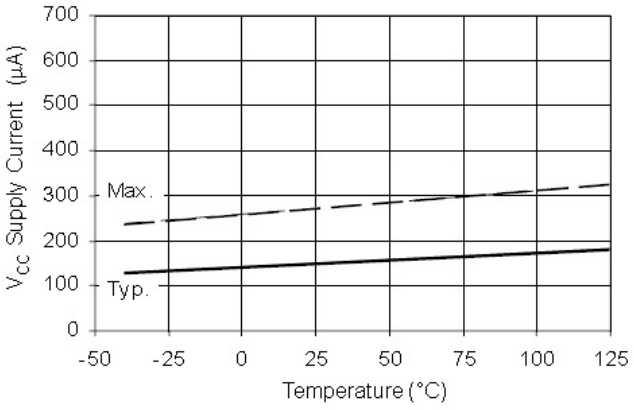


Figure 18A. V_{CC} Supply Current vs. Temperature

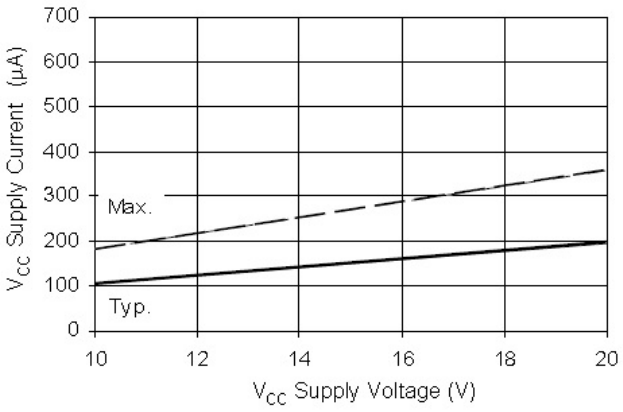


Figure 18B. V_{CC} Supply Current vs. Voltage

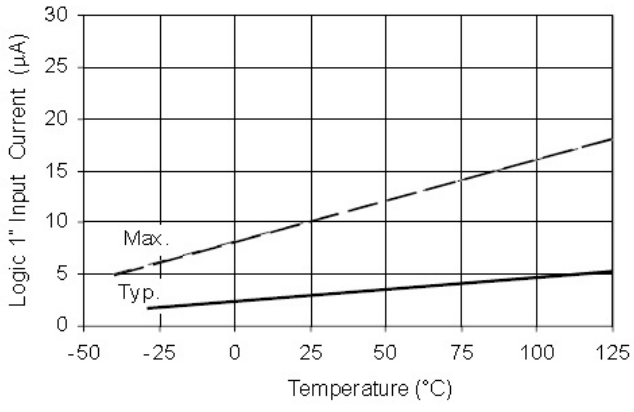


Figure 19A. Logic"1" Input Current vs. Temperature

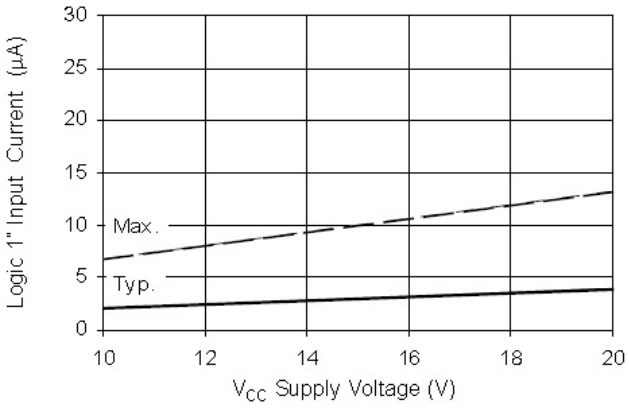


Figure 19B. Logic"1" Input Current vs. Voltage

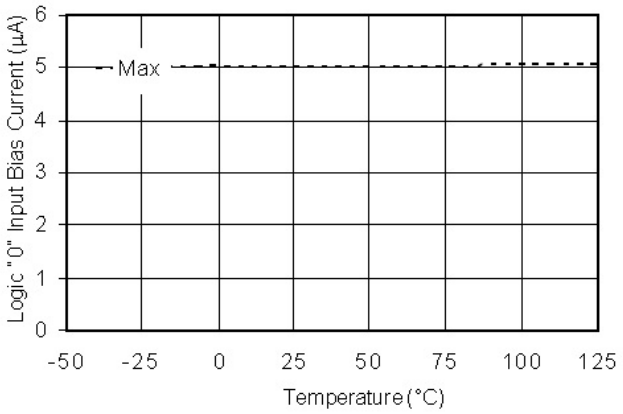


Figure 20A. Logic "0" Input Bias Current vs. Temperature

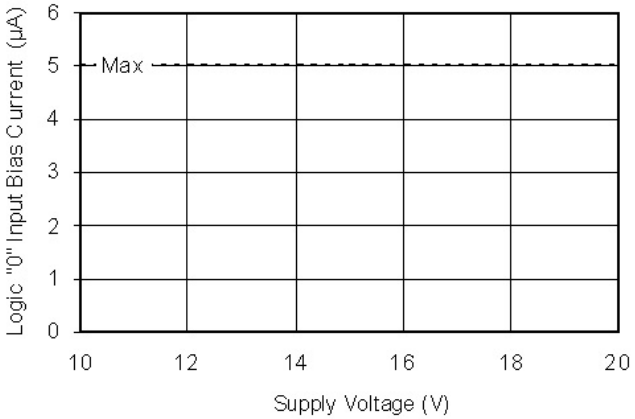


Figure 20B. Logic "0" Input Bias Current vs. Voltage

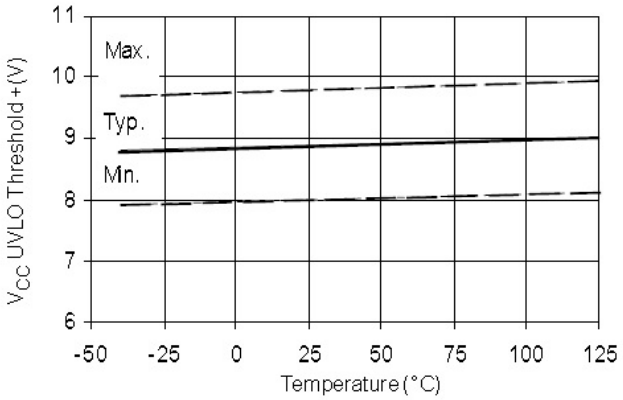


Figure 21A. V_{CC} Undervoltage Threshold(+) vs. Temperature

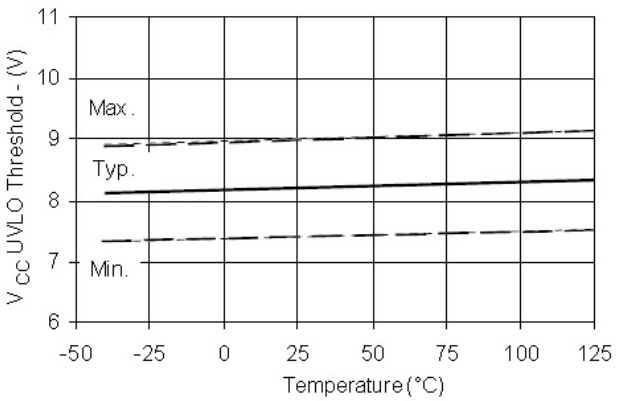


Figure 21B. V_{CC} Undervoltage Threshold(-) vs. Temperature

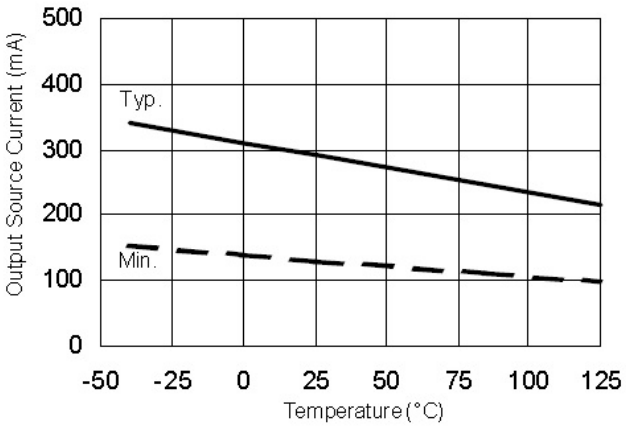


Figure 22A. Output Source Current vs. Temperature

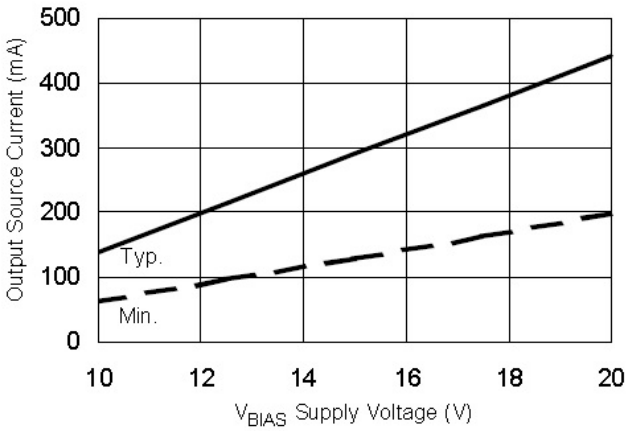


Figure 22B. Output Source Current vs. Voltage

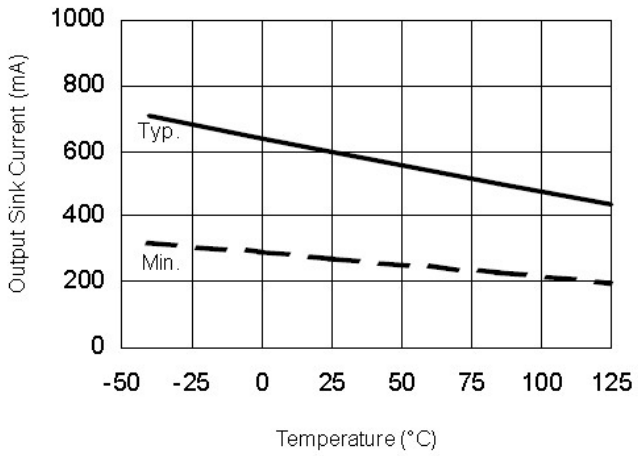


Figure 23A. Output Sink Current vs. Temperature

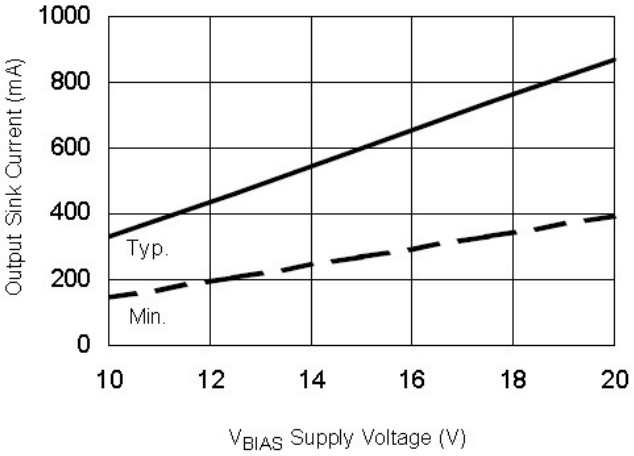


Figure 23B. Output Sink Current vs. Supply Voltage

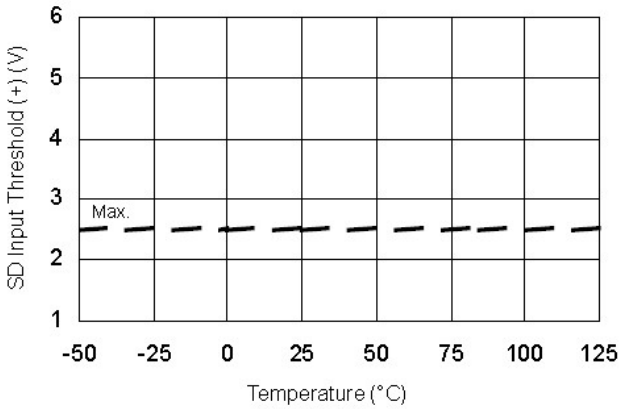


Figure 24A. SD Input Positive Going Threshold (+) vs. Temperature

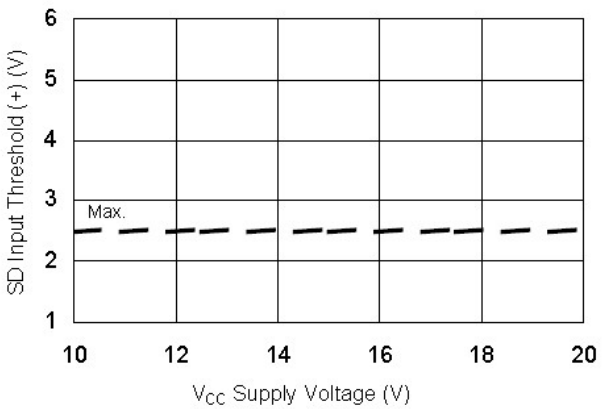
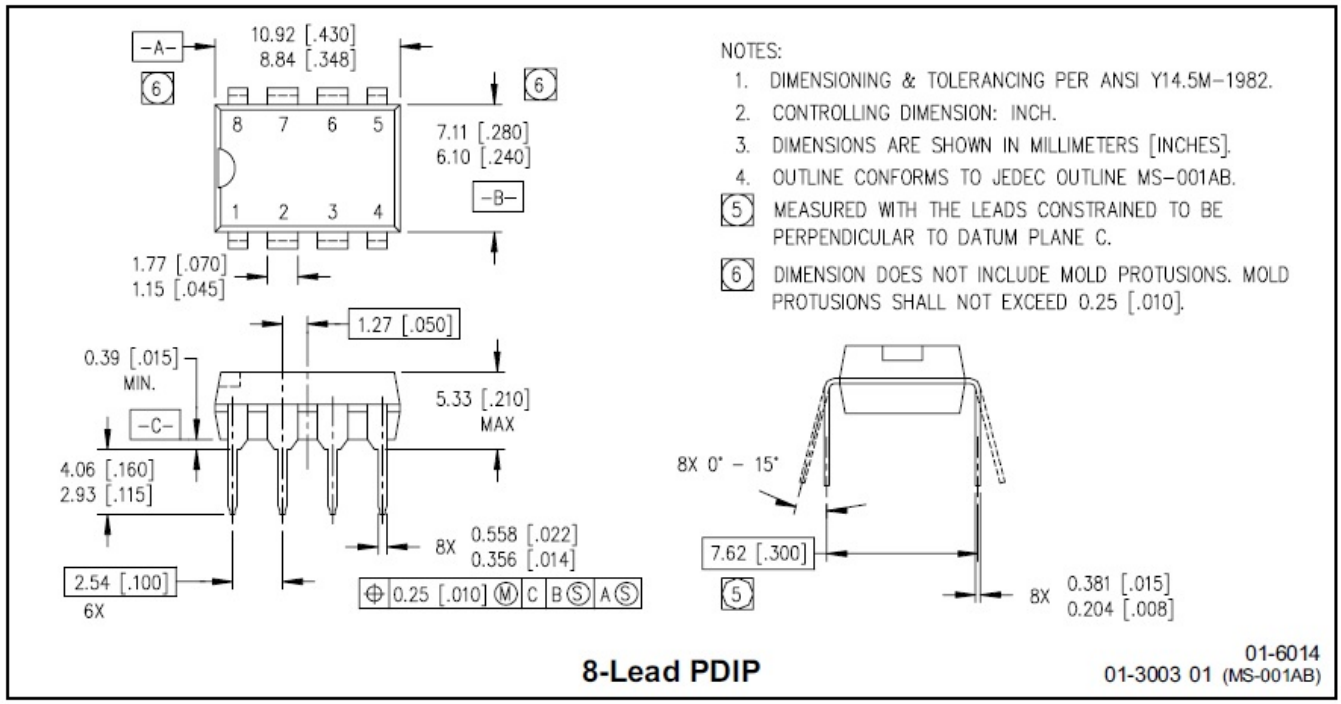


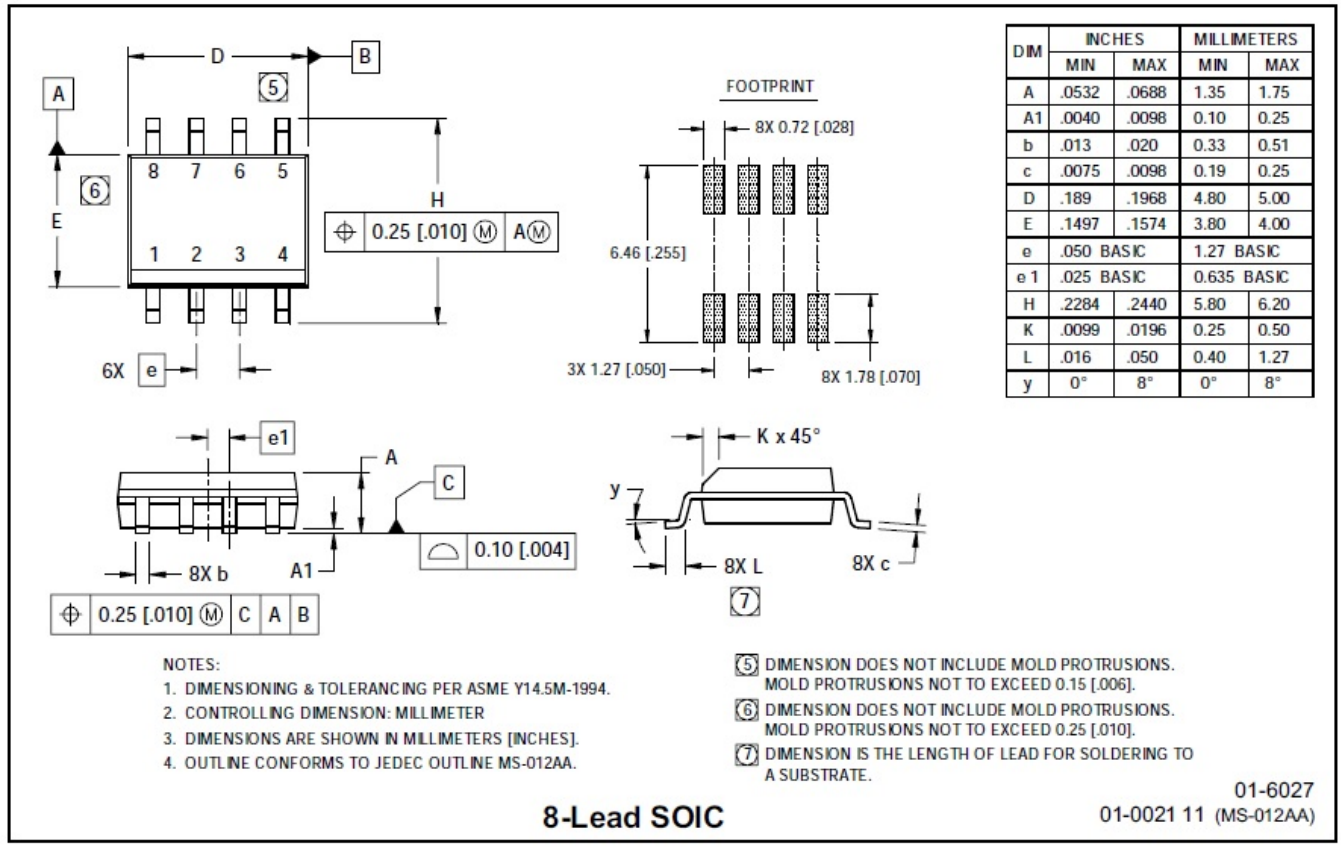
Figure 24B. SD Input Positive Going Threshold (+) vs. Supply Voltage

PACKAGE CASE OUTLINES



8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)

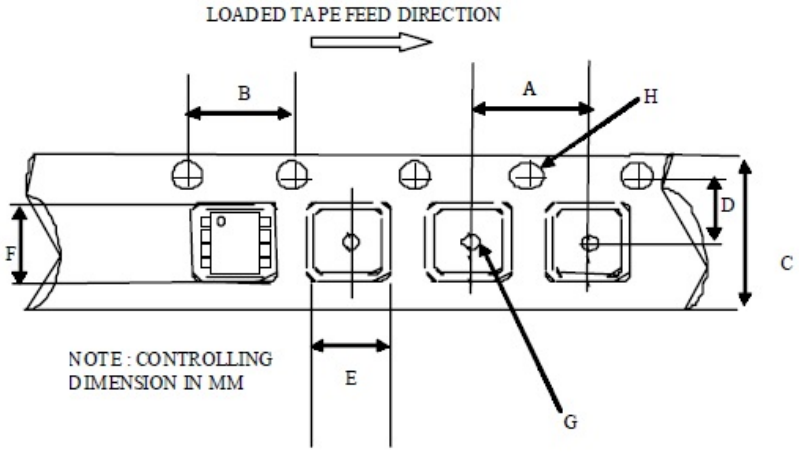


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

8-Lead SOIC

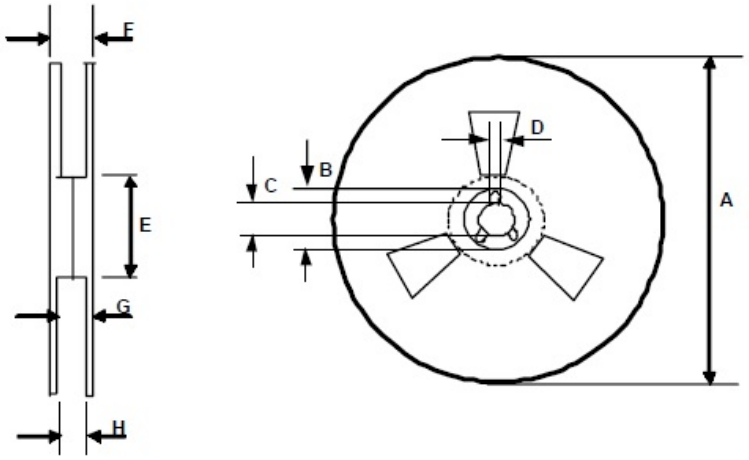
01-6027
01-0021 11 (MS-012AA)

Tape & Reel
8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Revision History

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2019-8-27	
Whole document	New company logo released
Page 1	Removed “Figure 1.” and “May 2019”
Page 5	Add UVLO threshold for V_{BS} voltage