# iCE40HX-8K Breakout Board

# Evaluation Board User Guide

FPGA-EB-02031-1.2

July 2020

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| CRAM | Configuration Random Access Memory |
| FPGA | Field-Programmable Gate Array |
| FTDI | Future Technology Devices International |
| I/O | Input/Output |
| LED | Light Emitting Diode |
| SPI | Serial Peripheral Interface |

# 1. Introduction

This document provides technical information and instructions for using the iCE40™HX-8K Breakout Board. This kit is based on the Lattice iCE40-HX8K-CT256 high performance FPGA device. Two source codes, one written in Verilog and the other in VHDL, are available to download for the iCE40HX-8K Breakout Board. Both codes are functionally the same. The contents of this user guide include demo operation, top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, switches, a complete set of schematics, and the bill of materials for the iCE40HX-8K Evaluation Board.

# 2. Features

The iCE40HX-8K Breakout Board includes:

- iCE40HX-8K Evaluation Board – The iCE40HX-8K Evaluation Board features the following onboard capabilities:
  - iCE40HX-8K CT256 device
  - Eight user-accessible LEDs
  - SPI Flash for programming configuration
  - 40 pin 0.1” header for user connectivity
  - 0.1” holes for user connectivity
  - FTDI 2232H for USB interface
  - 12 MHz oscillator
  - Jumpers to select programming the SPI flash or iCE40HX-8K
- Pre-loaded Demo – The kit comes with a default design that flashes the LEDs on and off.
- USB connector Cable – A mini B USB cable for programming the SRAM fabric of the iCE40HX-8K or the onboard SPI flash. The USB cable also powers the iCE40HX-8K evaluation board. Figure 2.1 shows the top side of the iCE40HX-8K Evaluation Board indicating the specific features that are designed on the board.

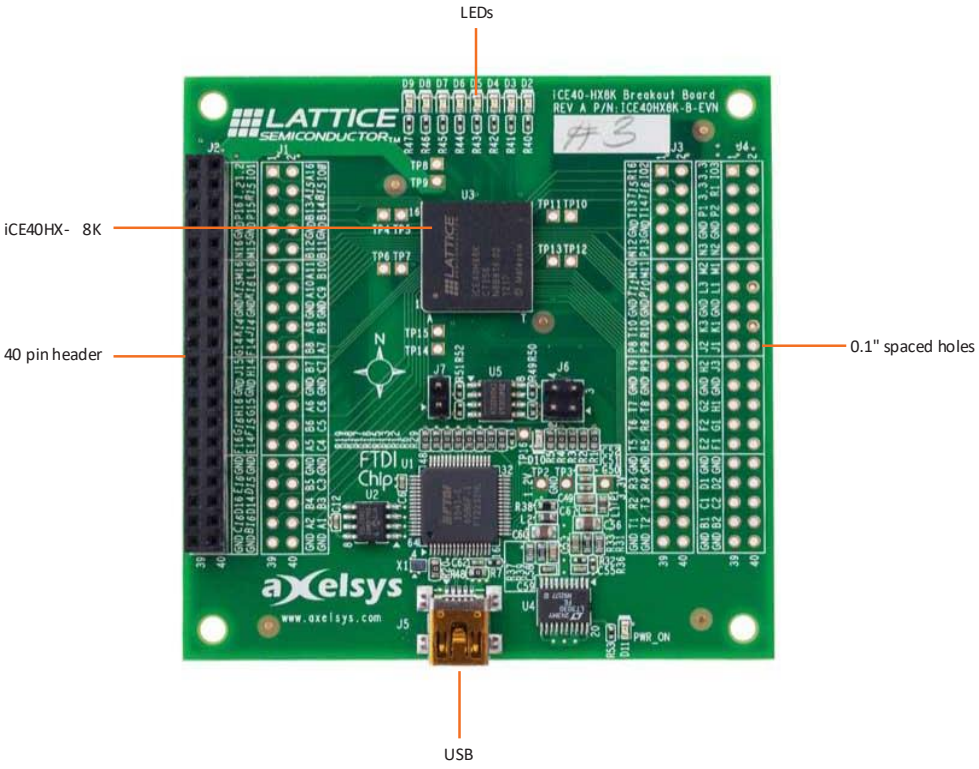


**Figure 2.1. Top Side of the iCE40HX-8K Evaluation Board**

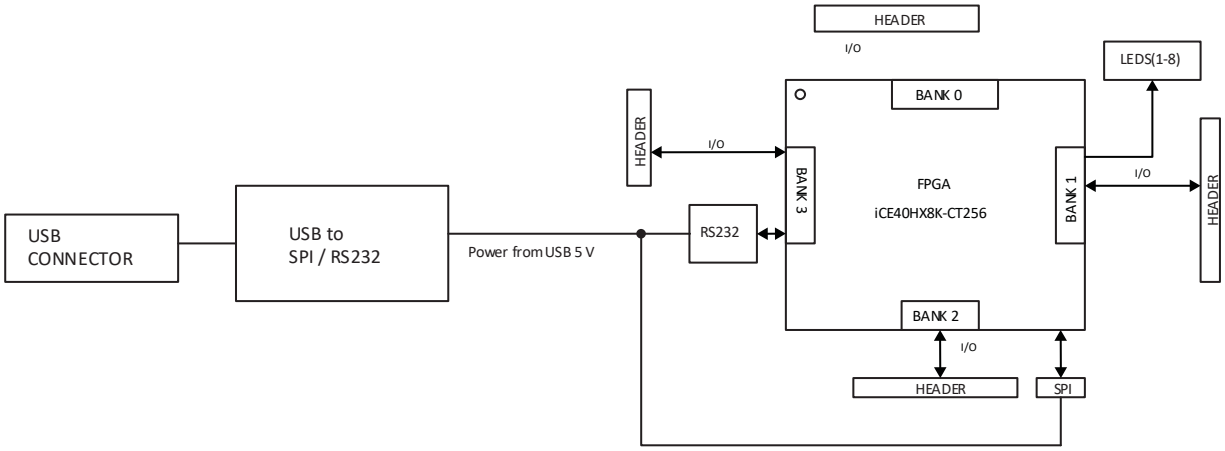


**Figure 2.2. Block Diagram**

# 3. iCE40 Device

This board features an iCE40HX-8K device with a 1.2 V core supply. It is packaged in a 256 caBGA package. For a complete description of this device, refer to iCE40 LP/HX Family Data Sheet (FPGA-DS-02029).

# 4. Software Requirements

You should install the following software before you begin developing designs for the evaluation board:

- Lattice iCEcube2™ Release – 2012.09SP1.22498 or later
- Diamond® Programmer – Version 2.2 or later

These software are available at the Lattice website Design Software and IP page. Make sure you log in to the Lattice website. Otherwise, these software downloads are not visible.

# 5. Demonstration Design

The design file iCE40HX8KLED.zip contains the following files:

- LED_VHDL.vhd (VHDL code)
- LED_Verilog.v (Verilog code)
- LED.pcf (pin constraint file)
- LED_VHDL_bitmap.hex (Bit stream file for programming FPGA)
- LED_Verilog_bitmap.hex (Bit stream file for programming FPGA)

Two source codes are provided, one written in VHDL and the other in Verilog. Both of these codes function identically. This provides you with an option to use either one of the codes when programming the iCE40HX-8K Breakout Board. When the FPGA is programmed with one of these codes, the red LEDs (D2 thru D9) flashes on for half a second and off for half a second. Figure 5.1 shows the block diagram of the Verilog or VHDL code.

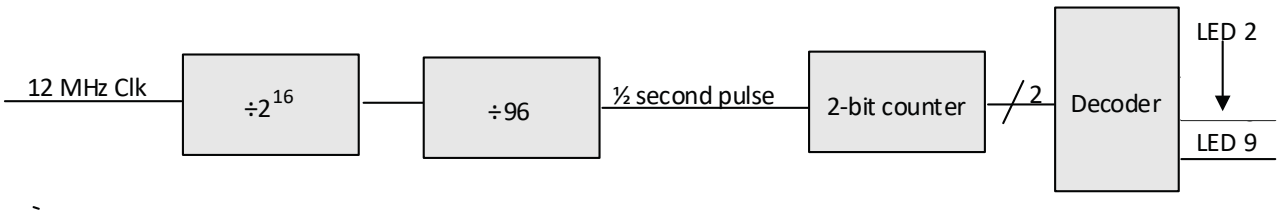


**Figure 5.1. Block Diagram of the Verilog or VHDL Code**

The source code has two counters that are used to divide the 12 MHz clock by 216 and 96, generating an approximately half-second pulse. This pulse along with the decoder turns the LEDs (D2 thru D9) on for half a second and off for half a second. The decoder can be modified to have any type of LED sequence by changing either the VHDL or Verilog code. When the board is plugged into a USB port, a +5 V power is applied to the board that lights a green LED (D11). After the FPGA is programmed, a green LED (D10) lights. This LED is connected to the CDONE line of the FPGA.

# 6. Board Power

The iCE40HX-8K evaluation board is powered with the USB cable. LED location D11 indicates that the board is powered up. All I/O are driven at 3.3 V. There are two versions of the BOM. Early versions have D1 populated with a CDBU0520 Schottky. Later versions populate D1 with a CDSU4148. The later version diode complies with the voltage requirements on the *Vpp_2V5* pin for NVCM programming/configuration.

# 7. Board I/O

The I/O that feed the holes and the 0.1” connector are driven at 3.3 V levels. Location J2 is the populated 2 x 20 row connector. Locations J1, J3, and J4 have hole locations that you can connect to for their specific I/O requirements.

# 8. Programming Options

Two jumpers, J6 and J7, can be set for two types of FPGA configurations:

- SPI Flash Mode, for programming the serial flash memory.
- SPI Peripheral Mode, for configuring the volatile CRAM in the FPGA.

In SPI Flash Mode the SPI signals from the FTDI USB interface chip programs the serial flash memory. After the memory is programmed, the FPGA reads from the memory and configures itself. The advantage of programming the serial flash is that the FPGA is reconfigured after power-up. Jumpers must be in locations J7:1-2, J6:2-4, and J6:1-3 as shown in Figure 8.1.

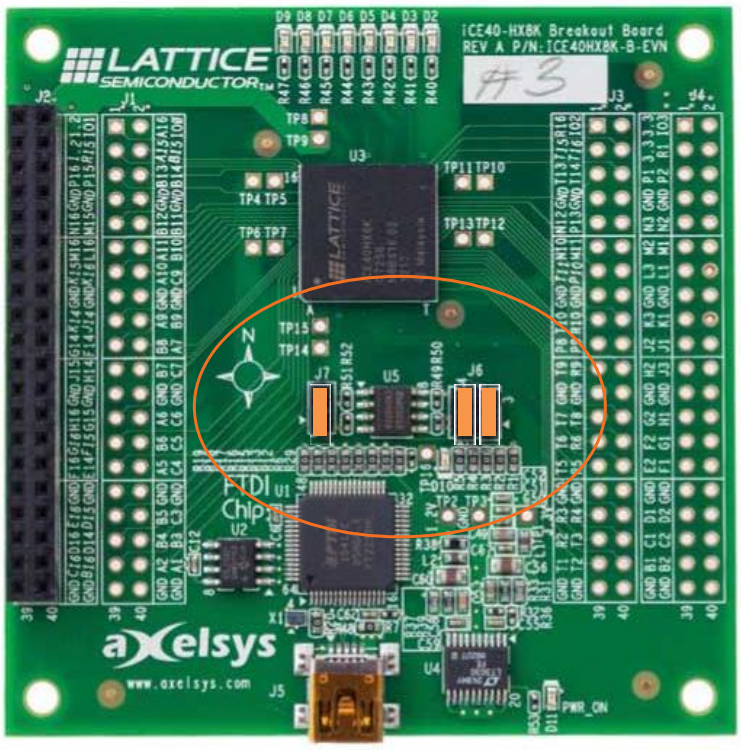


**Figure 8.1. SPI Flash Programming**

In SPI Peripheral Mode, the SPI signals load the program file into the CRAM (configuration RAM) of the FPGA directly. In this mode, the FPGA loses its configuration when power is removed and must be reconfigured. Jumpers must be in locations J6:1-2 and J6:3-4. Jumper J7 is not installed as shown in Figure 8.2.

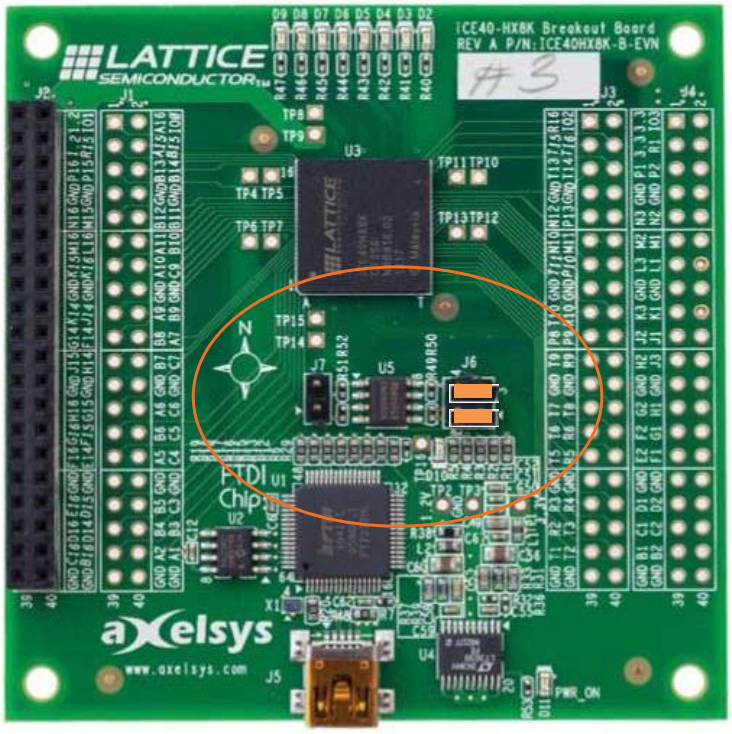


**Figure 8.2. CRAM Programming**

LED in location D10 is connected to the CDONE pin of the iCE40HX-8K. This can be monitored to determine that the iCE40HX-8K is programmed correctly.

# 9. Ordering Information

**Table 9.1. Ordering Information**

| Description | Ordering Part Number | China RoHS Environment-Friendly Use Period (EFUP) |
|---|---|---|
| iCE40HX-8K Breakout Board | iCE40HX8K-B-EVN |  |

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

# Appendix A. Schematic Diagrams

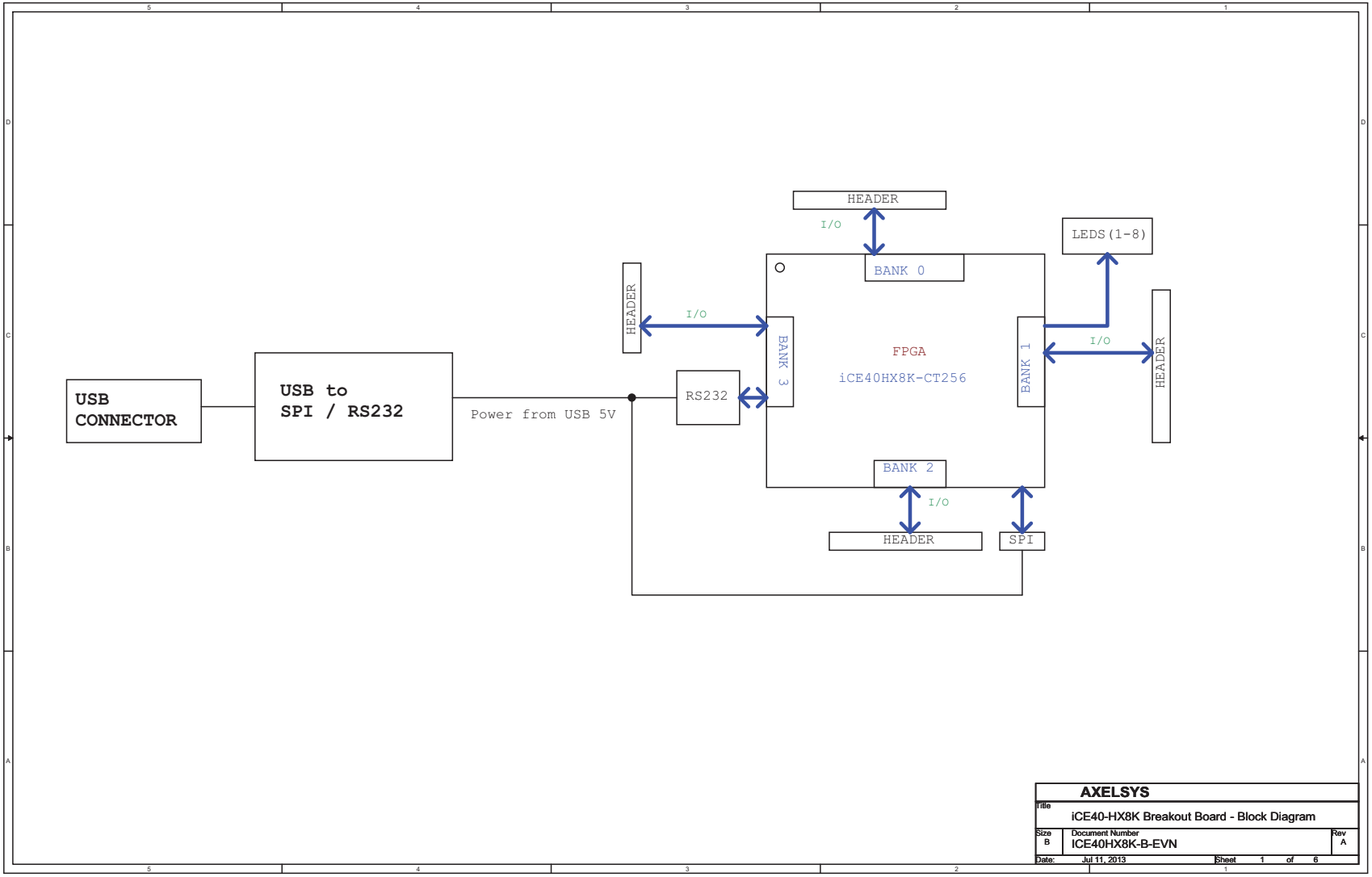


**Figure A.1. Block Diagram**

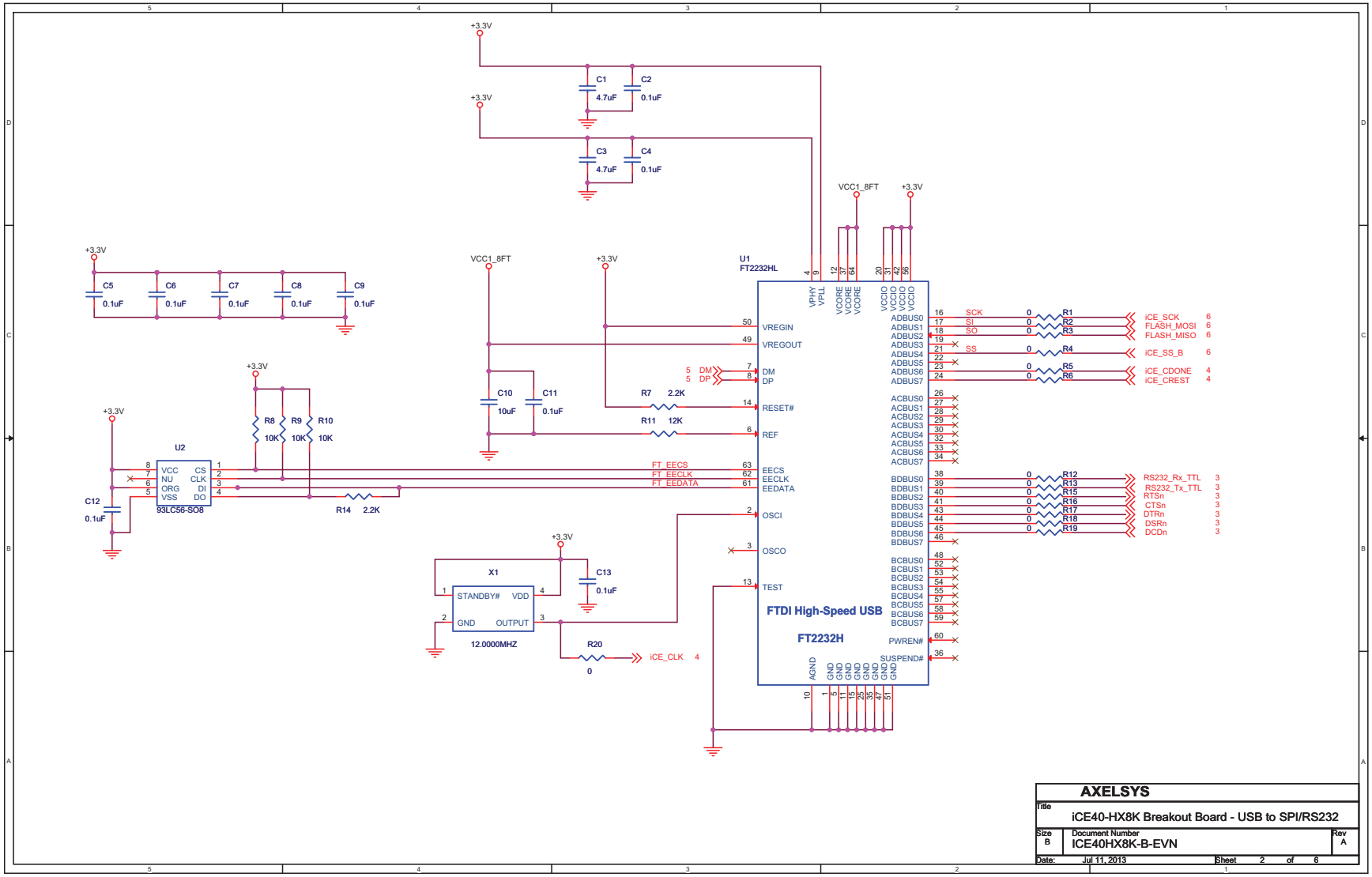


**Figure A.2. USB to SPI/RS232**

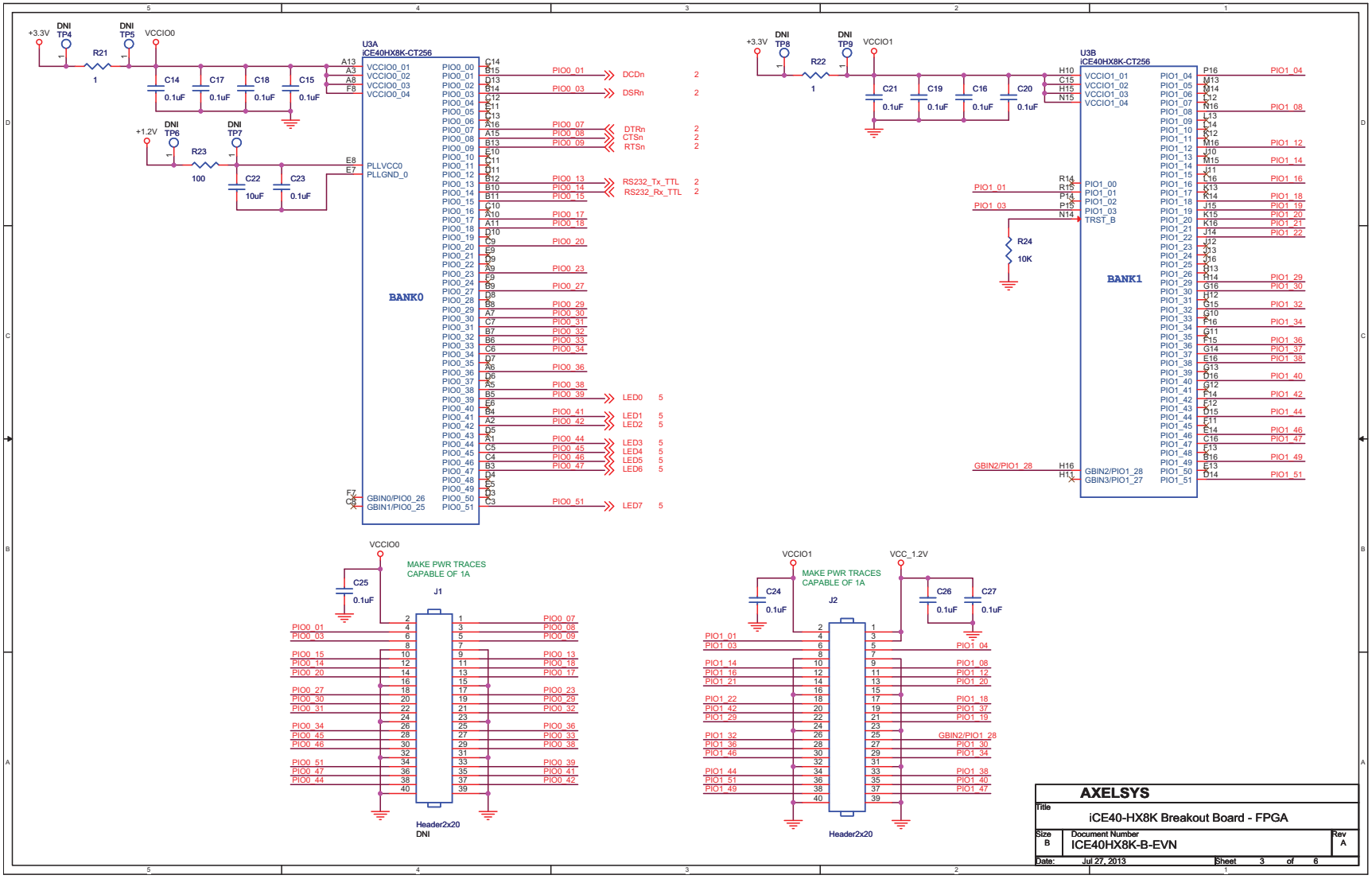


**Figure A.3. FPGA**

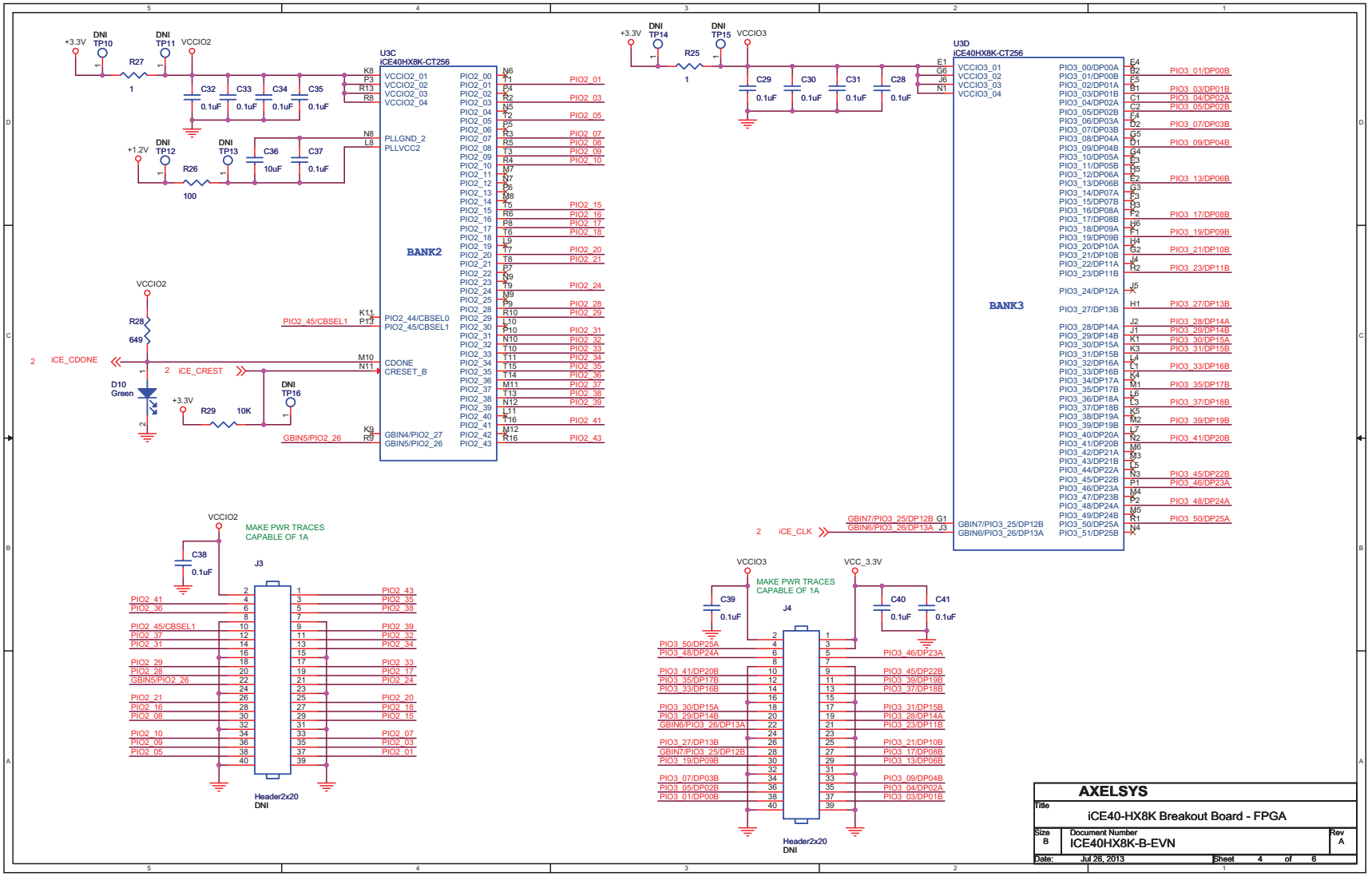


**Figure A.4. FPGA**

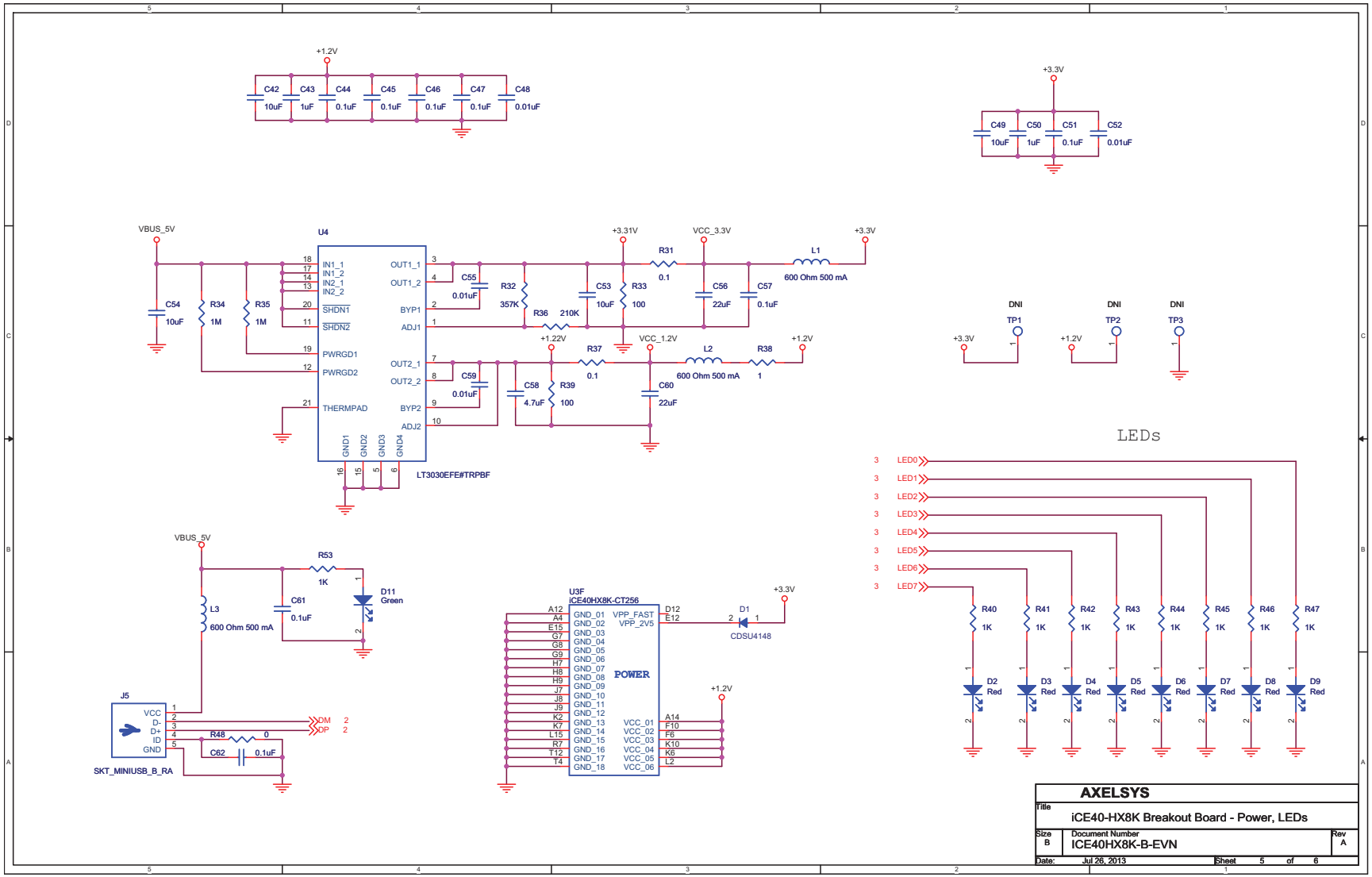


**Figure A.5. Power and LEDs**

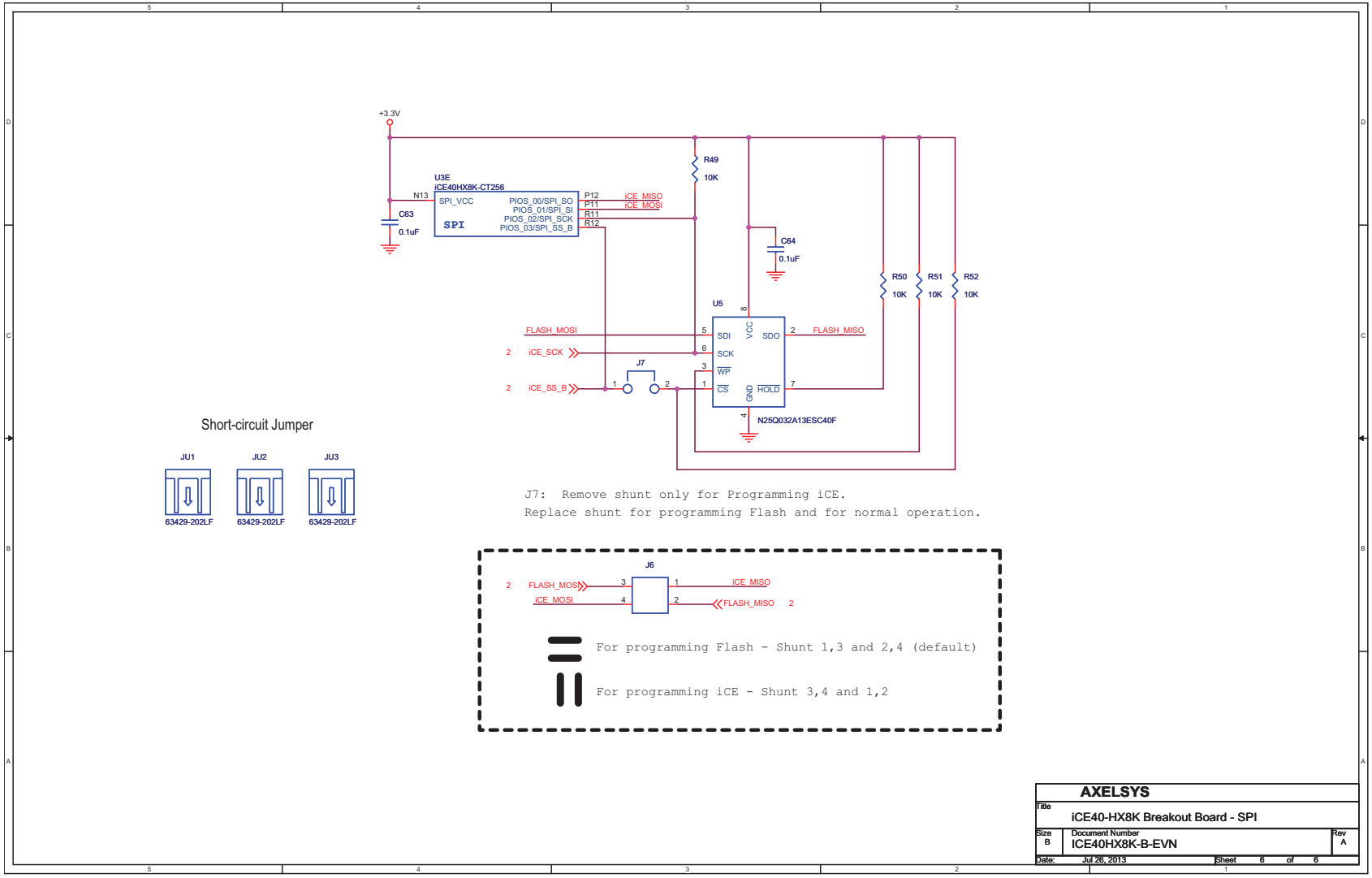


**Figure A.6. SPI**

# Revision History

**Revision 1.2, July 2020**

| Section | Change Summary |
|---|---|
| All | • Changed document number from EB85 to FPGA-EB-02031.<br>• Updated document template.<br>• Added Disclaimers section. |
| Acronyms in This Document | Added this section. |
| Board Power | Updated section content. |
| Appendix A. Schematic Diagrams | Updated Figure A.5. |

**Revision 1.1, January 2016**

| Section | Change Summary |
|---|---|
| Demonstration Design | Changed demonstration design to *design file*. |
| Technical Support Assistance | Updated this section. |

**Revision 1.0, November 2013**

| Section | Change Summary |
|---|---|
| All | Initial release. |


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